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High Speed Evaluation Board for Full Duplex M-LVDS Transceivers (ADN4692E, ADN4693E, ADN4695E, and ADN4697E)

FEATURES

- Easy evaluation of full-duplex M-LVDS transceivers ADN4692E, ADN4693E, ADN4695E, and ADN4697E
- Board layout optimized for high speed signaling
- Matched track lengths on M-LVDS input/output differential pairs, with controlled 50 Ω impedance tracks
- SMB jack inputs/outputs for high speed connections
  - Logic signals: RO, $\overline{RE}$, DE, and DI
  - M-LVDS bus signals: A, B, Y, and Z
- Power/ground connections through screw terminal blocks
- Jumper selectable enable/disable for $\overline{RE}$ and DE
- Test points for measuring all signals and multiple ground points to facilitate probing of multiple signals
- 50 Ω termination resistors across A and B, and Y and Z, to simulate double-terminated bus

APPLICATIONS

- Full-duplex M-LVDS part evaluation

EVALUATION KIT CONTENTS

- 1 EVAL-ADN469xEFDEBZ
- 1 ADN4692EBRZ
- 1 ADN4693EBRZ
- 1 ADN4695EBRZ
- 1 ADN4697EBRZ

EVAL-ADN469xEFDEBZ

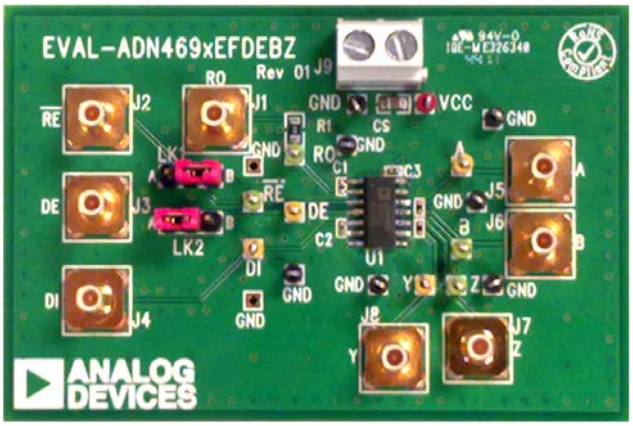

Figure 1.

GENERAL DESCRIPTION

The EVAL-ADN469xEFDEBZ allows quick and easy evaluation of full-duplex M-LVDS transceivers (ADN4692E, ADN4693E, ADN4695E, and ADN4697E). The evaluation board allows all of the input and output functions to be exercised without the need for external components. Screw terminal blocks provide convenient connections for power and ground, with SMB jack connectors for high speed logic and M-LVDS bus signals.

The evaluation board has a 14-lead SOIC footprint for a full-duplex M-LVDS transceiver from the ADN469xE family (see Table 1).

Table 1. ADN469xE Selection Table

Part No.	Receiver Type	Data Rate	Package	Half-Duplex/Full-Duplex	Evaluation Board
ADN4690E	Type 1	100 Mbps	8-lead SOIC	Half	EVAL-ADN469xEHDEBZ
ADN4691E	Type 1	200 Mbps	8-lead SOIC	Half	EVAL-ADN469xEHDEBZ
ADN4692E	Type 1	100 Mbps	14-lead SOIC	Full	EVAL-ADN469xEFDEBZ
ADN4693E	Type 1	200 Mbps	14-lead SOIC	Full	EVAL-ADN469xEFDEBZ
ADN4694E	Type 2	100 Mbps	8-lead SOIC	Half	EVAL-ADN469xEHDEBZ
ADN4695E	Type 2	100 Mbps	14-lead SOIC	Full	EVAL-ADN469xEFDEBZ
ADN4696E	Type 2	200 Mbps	8-lead SOIC	Half	EVAL-ADN469xEHDEBZ
ADN4697E	Type 2	200 Mbps	14-lead SOIC	Full	EVAL-ADN469xEFDEBZ

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REVISION HISTORY

3/12—Revision 0: Initial Version

EVALUATION BOARD CONFIGURATION

SETTING UP THE EVALUATION BOARD

The EVAL-ADN469xEFDEBZ allows the full-duplex parts in the ADN469xE family to be quickly and easily evaluated. The evaluation board allows all of the input and output functions to be exercised without the need for external components. Jumper configurations are shown in Table 2.

The board is powered by connecting a 3.3 V power supply to the screw terminals for VCC and GND. Supply current is typically 16 mA with both driver and receiver enabled or 1 mA with both disabled. A 10 µF decoupling capacitor, C1, is fitted at the connector between VCC and GND. The V_{CC} pin of the ADN469xE is fitted with a decoupling capacitor of 100 nF.

An example evaluation of the ADN4692E/ADN4693E/ADN4695E/ADN4697E driver is shown in Figure 2. A signal generator is connected to DI with an input signal of 50 MHz (ADN4692E/ADN4695E) or 100 MHz (ADN4693E/ADN4697E), with a 50% duty cycle and swing of between 0 V and 3.3 V. Jumpers LK1 and LK2 are connected in Position A to disable the receiver and enable the driver. Oscilloscope probes are connected to DI, Y, and Z.

Similarly, an evaluation of the ADN4692E/ADN4693E/ADN4695E/ADN4697E receiver is shown in Figure 3. A signal generator capable of applying a differential input signal is connected to J5 and J6, with the input swing between 1 V and 1.2 V (J6 input is the inverse of J5). Jumpers LK1 and LK2 are connected in Position B to enable the receiver and disable the driver. Oscilloscope probes are attached to RO, A, and B.

EVALUATION WITH APPLICATIONS

Two EVAL-ADN469xEFDEBZ boards can connect together in a point-to-point configuration, as shown in Figure 4. To allow part evaluation with a load equivalent to a parallel-terminated bus, the boards have been fitted with 50 Ω termination resistors. For the point-to-point configuration in Figure 4, replace these resistors with 100 Ω resistors.

A signal generator is connected onto the DI input of one board. The Y and Z outputs of this board are connected to the A and B inputs of the second board, respectively.

Connecting probes to DI on the first board, and A, B, and RO on the second, the propagation of the input signal across the bus and to the receiver output of the second board can be observed and evaluated.

Alternatively, the EVAL-ADN469xEFDEBZ can connect to an existing bus and a control board, as shown in Figure 5, to test the performance in the application. In this case, remove both termination resistors, as well as the jumpers on LK1 and LK2. Connect control signals to RO, $\overline{RE}$, DE, and DI.

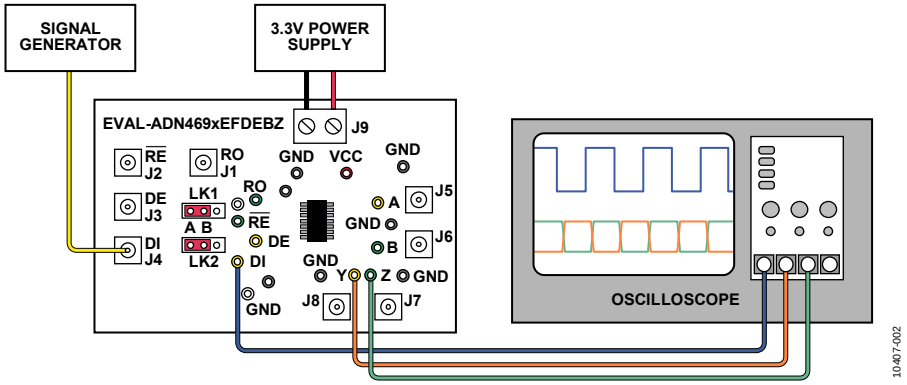

Figure 2. ADN4692E/ADN4693E/ADN4695E/ADN4697E Driver Evaluation with EVAL-ADN469xEFDEBZ

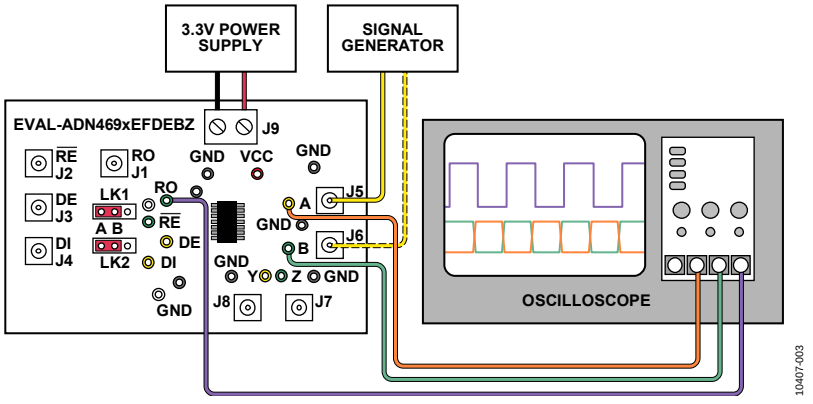

Figure 3. ADN4692E/ADN4693E/ADN4695E/ADN4697E Receiver Evaluation with EVAL-ADN469xEFDEBZ

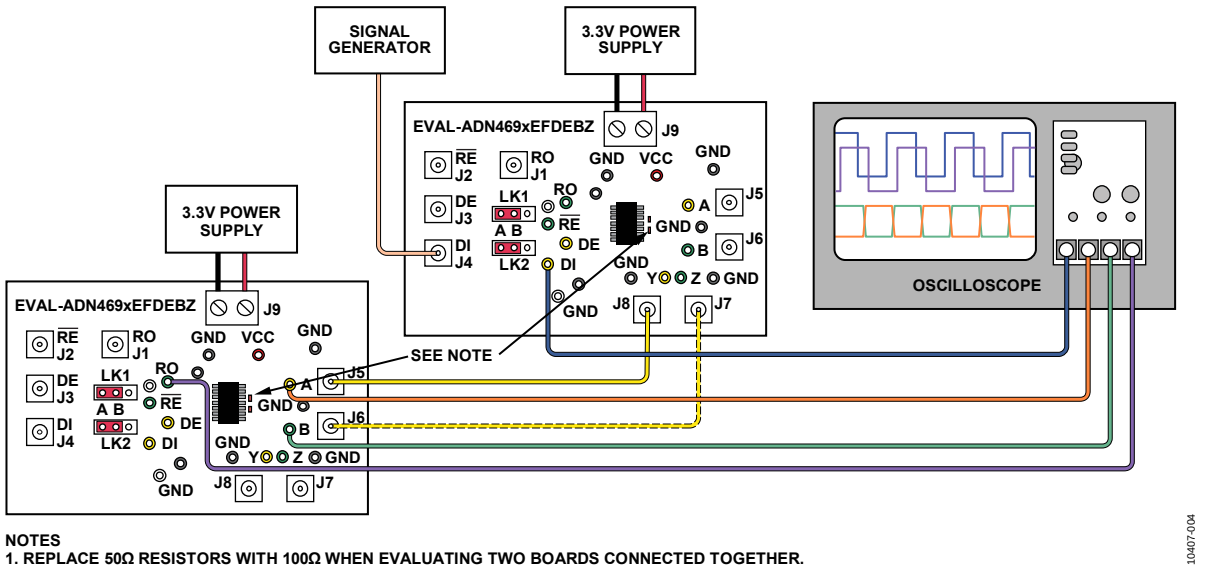

Figure 4. EVAL-ADN469xEFDEBZ Two Board Point-to-Point Evaluation

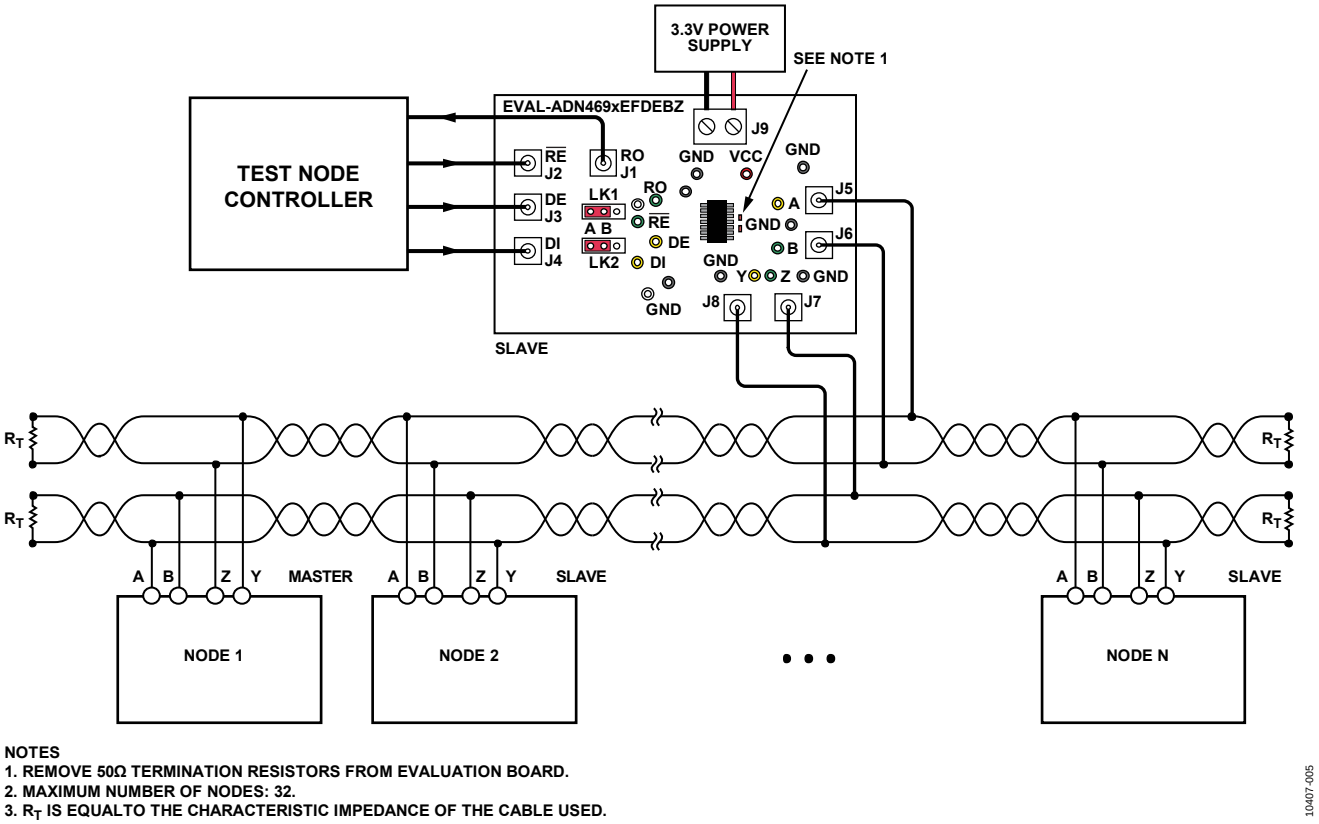

Figure 5. EVAL-ADN469xEFDEBZ Application Evaluation Connected to Bus and Control Board

Table 2. Jumper Configuration

Link	Connection	Description
LK1	A	Connects $\overline{RE}$ to VCC (disables receiver output). Disconnect J2 input.
	B	Connects $\overline{RE}$ to GND (enables receiver output). Disconnect J2 input.
	None	Allows $\overline{RE}$ input on J2.
LK2	A	Connects DE to VCC (enables driver outputs). Disconnect J3 input.
	B	Connects DE to GND (disables driver outputs). Disconnect J3 input.
	None	Allows DE input on J3.

EVALUATION BOARD SCHEMATIC AND LAYOUT

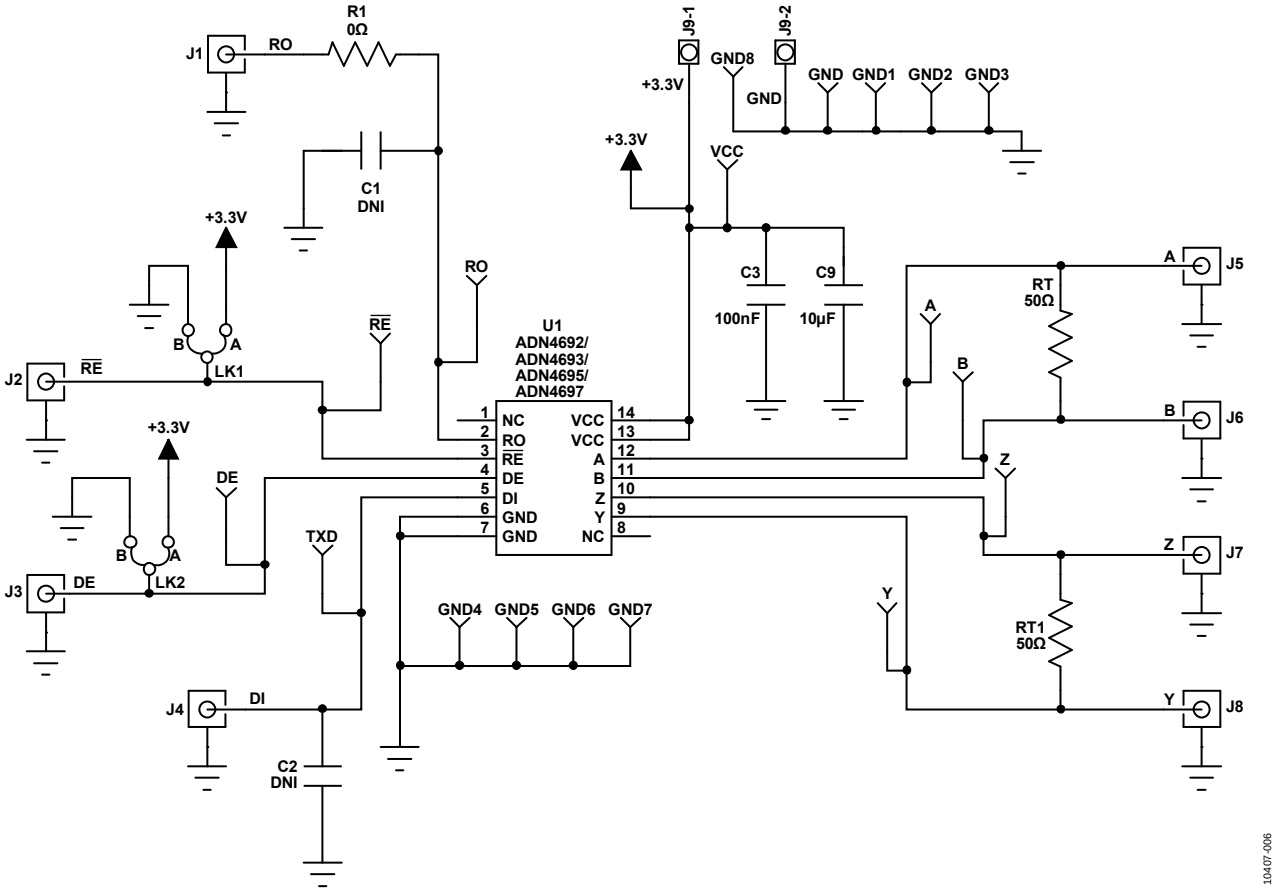

Figure 6. EVAL-ADN469xEFDEBZ Schematic

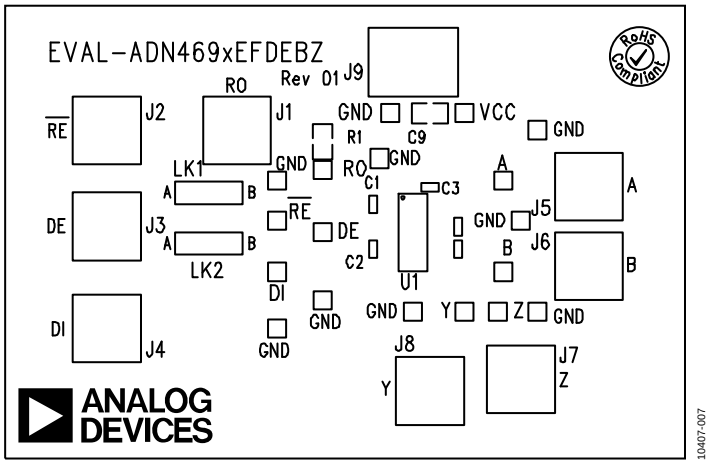

Figure 7. EVAL-ADN469xEFDEBZ Silkscreen

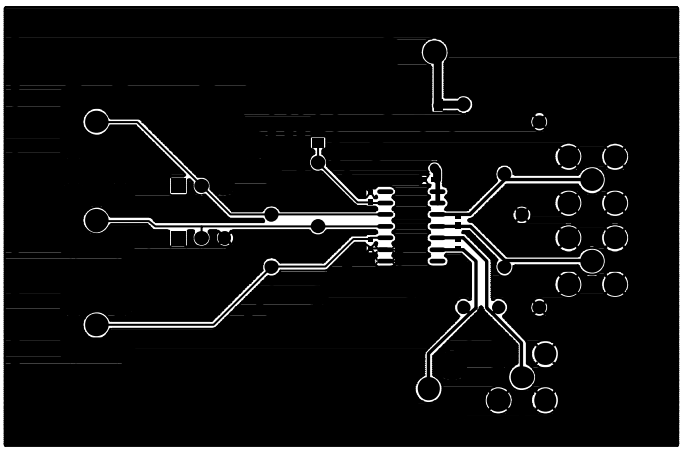

Figure 8. EVAL-ADN469xEFDEBZ Component Side

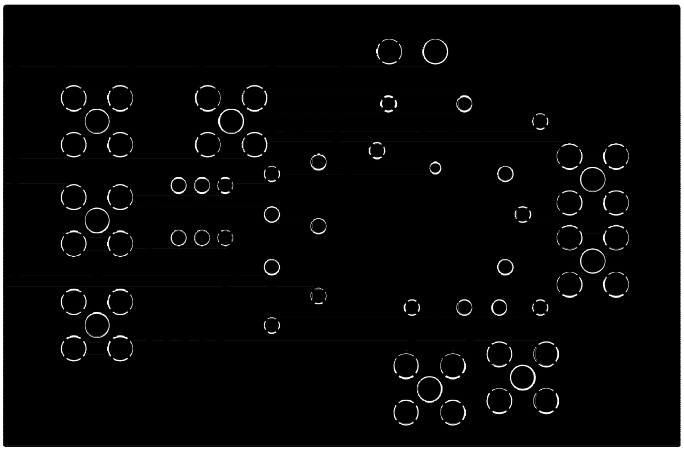

Figure 9. EVAL-ADN469xEFDEBZ Internal Layer 2

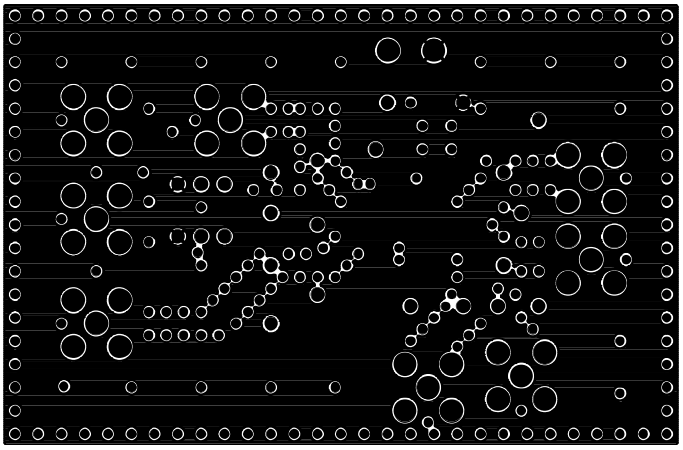

Figure 10. EVAL-ADN469xEFDEBZ Internal Layer 3

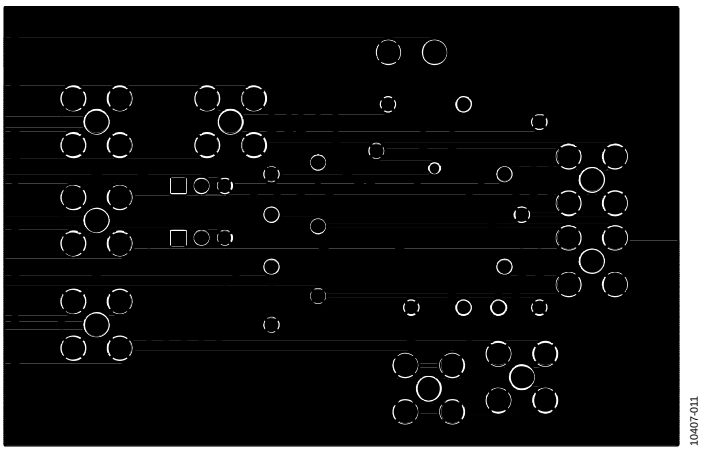

Figure 11. EVAL-ADN469xEFDEBZ Solder Side

ORDERING INFORMATION

BILL OF MATERIALS

Table 3.

Quantity	Reference Designator	Description	Supplier/Part Number
2	C1, C2	Not placed/optional	Not applicable
1	C3	Capacitor, 100 nF, 0805	Multicomp/MCCA000274
1	C9	Capacitor, 10 µF, 0805	AVX/0805ZD106KAT2A
4	A, DE, TXD, Y	Test point, yellow	Vero Technologies/20-313140
4	B, $\overline{RE}$, RO, Z	Test point, green	Vero Technologies/20-313138
9	GND (GND1 to GND8)	Test point, black (optional)	Vero Technologies/20-2137
8	J1 to J8	Connector, SMB jack	Multicomp/24-14-2-TGG
1	J9	2-way terminal block	Lumberg/KRM 02
2	LK1, LK2	3-pin (1 × 3) 0.1" header and shorting block	Harwin/M20-9990346 and Harwin/M7566-05
1	R1	Resistor, 0 Ω, 0805	Vishay Draloric/CRCW08050000Z0EA
2	RT1, RT	Resistor, 100 Ω, 0402	Vishay Draloric/CRCW0402100RFKEAHP
1	U1	16-lead SOIC (not placed)	Analog Devices/ADN4692E, ADN4693E, ADN4695E, or ADN4697E
1	VCC	Test point, red	Vero Technologies/20-313137

RELATED LINKS

Resource	Description
ADN4692E	Product Page, 3.3 V, 100 Mbps, Full-Duplex, High Speed M-LVDS Transceiver with Type 1 Receiver
ADN4693E	Product Page, 3.3 V, 200 Mbps, Full-Duplex, High Speed M-LVDS Transceiver with Type 1 Receiver
ADN4695E	Product Page, 3.3 V, 100 Mbps, Full-Duplex, High Speed M-LVDS Transceiver with Type 2 Receiver
ADN4697E	Product Page, 3.3 V, 200 Mbps, Full-Duplex, High Speed M-LVDS Transceiver with Type 2 Receiver

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