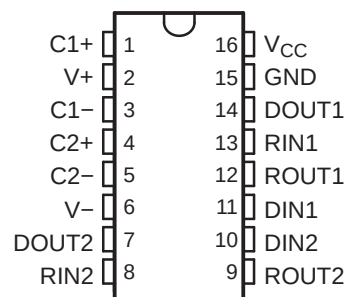


## FEATURES

- Operates With 3-V to 5.5-V  $V_{CC}$  Supply
- Operates up to 1 Mbit/s
- Low Supply Current . . . 300  $\mu$ A Typ
- External Capacitors . . .  $4 \times 0.1 \mu$ F
- Accept 5-V Logic Input With 3.3-V Supply
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection for RS-232 Pins
  - $\pm 15$ -kV Human-Body Model (HBM)
  - $\pm 15$ -kV IEC 61000-4-2 Air-Gap Discharge
  - $\pm 8$ -kV IEC 61000-4-2 Contact Discharge

D, DB, DW, OR PW PACKAGE  
(TOP VIEW)



## APPLICATIONS

- Battery-Powered Systems
- PDAs
- Notebooks
- Laptops
- Palmtop PCs
- Hand-Held Equipment

## DESCRIPTION/ORDERING INFORMATION

The TRSF3232E consists of two line drivers, two line receivers, and a dual charge-pump circuit with  $\pm 15$ -kV ESD protection pin to pin (serial-port connection pins, including GND). This device provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. The TRSF3232E operates at data signaling rates up to 1 Mbit/s and a driver output slew rate of 14 V/ $\mu$ s to 150 V/ $\mu$ s.

### ORDERING INFORMATION

| $T_A$         | PACKAGE <sup>(1)(2)</sup> |              | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---------------|---------------------------|--------------|-----------------------|------------------|
| 0°C to 70°C   | SOIC – D                  | Tube of 40   | TRSF3232ECD           | TRSF3232EC       |
|               |                           | Reel of 2500 | TRSF3232ECDR          |                  |
|               | SOIC – DW                 | Tube of 40   | TRSF3232ECDW          | TRSF3232EC       |
|               |                           | Reel of 2000 | TRSF3232ECDWR         |                  |
|               | SSOP – DB                 | Reel of 2000 | TRSF3232ECDBR         | RT32EC           |
|               | TSSOP – PW                | Tube of 90   | TRSF3232ECPW          | RT32EC           |
|               |                           | Reel of 2000 | TRSF3232ECPWR         |                  |
| –40°C to 85°C | SOIC – D                  | Tube of 40   | TRSF3232EID           | TRSF3232EI       |
|               |                           | SOIC – DW    | TRSF3232EIDR          |                  |
|               | SOIC – DW                 | Tube of 40   | TRSF3232EIDW          | TRSF3232EI       |
|               |                           | TSSOP – PW   | TRSF3232EIDWR         |                  |
|               | SSOP – DB                 | Reel of 2000 | TRSF3232EIDBR         | RT32EI           |
|               | TSSOP – PW                | Tube of 90   | TRSF3232EIPW          | RT32EI           |
|               |                           | Reel of 2000 | TRSF3232EIPWR         |                  |

(1) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).

(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

**TRSF3232E**  
**3-V TO 5.5-V TWO-CHANNEL RS-232 1-Mbit/s LINE DRIVER/RECEIVER**  
**WITH  $\pm 15$ -kV IEC ESD PROTECTION**

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**Table 1. 1-Mbit/s RS-232 Parts**

| TEMPERATURE RANGE | PART NO.  | NO. OF DRIVERS | NO. OF RECEIVERS | ESD                                                                                   | SUPPLY $V_{CC}$ (V) | FEATURE                              | PIN/ PACKAGE                   |
|-------------------|-----------|----------------|------------------|---------------------------------------------------------------------------------------|---------------------|--------------------------------------|--------------------------------|
| 0°C to 70°C       | TRSF3221E | 1              | 1                | $\pm 15$ -kV Air-Gap Discharge,<br>$\pm 8$ -kV Contact Discharge,<br>$\pm 15$ -kV HBM | 3.3 or 5            | Auto-powerdown                       | 16-pin<br>SOIC, SSOP,<br>TSSOP |
|                   | TRSF3232E | 2              | 2                | $\pm 15$ -kV Air-Gap Discharge,<br>$\pm 8$ -kV Contact Discharge,<br>$\pm 15$ -kV HBM | 3.3 or 5            | Low pin count                        | 16-pin<br>SOIC, SSOP,<br>TSSOP |
|                   | TRS3227   | 1              | 1                | $\pm 8$ -kV Air-Gap Discharge,<br>$\pm 8$ -kV Contact Discharge,<br>$\pm 15$ -kV HBM  | 3.3 or 5            | Auto-powerdown<br>plus, ready signal | 16-pin<br>SSOP                 |
|                   | TRSF3221  | 1              | 1                | $\pm 15$ -kV HBM                                                                      | 3.3 or 5            | Auto-powerdown                       | 16-pin<br>SOIC, SSOP,<br>TSSOP |
|                   | TRSF3222  | 2              | 2                | $\pm 15$ -kV HBM                                                                      | 3.3 or 5            | Enable,<br>powerdown<br>signal       | 20-pin<br>SOIC, SSOP,<br>TSSOP |
|                   | TRSF3223  | 2              | 2                | $\pm 15$ -kV HBM                                                                      | 3.5 or 5            | Auto-powerdown,<br>enable signal     | 20-pin<br>SOIC, SSOP,<br>TSSOP |
|                   | TRSF3232  | 2              | 2                | $\pm 15$ -kV HBM                                                                      | 3.3 or 5            | Low pin count                        | 16-pin<br>SOIC, SSOP,<br>TSSOP |
|                   | TRSF3238  | 5              | 3                | $\pm 15$ -kV HBM                                                                      | 3.3 or 5            | Auto-powerdown<br>plus               | 28-pin<br>SOIC, SSOP,<br>TSSOP |
|                   | TRSF3243  | 3              | 5                | $\pm 15$ -kV HBM                                                                      | 3.3 or 5            | Auto-powerdown                       | 28-pin<br>SOIC, SSOP,<br>TSSOP |
| –40°C to 85°C     | TRSF3221E | 1              | 1                | $\pm 15$ -kV Air-Gap Discharge,<br>$\pm 8$ -kV Contact Discharge,<br>$\pm 15$ -kV HBM | 3.3 or 5            | Auto-powerdown                       | 16-pin<br>SOIC, SSOP,<br>TSSOP |
|                   | TRSF3232E | 2              | 2                | $\pm 15$ -kV Air-Gap Discharge,<br>$\pm 8$ -kV Contact Discharge,<br>$\pm 15$ -kV HBM | 3.3 or 5            | Low pin count                        | 16-pin<br>SOIC, SSOP,<br>TSSOP |
|                   | TRS3227   | 1              | 1                | $\pm 8$ -kV Air-Gap Discharge,<br>$\pm 8$ -kV Contact Discharge,<br>$\pm 15$ -kV HBM  | 3.3 or 5            | Auto-powerdown<br>plus, ready signal | 16-pin<br>SSOP                 |
|                   | TRSF3221  | 1              | 1                | $\pm 15$ -kV HBM                                                                      | 3.3 or 5            | Auto-powerdown                       | 16-pin<br>SOIC, SSOP,<br>TSSOP |
|                   | TRSF3222  | 2              | 2                | $\pm 15$ -kV HBM                                                                      | 3.3 or 5            | Enable,<br>powerdown<br>signal       | 20-pin<br>SOIC, SSOP,<br>TSSOP |
|                   | TRSF3223  | 2              | 2                | $\pm 15$ -kV HBM                                                                      | 3.3 or 5            | Auto-powerdown,<br>enable signal     | 20-pin<br>SOIC, SSOP,<br>TSSOP |
|                   | TRSF3232  | 2              | 2                | $\pm 15$ -kV HBM                                                                      | 3.3 or 5            | Low pin count                        | 16-pin<br>SOIC, SSOP,<br>TSSOP |
|                   | TRSF3238  | 5              | 3                | $\pm 15$ -kV HBM                                                                      | 3.3 or 5            | Auto-powerdown<br>plus               | 28-pin<br>SOIC, SSOP,<br>TSSOP |
|                   | TRSF3243  | 3              | 5                | $\pm 15$ -kV HBM                                                                      | 3.3 or 5            | Auto-powerdown                       | 28-pin<br>SOIC, SSOP,<br>TSSOP |

## FUNCTION TABLES

### Each Driver<sup>(1)</sup>

| INPUT<br>DIN | OUTPUT<br>DOUT |
|--------------|----------------|
| L            | H              |
| H            | L              |

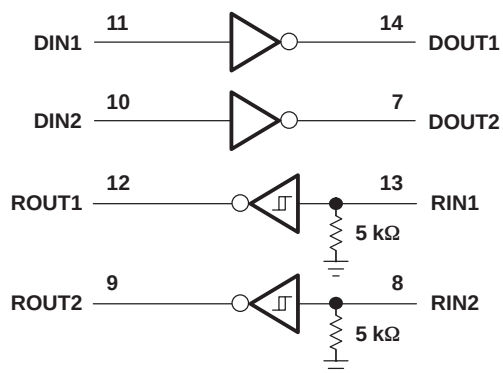
(1) H = high level, L = low level

### Each Receiver<sup>(1)</sup>

| INPUT<br>RIN | OUTPUT<br>ROUT |
|--------------|----------------|
| L            | H              |
| H            | L              |
| Open         | H              |

(1) H = high level, L = low level,  
Open = input disconnected or  
connected driver off

## LOGIC DIAGRAM (POSITIVE LOGIC)



# TRSF3232E

## 3-V TO 5.5-V TWO-CHANNEL RS-232 1-Mbit/s LINE DRIVER/RECEIVER

### WITH $\pm 15$ -kV IEC ESD PROTECTION

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#### Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

|                 |                                                     |            | MIN   | MAX            | UNIT |
|-----------------|-----------------------------------------------------|------------|-------|----------------|------|
| $V_{CC}$        | Supply voltage range <sup>(2)</sup>                 |            | –0.3  | 6              | V    |
| $V_{+}$         | Positive-output supply voltage range <sup>(2)</sup> |            | –0.3  | 7              | V    |
| $V_{-}$         | Negative-output supply voltage range <sup>(2)</sup> |            | 0.3   | –7             | V    |
| $V_{+} - V_{-}$ | Supply voltage difference <sup>(2)</sup>            |            |       | 13             | V    |
| $V_I$           | Input voltage range                                 | Drivers    | –0.3  | 6              | V    |
|                 |                                                     | Receivers  | –25   | 25             |      |
| $V_O$           | Output voltage range                                | Drivers    | –13.2 | 13.2           | V    |
|                 |                                                     | Receivers  | –0.3  | $V_{CC} + 0.3$ |      |
| $\theta_{JA}$   | Package thermal impedance <sup>(3)(4)</sup>         | D package  |       | 82             | °C/W |
|                 |                                                     | DB package |       | 46             |      |
|                 |                                                     | DW package |       | 57             |      |
|                 |                                                     | PW package |       | 108            |      |
| $T_J$           | Operating virtual junction temperature              |            |       | 150            | °C   |
| $T_{stg}$       | Storage temperature range                           |            | –65   | 150            | °C   |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to network GND.
- (3) Maximum power dissipation is a function of  $T_J(\text{max})$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_J(\text{max}) - T_A)/\theta_{JA}$ . Operating at the absolute maximum  $T_J$  of 150°C can affect reliability.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

#### Recommended Operating Conditions<sup>(1)</sup>

|                |                                 |                          | MIN                      | NOM | MAX | UNIT |
|----------------|---------------------------------|--------------------------|--------------------------|-----|-----|------|
| Supply voltage |                                 | $V_{CC} = 3.3 \text{ V}$ | 3                        | 3.3 | 3.6 | V    |
|                |                                 | $V_{CC} = 5 \text{ V}$   | 4.5                      | 5   | 5.5 |      |
| $V_{IH}$       | Driver high-level input voltage | DIN                      | $V_{CC} = 3.3 \text{ V}$ | 2   |     | V    |
|                |                                 |                          |                          |     |     |      |
| $V_{IL}$       | Driver low-level input voltage  | DIN                      | $V_{CC} = 5 \text{ V}$   | 2.4 |     | V    |
|                |                                 |                          |                          |     |     |      |
| $V_I$          | Driver input voltage            | DIN                      | 0                        | 5.5 |     | V    |
|                |                                 |                          |                          |     |     |      |
| $T_A$          | Operating free-air temperature  | TRSF3232EI               | –40                      |     | 85  | °C   |
|                |                                 | TRSF3232EC               | 0                        |     | 70  |      |

- (1) Test conditions are  $C1-C4 = 0.1 \mu\text{F}$  at  $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ;  $C1 = 0.047 \mu\text{F}$ ,  $C2-C4 = 0.33 \mu\text{F}$  at  $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$  (see Figure 4).

#### Electrical Characteristics<sup>(1)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN                                                | TYP <sup>(2)</sup> | MAX | UNIT |
|-----------|-----------------|----------------------------------------------------|--------------------|-----|------|
| $I_{CC}$  | Supply current  | No load, $V_{CC} = 3.3 \text{ V}$ or $5 \text{ V}$ | 0.3                | 1   | mA   |

- (1) Test conditions are  $C1-C4 = 0.1 \mu\text{F}$  at  $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ;  $C1 = 0.047 \mu\text{F}$ ,  $C2-C4 = 0.33 \mu\text{F}$  at  $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$  (see Figure 4).
- (2) All typical values are at  $V_{CC} = 3.3 \text{ V}$  or  $V_{CC} = 5 \text{ V}$ , and  $T_A = 25^\circ\text{C}$ .

## DRIVER SECTION

### Electrical Characteristics<sup>(1)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                                   | TEST CONDITIONS                                                     | MIN | TYP <sup>(2)</sup> | MAX      | UNIT     |
|-------------------------------------------------------------|---------------------------------------------------------------------|-----|--------------------|----------|----------|
| V <sub>OH</sub> High-level output voltage                   | DOUT at R <sub>L</sub> = 3 k $\Omega$ to GND, DIN = GND             | 5   | 5.5                |          | V        |
| V <sub>OL</sub> Low-level output voltage                    | DOUT at R <sub>L</sub> = 3 k $\Omega$ to GND, DIN = V <sub>CC</sub> | –5  | –5.4               |          | V        |
| I <sub>IH</sub> High-level input current                    | V <sub>I</sub> = V <sub>CC</sub>                                    |     | $\pm 0.01$         | $\pm 1$  | $\mu$ A  |
| I <sub>IL</sub> Low-level input current                     | V <sub>I</sub> at GND                                               |     | $\pm 0.01$         | $\pm 1$  | $\mu$ A  |
| I <sub>OS</sub> <sup>(3)</sup> Short-circuit output current | V <sub>CC</sub> = 3.6 V, V <sub>O</sub> = 0 V                       |     | $\pm 35$           | $\pm 60$ | mA       |
|                                                             | V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0 V                       |     | $\pm 35$           | $\pm 90$ |          |
| r <sub>o</sub> Output resistance                            | V <sub>CC</sub> , V+, and V– = 0 V, V <sub>O</sub> = $\pm 2$ V      | 300 | 10M                |          | $\Omega$ |

(1) Test conditions are C1–C4 = 0.1  $\mu$ F at V<sub>CC</sub> = 3.3 V  $\pm$  0.3 V; C1 = 0.047  $\mu$ F, C2–C4 = 0.33  $\mu$ F at V<sub>CC</sub> = 5 V  $\pm$  0.5 V (see Figure 4).

(2) All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

(3) Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.

### Switching Characteristics<sup>(1)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                                | TEST CONDITIONS                                                                                             | MIN | TYP <sup>(2)</sup>                                         | MAX  | UNIT       |
|----------------------------------------------------------|-------------------------------------------------------------------------------------------------------------|-----|------------------------------------------------------------|------|------------|
| Maximum data rate<br>(see Figure 1)                      | R <sub>L</sub> = 3 k $\Omega$ ,<br>One DOUT switching                                                       |     | C <sub>L</sub> = 250 pF, V <sub>CC</sub> = 3 V to 4.5 V    | 1000 | kbit/s     |
|                                                          |                                                                                                             |     | C <sub>L</sub> = 1000 pF, V <sub>CC</sub> = 3.5 V to 5.5 V | 1000 |            |
| t <sub>sk(p)</sub> Pulse skew <sup>(3)</sup>             | C <sub>L</sub> = 150 pF to 2500 pF, R <sub>L</sub> = 3 k $\Omega$ to 7 k $\Omega$ , See Figure 2            |     | 300                                                        |      | ns         |
| SR(tr) Slew rate,<br>transition region<br>(see Figure 1) | R <sub>L</sub> = 3 k $\Omega$ to 7 k $\Omega$ , C <sub>L</sub> = 150 pF to 1000 pF, V <sub>CC</sub> = 3.3 V |     | 14                                                         | 150  | V/ $\mu$ s |

(1) Test conditions are C1–C4 = 0.1  $\mu$ F at V<sub>CC</sub> = 3.3 V  $\pm$  0.3 V; C1 = 0.047  $\mu$ F, C2–C4 = 0.33  $\mu$ F at V<sub>CC</sub> = 5 V  $\pm$  0.5 V (see Figure 4).

(2) All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

(3) Pulse skew is defined as |t<sub>PLH</sub> – t<sub>PHL</sub>| of each channel of the same device.

## ESD Protection

| TERMINAL |       | TEST CONDITIONS                 | TYP      | UNIT |
|----------|-------|---------------------------------|----------|------|
| NAME     | NO.   |                                 |          |      |
| DOUT     | 7, 14 | HBM                             | $\pm 15$ | kV   |
|          |       | IEC 61000-4-2 Air-Gap Discharge | $\pm 15$ |      |
|          |       | IEC 61000-4-2 Contact Discharge | $\pm 8$  |      |

**TRSF3232E**  
**3-V TO 5.5-V TWO-CHANNEL RS-232 1-Mbit/s LINE DRIVER/RECEIVER**  
**WITH  $\pm 15$ -kV IEC ESD PROTECTION**

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## RECEIVER SECTION

### Electrical Characteristics<sup>(1)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                                                | TEST CONDITIONS                          | MIN                   | TYP <sup>(2)</sup>    | MAX | UNIT       |
|--------------------------------------------------------------------------|------------------------------------------|-----------------------|-----------------------|-----|------------|
| V <sub>OH</sub> High-level output voltage                                | I <sub>OH</sub> = –1 mA                  | V <sub>CC</sub> – 0.6 | V <sub>CC</sub> – 0.1 |     | V          |
| V <sub>OL</sub> Low-level output voltage                                 | I <sub>OL</sub> = 1.6 mA                 |                       |                       | 0.4 | V          |
| V <sub>IT+</sub> Positive-going input threshold voltage                  | V <sub>CC</sub> = 3.3 V                  |                       | 1.5                   | 2.4 | V          |
|                                                                          | V <sub>CC</sub> = 5 V                    |                       | 1.8                   | 2.4 |            |
| V <sub>IT–</sub> Negative-going input threshold voltage                  | V <sub>CC</sub> = 3.3 V                  | 0.6                   | 1.2                   |     | V          |
|                                                                          | V <sub>CC</sub> = 5 V                    | 0.8                   | 1.5                   |     |            |
| V <sub>hys</sub> Input hysteresis (V <sub>IT+</sub> – V <sub>IT–</sub> ) |                                          |                       | 0.3                   |     | V          |
| r <sub>i</sub> Input resistance                                          | V <sub>I</sub> = $\pm 3$ V to $\pm 25$ V | 3                     | 5                     | 7   | k $\Omega$ |

(1) Test conditions are C1–C4 = 0.1  $\mu$ F at V<sub>CC</sub> = 3.3 V  $\pm$  0.3 V; C1 = 0.047  $\mu$ F, C2–C4 = 0.33  $\mu$ F at V<sub>CC</sub> = 5 V  $\pm$  0.5 V (see Figure 4).

(2) All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

### Switching Characteristics<sup>(1)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                                          | TEST CONDITIONS         | TYP <sup>(2)</sup> | UNIT |
|--------------------------------------------------------------------|-------------------------|--------------------|------|
| t <sub>PLH</sub> Propagation delay time, low- to high-level output | C <sub>L</sub> = 150 pF | 300                | ns   |
| t <sub>PHL</sub> Propagation delay time, high- to low-level output | C <sub>L</sub> = 150 pF | 300                | ns   |
| t <sub>sk(p)</sub> Pulse skew <sup>(3)</sup>                       |                         | 300                | ns   |

(1) Test conditions are C1–C4 = 0.1  $\mu$ F at V<sub>CC</sub> = 3.3 V  $\pm$  0.3 V; C1 = 0.047  $\mu$ F, C2–C4 = 0.33  $\mu$ F at V<sub>CC</sub> = 5 V  $\pm$  0.5 V (see Figure 4).

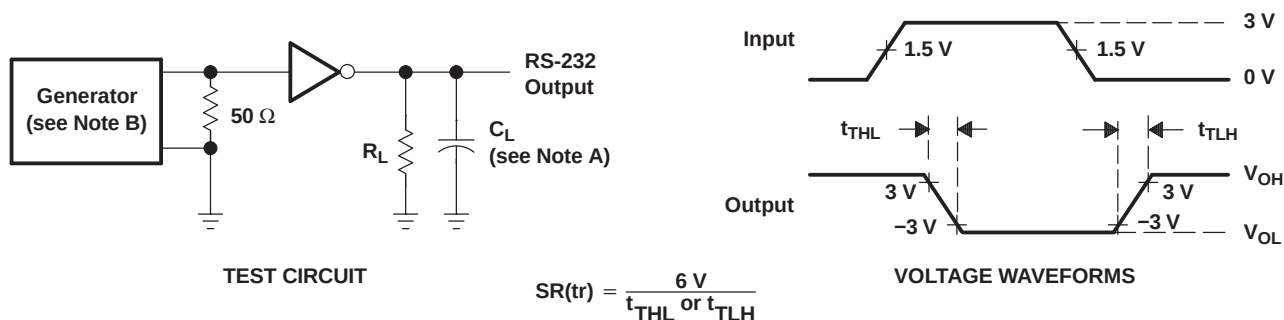
(2) All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

(3) Pulse skew is defined as |t<sub>PLH</sub> – t<sub>PHL</sub>| of each channel of the same device.

## ESD Protection

| TERMINAL |       | TEST CONDITIONS                 | TYP      | UNIT |
|----------|-------|---------------------------------|----------|------|
| NAME     | NO.   |                                 |          |      |
| RIN      | 8, 13 | HBM                             | $\pm 15$ | kV   |
|          |       | IEC 61000-4-2 Air-Gap Discharge | $\pm 15$ |      |
|          |       | IEC 61000-4-2 Contact Discharge | $\pm 8$  |      |

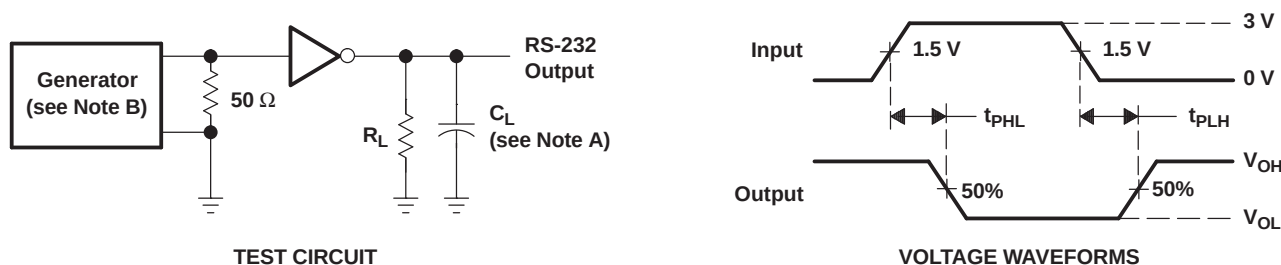
## PARAMETER MEASUREMENT INFORMATION



NOTES: A.  $C_L$  includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 250 kbit/s,  $Z_O = 50\ \Omega$ , 50% duty cycle,  $t_r \leq 10\ \text{ns}$ ,  $t_f \leq 10\ \text{ns}$ .

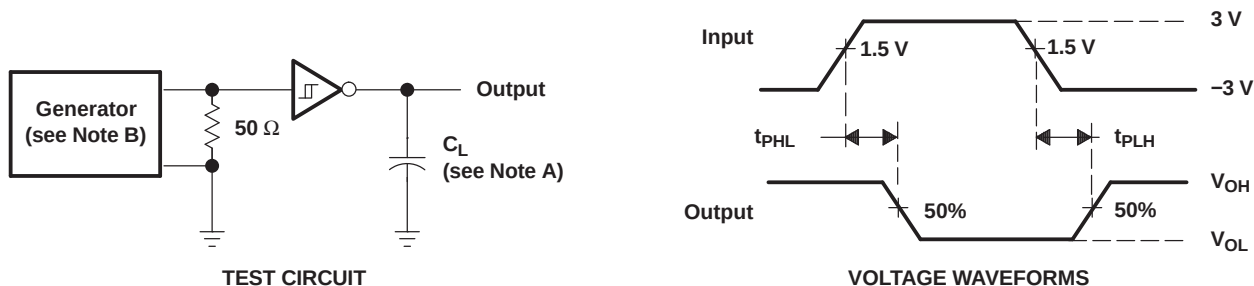
Figure 1. Driver Slew Rate



NOTES: A.  $C_L$  includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 250 kbit/s,  $Z_O = 50\ \Omega$ , 50% duty cycle,  $t_r \leq 10\ \text{ns}$ ,  $t_f \leq 10\ \text{ns}$ .

Figure 2. Driver Pulse Skew

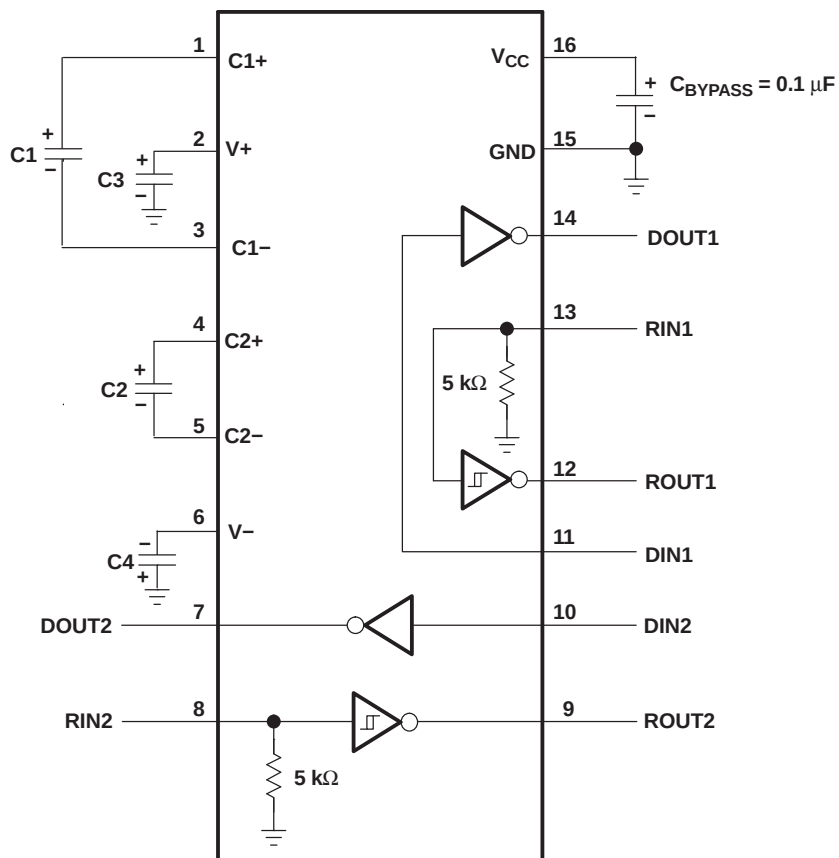


NOTES: A.  $C_L$  includes probe and jig capacitance.

B. The pulse generator has the following characteristics:  $Z_O = 50\ \Omega$ , 50% duty cycle,  $t_r \leq 10\ \text{ns}$ ,  $t_f \leq 10\ \text{ns}$ .

Figure 3. Receiver Propagation Delay Times

## APPLICATION INFORMATION



**V<sub>CC</sub> vs CAPACITOR VALUES**

| V <sub>CC</sub>   | C1            | C2, C3, C4   |
|-------------------|---------------|--------------|
| 3.3 V $\pm$ 0.3 V | 0.1 $\mu$ F   | 0.1 $\mu$ F  |
| 5 V $\pm$ 0.5 V   | 0.047 $\mu$ F | 0.33 $\mu$ F |
| 3 V to 5.5 V      | 0.1 $\mu$ F   | 0.47 $\mu$ F |

- A. C3 can be connected to V<sub>CC</sub> or GND.

**Figure 4. Typical Operating Circuit and Capacitor Values**



## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| TRSF3232ECD      | ACTIVE        | SOIC         | D                  | 16   | 40             | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | 0 to 70      | TRSF3232EC              | <a href="#">Samples</a> |
| TRSF3232ECDB     | ACTIVE        | SSOP         | DB                 | 16   | 80             | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | 0 to 70      | RT32EC                  | <a href="#">Samples</a> |
| TRSF3232ECDBR    | ACTIVE        | SSOP         | DB                 | 16   | 2000           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | 0 to 70      | RT32EC                  | <a href="#">Samples</a> |
| TRSF3232ECDBRG4  | ACTIVE        | SSOP         | DB                 | 16   | 2000           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | 0 to 70      | RT32EC                  | <a href="#">Samples</a> |
| TRSF3232ECDR     | ACTIVE        | SOIC         | D                  | 16   | 2500           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | 0 to 70      | TRSF3232EC              | <a href="#">Samples</a> |
| TRSF3232ECDWR    | ACTIVE        | SOIC         | DW                 | 16   | 2000           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | 0 to 70      | TRSF3232EC              | <a href="#">Samples</a> |
| TRSF3232ECPWR    | ACTIVE        | TSSOP        | PW                 | 16   | 2000           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | 0 to 70      | RT32EC                  | <a href="#">Samples</a> |
| TRSF3232EID      | ACTIVE        | SOIC         | D                  | 16   | 40             | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -40 to 85    | TRSF3232EI              | <a href="#">Samples</a> |
| TRSF3232EIDBR    | ACTIVE        | SSOP         | DB                 | 16   | 2000           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -40 to 85    | RT32EI                  | <a href="#">Samples</a> |
| TRSF3232EIDR     | ACTIVE        | SOIC         | D                  | 16   | 2500           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -40 to 85    | TRSF3232EI              | <a href="#">Samples</a> |
| TRSF3232EIDW     | ACTIVE        | SOIC         | DW                 | 16   | 40             | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -40 to 85    | TRSF3232EI              | <a href="#">Samples</a> |
| TRSF3232EIDWR    | ACTIVE        | SOIC         | DW                 | 16   | 2000           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -40 to 85    | TRSF3232EI              | <a href="#">Samples</a> |
| TRSF3232EIPW     | ACTIVE        | TSSOP        | PW                 | 16   | 90             | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -40 to 85    | RT32EI                  | <a href="#">Samples</a> |
| TRSF3232EIPWR    | ACTIVE        | TSSOP        | PW                 | 16   | 2000           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -40 to 85    | RT32EI                  | <a href="#">Samples</a> |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  $\leq 1000$ ppm threshold. Antimony trioxide based flame retardants must also meet the  $\leq 1000$ ppm threshold requirement.

<sup>(3)</sup> **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

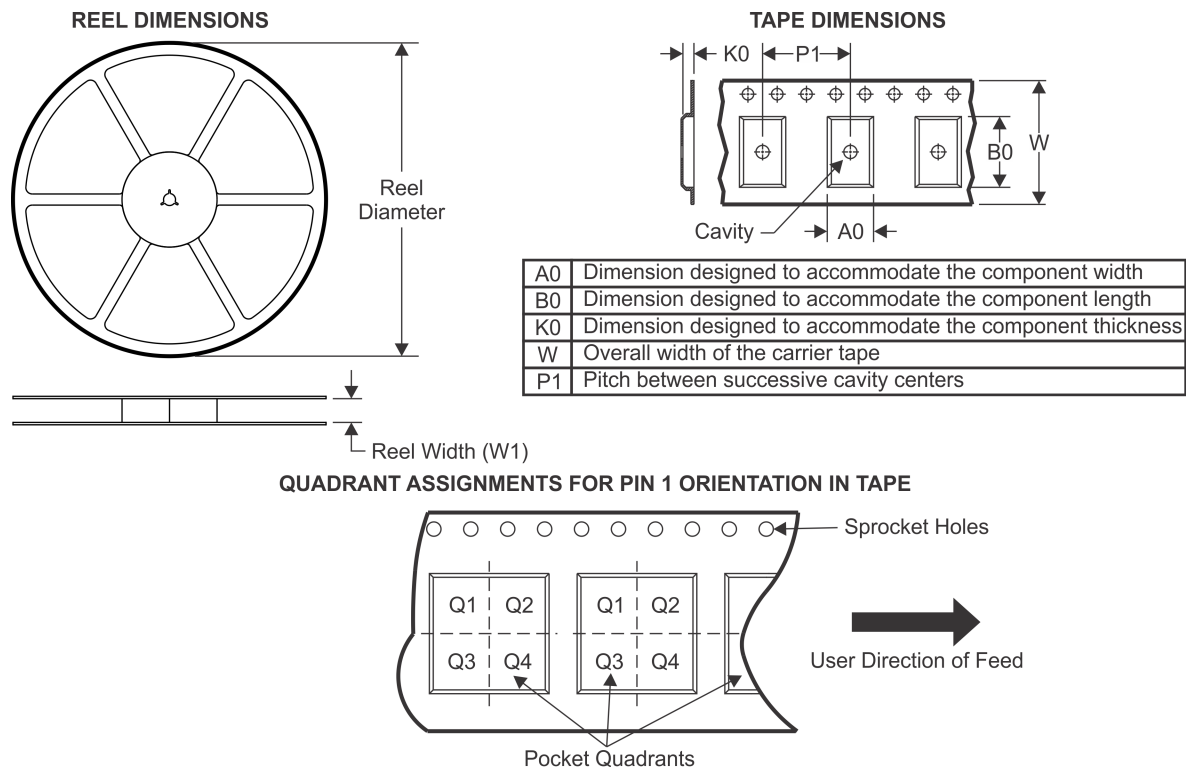
<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> **Lead/Ball Finish** - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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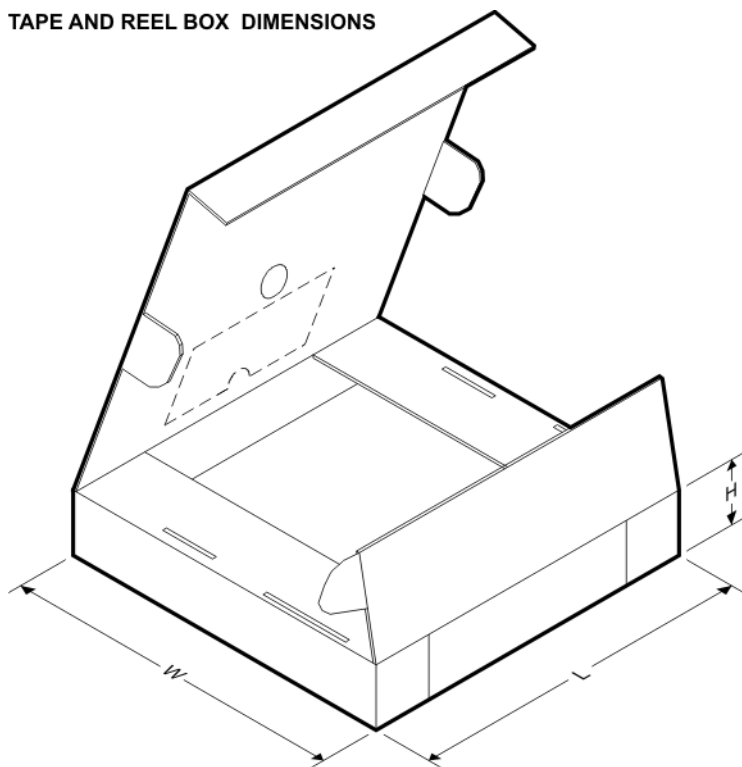
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**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TRSF3232ECDR  | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |
| TRSF3232ECDWR | SOIC         | DW              | 16   | 2000 | 330.0              | 16.4               | 10.75   | 10.7    | 2.7     | 12.0    | 16.0   | Q1            |
| TRSF3232ECPWR | TSSOP        | PW              | 16   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| TRSF3232EIDR  | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |
| TRSF3232EIDWR | SOIC         | DW              | 16   | 2000 | 330.0              | 16.4               | 10.75   | 10.7    | 2.7     | 12.0    | 16.0   | Q1            |
| TRSF3232EIPWR | TSSOP        | PW              | 16   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS

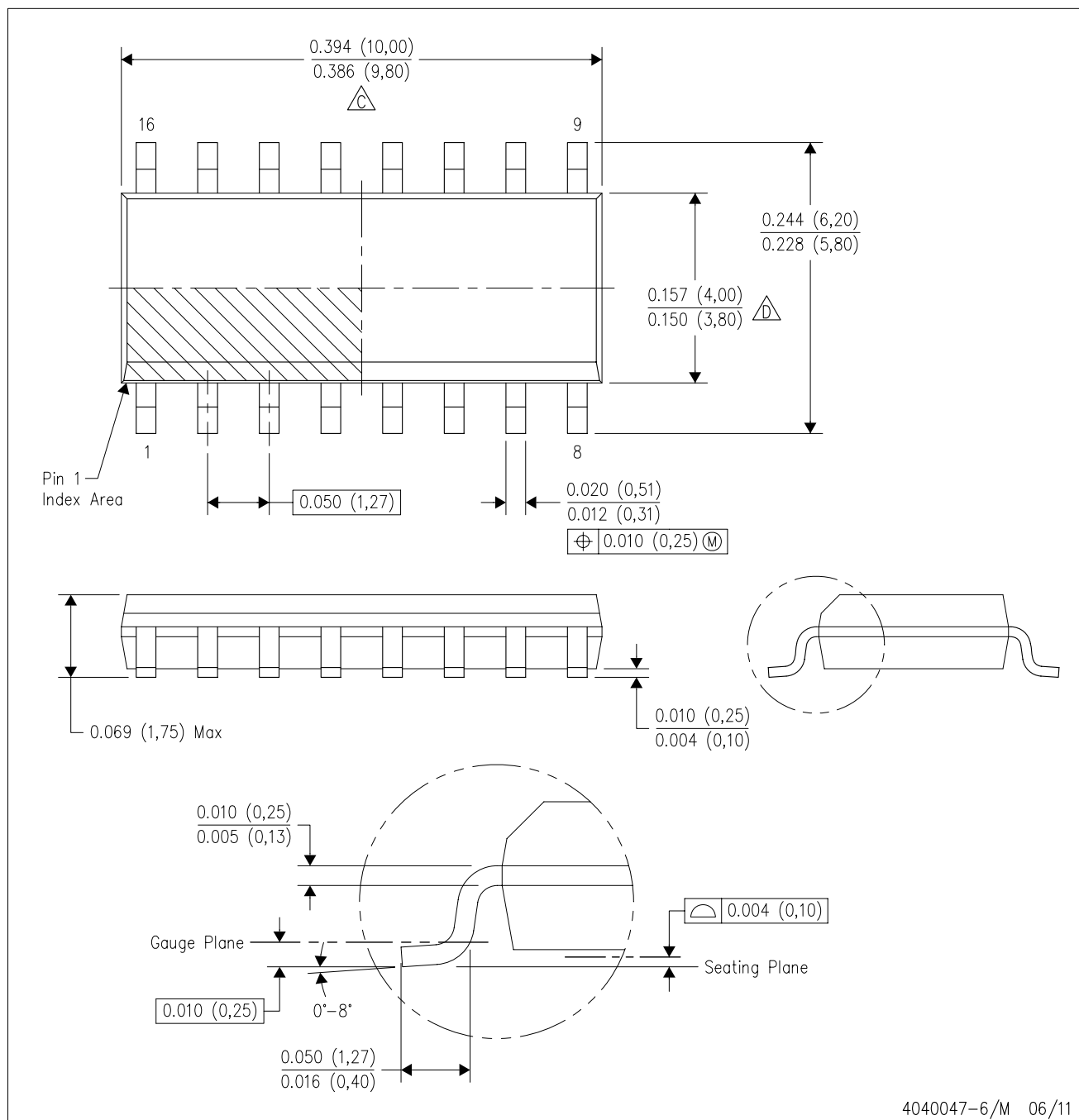


\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TRSF3232ECDR  | SOIC         | D               | 16   | 2500 | 367.0       | 367.0      | 38.0        |
| TRSF3232ECDWR | SOIC         | DW              | 16   | 2000 | 350.0       | 350.0      | 43.0        |
| TRSF3232ECPWR | TSSOP        | PW              | 16   | 2000 | 367.0       | 367.0      | 35.0        |
| TRSF3232EIDR  | SOIC         | D               | 16   | 2500 | 367.0       | 367.0      | 38.0        |
| TRSF3232EIDWR | SOIC         | DW              | 16   | 2000 | 350.0       | 350.0      | 43.0        |
| TRSF3232EIPWR | TSSOP        | PW              | 16   | 2000 | 367.0       | 367.0      | 35.0        |

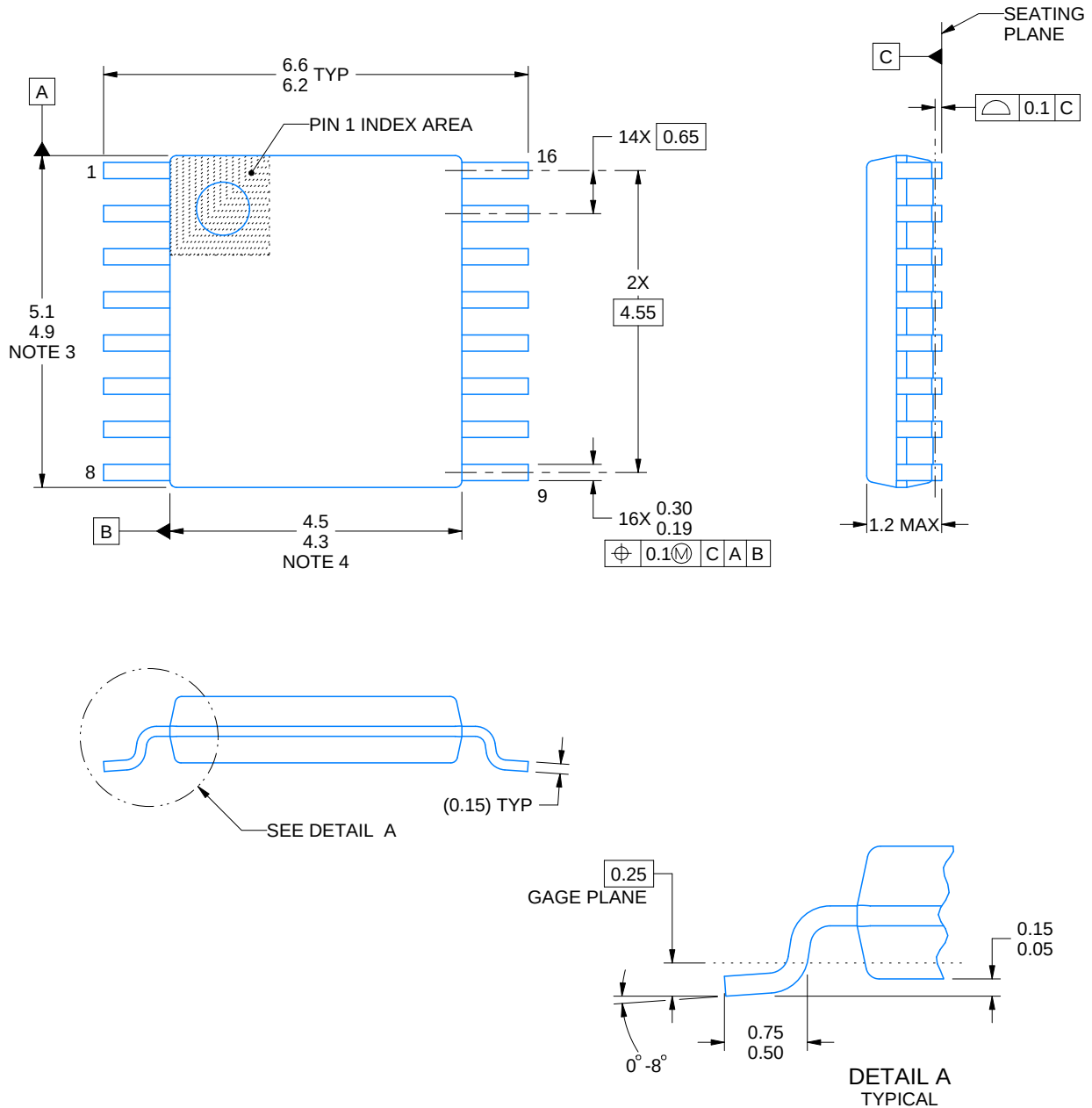
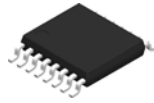
D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.



4220204/A 02/2017

## NOTES:

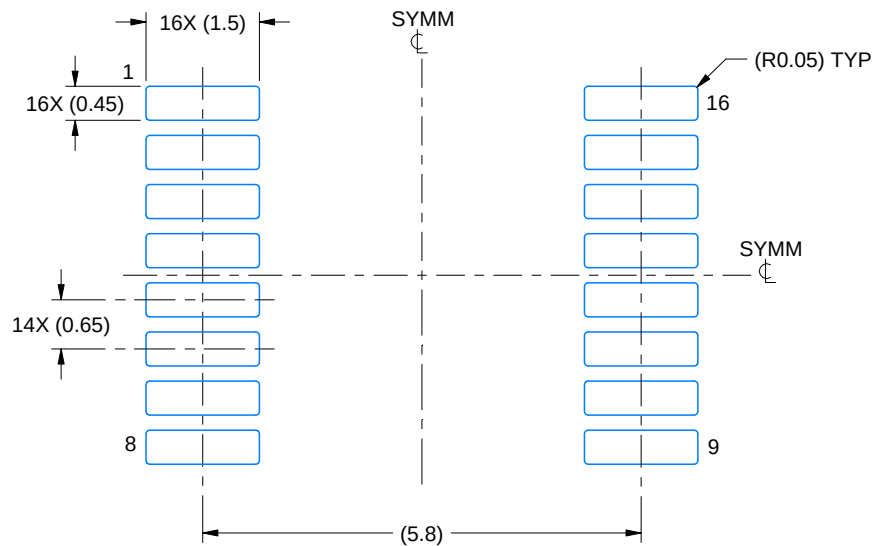
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

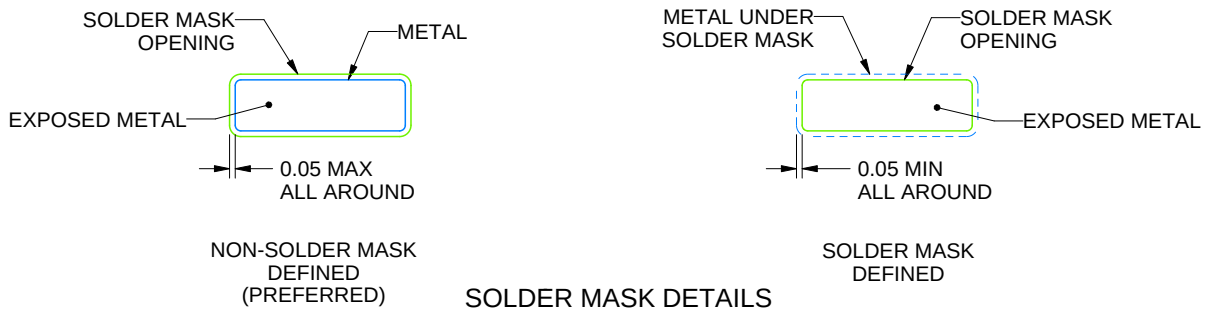
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

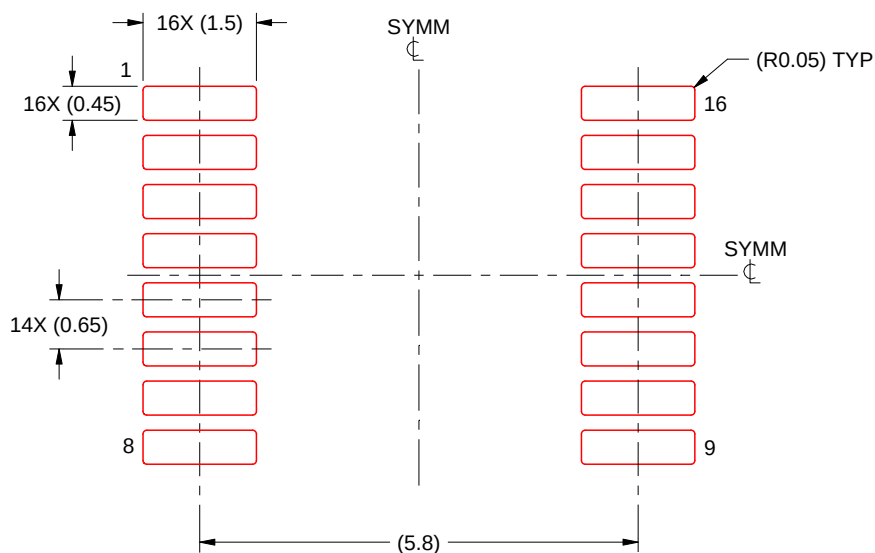
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



## GENERIC PACKAGE VIEW

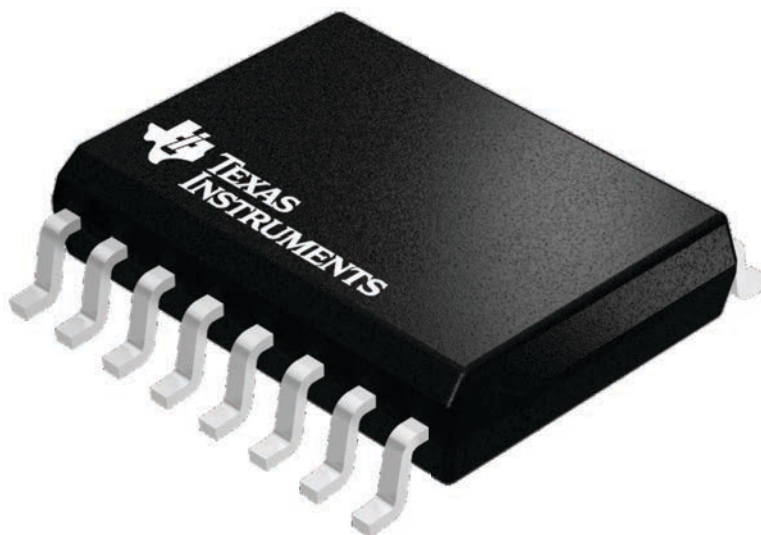
**DW 16**

**SOIC - 2.65 mm max height**

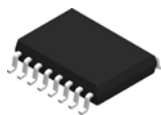
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4224780/A

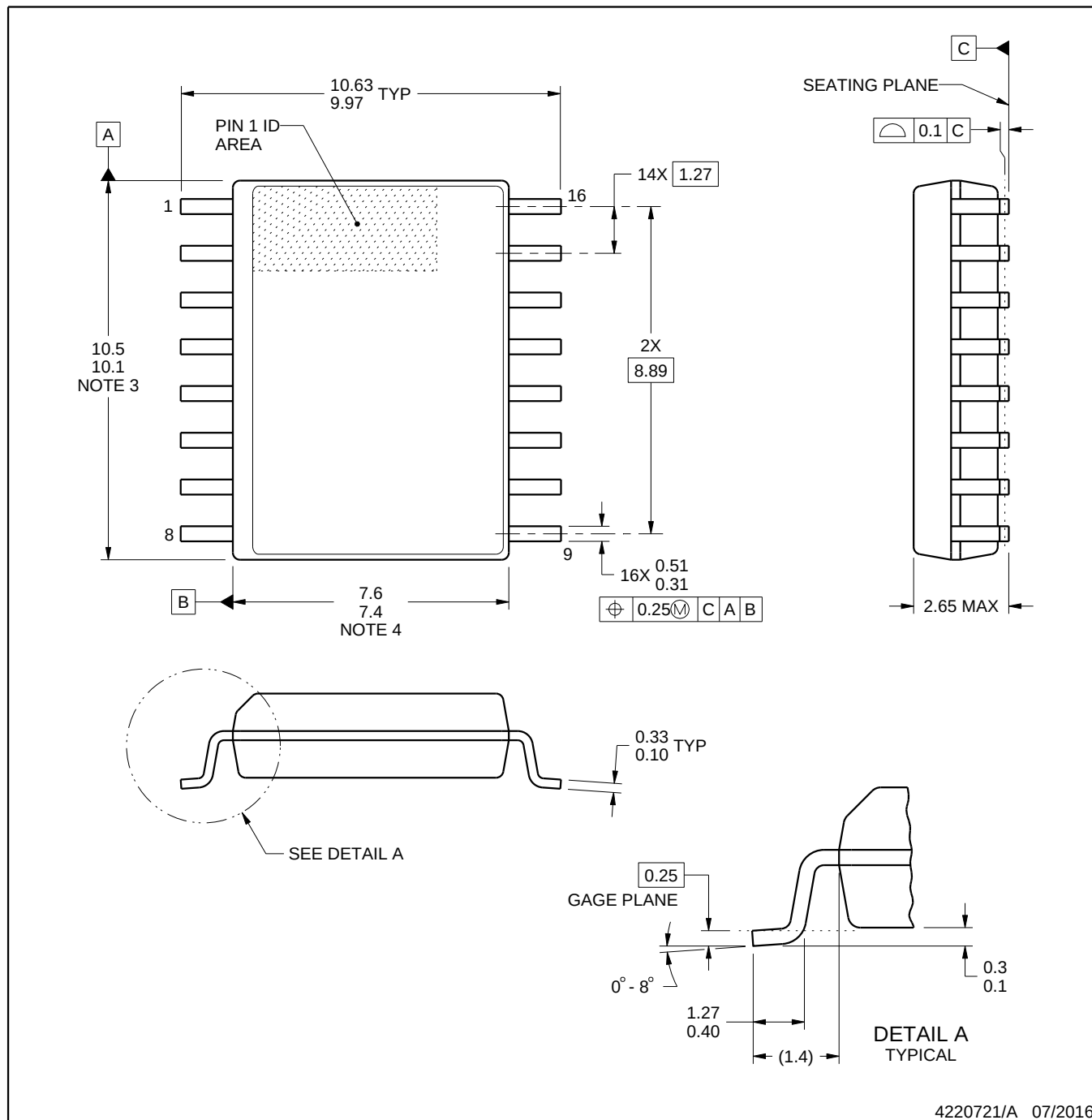


DW0016A

# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4220721/A 07/2016

### NOTES:

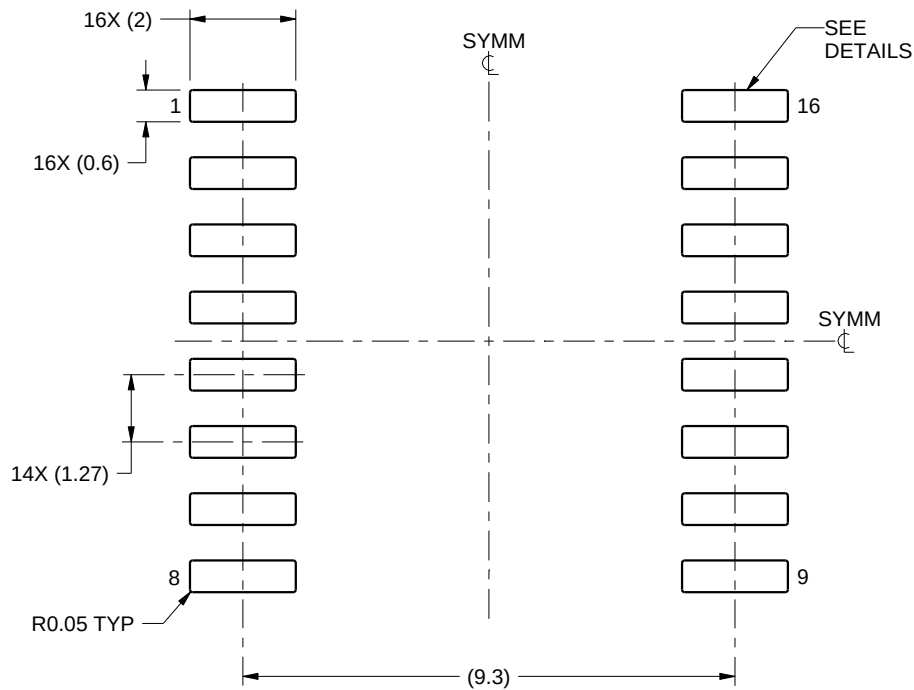
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

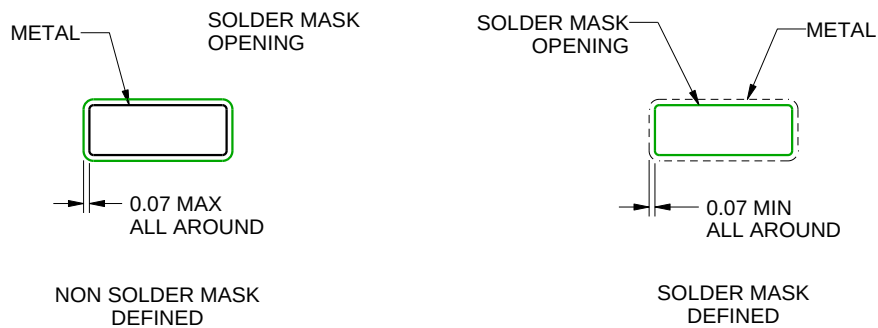
DW0016A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:7X



SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

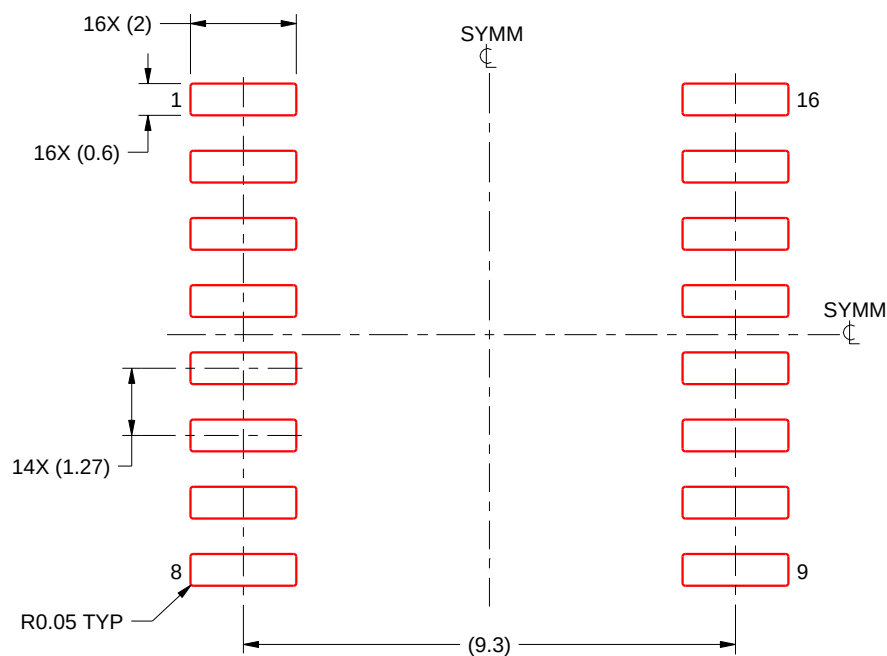
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0016A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:7X

4220721/A 07/2016

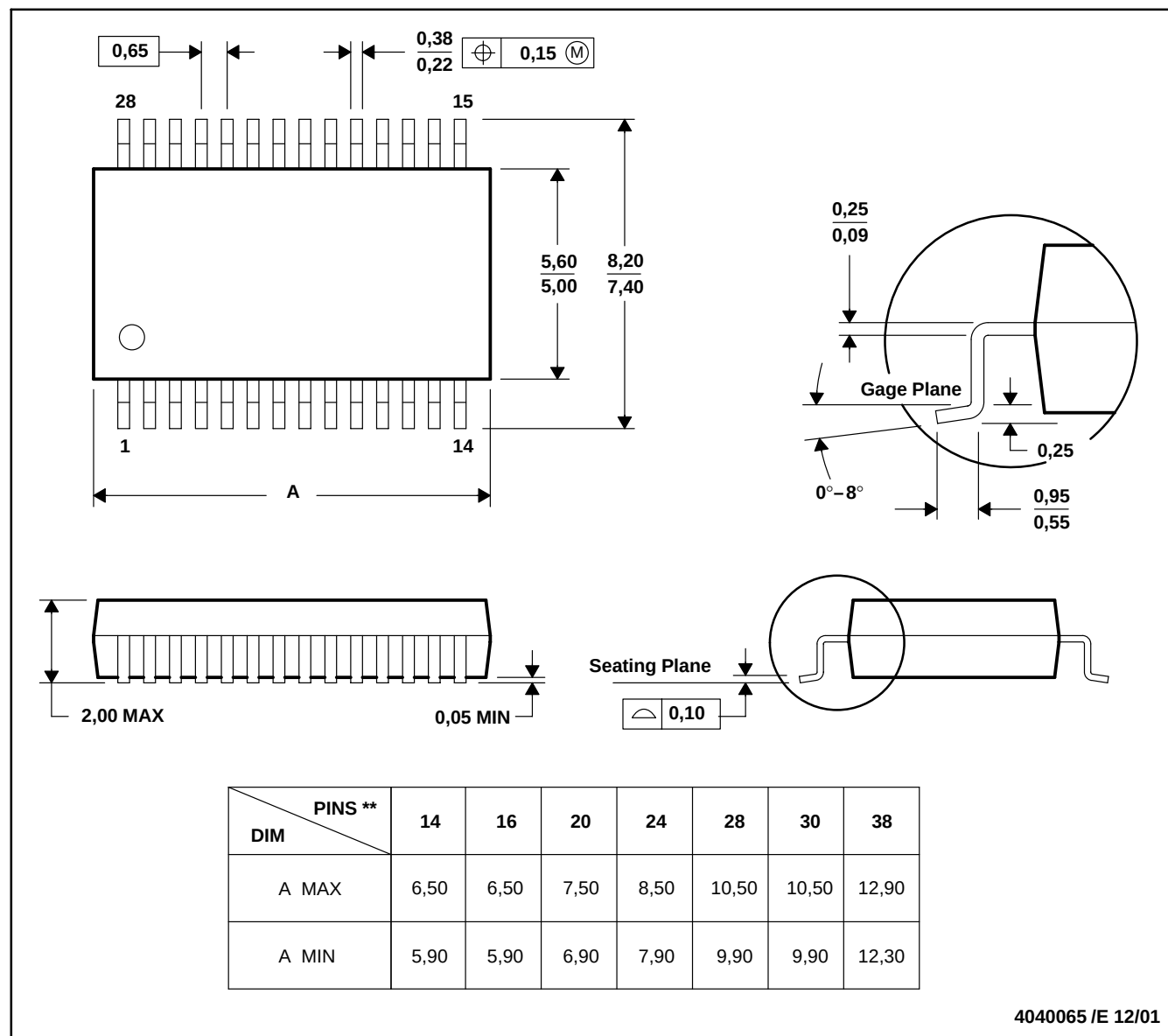
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## DB (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

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