



MX574BBJ322M265

Ultra-Low Jitter 322.265625MHz HCSL XO

ClockWorks® FUSION

General Description

The MX574BBJ322M265 is an ultra-low phase jitter XO with HCSL output optimized for high line rate applications.

Applications

- Optical communications
- Forward error correction (FEC) rates
- FPGA SERDES reference clock

Absolute Maximum Ratings

Supply Voltage (VIN).....+4.6V
Lead Temperature (soldering, 10s).....260°C
Storage Temperature (T_s).....125°C
ESD Rating (HBM).....2kV

Electrical Characteristics

VDD = 2.5V ±5% or 3.3V ±10%, -40°C to +85°C, outputs terminated with 50 Ohms to VSS.¹

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
IDD	Supply Current				95	mA
F0	Center Frequency			322.265625		MHz
	Frequency Stability	Note 2			±50	ppm
Øj	Phase Noise	Integration Range (12kHz to 20MHz) Integration Range (1.875MHz to 20MHz)		143 98		fsRMS
Tstart	Start-Up Time				10	ms
TR/TF	Rise/Fall time	20%-80%	150	300	450	ps
	Duty Cycle		48	50	52	%
VOH	Output High Voltage	HCSL output levels	660	700	850	mV
VOL	Output Low Voltage	HCSL output levels	-150	0	27	mV
VOVS	Max Output Including Overshoot				VOH + 0.3	V
VUDS	Min Output Including Undershoot		VOL - 0.3			V
VRB	Ringback Voltage		0.2			V
VOX	Absolute Crossing Point		250	350	550	mV
Vswing	Peak to Peak Output Voltage Swing		640	700	950	mV

Notes:

1. Guaranteed after thermal equilibrium.
2. Inclusive of initial accuracy, temperature drift, aging, shock, vibration.

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Features

- 322.265625MHz HCSL
- Supports FEC line rate
- Typical phase noise:
 - 98fs (Integration range: 1.875MHz-20MHz)
- ±50ppm total frequency stability
- -40°C to +85°C temperature range
- Industry standard 6-Pin 7mm x 5mm LGA package

Operating Ratings

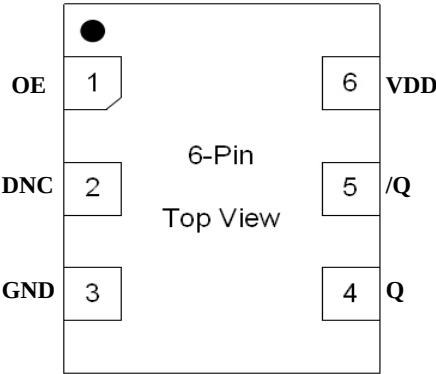
Supply Voltage (VIN).....+2.375V to +3.63V
Ambient Temperature (TA).....-40°C to +85°C

Ordering Information

Ordering Part Number	Marking Line 1	Marking Line 3	Shipping	Package
MX574BBJ322M265	MX574BB	J322M265	Tube	6-Pin 7mm x 5mm LGA
MX574BBJ322M265 TR	MX574BB	J322M265	Tape and Reel	6-Pin 7mm x 5mm LGA

Devices are Green and RoHS compliant. Sample material may have only a partial top mark.

Pin Configuration



Pin Description

Pin Number	Pin Name	Pin Type	Pin Level	Pin Function
1	OE	I, SE	LVC MOS	Output Enable, disables output to tri-state, 1 = Disabled, 0 = Enabled, 50k Ohms Pull-Down
2	DNC			Make no connection, leave floating.
3	GND	PWR		Power Supply Ground
4, 5	Q, /Q	O, Diff	HCSL	Clock Output Frequency = 322.265625MHz
6	VDD	PWR		Power Supply

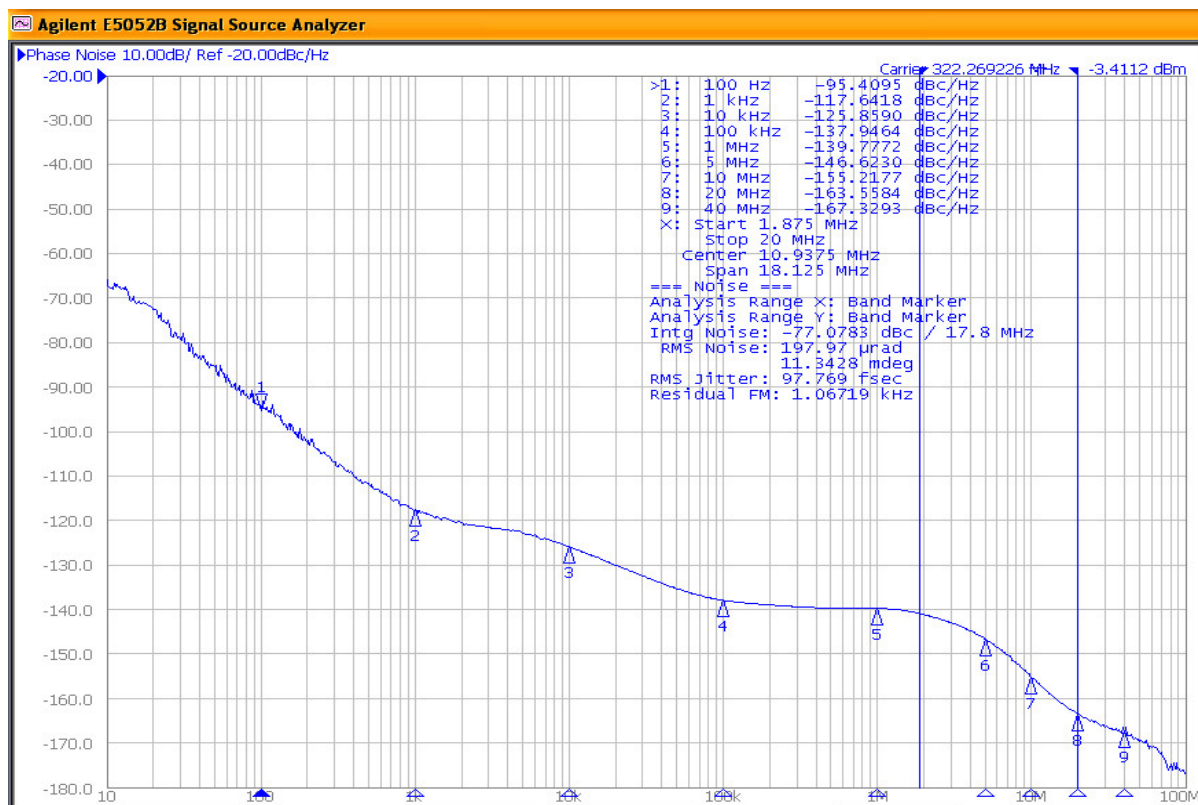


Figure 1. HCSL Output 322.265625MHz 1.875MHz-20MHz 98fs

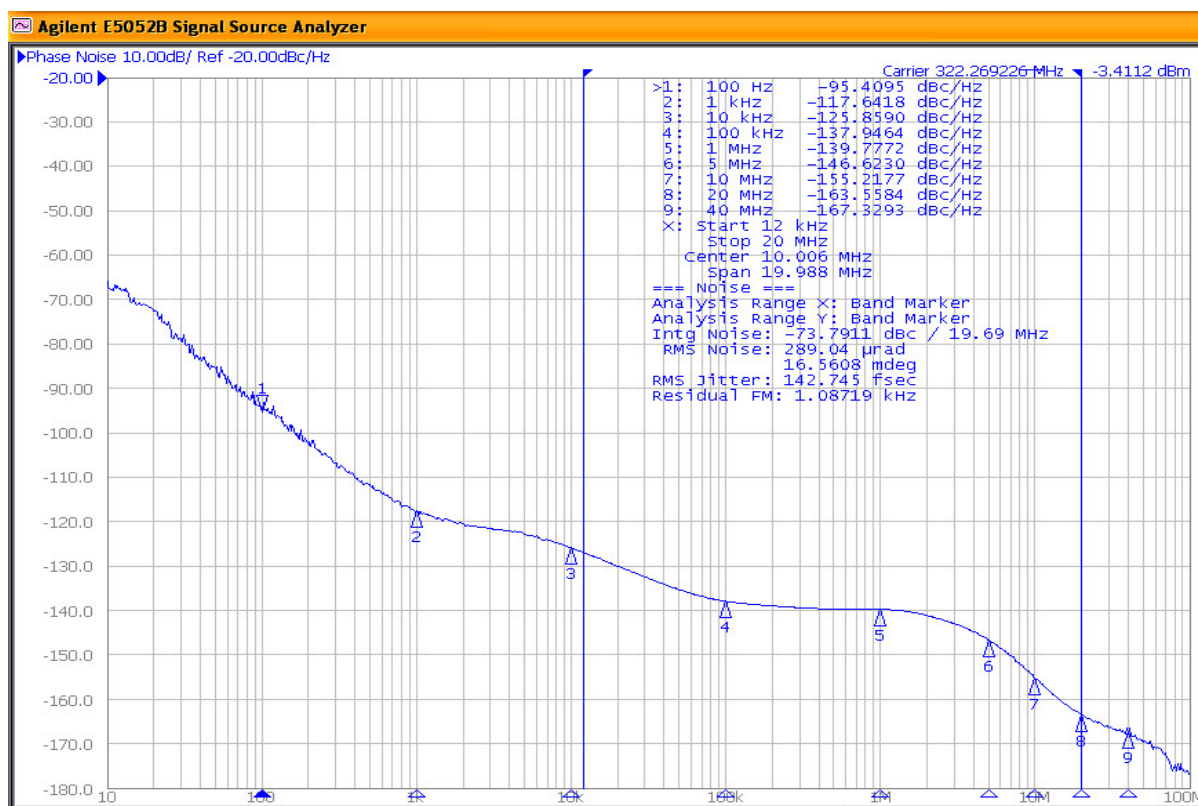
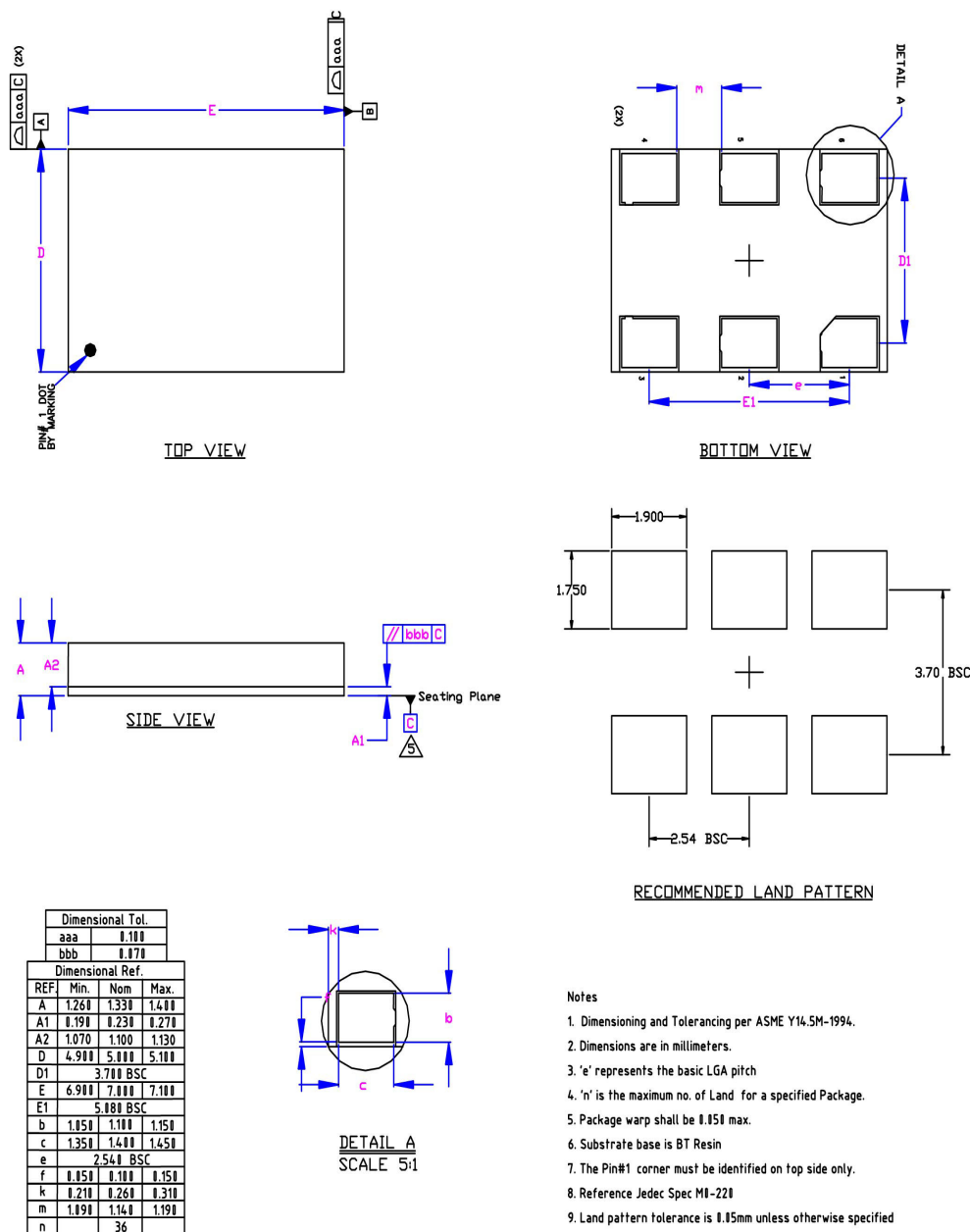


Figure 2. HCSL Output 322.265625MHz 12kHz-20MHz 143fs

Package Information and Recommended Land Pattern for 6-Pin LGA³



6-Pin LGA (7x5mm)

Note:

3. Package information is correct as of the publication date. For updates and most current information, go to www.microchip.com.

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