AN-1444 LM2695 Evaluation Board

1 Introduction

The LM2695EVAL evaluation board provides the design engineer with a fully functional buck regulator, employing the constant on-time (COT) operating principle. This evaluation board provides a 10 V output over an input range of 12 V - 30 V. The circuit delivers load currents to 1A, with current limit set at ≅1.3A. The board is populated with all external components except R5, C8 and C11. These components provide options for changing the current limit threshold, and managing the output ripple as described later in this document.

The board's specification are:

- Input Voltage: 12 V to 30 V
- Output Voltage: 10 V
- Maximum load current: 1.0A
- Minimum load current: 0A
- Current Limit: 1.3A
- Measured Efficiency: 96.3% (V_{IN} = 12 V, I_{OUT} = 300 mA)
- Nominal Switching Frequency: 380 kHz
- Size: 2.25 in. x 0.88 in. x 0.47 in

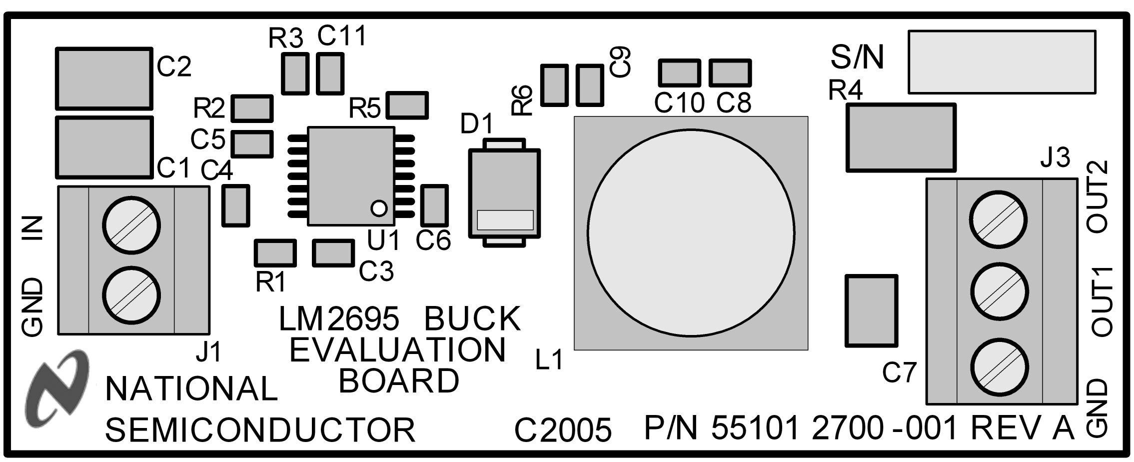

Figure 1. Evaluation Board - Top Side

2 Theory of Operation

Figure 6 shows a simplified block diagram of the LM2695. When the circuit is in regulation, the buck switch is on each cycle for a time determined by R1 and V_{IN} according to Equation 1:

$$t_{ON} = \frac{1.3 \times 10^{-10} \times R1}{V_{IN}} \quad (1)$$

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The on-time of this evaluation board ranges from ≅2300 ns at V_{IN} = 12 V, to ≅900 ns at V_{IN} = 30 V. The on-time varies inversely with V_{IN} to maintain a nearly constant switching frequency. At the end of each on-time the Minimum Off-Timer ensures the buck switch is off for at least 250 ns. In normal operation, the off-time is much longer. During the off-time, the output capacitor (C7) is discharged by the load current. When the output voltage falls sufficiently that the voltage at FB is below 2.5 V, the regulation comparator initiates a new on-time period. For stable, fixed frequency operation, ≅25 mV of ripple is required at FB to switch the regulation comparator. For a more detailed block diagram and a complete description of the various functional blocks, see the *LM2695 High Voltage (30V, 1.25A) Step Down Switching Regulator Data Sheet* (SNVS413).

3 Board Layout and Probing

The pictorial in Figure 1 shows the placement of the circuit components. The following should be kept in mind when the board is powered:

- When operating at high input voltage and high load current, forced air flow is recommended.
- The LM2695, and diode D1 may be hot to the touch when operating at high input voltage and high load current.
- Use CAUTION when probing the circuit at high input voltages to prevent injury, as well as possible damage to the circuit.
- At maximum load current (1A), the wire size and length used to connect the load becomes important. Ensure there is not a significant drop in the wires between this evaluation board and the load.

4 Board Connection/Start-up

The input connections are made to the J1 connector. The load is normally connected to the OUT1 and GND terminals of the J3 connector. Ensure the wires are adequately sized for the intended load current. Before start-up a voltmeter should be connected to the input terminals, and to the output terminals. The load current should be monitored with an ammeter or a current probe. It is recommended that the input voltage be increased gradually to 12 V, at which time the output voltage should be 10 V. If the output voltage is correct with 12 V at V_{IN}, then increase the input voltage as desired and proceed with evaluating the circuit.

5 Output Ripple Control

The LM2695 requires a minimum of 25 mVp-p ripple at the FB pin, in phase with the swtiching waveform at the SW pin, for proper operation. In the simplest configuration that ripple is derived from the ripple at V_{OUT1}, generated by the inductor's ripple current flowing through R4. That ripple voltage is attenuated by the feedback resistors, requiring that the ripple amplitude at V_{OUT1} be higher than the minimum of 25 mVp-p by the gain factor. Options for reducing the output ripple are discussed below, and the results are shown in the graph of Figure 9.

5.1 Minimum Output Ripple

This evaluation board is configured for minimum ripple at V_{OUT1} by setting R4 to 0 Ω, and including components R6, C9 and C10. The output ripple that ranges from 3mVp-p at V_{IN} = 12 V to 8 mVp-p at V_{IN} = 30 V is determined primarily by the ESR of output capacitor (C7), and the inductor's ripple current that ranges from 50 mAp-p to 195 mAp-p over the input voltage range. The ripple voltage required by the FB pin is generated by R6, C9 and C10 since the SW pin switches from -1 V to V_{IN}, and the right end of C9 is a virtual ground. The values for R6 and C9 are chosen to generate a 30-40 mVp-p triangle waveform at their junction. That triangle wave is then coupled to the FB pin through C10. The following procedure is used to calculate values for R6, C9 and C10:

- Calculate the voltage V_A as shown in Equation 2:

$$V_A = V_{OUT} - (V_{SW} \times (1 - (V_{OUT}/V_{IN}))) \quad (2)$$

where, V_{SW} is the absolute value of the voltage at the SW pin during the off-time (typically 1 V) and V_{IN} is the minimum input voltage. For this circuit, V_A calculates to 9.83 V. This is the DC voltage at the R6/C9 junction, and is used in Equation 3.

- Calculate the R6 x C9 product as shown in Equation 3:

$$R6 \times C9 = \frac{(V_{IN} - V_A) \times t_{ON}}{\Delta V} \tag{3}$$

where t_{ON} is the maximum on-time (≅2300 ns), V_{IN} is the minimum input voltage, and ΔV is the desired ripple amplitude at the R6/C9 junction, 30 mVp-p for this example.

$$R6 \times C9 = \frac{(12V - 9.83V) \times 2300\ ns}{0.03V} = 1.66 \times 10^{-4} \tag{4}$$

R6 and C9 are then chosen from standard value components to satisfy the above product. For example, C9 can be 1000 pF requiring R6 to be 166 kΩ. C10 is chosen to be 0.01 µF, large compared to C9. The circuit as supplied on this EVB is shown in Figure 2.

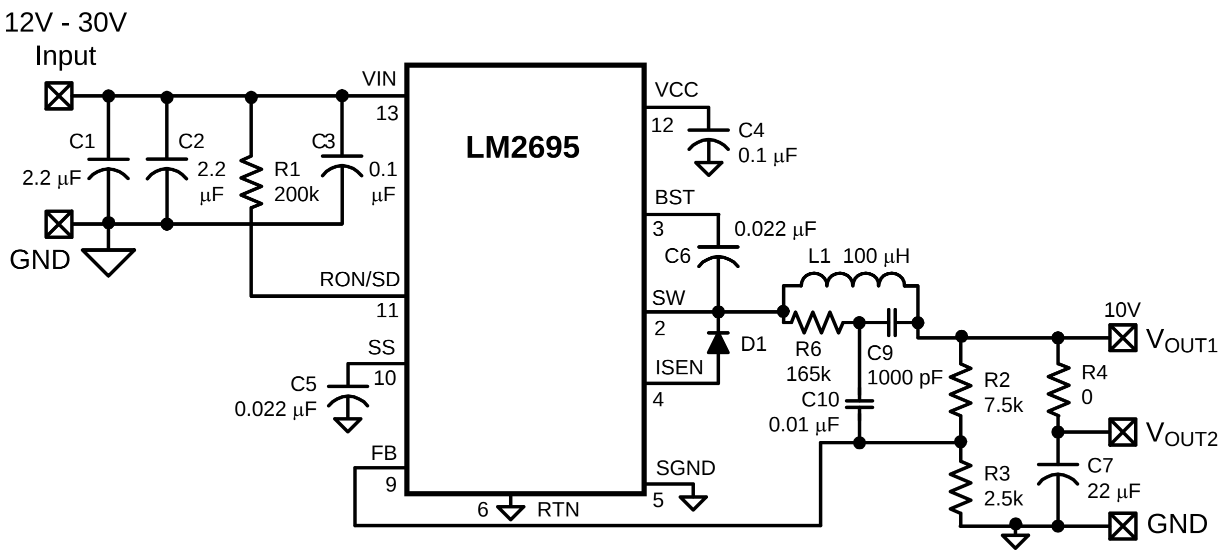

Figure 2. Minimum Ripple Using R6, C9, C10

5.2 Intermediate Ripple Level Configuration

This configuration generates more ripple at V_{OUT1} than the above configuration, but uses one less capacitor. If some ripple can be tolerated in the application, this configuration is slightly more economical, and simpler. R4 and C8 are used instead of R6, C9, and C10, as shown in Figure 3.

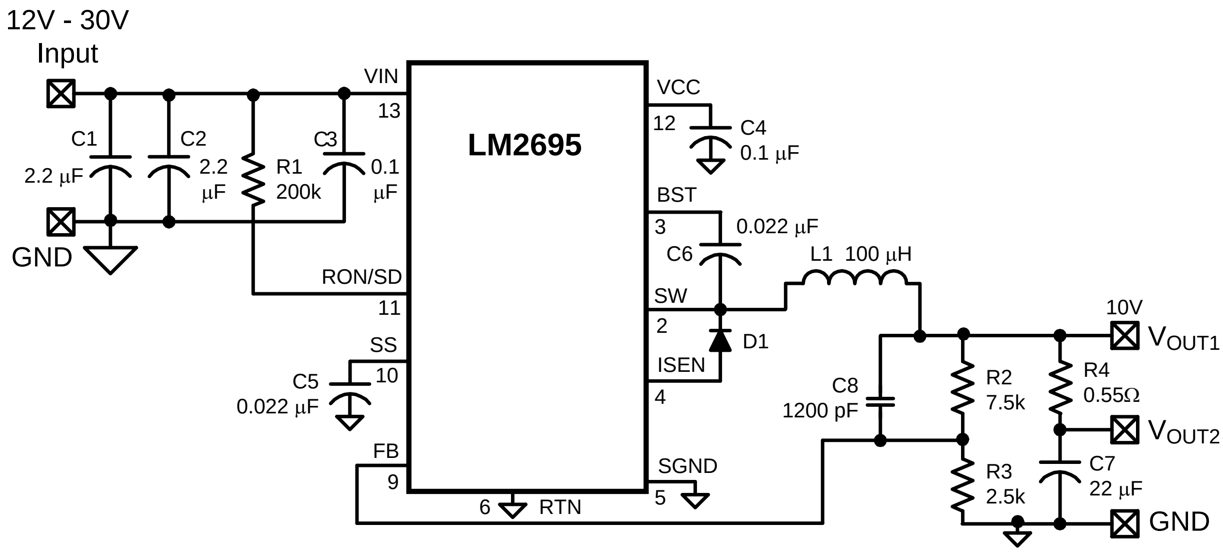

Figure 3. Intermediate Ripple Level Configuration Using C8 and R4

R4 is chosen to generate ≥25 mV - 30 mVp-p at V_{OUT1}, knowing that the minimum ripple current in this circuit is 50 mAp-p at minimum V_{IN}. C8 couples that ripple to the FB pin without the attenuation of the feedback resistors. C8's minimum value is calculated from Equation 5:

$$C8 = \frac{t_{ON(max)}}{(R2//R3)} \tag{5}$$

where $t_{ON(max)}$ is the maximum on-time (at minimum V_{IN}), and R2//R3 is the equivalent parallel value of the feedback resistors. For this evaluation board $t_{ON(max)}$ is approximately 2300 ns, and R2//R3 = 1.875 kΩ, and C8 calculates to a minimum of 1200 pF. The resulting ripple at V_{OUT1} ranges from 27 mVp-p to 105 mVp-p over the input voltage range.

5.3 Lowest Cost Configuration

This configuration is the same as option B above, but without C8. Since 25 mVp-p are required at the FB pin, R4 is chosen to generate 100 mV at V_{OUT1}, knowing that the minimum ripple current in this circuit is 50 mAp-p at minimum V_{IN}. To allow for tolerances, 2.2 Ω is used for R4. The resulting ripple at V_{OUT1} ranges from ≅110 mVp-p to ≅420 mVp-p over the input voltage range. If the application can tolerate this ripple level, this is the most economical solution. The circuit is shown in Figure 4.

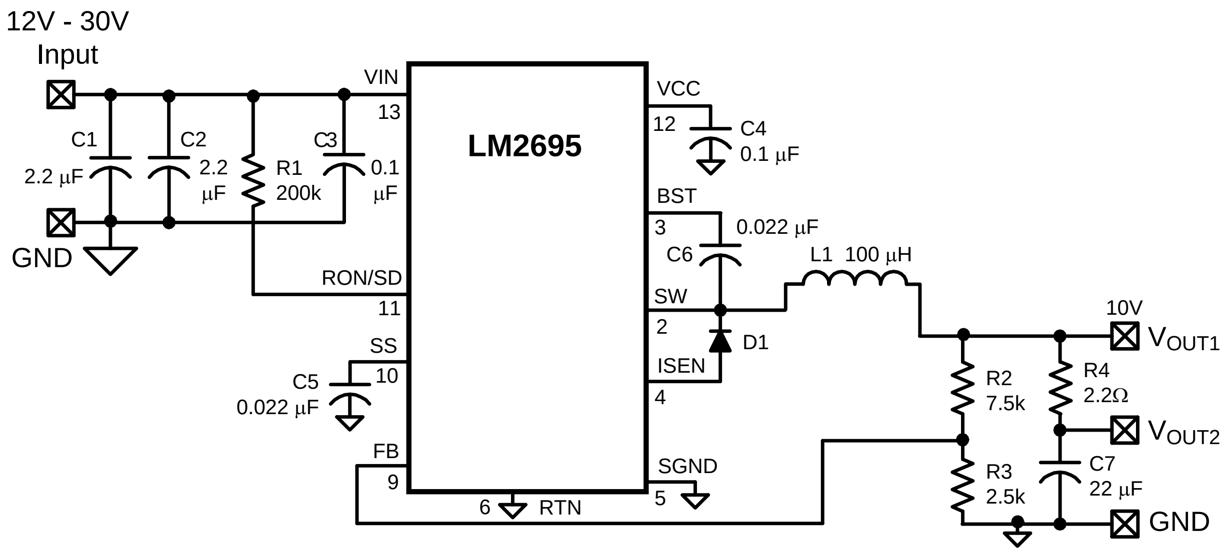

Figure 4. Lowest Cost Configuration

5.4 Alternate Lowest Cost Configuration

A low ripple output can be obtained by connecting the load to V_{OUT2} in the circuits of options B or C above. Since R4 slightly degrades load regulation, this alternative may be viable for applications where the load current is relatively constant. If this method is used, ensure R4's power rating is appropriate.

6 Increasing the Current Limit

The current limit threshold is nominally 1.25A, with a minimum guaranteed value of 1.0A. If, at maximum load current, the lower peak of the inductor current (I_{PK-} in Figure 5) exceeds 1.0A, resistor R5 must be added between SGND and ISEN to increase the current limit threshold to equal or exceed the lower peak. This resistor diverts some of the recirculating current from the internal sense resistor so that a higher current level is needed to switch the internal current limit comparator. I_{PK-} is calculated from Equation 6:

$$I_{PK-} = I_{O(max)} - \frac{I_{OR(min)}}{2} \tag{6}$$

where, $I_{O(max)}$ is the maximum DC load current, and $I_{OR(min)}$ is the minimum ripple current calculated using Equation 7.

$$I_{OR(min)} = \frac{V_{OUT} \times (V_{IN(min)} - V_{OUT})}{L1_{max} \times F_{S(max)} \times V_{IN(min)}} \tag{7}$$

where, $V_{IN(min)}$ is the minimum input voltage, V_{OUT} = 10 V, $L1_{max}$ is the maximum inductor value based on the manufacturer's tolerance, and $F_{S(max)}$ is the maximum switching frequency (380 kHz + 25% = 475 kHz for this evaluation board). R5 is calculated from Equation 8:

$$R_5 = \frac{1.0A \times 0.11\Omega}{I_{PK-} - 1.0A} \tag{8}$$

where, 0.11Ω is the minimum value of the internal resistance from SGND to ISEN. The next smaller standard value resistor should be used for R5. With the addition of R5 it is necessary to check the average and peak current values to ensure they do not exceed the LM2695 limits. At maximum load current the average current through the internal sense resistor is shown in Equation 9:

$$I_{AVE} = \frac{I_{O(max)} \times R_5 \times (V_{IN(max)} - V_{OUT})}{(R5 + 0.11\Omega) \times V_{IN(max)}} \tag{9}$$

If I_{AVE} is less than 1.5A no changes are necessary. If it exceeds 1.5A, R5 must be reduced. The upper peak of the inductor current (I_{PK+}), at maximum load current, is calculated using Equation 10:

$$I_{PK+} = I_{O(max)} + \frac{I_{OR(max)}}{2} \tag{10}$$

where $I_{OR(max)}$ is calculated using Equation 11.

$$I_{OR(max)} = \frac{V_{OUT1} \times (V_{IN(max)} - V_{OUT1})}{L1_{min} \times F_{S(min)} \times V_{IN(max)}} \tag{11}$$

where, $L1_{min}$ is the minimum inductor value based on the manufacturer's tolerance, and $F_{S(min)}$ is the minimum switching frequency (380 kHz - 25% = 285 kHz for this evaluation board). If I_{PK+} exceeds 2A , the inductor value must be increased to reduce the ripple amplitude. This necessitates recalculation of $I_{OR(min)}$, I_{PK-}, and R5. When the circuit is in current limit, the upper peak current out of the SW pin can be as high as:

$$I_{PK+(CL)} = \frac{1.5A \times (150\ m\Omega + R_5)}{R_5} + I_{OR(max)} \tag{12}$$

The inductor L1 and diode D1 must be rated for this current.

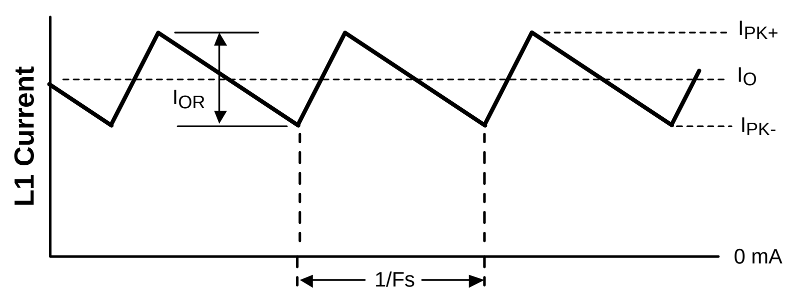

Figure 5. Inductor Current

7 Minimum Load Current

The LM2695 requires a minimum load current of ≅500 µA to ensure the boost capacitor (C6) is recharged sufficiently during each off-time. In this evaluation board, the minimum load current is provided by the feedback resistor (R2, R3), allowing the board's minimum load current at V_{OUT1} (or V_{OUT2}) to be specified at zero.

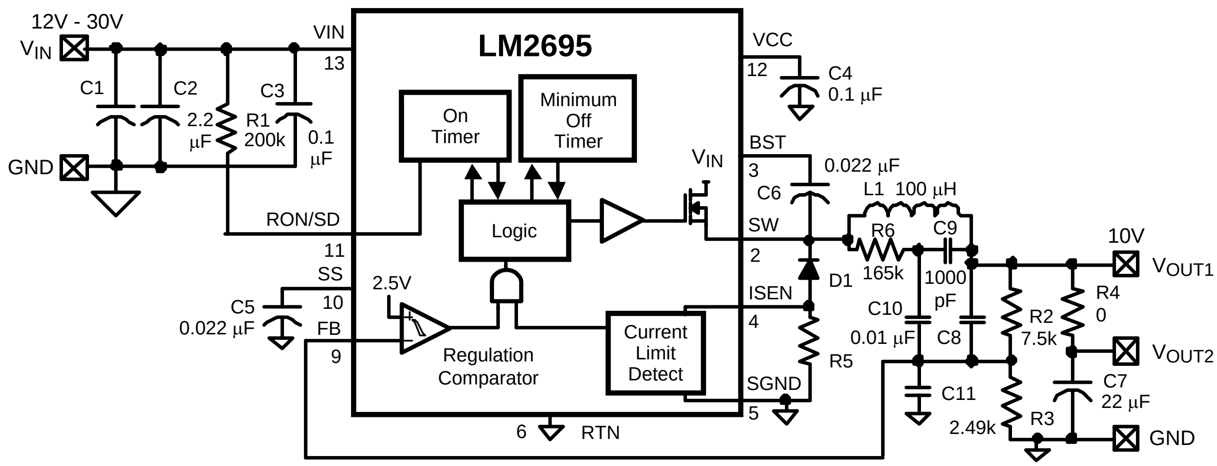

Figure 6. Evaluation Board Schematic

Table 1. Bill of Materials (BOM)

Item	Description	Mfg., Part Number	Package	Value
C1, 2	Ceramic Capacitor	TDK C4532X7R2A225M	1812	2.2 µF, 100 V
C3	Ceramic Capacitor	TDK C2012X7R2A104M	0805	0.1 µF, 100 V
C4	Ceramic Capacitor	TDK C2012X7R1C104M	0805	0.1 µF, 16 V
C5, 6	Ceramic Capacitor	TDK C2012X7R1C223M	0805	0.022 µF, 16 V
C7	Ceramic Capacitor	TDK C3225X7R1C226M	1210	22 µF, 16 V
C8		Unpopulated	0805	
C9	Ceramic Capacitor	TDK C2012X7R2A102M	0805	1000 pF
C10	Ceramic Capacitor	TDK C2012X7R2A103M	0805	0.01 µF
C11		Unpopulated	0805	
D1	Schottky Diode	Diodes Inc. DLFS160	Power DI 123	60 V, 1A
L1	Power Inductor	TDK SLF12575T-101M1R9, or Cooper Bussmann DR125-101	12.5 mm x 12.5 mm	100 µH, 1.9A
R1	Resistor	CRCW08052003F	0805	200 kΩ
R2	Resistor	CRCW08057501F	0805	7.50 kΩ
R3	Resistor	CRCW08052491F	0805	2.49 kΩ
R4	Resistor	CRCW2512000ZR67	2512	0 Ω
R5		Unpopulated	0805	
R6	Resistor	CRCW08051653F	0805	165 kΩ
U1	Switching Regulator	LM2695	TSSOP - 14EP	

8 Circuit Performance

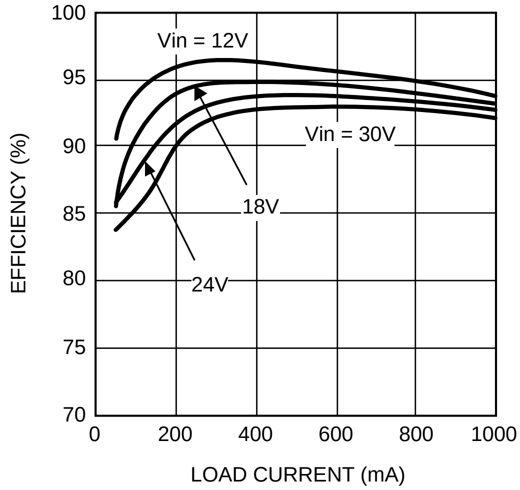

Figure 7. Efficiency vs Load Current

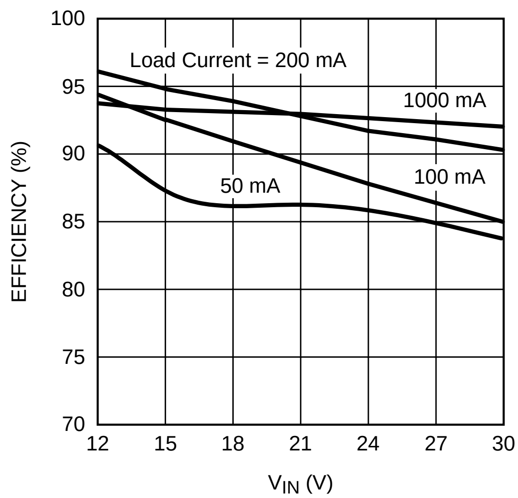

Figure 8. Efficiency vs Input Voltage

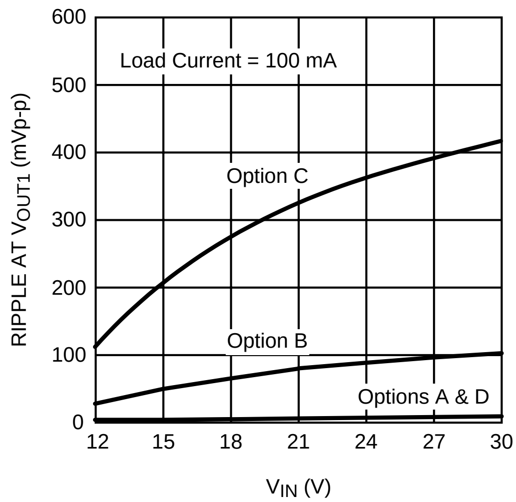

Figure 9. Output Voltage Ripple

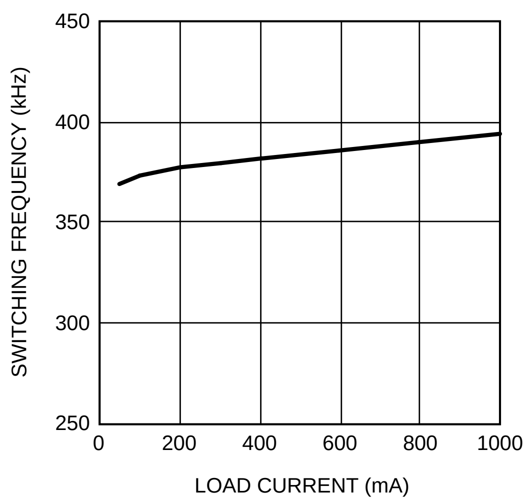

Figure 10. Switching Frequency vs. Load Current

9 PCB Layout

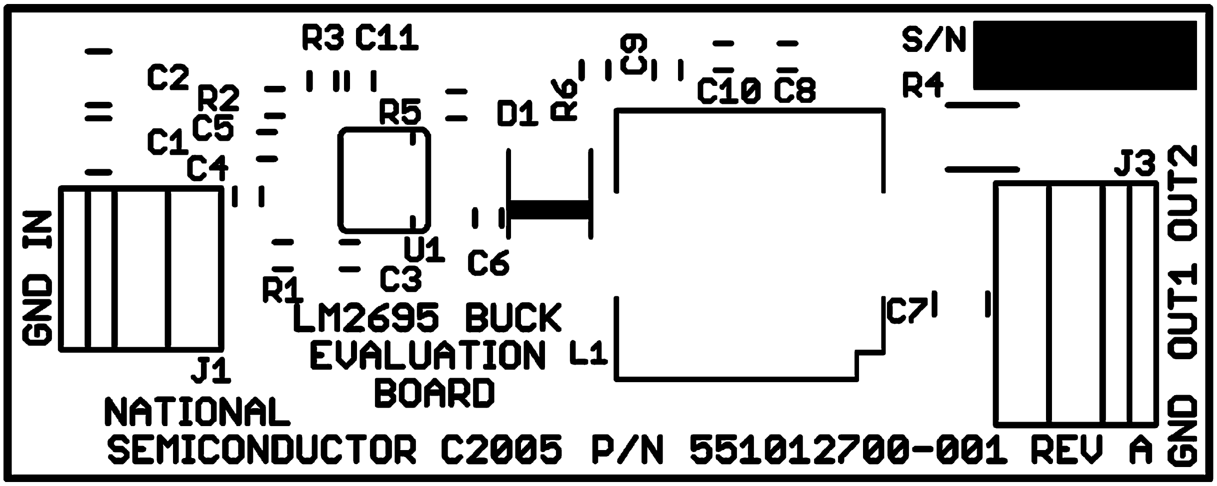

Figure 11. Board Silkscreen

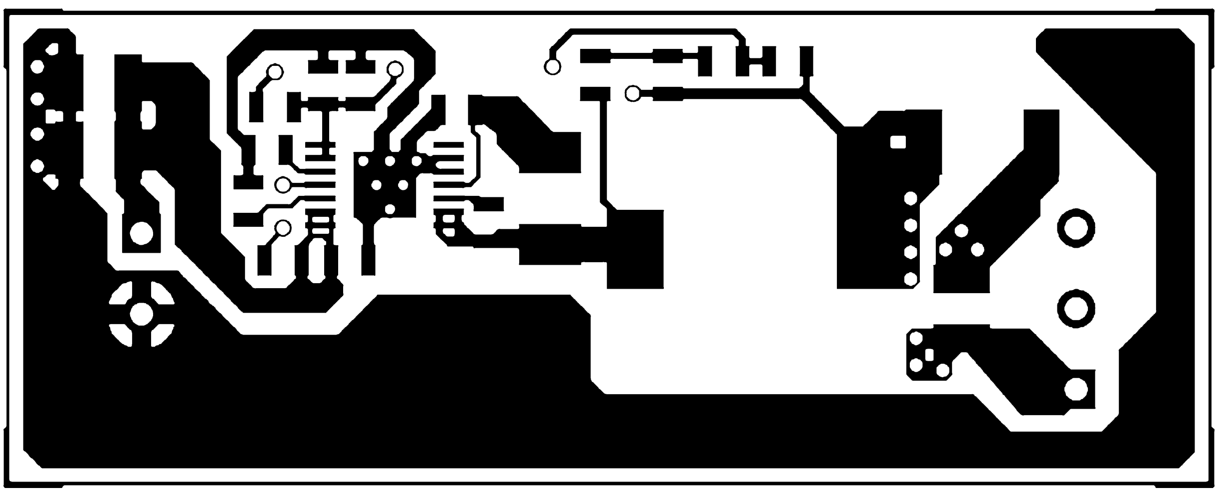

Figure 12. Board Top Layer

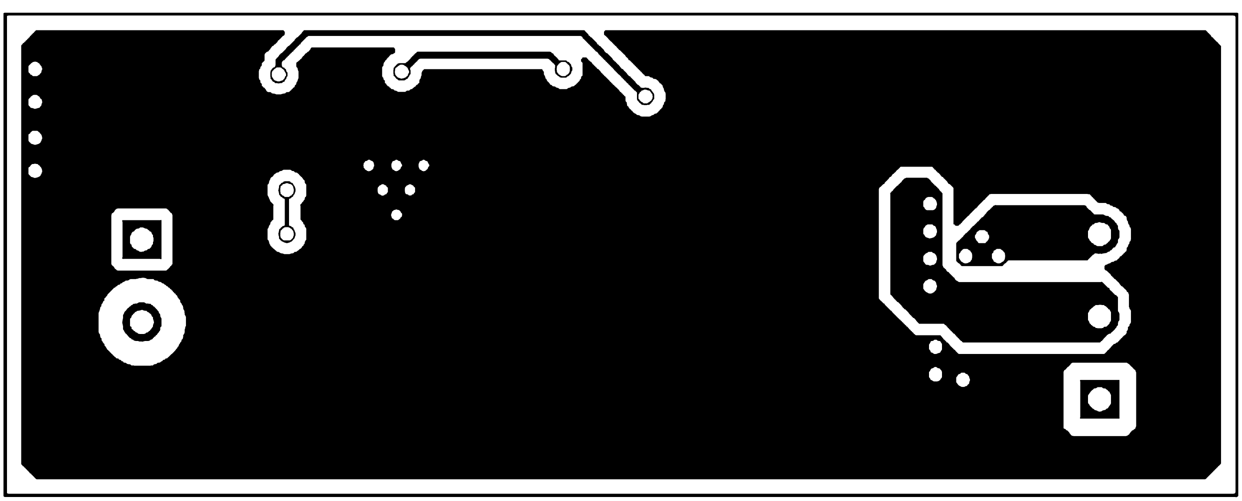

Figure 13. Board Bottom Layer (viewed from top)