16-Bit, 400 MSPS Digital-to-Analog Converter

AD9726

FEATURES

Dynamic performance
- **SFDR ≥ 78 dBc at f_{OUT} = 20 MHz**
- **IMD ≥ 82 dBc at f_{OUT} = 70 MHz**
- **ACLR ≥ 76 dBc at f_{OUT} = 70 MHz**
- **NSD ≤ −160 dB/Hz at f_{OUT} = 70 MHz**

Precision calibrated linearity
- **DNL ≤ ±0.5 LSB at +25°C**
- **INL ≤ ±1.0 LSB at +25°C**
- **THD ≤ −95 dB at f_{OUT} = 1 MHz**

LVDS inputs with internal 100 Ω terminations
Automatic data/clock timing synchronization
Single data rate or double data rate capable
Differential current outputs
Internal precision reference
Operates on 2.5 V and 3.3 V supplies
Extended industrial temperature range
Thermally enhanced, 80-lead, RoHS-compliant
- **TQFP_EP package**

APPLICATIONS

Instrumentation
Test equipment
Waveform synthesis
Communications systems

FUNCTIONAL BLOCK DIAGRAM

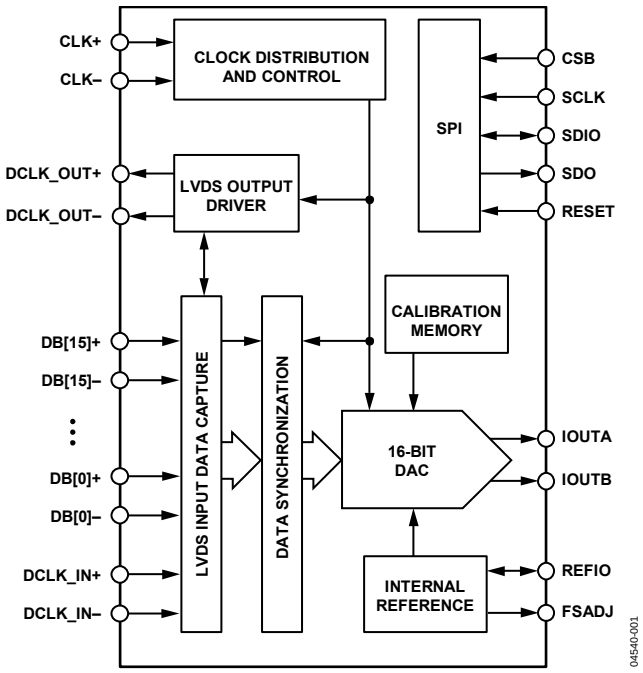

Figure 1.

GENERAL DESCRIPTION

The AD9726 is a 16-bit digital-to-analog converter (DAC) that offers leading edge performance at conversion rates of up to 400 MSPS. The device uses low voltage differential signaling (LVDS) inputs and includes internal 100 Ω terminations. The analog output can be single-ended or differential current. An internal precision reference is included.

The AD9726 also features synchronization logic to monitor and optimize the timing between incoming data and the sample clock. This reduces system complexity and simplifies timing requirements. An LVDS clock output is also available to drive an external data pump in either single data rate (SDR) or double data rate (DDR) mode.

All device operation is fully programmable using the flexible serial port interface (SPI). The AD9726 is also fully functional in its default state for applications without a controller.

PRODUCT HIGHLIGHTS

1. A unique combination of precision and performance makes the AD9726 equally suited to applications with demanding frequency domain or demanding time domain requirements.
2. Nonvolatile factory calibration assures a highly linear transfer function. Internal logic offers on demand self-calibration for linearity even at extended operating temperatures.
3. Proprietary architecture minimizes data dependent, discrete mixing spurs and offers enhanced dynamic performance over a wide range of output frequencies. High input data rates create a very high frequency synthesis bandwidth.
4. The fully automatic, transparent synchronizer maintains optimized timing between clock and data in real time and offers programmable control options for added flexibility.
5. Full-scale output current is external resistor programmable.

Rev. B
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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113 **© 2005-2010 Analog Devices, Inc. All rights reserved.**

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REVISION HISTORY

2/10—Rev. A to Rev. B

Changes to Table 4 ... 5
Added Figure 4 and Figure 5, Renumbered Sequentially ... 6
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Added Data Synchronization Circuitry Bypass Section ... 18
Changes to Ordering Guide ... 24

11/05—Rev. 0 to Rev. A

Changes to Features ... 1
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7/05—Revision 0: Initial Version

SPECIFICATIONS

DC SPECIFICATIONS

DBVDD = AVDD1 = AVDD2 = 3.3 V, DVDD = CLKVDD = ADVDD = ACVDD = 2.5 V, I_{OUT-FS} = 20 mA, internal reference, T_{MIN} to T_{MAX}, unless otherwise specified.

Table 1.

Parameter	Min	Typ	Max	Unit
ACCURACY[1]				
DNL		±0.5	±1.0	LSB
INL		±1.0	±2.5	LSB
Offset Error		0.003		% FS
Gain Error		0.003		% FS
ANALOG OUTPUT				
Full-Scale Current		20		mA
Compliance Voltage		±1		V
Output Impedance		10		MΩ
INTERNAL REFERENCE				
Output Voltage	1.18	1.22	1.27	V
Output Current[2]		1		µA
EXTERNAL REFERENCE				
Input Voltage		1.2		V
Input Resistance		10		MΩ
Small Signal Bandwidth		200		kHz
TEMPERATURE COEFFICIENTS				
Gain Drift		±10		ppm of FS/°C
Offset Drift		±10		ppm of FS/°C
Reference Drift		±30		ppm/°C
POWER SUPPLIES[3]				
AVDD1, AVDD2				
Voltage Range	3.13		3.47	V
Supply Current (I_{AVDD1} + I_{AVDD2})		52	60	mA
ADVDD, ACVDD				
Voltage Range	2.37		2.63	V
Supply Current (I_{ACVDD} + I_{ADVDD})		16	18	mA
CLKVDD				
Voltage Range	2.37		2.63	V
Supply Current (I_{CLKVDD})		45	50	mA
DVDD				
Voltage Range	2.37		2.63	V
Supply Current (I_{DVDD})		80	90	mA
DBVDD				
Voltage Range	3.13		3.47	V
Supply Current (I_{DBVDD})		16	18	mA
POWER DISSIPATION (P_{DISS})		575		mW
Sleep Mode		465		mW
Power-Down Mode		≤10		mW
OPERATING TEMPERATURE RANGE	−40		+85	°C

[1] T_{AMB} = 25°C.
[2] Use buffer amplifier to drive external load.
[3] Supply currents and power dissipation measured in SDR with f_{DAC} = 400 MHz and f_{OUT} = 1 MHz.

AC SPECIFICATIONS

DBVDD = AVDD1 = AVDD2 = 3.3 V, DVDD = CLKVDD = ADVDD = ACVDD = 2.5 V, I_{OUT-FS} = 20 mA, internal reference, T_{MIN} to T_{MAX}, unless otherwise specified.

Table 2.

Parameter	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE				
Output Settling Time (t_{ST}) to 0.1%		10.5		ns
Output Rise Time (10% to 90%)		500		ns
Output Fall Time (90% to 10%)		500		ns
Output Noise (I_{OUTFS} = 20 mA)		45		pA/√Hz
TOTAL HARMONIC DISTORTION (THD)				
f_{DAC} = 400 MHz, f_{OUT} = 1 MHz, 0 dBFS		−95		dB
SPURIOUS-FREE DYNAMIC RANGE (SFDR)				
f_{DAC} = 400 MHz, 0 dBFS				
f_{OUT} = 20 MHz		78		dBc
f_{OUT} = 70 MHz		68		dBc
f_{OUT} = 140 MHz		62		dBc
f_{DAC} = 400 MHz, −3 dBFS				
f_{OUT} = 20 MHz		80		dBc
f_{OUT} = 70 MHz		70		dBc
f_{OUT} = 140 MHz		62		dBc
f_{DAC} = 200 MHz, 0 dBFS				
f_{OUT} = 20 MHz		84		dBc
f_{OUT} = 70 MHz		62		dBc
f_{DAC} = 200 MHz, −3 dBFS				
f_{OUT} = 20 MHz		82		dBc
f_{OUT} = 70 MHz		68		dBc
TWO-TONE INTERMODULATION DISTORTION (IMD)				
f_{DAC} = 400 MHz, 0 dBFS				
f_{OUT1} = 20 MHz, f_{OUT2} = 21 MHz		86		dBc
f_{OUT1} = 70 MHz, f_{OUT2} = 71 MHz		82		dBc
f_{OUT1} = 140 MHz, f_{OUT2} = 141 MHz		74		dBc
ADJACENT CHANNEL LEAKAGE RATIO (ACLR)				
f_{DATA} = 245.76 MSPS, $f_{CARRIER}$ = 70 MHz, One-Carrier WCDMA		76		dBc
f_{DATA} = 245.76 MSPS, $f_{CARRIER}$ = 70 MHz, Two-Carrier WCDMA		70		dBc
f_{DATA} = 245.76 MSPS, $f_{CARRIER1}$ = 70 MHz, Four-Carrier WCDMA		66		dBc
f_{DATA} = 245.76 MSPS, $f_{CARRIER1}$ = 70 MHz, Eight-Carrier WCDMA		62		dBc
NOISE SPECTRAL DENSITY (NSD)				
f_{DAC} = 400 MHz, f_{OUT} = 70 MHz, 0 dBFS		−160		dBm/Hz
f_{DAC} = 400 MHz, f_{OUT} = 70 MHz, −3 dBFS		−163		dBm/Hz
f_{DAC} = 400 MHz, f_{OUT} = 70 MHz, −6 dBFS		−165		dBm/Hz
UPDATE RATE	0		400	MSPS

DIGITAL SIGNAL SPECIFICATIONS

DBVDD = AVDD1 = AVDD2 = 3.3 V, DVDD = CLKVDD = ADVDD = ACVDD = 2.5 V, I_{OUT-FS} = 20 mA, internal reference, T_{MIN} to T_{MAX}, unless otherwise specified.

Table 3.

Parameter	Min	Typ	Max	Unit
DAC CLOCK INPUTS (CLK±)				
Differential Voltage	0.5	1.0		V
Common-Mode Voltage	1.0	1.25		V
LVDS INPUTS (DB[15:0]±, DCLK_IN±)				
Input Voltage Range	825		1575	mV
Differential Threshold Voltage			100	mV
Differential Input Impedance		100		Ω
LVDS OUTPUT (DCLK_OUT±)				
Differential Output Voltage[1]	250	400		mV
Offset Voltage	1.0	1.2		V
Short-Circuit Output Current		20		mA
CMOS INPUTS (CSB, SCLK, SDIO, RESET)				
Logic 0 Voltage			0.5	V
Logic 1 Voltage	2.5			V
Input Current		1		nA
CMOS OUTPUTS (SDO, SDIO)				
Logic 0 Voltage			0.5	V
Logic 1 Voltage	3.0			V
Short-Circuit Output Current		10		mA
CONTROL INPUTS (SPI_DIS, SDR_EN)				
Logic 0 Voltage			0.5	V
Logic 1 Voltage	2.0			V
Input Current		1		nA

[1] With 100 Ω external load.

TIMING SPECIFICATIONS

DBVDD = AVDD1 = AVDD2 = 3.3 V, DVDD = CLKVDD = ADVDD = ACVDD = 2.5 V, I_{OUT-FS} = 20 mA, internal reference, T_{MIN} to T_{MAX}, unless otherwise specified.

Table 4.

Parameter	Min	Typ	Max	Unit
LVDS DATA BUS				
Data Synchronization Enabled (Default)				
DDR DCLK_OUT± Propagation Delay ($t_{DCPD-DDR}$)			2000	ps
DDR DB[15:0]± Setup Time ($t_{DSU-DDR}$)	−100			ps
DDR DB[15:0]± Hold Time (t_{DH-DDR})	500			ps
SDR DCLK_OUT± Propagation Delay ($t_{DCPD-SDR}$)			300	ps
SDR DB[15:0]± Setup Time ($t_{DSU-SDR}$)	−100			ps
SDR DB[15:0]± Hold Time (t_{DH-SDR})	500			ps
Data Synchronization Bypassed				
DB[15:0]± Setup Time ($t_{DSU-BYPASS}$)	800			ps
DB[15:0]± Hold Time ($t_{DH-BYPASS}$)	50			ps
CLK± to IOUT Propagation Delay ($t_{PD-BYPASS}$)		0.85		ns
DB[15:0]± to IOUT Pipeline Delay ($t_{PIPE-BYPASS}$)		4		DAC clock cycles

Parameter	Min	Typ	Max	Unit
SERIAL PORT INTERFACE				
SCLK Frequency (f_{SCLK})			15	MHz
SCLK Rise/Fall Time			1	ms
SCLK Pulse Width High (t_{CPWH})	30			ns
SCLK Pulse Width Low (t_{CPWL})	30			ns
SCLK Setup Time (t_{CSU})	30			ns
SDIO Setup Time (t_{DSU})	30			ns
SDIO Hold Time (t_{DH})	0			ns
SDIO/SDO Valid Time (t_{DV})			30	ns
RESET PULSE WIDTH	1.5			ns

TIMING DIAGRAMS

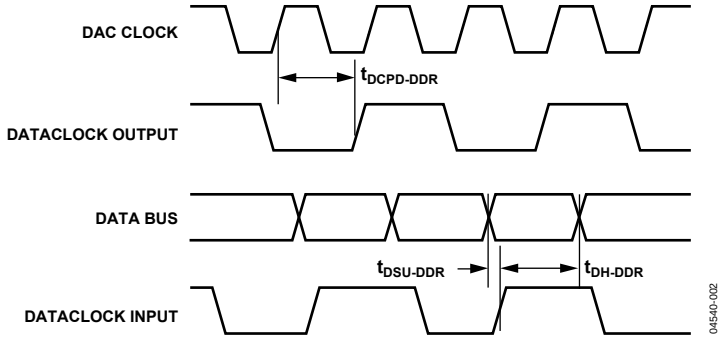


Figure 2. DDR Timing Diagram

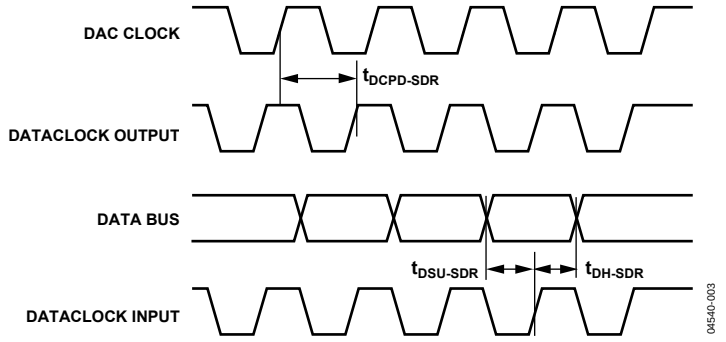


Figure 3. SDR Timing Diagram

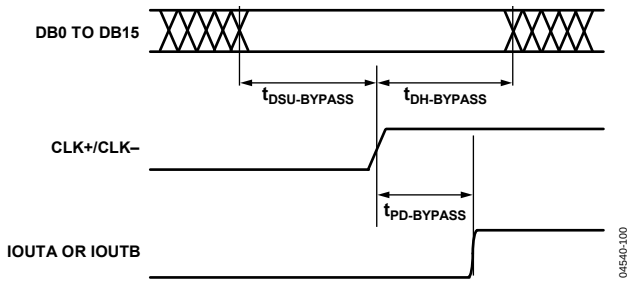


Figure 4. Data Synchronization Bypass Timing Diagram

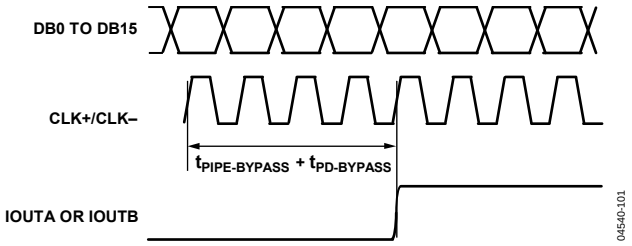


Figure 5. Data Synchronization Bypass Pipeline Delay

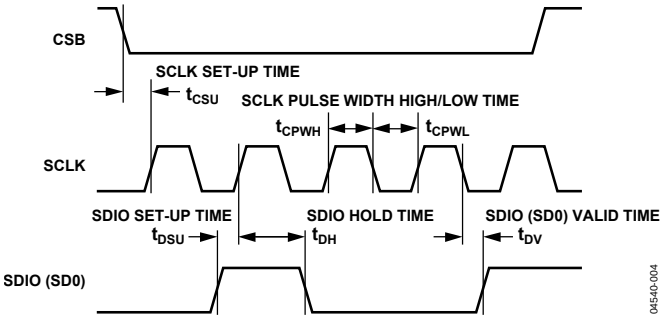


Figure 6. SPI Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	With Respect to	Rating
DBVDD, AVDD1, AVDD2	DBGND, AGND1, AGND2	−0.3 V to 3.6 V
DVDD, CLKVDD, ACVDD, ADVDD	DGND, CLKGND, ACGND, ADGND	−0.3 V to 2.8 V
DBGND, AGND1, AGND2	DBGND, AGND1, AGND2	−0.3 V to +0.3 V
DGND, CLKGND, ACGND, ADGND	DGND, CLKGND, ACGND, ADGND	−0.3 V to +0.3 V
REFIO, FSDAJ	AGND1	−0.3 V to AVDD1 + 0.3 V
IOUTA, IOUTB	AGND1	−1.0 V to AVDD1 + 0.3 V
CLK±	CLKGND	−0.3 V to CLKVDD + 0.3 V
DB[15:0]±, DCLK_IN±, DCLK_OUT±	DBGND	−0.3 V to DBVDD + 0.3 V
CSB, SCLK, SDIO, SDO, RESET, REXT	DBGND	−0.3 V to DBVDD + 0.3 V
SDR_EN, SPI_DIS	ADGND	−0.3 V to ADVDD + 0.3 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

Thermal impedance can be lowered to 23°C/W by soldering the exposed package pad to an external heat sink (for example, the internal PCB copper ground plane). However, this is not necessary for the power dissipation and operating temperature range of the AD9726.

Table 6. Thermal Resistance

Package Type	θ_{JA}	Unit
80-Lead TQFP_EP Package, Thermally Enhanced	32	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

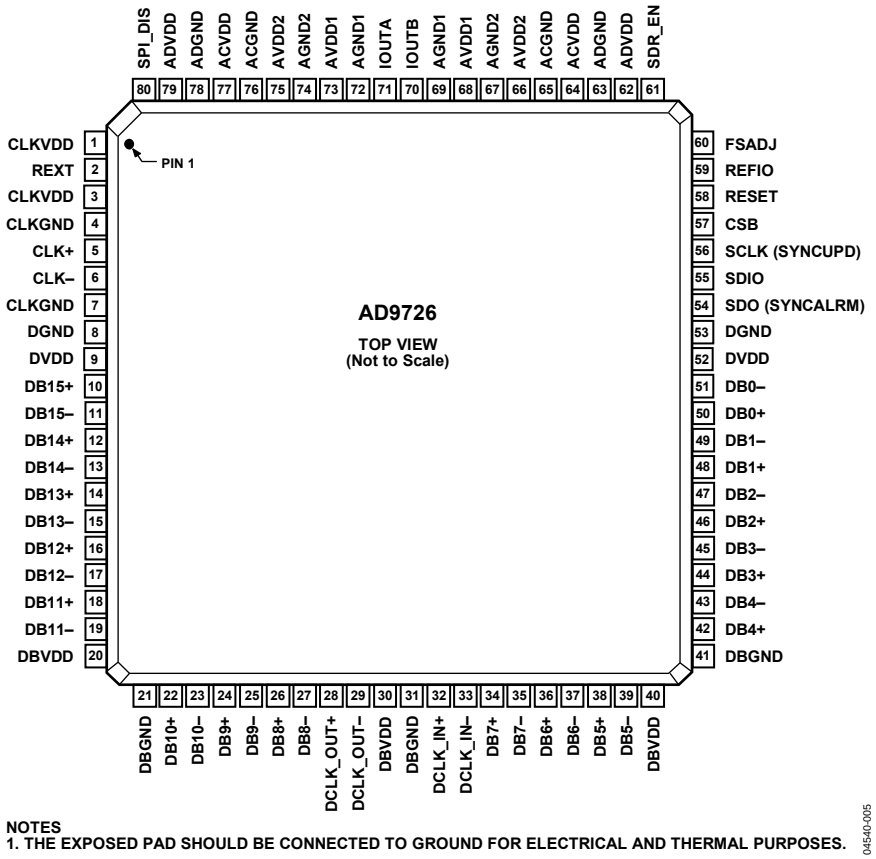


Figure 7. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	CLKVDD	Clock Supply Voltage
2	REXT	Sets Data Clock Output Drive[1]
3	CLKVDD	Clock Supply Voltage
4	CLKGND	Clock Supply Common
5	CLK+	DAC Clock Input True
6	CLK–	DAC Clock Input Complement
7	CLKGND	Clock Supply Common
8	DGND	Digital Supply Common
9	DVDD	Digital Supply Voltage
10	DB15+	Data Bit 15 True
11	DB15–	Data Bit 15 Complement
12	DB14+	Data Bit 14 True
13	DB14–	Data Bit 14 Complement
14	DB13+	Data Bit 13 True
15	DB13–	Data Bit 13 Complement
16	DB12+	Data Bit 12 True
17	DB12–	Data Bit 12 Complement
18	DB11+	Data Bit 11 True
19	DB11–	Data Bit 11 Complement
20	DBVDD	Data Bus Supply Voltage
21	DBGND	Data Bus Supply Common
22	DB10+	Data Bit 10 True
23	DB10–	Data Bit 10 Complement
24	DB9+	Data Bit 9 True
25	DB9–	Data Bit 9 Complement
26	DB8+	Data Bit 8 True
27	DB8–	Data Bit 8 Complement
28	DCLK_OUT+	Data Clock Output True
29	DCLK_OUT–	Data Clock Output Complement
30	DBVDD	Data Bus Supply Voltage
31	DBGND	Data Bus Supply Common
32	DCLK_IN+	Data Clock Input True
33	DCLK_IN–	Data Clock Input Complement
34	DB7+	Data Bit 7 True
35	DB7–	Data Bit 7 Complement
36	DB6+	Data Bit 6 True
37	DB6–	Data Bit 6 Complement
38	DB5+	Data Bit 5 True
39	DB5–	Data Bit 5 Complement
40	DBVDD	Data Bus Supply Voltage
41	DBGND	Data Bus Supply Common
42	DB4+	Data Bit 4 True

Pin No.	Mnemonic	Description
43	DB4−	Data Bit 4 Complement
44	DB3+	Data Bit 3 True
45	DB3−	Data Bit 3 Complement
46	DB2+	Data Bit 2 True
47	DB2−	Data Bit 2 Complement
48	DB1+	Data Bit 1 True
49	DB1−	Data Bit 1 Complement
50	DB0+	Data Bit 0 True
51	DB0−	Data Bit 0 Complement
52	DVDD	Digital Supply Voltage
53	DGND	Digital Supply Common
54	SDO (SYNCALRM)	SPI Data Output (SYNCALRM)[2]
55	SDIO	SPI Data Input/Output[3]
56	SCLK (SYNCUPD)	SPI Clock Input (SYNCUPD)[4]
57	CSB	SPI Chip Select Bar (Active Low)
58	RESET	Hardware Reset (Active High)
59	REFIO	Internal Reference Input/Output[5]
60	FSADJ	Output Current Full-Scale Adjust[6]
61	SDR_EN	Single Data Rate Mode Enable[7]
62	ADVDD	Analog Supply Voltage
63	ADGND	Analog Supply Common
64	ACVDD	Analog Supply Voltage
65	ACGND	Analog Supply Common
66	AVDD2	Analog Supply Voltage
67	AGND2	Analog Supply Common
68	AVDD1	Analog Supply Voltage
69	AGND1	Analog Supply Common
70	IOUTB	Analog Current Output Complement
71	IOUTA	Analog Current Output True
72	AGND1	Analog Supply Common
73	AVDD1	Analog Supply Voltage
74	AGND2	Analog Supply Common
75	AVDD2	Analog Supply Voltage
76	ACGND	Analog Supply Common
77	ACVDD	Analog Supply Voltage
78	ADGND	Analog Supply Common
79	ADVDD	Analog Supply Voltage
80	SPI_DIS	Serial Port Interface Disable[8]
	EPAD	Analog Ground. Serves as an electrical connection to the substrate of the die and should be connected to ground for electrical and thermal purposes.

[1] Nominally 1 kΩ to DBGND (may be omitted if data clock output is unused).
[2] SDO is output in 4-wire SPI mode and three-state in 3-wire SPI mode. If SPI is disabled (SPI_DIS = ADVDD), the alternate pin function is SYNCALRM output.
[3] SDIO is input only in 4-wire SPI mode and bidirectional in 3-wire SPI mode.
[4] If SPI is disabled (SPI_DIS = ADVDD), the alternate pin function is SYNCUPD.
[5] Bypass with 0.1 µF to AGND1. Use the buffer amp to drive external circuitry. Limit the output current to 1 µA. Apply an external reference to this pin.
[6] Nominally 2 kΩ to AGND1 for 20 mA full-scale output (internal reference).
[7] If SPI is disabled, tie the pin to ADVDD to enable SDR. Otherwise, tie to ADGND.
[8] Tie the pin to ADVDD to disable SPI; otherwise, tie to ADGND.

TERMINOLOGY

Integral Nonlinearity (INL)
The maximum deviation of the actual analog output from the ideal output, as determined by a straight line drawn from zero scale to full scale.

Differential Nonlinearity (DNL)
A measure of the maximum deviation in analog output associated with any single value change in the digital input code relative to an ideal LSB.

Offset Error
The deviation of the output current from the ideal zero-scale current. For differential outputs, 0 mA is expected at I_{OUTA} when all inputs are low, and 0 mA is expected at I_{OUTB} when all inputs are high.

Monotonicity
A DAC is monotonic if the analog output increases or remains constant in response to an increase in the digital input.

Gain Error
The deviation of the output current from the ideal full-scale current. Actual full-scale output current is determined by subtracting the output when all inputs are low from the output when all inputs are high.

Output Compliance Range
The range of allowable voltage seen by the analog output of a current output DAC. Operation beyond the compliance limits may cause output stage saturation and/or breakdown resulting in nonlinear performance.

Temperature Drift
Temperature drift is specified as the maximum change in a parameter from ambient temperature (25°C) to either T_{MIN} or T_{MAX} and is typically reported as ppm/°C.

Power Supply Rejection
The maximum change in the full-scale output as all power supplies are varied over their respective operating voltage range.

Spurious-Free Dynamic Range (SFDR)
The difference in decibels between the peak amplitude of a test tone and the peak amplitude of the largest spurious signal over the specified bandwidth.

Intermodulation Distortion (IMD)
The difference in decibels between the maximum peak amplitude of two test tones and the maximum peak amplitude of the distortion products created from the sum or difference of integer multiples of the test tones.

Adjacent Channel Leakage Ratio (ACLR)
The ratio between the measured power of a wideband signal within a channel relative to the measured power in an empty adjacent channel.

Noise Spectral Density (NSD)
The measured noise power over a 1 Hz bandwidth seen at the analog output.

Total Harmonic Distortion (THD)
The ratio in decibels of the rms power sum of the first six harmonic components to the rms power of the output signal.

TYPICAL PERFORMANCE CHARACTERISTICS

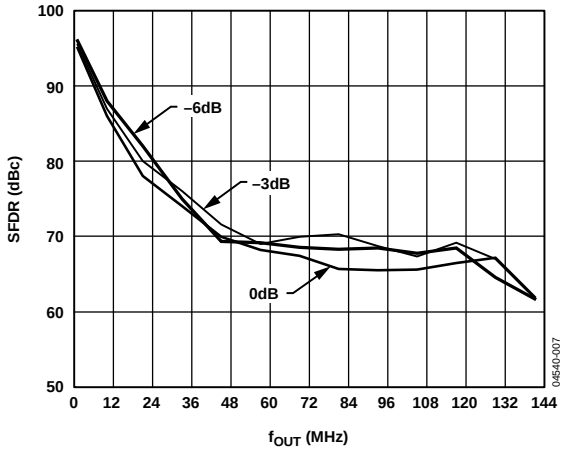


Figure 8. SFDR vs. f_{OUT} at 400 MSPS

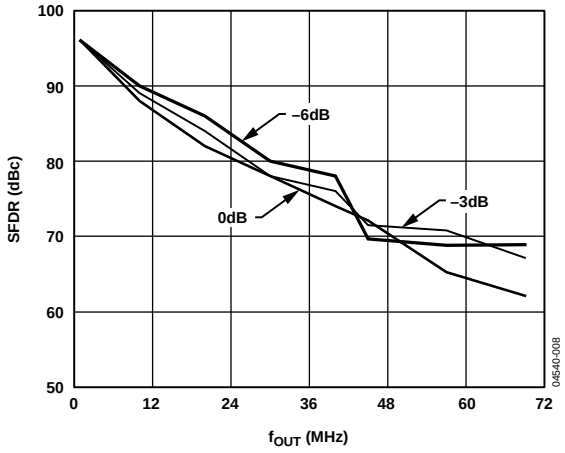


Figure 9. SFDR vs. f_{OUT} at 200 MSPS

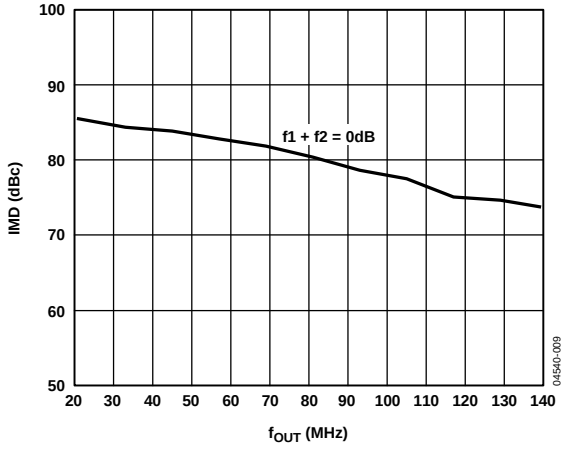


Figure 10. Two-Tone IMD vs. f_{OUT} at 400 MSPS

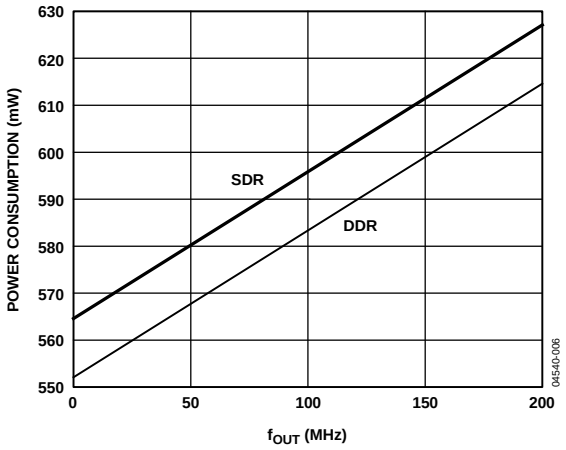


Figure 11. Power Consumption vs. f_{OUT} at 400 MSPS

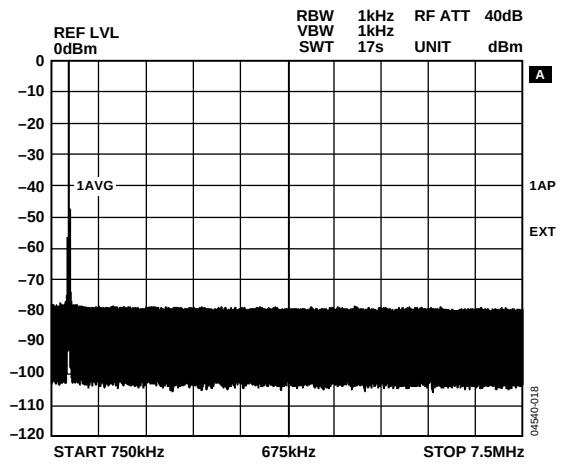


Figure 12. THD at 400 MSPS and f_{OUT} = 1 MHz (Diplexer Low-Pass Output Showing 0 dBm Fundamental (See the Performance Effects of Calibration Section))

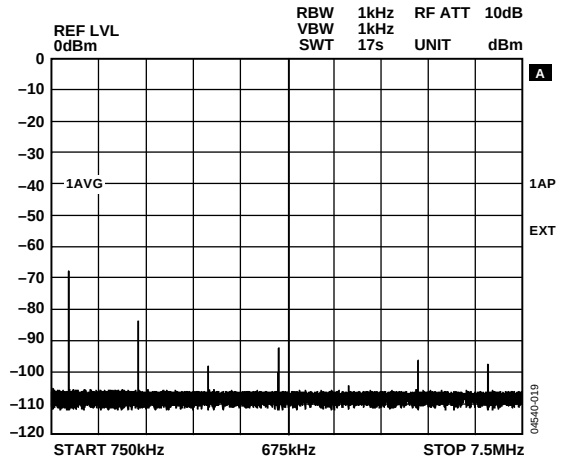


Figure 13. THD at 400 MSPS and f_{OUT} = 1 MHz (Diplexer High-Pass Output Showing Harmonics Before Calibration; (See the Performance Effects of Calibration Section))

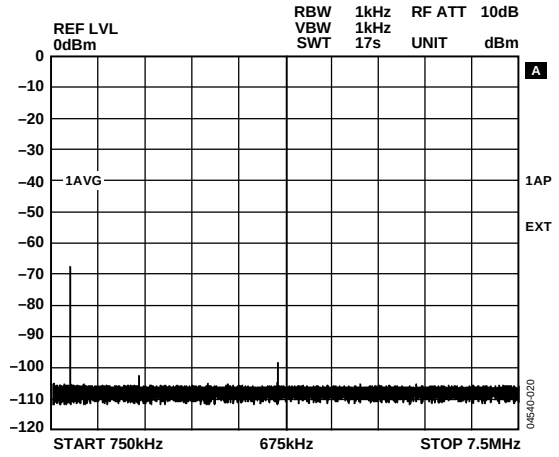


Figure 14. THD at 400 MSPS and f_{OUT} = 1 MHz (Diplexer High-Pass Output Showing Harmonics After Calibration, See the Performance Effects of Calibration Section)

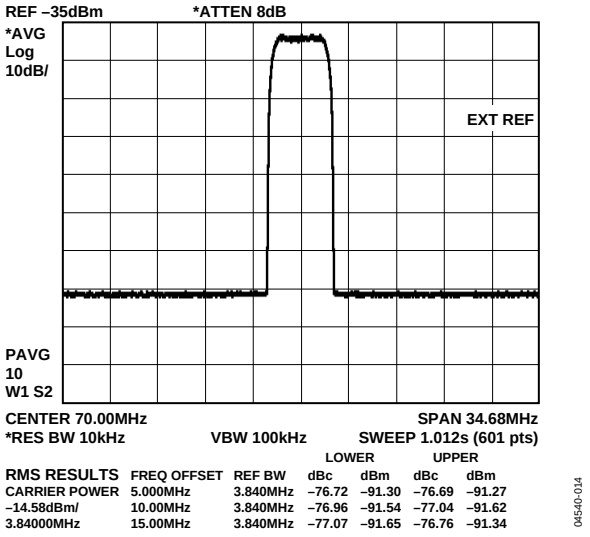


Figure 15. One-Carrier WCDMA at 400 MSPS f_{OUT} = 70 MHz

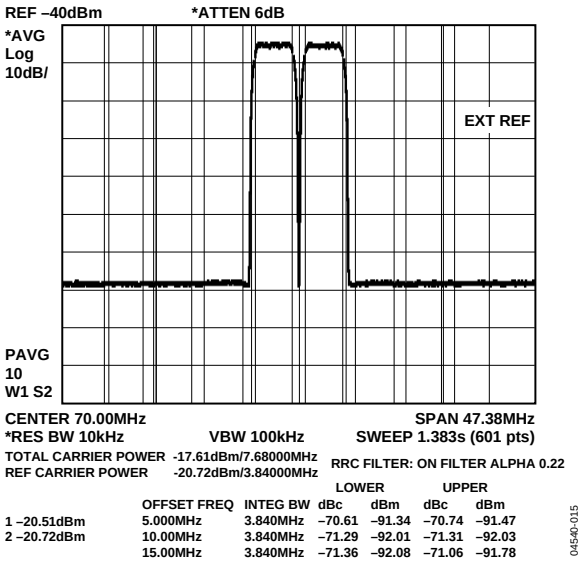


Figure 16. Two-Carrier WCDMA at 400 MSPS f_{OUT} = 70 MHz

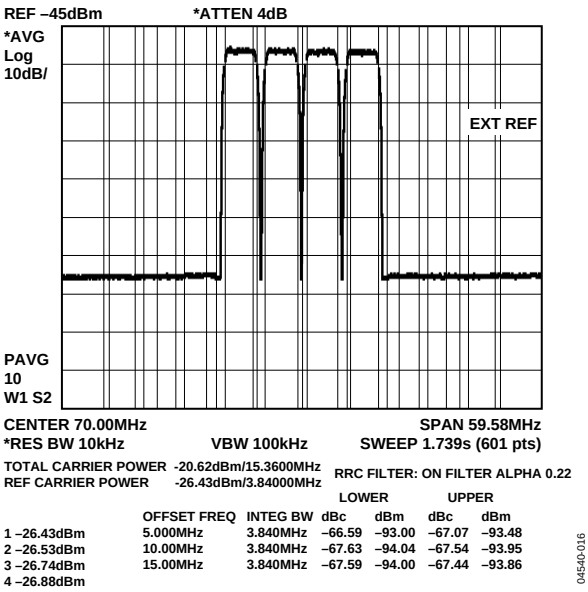


Figure 17. Four-Carrier WCDMA at 400 MSPS f_{OUT} = 70 MHz

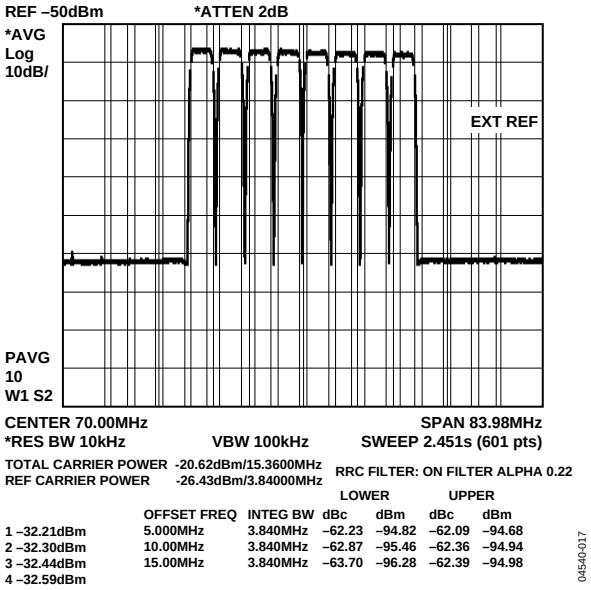


Figure 18. Eight-Carrier WCDMA at 400 MSPS f_{OUT} = 70 MHz

SERIAL PORT INTERFACE

Table 8. SPI Register Map

Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	SDIODIR	DATADIR	SWRESET	SLEEP	PWRDWN			EXTREF
0x02	DATAFMT	DATARATE	INVDCLKI	INVDCLKO	DISDCLKO	SYNCMAN	SYNCUPD	SYNCALRM
0x0E			CALMEM[1]	CALMEM[0]		CALCLK[2]	CALCLK[1]	CALCLK[0]
0x0F	SCALSTAT	SELFCAL	XFERSTAT	MEMXFER	SMEMWR	SMEMRD	FMEMRD	UNCAL
0x10	MEMADR[7]	MEMADR[6]	MEMADR[5]	MEMADR[4]	MEMADR[3]	MEMADR[2]	MEMADR[1]	MEMADR[0]
0x11			MEMDAT[5]	MEMDAT[4]	MEMDAT[3]	MEMDAT[2]	MEMDAT[1]	MEMDAT[0]
0x15							SYNCOUT[1]	SYNCOUT[0]
0x16		BYPASS	SYNCEXT	SYNCIN[1]	SYNCIN[0]			

Table 9. SPI Register Bit Default and Descriptions Values

Addr	Name	Bits	I/O	Default	Description
0x00	SDIODIR	7	I	0	0: SDIO is input only (4-wire SPI mode), and SDO is used for output. 1: SDIO is input/output (3-wire SPI mode), and SDO is unused.
	DATADIR	6	I	0	0: SPI serial data byte is MSB first format. 1: SPI serial data byte is LSB first format.
	SWRESET	5	I	0	1: software reset: SPI registers (except 0x00) to default values.[1]
	SLEEP	4	I	0	1: analog outputs temporarily disabled.
	PWRDWN	3	I	0	1: full device power-down; all circuits disabled except SPI.
	EXTREF	0	I	0	1: power-down internal reference; use external reference source.[2]
0x02	DATAFMT	7	I	0	0: input data-word is twos complement binary format. 1: input data-word is unsigned binary format.
	DATARATE	6	I	0	0: DDR mode. 1: SDR mode.
	INVDCLKI	5	I	0	1: inverts the polarity of the data clock input.
	INVDCLKO	4	I	0	1: inverts the polarity of the data clock output.
	DISDCLKO	3	I	0	1: disables the data clock output.
	SYNCMAN	2	I	0	1: enables sync manual mode; disables automatic update.
	SYNCUPD	1	I	0	1: forces manual sync update.
	SYNCALRM	0	O	0	1: indicates that sync logic requires update.
0x0E	CALMEM	[5:4]	O	00	2-bit SMEM contents and calibration status indicator. 00: uncalibrated; SMEM contains default values (63). 01: self-calibrated; SMEM contains values from self-calibration. 10: factory-calibrated; SMEM values are transferred from FMEM. 11: user-calibrated; SMEM contains user-entered values.
	CALCLK	[2:0]	I	000	3-bit self-calibration clock divider ratio. Affects time available for algorithm settling. Each value increase reduces time by 50%.[3] 000: self-calibration clock is DAC clock/4096 (maximum self-calibration settling time for highest linearity accuracy). 001,010,011: self-calibration clock is DAC clock/2048,1024,512. 100,101,110: self-calibration clock is DAC clock/256,128,64. 111: self-calibration clock is DAC clock/32 (minimum self-calibration settling time for fastest algorithm completion).
0x0F	SCALSTAT	7	O	0	1: indicates completion of self-calibration cycle.
	SELFCAL	6	I	0	1: initiates self-calibration cycle.[4]
	XFERSTAT	5	O	0	1: indicates completion of memory transfer cycle.
	MEMXFER	4	I	0	1: initiates FMEM to SMEM transfer.[5]
	SMEMWR	3	I	0	1: enables static memory (SMEM) write operation.
	SMEMRD	2	I	0	1: enable sstatic memory (SMEM) read operation.
	FMEMRD	1	I	0	1: enables factory memory (FMEM) read operation.
	UNCAL	0	I	0	1: enables uncalibrated operation; all SMEM to default values.[6]

Addr	Name	Bits	I/O	Default	Description
0x10	MEMADR	[7:0]	I	00000000	8-bit memory address value for read/write operations.
0x11	MEMDAT	[5:0]	I/O	000000	6-bit memory data value for read/write operations.
0x15	SYNCOUT	[1:0]	O	00	2-bit output value indicates current sync quadrant.
0x16	BYPASS	6	I	0	1: bypasses data synchronization circuitry. Data is sampled using the DAC clock (CLK±)
	SYNCEXT	5	I	0	1: enables sync external mode; disable auto quadrant select.
	SYNCIN	[4:3]	I	00	2-bit input value is used to specify the sync quadrant.

[1] SWRESET also resets itself. SMEM contents are unaffected by SWRESET; however, CALMEM reports an uncalibrated state.
[2] EXTREF is optional because the internal reference circuit is designed to be overdriven by an external source.
[3] The self-calibration clock is also used for the memory transfer cycle; therefore, the CALCLK value affects the MEMXFER process time.
[4] Register Bits 3:0 must all be 0 to assert SELFCAL. The time required for the self-calibration cycle is ~100 ms at 100 MHz with CALCLK = 0.
[5] Register Bits 3:0 must all be 0 to assert MEMXFER. The time required for the memory transfer cycle is ~15 ms at 100 MHz with CALCLK = 0.
[6] The UNCAL bit remains asserted after the cycle completes (SMEM contents held at default values) until the bit is cleared by the user.

THEORY OF OPERATION

The AD9726 uses LVDS for input data to enable high sample rates and high performance. LVDS technology uses differential signals for noise rejection and small signal amplitude for fast speed with lower power. Each LVDS input on the AD9726 has an internal 100 Ω active load for proper termination.

DAC CLOCK AND DATA CLOCK OUTPUT

The AD9726 uses two clock inputs and offers one clock output. All are differential signals.

The AD9726 is driven by a master input clock that initiates conversion and controls all on-chip activity. This signal is referred to as the DAC clock. It is not LVDS, and the CLK+ and CLK– pins are high impedance inputs.

The DAC clock is then used to generate the data clock output. The DCLK_OUT+ and DCLK_OUT– pins form an LVDS signal that can be used to drive an external FPGA or another data pump. In SDR mode, the data clock output always runs at the same frequency as the DAC clock. In DDR mode, the data clock output always runs at ½ the DAC clock frequency.

Use of the data clock output is optional. It is meant to serve as a convenient means of regulating the incoming data stream. The driver can be loaded by a 100 Ω differential termination. An external 1 kΩ resistor from the REXT pin to DBGND is also required to set the drive strength. If unused, the data clock output pins can be left unconnected, and the 1 kΩ resistor at REXT can be omitted.

The data clock output can also be inverted by asserting the INVDCLKO bit in SPI Register 0x02, or the driver can be disabled by asserting the DISDCLKO bit in the same register.

DATA CLOCK INPUT

The remaining clock signal associated with the AD9726 is the data clock input. This LVDS signal is not optional and must accompany the 16-bit data bus. The data clock input is used to latch incoming data into the synchronization (sync) logic.

The data clock input always runs at the same frequency as the data clock output in both SDR and DDR modes. A logical inversion can be accomplished by asserting the INVDCLKI bit.

Driving the DAC Clock Inputs

The DAC clock must be precise and spectrally pure to ensure the highest ac performance. A symmetrical 50% duty cycle should be maintained at all times.

The CLK+ and CLK– input pins should be driven by a signal with a common-mode voltage near ½ of CLKVDD. From this point, peak-to-peak signal amplitude should swing over a range of at least several hundred millivolts.

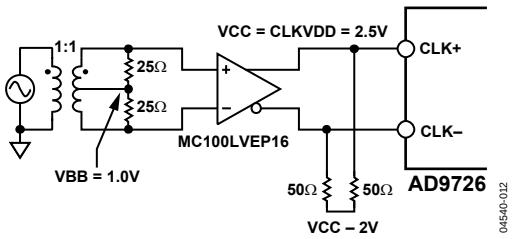


Figure 19. Active DAC Clock Drive Circuit

The circuit option shown in Figure 19 uses a receiver/driver IC from the 2.5 V LVPECL logic family to provide complementary outputs that fall within these guidelines. A transformer helps ensure a 50% duty cycle and provides a single-ended to differential conversion at the input.

The LVPECL device can be conveniently powered from the same power supply as CLKVDD. The center tap of the transformer secondary must be held at 1 V, the switching threshold of the receiver/driver inputs (use a resistive divider to generate this voltage or use the internal VBB source with a buffer amplifier). Based on a 1:1 impedance ratio, 25 Ω resistors across the secondary provide a matched load to a 50 Ω source.

The driver outputs are terminated as close as possible to the AD9726 with 50 Ω to VCC – 2 V (or use a Thevenin equivalent circuit). Controlled impedance PCB traces should be used to minimize reflections. Signal levels at the CLK+ and CLK– pins transition between a high near 1500 mV to a low near 750 mV.

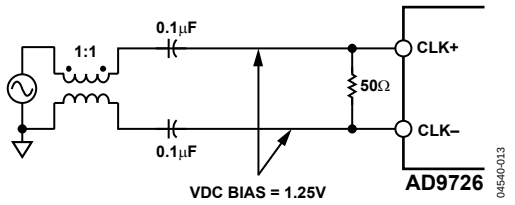


Figure 20. Passive DAC Clock Drive Circuit

An alternative circuit option for driving the DAC clock inputs employs a transmission line transformer (balun) to accomplish the single-ended to differential conversion. This all-passive circuit is considerably simpler and less costly, and it provides acceptable performance over a limited range of frequencies.

In this implementation, a sine wave (or other single-ended source) is coupled directly to the differential DAC clock inputs through a 50 Ω transformer. Capacitors are used for isolation, and each DAC clock pin must be dc-biased to a level of 1.25 V (a pair of simple resistive dividers can be used).

The 50 Ω termination resistor should be placed as close as possible to the input pins, and controlled impedance PCB traces should be used.

Good ac performance can be expected from either the active or passive DAC clock drive circuit. However, in a passive circuit, the output slew rate is dependent on the frequency of the input; whereas an active circuit provides consistently high output slew rates over a wide range of input frequencies.

DATA SYNCHRONIZATION CIRCUITRY

The high performance of the AD9726 requires maintaining synchronization between the incoming bits and the DAC clock used to sample and convert the data. Despite the inherent difficulty in specifying the phase relationship of the DAC clock and the LVDS data clock input and the challenge presented by the high operating speed of the interface, the AD9726 contains real-time logic to automatically monitor and align the data bus with the DAC clock.

Whether in SDR or DDR mode, input data is always provided at the same rate. Furthermore, the rate of incoming data always equals the frequency period of the DAC clock. The data rate and the DAC clock must also be frequency locked. To accomplish this, the primary purpose of the data clock output is to provide a time base for data that is derived directly from the DAC clock.

The function of the data clock input is to latch incoming data into the sync block. From there, it is the function of the synchronization logic to position the data with respect to the DAC clock for optimal ac performance.

Individual data bits must maintain close alignment with one another so that PCB traces have matched delays across the width of the 16-bit bus. In addition, a fixed setup and hold timing relationship between the data clock input and the data bus is required.

However, because of the sync logic, the phase relationship between the data bus and the DAC clock is internally optimized. Furthermore, if the phase between the data bus and the DAC clock drifts over time or temperature, the sync logic automatically updates and adjusts for it. After synchronization is reached, the phase between the data bus and the DAC clock can vary by a full cycle without loss or corruption of data.

More detailed explanations of sync operation and optional programmable modes are presented in the Sync Logic Operation and Programming section, which also includes an explanation of how to use the sync logic without the SPI.

Data Synchronization Circuitry Bypass

Due to internal design limitations, the data synchronization circuitry does not assure a fixed or predictable pipeline delay between the data input and the analog output after power-up. For designs where multichip synchronization or fixed pipeline delay is important, the AD9726 can be configured to bypass the resynchronization circuitry and assure a fixed pipeline delay of four DAC clock cycles. In this mode, the data is sampled into the DAC using the DAC clock (CLK±) and following the timing presented in Figure 4, Figure 5, and Table 4.

The data synchronization circuitry bypass is enabled by writing 0x40 to Address 0x16. The AD9726 should also be configured in single data rate mode by writing 0x80 to Address 0x02. In this mode, the sync logic is bypassed, making its configurations and status reporting irrelevant.

ANALOG OUTPUT

The AD9726 is based around a high dynamic range CMOS core. The analog output consists of differential current sources, each capable of up to 20 mA full scale. Discrete output devices are PMOS and capable of sourcing current into an output termination within a compliance voltage range of ±1 V.

In a typical application, both outputs drive discrete resistors-to-analog ground. From there, especially for higher frequency outputs, they feed the center-tap secondary of a 1:1 RF transformer. A differential-to-single-ended conversion is accomplished that provides added gain and cancellation of even ordered harmonics.

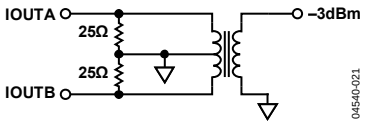


Figure 21. Transformer Output Circuit

For maximum output power, resistor values can be increased to 50 Ω to provide up to 0 dBm into a 50 Ω load without loss of performance for most transformers.

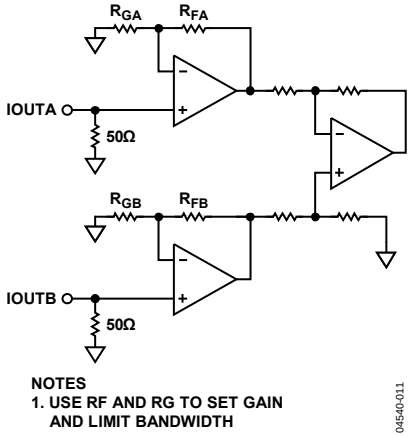


Figure 22. Op Amp Output Circuit

As an alternative, an active output stage can be used in the classic instrumentation amplifier configuration. Here, each DAC output feeds the noninverting input of one of the Analog Devices, Inc., high speed transimpedance op amps.

INTERNAL REFERENCE AND FULL-SCALE OUTPUT

The AD9726 contains an internal 1.2 V precision reference source; this reference voltage appears at the REFIO pin. It can be used to drive external circuitry if properly buffered.

Apply an external reference voltage source to the REFIO pin if desired. The internal source is designed to be easily overdriven by an external source; however, the internal reference can also be powered down using the EXTREF bit in SPI Register 0x00.

The reference voltage (either internal or external) is applied to an external precision resistor at the FSADJ pin. The resulting current is internally amplified to provide the full-scale current at the DAC output according to the following equation:

$$I_{OUTFS} = VREF/R_{FSADJ} \times 32$$

Taking into account the binary value appearing at the data bus inputs, the output currents I_{OUTA} and I_{OUTB} can be determined according to the following equations:

$$IOUTA = I_{OUTFS} \times DB[15:0]/65536$$
$$IOUTB = I_{OUTFS} \times (1 - DB[15:0])/65536$$

Note that the AD9726 features nonvolatile, factory-calibrated gain using the internal reference source and a precision 2 kΩ load. Gain accuracy in any application is, therefore, dependent upon the accuracy of R_{FSADJ}.

RESET

Following initial power-up and application of a valid DAC clock signal, the AD9726 should always be initialized with an active high pulse on the RESET pin. This defaults the programmable registers, initializes volatile calibration memory, and prepares the synchronization logic for data. The data bus should be static prior to the reset pulse. After reset, LVDS data can flow.

The default state of the AD9726 is DDR and twos complement binary input data. To use the AD9726 in this mode, it is not necessary to program any device registers. However, the SPI is enabled by default unless the SPI_DIS pin is connected high. If not disabled, SPI input pins should not be left floating.

SERIAL PORT INTERFACE

The serial port interface is a flexible and synchronous serial communications port allowing easy interface to many industry standard microcontroller and microprocessor protocols (including both Motorola SPI® and Intel® SSR). The interface provides read/write access to registers that configure the operation of the AD9726.

The AD9726 SPI supports single-byte and multibyte transfers as well as MSB- or LSB-justified data formats. The interface can be configured in 3-wire mode (in which SDIO is bidirectional) or the default 4-wire mode (in which SDIO and SDO function as unidirectional data input and data output, respectively).

Communication Cycle

All communication cycles have two phases. The first phase is concerned with writing an instruction byte into the SPI controller and always coincides with the first eight rising edges of SCLK. The instruction byte provides the controller with information regarding the second phase of the cycle, namely the data transfer phase. The instruction byte contains the number of data bytes to be transferred (one to four), a register address, and a bit initiating a read or write operation.

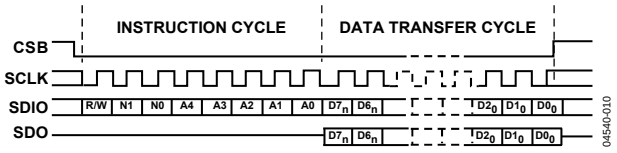


Figure 23. SPI Communication Cycle

Any communication cycle begins with CSB going low, which also resets the SPI control logic. Similarly, any communication cycle ends with CSB going high, which aborts any incomplete data transfer. After a communication cycle begins, the next eight SCLK rising edges interpret data on the SDIO pin as the instruction byte.

Instruction Byte

The instruction byte bits are shown in the following bit map.

B7	B6	B5	B4	B3	B2	B1	B0
R/$\overline{W}$	N1	N0	A4	A3	A2	A1	A0

R/$\overline{W}$

Bit 7 of the instruction byte selects a read or write transfer. If the bit is set high, a read operation is indicated. If the bit is low, a write operation is indicated.

N1, N0

Bit 6 and Bit 5 of the instruction byte determine the number of data bytes to be transferred, as shown in Table 10.

Table 10.

N1	N0	Description
0	0	Transfer one data byte
0	1	Transfer two data bytes
1	0	Transfer three data bytes
1	1	Transfer four data bytes

A4, A3, A2, A1, A0

Bit 4 through Bit 0 of the instruction byte specify a 5-bit binary value corresponding to a valid register address. In the case of multibyte transfers, the location specified is either an initial or a concluding register address. The SPI controller increments or decrements this value to generate successive address values depending on whether LSB or MSB justification is active.

MSB/LSB Transfers

The SPI can support both MSB- and LSB-justified serial data byte formats. This functionality is determined by Bit 6 in SPI Register 0x00. This bit defaults low, which is MSB justification. In this mode, serial data bits are written to and/or read from registers sequentially from Bit 7 to Bit 0.

If Bit 6 of SPI Register 0x00 is set high, the controller switches to LSB justification. In this mode, data bits are written to or read from registers sequentially from Bit 0 to Bit 7. Writing to the instruction bytes is also affected by the active justification.

For multibyte transfers with MSB justification, the address in the instruction byte is interpreted as a final address, and its value is decremented automatically by the controller. For multibyte transfers with LSB justification, the address in the instruction byte is interpreted as an initial address, and its value is incremented automatically by the controller.

Care must be exercised when switching from MSB to LSB justification. The controller switches modes immediately once all eight bits of SPI Register 0x00 are written (even if in the process of a multibyte transfer). For this reason, a single byte command is recommended when changing justification.

3-Wire and 4-Wire Operation

Bit 7 of SPI Register 0x00 defaults low, enabling 4-wire SPI operation. In this mode, serial data is input from the SDIO pin, and serial data is output on the SDO pin. Setting Bit 7 of SPI Register 0x00 high enables 3-wire operation. In this mode, SDIO becomes bidirectional and switches automatically from input to output when necessary. The SDO pin in this mode is unused and assumes a high impedance state.

As with MSB or LSB justification, care must be exercised when switching operational modes. The change occurs immediately once all eight bits of SPI Register 0x00 are written.

Writing and Reading Register Data

Bringing CSB low initiates a new communication cycle. The next eight rising edges of SCLK latch data from SDIO into the instruction byte. If Bit 7 of the instruction byte is low, a write operation is enabled. If Bit 7 is high, a read operation is enabled.

For a write operation, a data byte is latched from the SDIO pin into a register on the next eight rising edges of SCLK. If the instruction byte Bit 6 and Bit 5 are not both 0, a multibyte transfer latches data bytes into adjacent registers after each successive set of eight rising SCLK edges. Depending upon MSB or LSB justification, the controller decrements or increments the address value in the instruction byte during the cycle as necessary.

If a read operation is enabled, data bits from the register being addressed appear on SDO (or SDIO) with each falling edge of SCLK. Note that for a read operation, the eighth bit of the instruction byte is latched on the eighth rising edge of SCLK, and the first output bit is enabled on the immediately following falling SCLK edge.

For multibyte read sequences, the controller adjusts the register address when necessary, and subsequent data bit values appear at the output with each falling SCLK edge.

Disabling the SPI

Tie the SPI_DIS pin high to ADVDD to disable the serial port inteface. In this state, the default DDR operational mode can be changed to SDR by pulling the SDR_EN pin high to ADVDD. In addition, with the SPI disabled, the sync logic no longer operates in a fully automatic mode. See the Sync Logic Operation and Programming section for a full explanation of sync operational modes.

SPI PIN DESCRIPTION

The AD9726 SPI logic runs from the DBVDD supply rail, and input/output thresholds are based upon a nominal 3.3 V level. The maximum frequency of operation is 15 MHz.

Chip Select (CSB)

The CSB pin is an active low input. It begins and ends any communication cycle and must remain low during the entire cycle. An incomplete cycle is aborted if CSB is prematurely returned high.

Serial Clock (SCLK)

The SCLK pin is used to synchronize data to and from the SPI registers, and the controller state machine runs from this input. It is, therefore, possible to read and write register data (but not SMEM/FMEM) without a valid DAC clock. All input data is registered on the rising edge of SCLK, and output data bits are enabled on the falling edge of SCLK.

Serial Data Input/Output (SDIO)

Data is always written into the SPI on the SDIO pin. In 3-wire mode, however, data is also driven out using this pin. The switch from input to output occurs automatically between the instruction and data transfer phases of a read operation. In the default 4-wire mode, SDIO is unidirectional and input only.

Serial Data Output (SDO)

Serial data is driven out on the SDO pin when the SPI is in its default 4-wire mode. In 3-wire mode (or whenever CSB is high), SDO is set to a high impedance state.

CALIBRATION

To ensure linearity to the 16-bit level, the AD9726 incorporates 132 calibration DACs (CALDACs), which are used to linearize the current output transfer function. Each CALDAC is a 6-bit device and takes its input directly from static memory (SMEM).

There are 127 CALDACs associated with each major transition of the 16-bit input data-word (that is, any transition involving the upper 7 MSBs). A 128th CALDAC operates on the sum total of the lower nine LSBs. The remaining four CALDACs (129 to 132) are used to adjust the DAC's overall transfer function gain.

Linearity CALDACs operate inversely from their input; that is, as their binary input value increases, the magnitude of their current contribution seen at the AD9726 output decreases. Gain CALDACs are an exception to this. Their contribution seen at the AD9726 output is in direct proportion to their binary input.

Gain CALDACs are also half strength as compared to linearity CALDACs, but they are intended to be used together as a unit and thus, together, provide twice the current adjustment range.

Calibration Memory

During production testing, the linearity of the AD9726 is measured and optimized. Values for all CALDACs are permanently stored in nonvolatile factory memory (FMEM). At reset, all factory memory contents are transferred to static memory. CALMEM, Bits[5:4] in Register 0x0E, indicates a factory calibrated state (CALMEM = 10b).

It is also possible at any time to transfer the contents of FMEM to SMEM by asserting the MEMXFER bit in Register 0x0F. The XFERSTAT indicator bit (Bit 5 in Register 0x0F) then reports the successful completion of the transfer cycle, and MEMXFER is cleared.

Note that the MEMXFER bit (and SELFCAL, Bit 6, Register 0x0F) cannot be asserted if any other memory access function is currently enabled (that is, if any one of Bits[3:0] in Register 0x0F is high). Attempting to assert MEMXFER (or SELFCAL) in this case clears any asserted bits in Register 0x0F, but the requested cycle does not commence.

The factory-to-static memory data transfer cycle requires a number of DAC clock cycles. The total depends on the value of CALCLK. This value sets a divider used to create a slow version of the DAC clock, which is intended to extend the settling time available to the self-calibration cycle. However, this divided clock is also used to sequence a memory transfer cycle.

The divider is set to its maximum value with CALCLK at its default value. A memory transfer cycle requires about 15 ms at a DAC clock frequency of 100 MHz. This time can be reduced by 50% for every increase in the value of CALCLK.

Accessing Calibration Memory

SMEM or FMEM locations can be read at any time by setting the SMEMRD or FMEMRD bit in SPI Register 0x0F. Address and data information can be input and/or output through SPI Register 0x10 and SPI Register 0x11, respectively.

SMEM locations can also be written by setting the SMEMWR bit in Register 0x0F. Register 0x10 and Register 0x11 are again used for addresses and data. Any time after the SMEMWR bit has been asserted, the device reports a user-calibrated state (CALMEM = 11b) until another action changes the calibration memory status.

To reset static memory at any time, assert the UNCAL bit in Register 0x0F. All SMEM locations are then reset to their default values (63). CALMEM reports an uncalibrated state (CALMEM = 00b). Note that UNCAL remains asserted (and the contents of SMEM remains at default values) indefinitely. UNCAL does not clear itself (like SWRESET) and must be cleared by the user.

Note also that although SPI registers do not depend on the DAC clock (they use SCLK to sequence the controller state machine), SMEM and/or FMEM access does require a valid DAC clock.

SMEM/FMEM Read/Write Procedures

Static and factory memory is accessed through the SPI, but it is not part of the SPI logic. For this reason, memory access requires a valid DAC clock, while SPI register access does not.

Because the AD9726 SPI is so flexible, allowing single and multiple byte reads and writes as well as MSB or LSB justified data, there are a number of ways in which a user can access one or more SMEM or FMEM locations.

To avoid potential errors, the following procedures for accessing static or factory memory should be followed. These procedures use only single-byte SPI commands to ensure the enabling of addresses and the sequencing of memory access.

To read from SMEM or FMEM,

1. Ensure that Bits [3:0] of Register 0x0F are clear.
2. Begin the sequence by writing the memory address value to Register 0x10 with a single-byte SPI write command.
3. Assert the SMEMRD or FMEMRD bit in Register 0x0F with another single-byte SPI write command.
4. Import the contents of Register 0x11 using a single-byte SPI read command.
5. Clear the SMEMRD or FMEMRD bit with another single-byte command.

To write to SMEM,

1. Ensure that Bits [3:0] of Register 0x0F are clear.
2. Begin the sequence by writing the data value to Register 0x11 using a single-byte SPI write command.
3. Assert the SMEMWR bit using a single-byte SPI write command.
4. Place the memory address value in Register 0x10 using a single-byte SPI write command.
5. Clear the SMEMWR bit with a fourth single-byte SPI write command.

Self-Calibration

The AD9726 features an internal self-calibration engine to linearize the transfer function automatically. This can be very useful at temperature extremes where factory calibration no longer applies. The automated cycle can be initiated by asserting the SELFCAL bit.

The self-calibration process calibrates all linearity and gain CALDACs based upon a fixed internal reference current. Values for all CALDACs are stored in volatile static memory. The CALSTAT bit indicates the successful completion of the cycle,

and the SELFCAL bit is cleared. Following the cycle, the device reports a self-calibrated state (CALMEM = 01b).

As with MEMXFER, successful assertion of the SELFCAL bit (Bit 6 in Register 0x0F)requires that Bits[3:0] in Register 0x0F be clear. If any of these bits are asserted (such that an SMEM/FMEM read/write/clear state is enabled), the self-calibration cycle does not begin.

The time required to self-calibrate is dependent on both the DAC clock frequency and the value of CALCLK (Bits[5:0] in Register 0x0E). Because self-calibration requires more time than ordinary operation, the DAC clock is divided into a slower version and used to step through the process. Time made available to the self-calibration algorithm directly impacts its ability to provide accurate results.

A maximum fixed division ratio (4096) corresponds to the minimum default value of CALCLK (0). The division ratio can be decreased by increasing the value of CALCLK. Each increase in the value of CALCLK reduces the DAC clock division factor (and, therefore, the time made available to self-calibration) by 50%. With CALCLK at its maximum value (7), the divide ratio declines to its minimum value (32).

With CALCLK at its default value, self-calibration requires approximately 100 ms at a DAC clock frequency of 100 MHz. This time can be reduced to under 0.8 ms if CALCLK = 7. Time scales relative to DAC clock frequency.

Performance Effects of Calibration

Harmonic distortion for low frequency outputs is primarily a function of DAC linearity. Figure 12 to Figure 14 show the harmonic distortion performance of the AD9726.

Figure 12 shows a 1 MHz full-scale output tone. The output drives a unique low-pass and high-pass filter called a diplexer. This type of filter presents a uniform 50 Ω load to the DAC and splits the output signal into low and high frequency paths. The diplexer's low-pass output passes the 1 MHz fundamental but attenuates higher frequencies, and the diplexer's high-pass output passes higher frequencies and attenuates the 1 MHz fundamental. Figure 12 also shows the diplexer's low-pass output. Here the noise floor is higher than the harmonic distortion because with a high power input signal, attenuation is required by the spectrum analyzer.

Figure 13 shows the diplexer's high pass output where the attenuated input signal can be seen. The spectrum analyzer attenuation is also reduced, which lowers the noise floor. Harmonic products at integer multiples of the fundamental are thus revealed. This is the response using the AD9726 in an uncalibrated state.

Figure 14 shows a response using the AD9726 in a calibrated state. Harmonic distortion due to the nonlinearities of the digital-to-analog conversion are virtually eliminated.

SYNC LOGIC OPERATION AND PROGRAMMING

Recall that a fixed setup and hold timing relationship between the data clock input and the data bus must be established and maintained. Recall also that the data bus and the DAC clock must be frequency locked. Because of the sync logic, however, the phase relationship between the data bus and the DAC clock is internally optimized. Therefore, data arrival propagation delays and concern about data transitions near the sampling instant are eliminated.

Synchronization is automatically enabled upon reset. After data arrives and synchronization is achieved, the sync logic continuously monitors itself so that automatic adjustments are made if phase drifts occur over time and/or temperature.

Note that the sync function and operation of the sync logic block are transparent, automatic, and ongoing. No programming is required. For applications where it is useful, however, the following programmable control is provided.

SYNC Operating States

The sync logic can operate in one of three possible modes. The default mode is fully automatic.

Fully automatic synchronization is accomplished by demultiplexing the incoming data stream into four channels, each containing every fourth data-word. Data-words are present for four DAC clock cycles. Data is remultiplexed by sampling each channel with the optimum DAC clock cycle.

Initial synchronization is first established through a hardware reset. This also fully enables the synchronization logic to monitor and resynchronize, as necessary. The AD9726 resynchronizes only if conditions change enough to alter the phase between the data bus and the DAC clock by more than one full clock cycle. In this event, an internal alarm occurs and is followed by an automatic update. During resynchronization, two data-words are typically lost or repeated.

In addition to fully automatic mode, two semi-automatic modes are available.

Sync Manual Mode

In fully automatic mode, the AD9726 both detects when a resynchronization is necessary and initiates an update. In manual mode, automatic updating is disabled. Enable manual mode by setting the SYNCMAN bit in SPI Register 0x02.

In manual mode, the sync logic still monitors incoming data and the DAC clock, but it indicates the need for an update by asserting the SYNCALRM bit (Bit 0 in Register 0x02). In this mode, the user is expected to regularly poll the SYNCALRM bit. When this bit is read back high, the user can issue a manual sync update also by asserting the SYNCUPD bit (Bit 1) in SPI Register 0x02.

SYNCALRM does not indicate that data is being lost but that conditions are close to the point where data may be lost. The

sync logic should be resynchronized by asserting SYNCUPD at the next convenient time.

In manual mode, users can choose when to update the sync logic. When operating with burst data, issuing a sync update between active bursts updates the system without risking the loss of any data. In fact, because SYNCUPD always forces a resynchronization regardless of operational mode, even users in fully automatic mode can reduce the possibility of data loss by occasionally forcing a sync update during idle activity.

If either the data clock or the DAC clock is interrupted for any reason, a SYNCUPD should always be executed to ensure that data bus and DAC clock phase alignment remains optimized.

SYNC External Mode

Going beyond manual mode, sync external mode offers a greater level of control and can be useful if multiple DAC channels are employed in an application. Enable sync external mode by asserting the SYNCEXT bit (Bit 5) in SPI Register 0x16. Manual mode must also be enabled.

The four channels into which each incoming data-word is multiplexed are called quadrants. In any mode, the current quadrant value can always be read back via SYNCOUT (Bits [1:0] of SPI Register 0x15). At sync update, the logic chooses the optimal quadrant and refreshes the value of SYNCOUT.

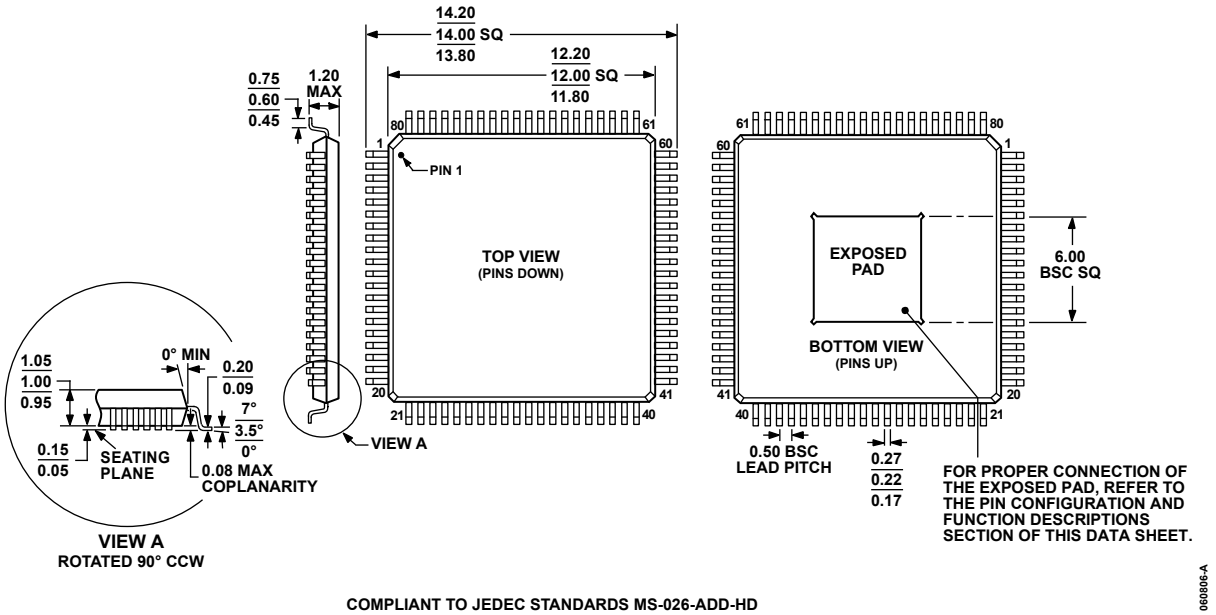
It is also possible to enter a value into SYNCIN (Bits [4:3] of SPI Register 0x16). When external mode is enabled, the logic operates as expected, except that the quadrant value in SYNCIN is used following an update. This can be used to align delays between multiple device outputs.

Operating With SPI Disabled

If the SPI_DIS pin is connected high to ADVDD and the SPI is disabled, the sync logic is placed into manual mode.

SYNCALRM status can then be monitored in hardware via the unused SPI pin SDO (54), and SYNCUPD requests can be entered in hardware via the unused SPI pin SCLK (56). If these two pins are connected together, fully automatic sync operation can be achieved.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-026-ADD-HD

Figure 24. 80-Lead Thin Plastic Quad Flat Package, Exposed Pad [TQFP_EP]
(SV-80-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD9726BSVZ	−40°C to +85°C	80-Lead TQFP_EP	SV-80-1
AD9726BSVZRL	−40°C to +85°C	80-Lead TQFP_EP	SV-80-1
AD9726-EBZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

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