TPS84210 2.95-V to 6-V Input, 2-A Synchronous Buck, Integrated Power Solution

1 Features

- Complete Integrated Power Solution Allows Small Footprint, Low-Profile Design
- Efficiencies Up To 96%
- Wide-Output Voltage Adjust 0.8 V to 3.6 V, with ±1% Reference Accuracy
- Adjustable Switching Frequency (500 kHz to 2 MHz)
- Synchronizes to an External Clock
- Adjustable Slow-Start
- Output Voltage Sequencing / Tracking
- Power Good Output
- Programmable Undervoltage Lockout (UVLO)
- Output Overcurrent Protection
- Over Temperature Protection
- Operating Temperature Range: –40°C to 85°C
- Enhanced Thermal Performance: 12°C/W
- Meets EN55022 Class B Emissions

2 Applications

- Broadband & Communications Infrastructure
- Automated Test and Medical Equipment
- Compact PCI / PCI Express / PXI Express
- DSP and FPGA Point of Load Applications
- High Density Distributed Power Systems

3 Description

The TPS84210RKG is an easy-to-use integrated power solution that combines a 2-A DC/DC converter with power MOSFETs, an inductor, and passives into a low profile, BQFN package. This total power solution requires as few as 3 external components and eliminates the loop compensation and magnetics part selection process.

The BQFN package is easy to solder onto a printed circuit board and allows a compact point-of-load design with greater than 90% efficiency and excellent power dissipation with a thermal impedance of 12°C/W junction to ambient. The device delivers the full 2-A rated output current at 85°C ambient temperature without airflow.

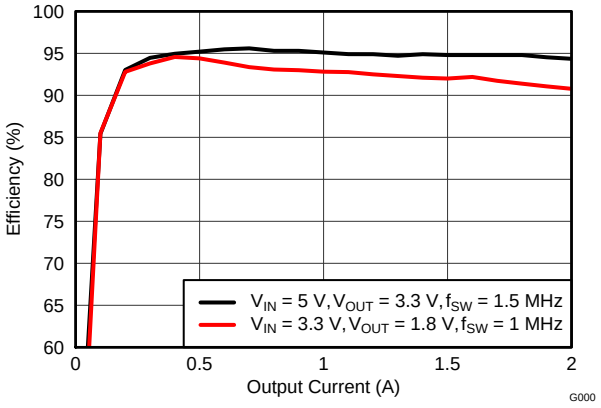
The TPS84210 offers the flexibility and the feature-set of a discrete point-of-load design and is ideal for powering performance DSPs and FPGAs. Advanced packaging technology afford a robust and reliable power solution compatible with standard QFN mounting and testing techniques.

Device Information(1)

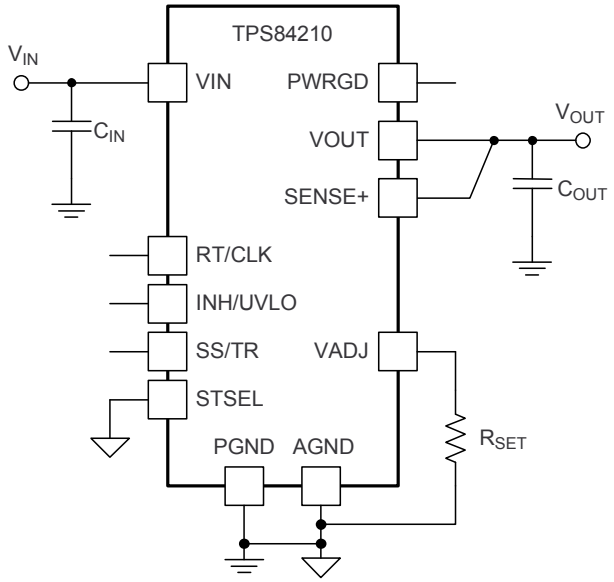
DEVICE NUMBER	PACKAGE	BODY SIZE
TPS84210	QFN (39)	11.0 mm × 9.0 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Application



Efficiency vs Output Current



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (June 2017) to Revision C — **Page**

- Added *Device Information* table ... 1
- Increased the peak reflow temperature and maximum number of reflows to JEDEC specifications for improved manufacturability ... 4
- Added *Mechanical, Packaging, and Orderable Information* section ... 26

Changes from Revision A (March 2012) to Revision B — **Page**

- Added peak reflow and maximum number of reflows information ... 4

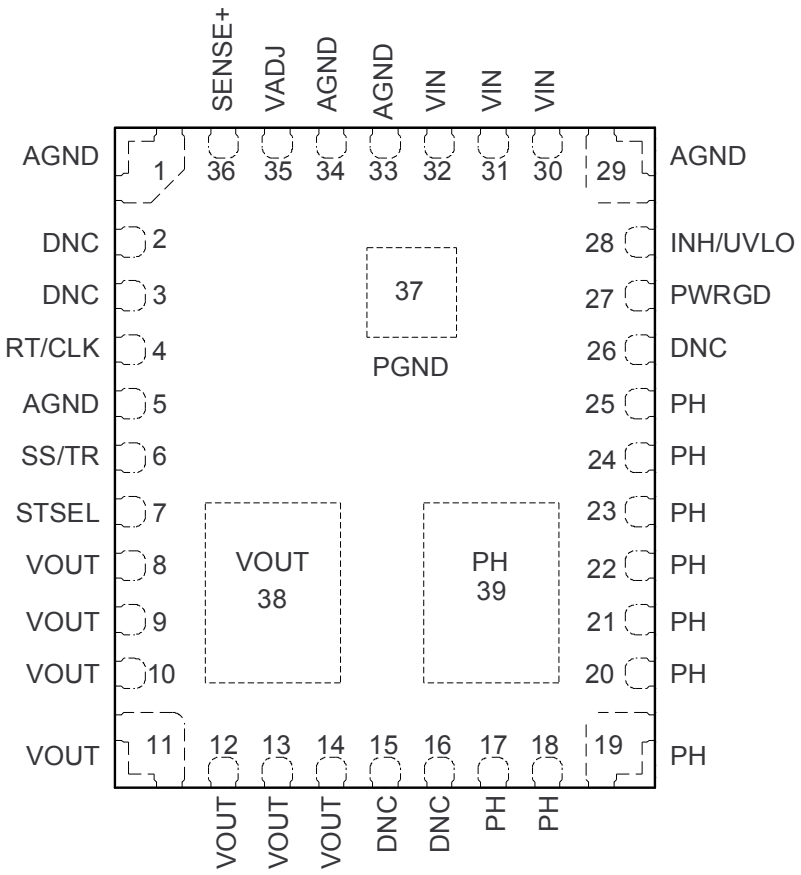
Changes from Original (SEPTEMBER 2011) to Revision A — **Page**

- Adjusted voltage levels in Table 7 ... 20

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5 Pin Configuration and Functions

RKG PACKAGE
39 PINS
(TOP VIEW)



Pin Functions

TERMINAL		DESCRIPTION
NAME	NO.	
AGND	1, 5, 29 33, 34	Zero VDC reference for the analog control circuitry. These pins should be connected directly to the PCB analog ground plane. Not all pins are connected together internally. All pins must be connected together externally with a copper plane or pour directly under the module. Connect the AGND copper area to the PGND copper area at a single point; directly at the pin 37 PowerPAD using multiple vias. See the recommended layout in Figure 34.
PowerPAD (PGND)	37	This pad provides both an electrical and thermal connection to the PCB. This pad should be connected directly to the PCB power ground plane using multiple vias for good electrical and thermal performance. The same vias should also be used to connect to the PCB analog ground plane. See the recommended layout in Figure 34.
DNC	2, 3, 15, 16, 26	Do Not Connect. Do not connect these pins to AGND, to another DNC pin, or to any other voltage. These pins are connected to internal circuitry. Each pin must be soldered to an isolated pad.
INH/UVLO	28	Inhibit and UVLO adjust pin. Use an open drain or open collector output logic to control the INH function. A resistor between this pin and AGND adjusts the UVLO voltage.
PH	17, 18, 19, 20, 21, 22, 23, 24, 25, 39	Phase switch node. These pins should be connected by a small copper island under the device for thermal relief. Do not connect any external component to this pin or tie it to a pin of another function.
PWRGD	27	Power good fault pin. Asserts low if the output voltage is out of tolerance. A pull-up resistor is required.
RT/CLK	4	This pin automatically selects between RT mode and CLK mode. An external timing resistor adjusts the switching frequency of the device. In CLK mode, the device synchronizes to an external clock.

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Pin Functions (continued)

TERMINAL		DESCRIPTION
NAME	NO.	
SENSE+	36	Remote sense connection. Connect this pin to VOUT at the load for improved regulation. This pin must be connected to VOUT at the load, or at the module pins.
SS/TR	6	Slow-start and tracking pin. Connecting an external capacitor to this pin adjusts the output voltage rise time. A voltage applied to this pin allows for tracking and sequencing control.
STSEL	7	Slow-start or track feature select. Connect this pin to AGND to enable the internal SS capacitor with a SS interval of approximately 1.1 ms. Leave this pin open to enable the TR feature.
VADJ	35	Connecting a resistor between this pin and AGND sets the output voltage above the 0.8 V default voltage.
VIN	30, 31, 32	The positive input voltage power pins, which are referenced to PGND. Connect external input capacitance between these pins and the PGND plane, close to the device.
VOUT	8, 9, 10, 11, 12, 13, 14, 38	Output voltage. Connect output capacitors between these pins and the PGND plane, close to the device.

6 Specifications

6.1 Absolute Maximum Ratings(1)

over operating temperature range (unless otherwise noted)

			MIN	MAX	UNIT
Input Voltage	VIN, PWRGD		–0.3	7	V
	INH/UVLO, RT/CLK		–0.3	3.3	V
	SS/TR, STSEL, VADJ		–0.3	3	V
	SENSE+	VADJ rating must also be met	-0.3	VOUT	V
Output Voltage	PH		–0.6	7	V
	PH 10 ns Transient		–2	7	V
	VOUT		-0.6	VIN	V
V_{DIFF} (GND to exposed thermal pad)			–0.2	0.2	V
Source Current	RT/CLK, INH/UVLO			±100	µA
	PH			Current Limit	A
Sink Current	PH			Current Limit	A
	SS/TR			±100	µA
	PWRGD			10	mA
Operating Junction Temperature(2)			–40	125(2)	°C
Storage Temperature			–65	150	°C
Peak Reflow Case Temperature(3)				250(4)	°C
Maximum Number of Reflows Allowed(3)				3(4)	
Mechanical shock	Mil-STD-883D, Method 2002.3, 1 msec, 1/2 sine, mounted			1500	G
Mechanical vibration	Mil-STD-883D, Method 2007.2, 20-2000Hz			20	G

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) See the temperature derating curves in the *Typical Characteristics* section for thermal information.
(3) For soldering specifications, refer to the Soldering Requirements for BQFN Packages application note.
(4) Devices with a date code prior to week 14 2018 (1814) have a peak reflow case temperature of 240°C with a maximum of one reflow.

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6.2 Package Specifications

TPS84210		UNIT
Weight		0.85 grams
Flammability	Meets UL 94 V-O	
MTBF Calculated reliability	Per Bellcore TR-332, 50% stress, T_A = 40°C, ground benign	38.5 MHrs

6.3 Thermal Information

THERMAL METRIC(1)		TPS84210 RKG (QFN) 39 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance(2)	12	°C/W
ψ_{JT}	Junction-to-top characterization parameter(3)	2.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter(4)	9.7	°C/W

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.
(2) The junction-to-ambient thermal resistance, θ_{JA}, applies to devices soldered directly to a 100 mm x 100 mm double-sided PCB with 1 oz. copper and natural convection cooling. Additional airflow reduces θ_{JA}.
(3) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature, T_J, of a device in a real system, using a procedure described in JESD51-2A (sections 6 and 7). $T_J = \psi_{JT} * Pdis + T_T$; where Pdis is the power dissipated in the device and T_T is the temperature of the top of the device.
(4) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature, T_J, of a device in a real system, using a procedure described in JESD51-2A (sections 6 and 7). $T_J = \psi_{JB} * Pdis + T_B$; where Pdis is the power dissipated in the device and T_B is the temperature of the board 1mm from the device.

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6.4 Electrical Characteristics

Over -40°C to 85°C free-air temperature, VIN = 3.3 V, V_{OUT} = 1.8 V, I_{OUT} = 2 A, C_{IN1} = 47 µF ceramic, C_{IN2} = 220 µF poly-tantalum, C_{OUT1} = 47 µF ceramic, C_{OUT2} = 100 µF poly-tantalum (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{OUT}	Output current	T_A = 85°C, natural convection		0		2	A
VIN	Input voltage range	Over I_{OUT} range		2.95 (1)		6	V
UVLO	VIN Undervoltage lockout	VIN = increasing			3.05	3.135	V
		VIN = decreasing		2.5	2.75		
$V_{OUT(adj)}$	Output voltage adjust range	Over I_{OUT} range		0.8		3.6	V
V_{OUT}	Set-point voltage tolerance	T_A = 25°C, I_{OUT} = 0A				±1.0% (2)	
	Temperature variation	-40°C ≤ T_A ≤ +85°C, I_{OUT} = 0A			±0.3%		
	Line regulation	Over VIN range, T_A = 25°C, I_{OUT} = 0A			±0.1%		
	Load regulation	Over I_{OUT} range, T_A = 25°C			±0.1%		
	Total output voltage variation	Includes set-point, line, load, and temperature variation				±1.5% (2)	
η	Efficiency	VIN = 5 V, I_O = 1 A	V_{OUT} = 3.3V, f_{SW} = 1.5 MHz		95%		
			V_{OUT} = 2.5V, f_{SW} = 1.5 MHz		93%		
			V_{OUT} = 1.8V, f_{SW} = 1 MHz		92%		
			V_{OUT} = 1.5V, f_{SW} = 1 MHz		91%		
			V_{OUT} = 1.2V, f_{SW} =750 kHz		90%		
			V_{OUT} = 1.0V, f_{SW} = 650 kHz		88%		
			V_{OUT} = 0.8V, f_{SW} = 650 kHz		87%		
		VIN = 3.3V, I_O = 1 A	V_{OUT} = 1.8V, f_{SW} = 1 MHz		93%		
			V_{OUT} = 1.5V, f_{SW} = 1 MHz		92%		
			V_{OUT} = 1.2V, f_{SW} = 750 kHz		91%		
			V_{OUT} = 1.0V, f_{SW} = 650 kHz		89%		
			V_{OUT} = 0.8V, f_{SW} = 650 kHz		87%		
V_{OUT} ripple	Output voltage ripple	20-MHz bandwith			9		mV_{PP}
I_{LIM}	Overcurrent threshold				3.5		A
	Transient response	1.0 A/µs load step from 0.5A to 1.5A	Recovery time		80		µs
			V_{OUT} over/undershoot		45		mV
V_{INH-H}	Inhibit Control	Inhibit High Voltage			1.25	Open (3)	V
V_{INH-L}		Inhibit Low Voltage		–0.3		1.0	
$I_{I(stby)}$	Input standby current	INH pin to AGND			70	100	µA
Power Good	PWRGD Thresholds	V_{OUT} rising	Good		93%		
			Fault		107%		
		V_{OUT} falling	Fault		91%		
			Good		105%		
	PWRGD Low Voltage	I(PWRGD) = 0.33 mA				0.3	V
	Thermal Shutdown	Shutdown Temperature			175		°C
		Hysteresis			15		°C
C_{IN}	External input capacitance		Ceramic	47 (4)			µF
			Non-ceramic		220 (4)		

(1) The minimum VIN depends on VOUT and the switching frequency. Please refer to Table 7 for operating limits.
(2) The stated limit of the set-point voltage tolerance includes the tolerance of both the internal voltage reference and the internal adjustment resistor. The overall output voltage tolerance will be affected by the tolerance of the external R_{SET} resistor.
(3) This control pin has an internal pullup. Do not place an external pull-up resistor on this pin. If this pin is left open circuit, the device operates when input power is applied. A small low-leakage MOSFET is recommended for control. See the application section for further guidance.
(4) A minimum of 47µF of ceramic capacitance is required across the input for proper operation. Locate the capacitor close to the device. An additional 220µF of bulk capacitance is recommended. See Table 5 for more details.

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Electrical Characteristics (continued)

Over -40°C to 85°C free-air temperature, VIN = 3.3 V, V_{OUT} = 1.8 V, I_{OUT} = 2 A, C_{IN1} = 47 µF ceramic, C_{IN2} = 220 µF poly-tantalum, C_{OUT1} = 47 µF ceramic, C_{OUT2} = 100 µF poly-tantalum (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{OUT}	External output capacitance	Ceramic	47 (5)	150	650 (6)	µF
		Non-ceramic		100 (5)	1000 (6)	
		Equivalent series resistance (ESR)			25	mΩ

(5) The amount of required output capacitance varies depending on the output voltage (see Table 3). The amount of required capacitance must include at least 47µF of ceramic capacitance. Locate the capacitance close to the device. Adding additional capacitance close to the load improves the response of the regulator to load transients. See Table 3 and Table 5 for more details.
(6) When using both ceramic and non-ceramic output capacitance, the combined maximum must not exceed 1200µF.

6.5 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SW}	Switching frequency	Over VIN and I_{OUT} ranges, RT/CLK pin OPEN	400	500	600	kHz
f_{CLK}	CLK Control	Synchronization frequency	500		2000	kHz
V_{CLK-H}		CLK high level	2.2		3.3	V
V_{CLK-L}		CLK low level	–0.3		0.4	V
CLK_PW		CLK Pulse Width	75 (1)			ns

(1) The maximum synchronization clock pulse width is dependant on VIN, V_{OUT}, and the synchronization frequency. See the Synchronization (CLK) section for more information.

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6.6 Typical Characteristics (VIN = 5 V)

The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter. Applies to Figure 1, Figure 2, and . The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to devices soldered directly to a 100 mm × 100 mm double-sided PCB with 1 oz. copper. Applies to Figure 4.

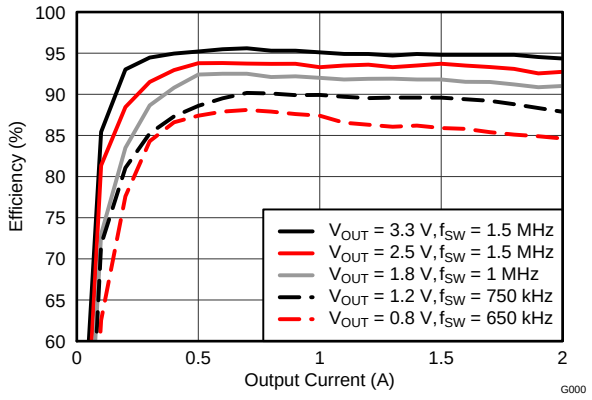


Figure 1. Efficiency vs. Output Current

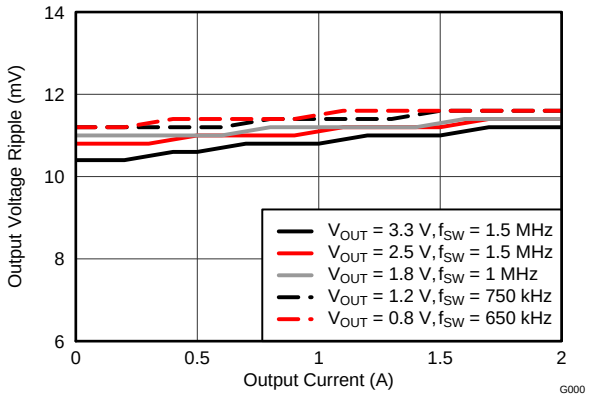


Figure 2. Voltage Ripple vs. Output Current

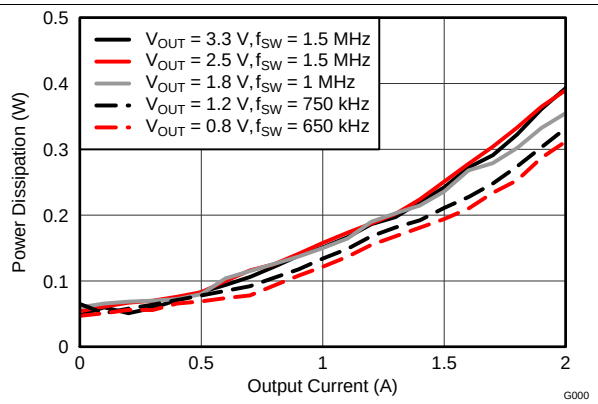


Figure 3. Power Dissipation vs. Output Current

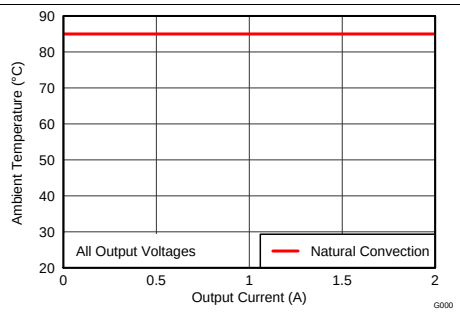


Figure 4. Safe Operating Area

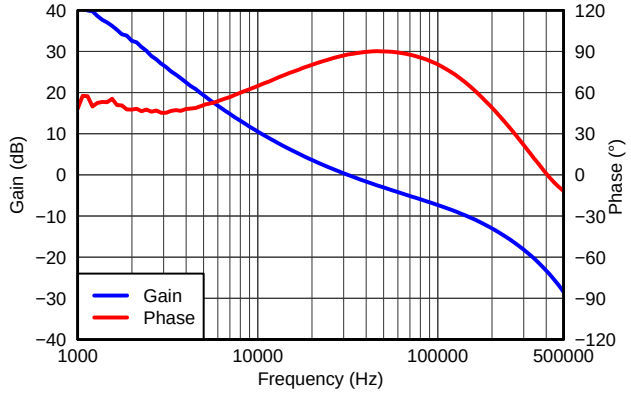


Figure 5. V_{OUT}= 1.8 V, I_{OUT}= 2 A, C_{OUT1}= 47 µF ceramic, C_{OUT2}= 100 µF POSCAP, f_{SW}= 1 MHz

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6.7 Typical Characteristics (VIN = 3.3 V)

The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter. Applies to Figure 6, Figure 7, and Figure 8. The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to devices soldered directly to a 100 mm × 100 mm double-sided PCB with 1 oz. copper. Applies to Figure 9.

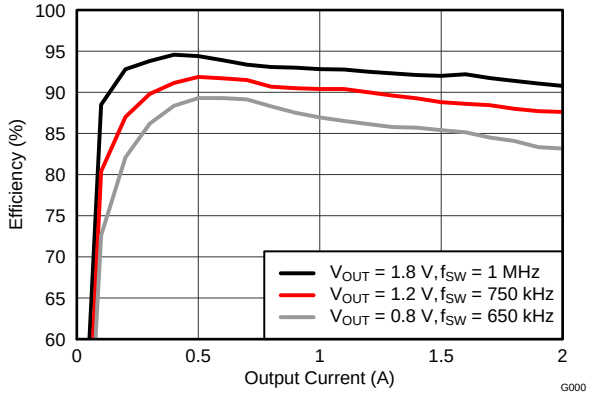


Figure 6. Efficiency vs. Output Current

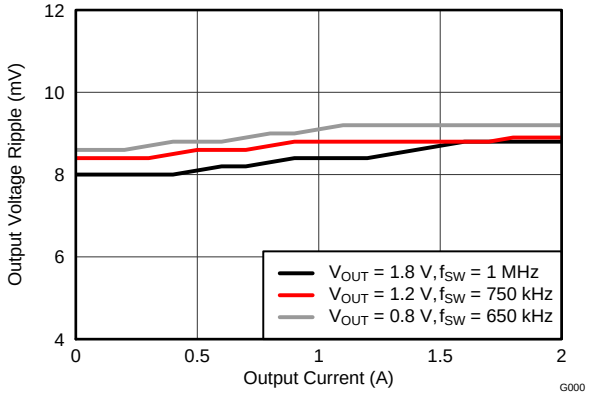


Figure 7. Voltage Ripple vs. Output Current

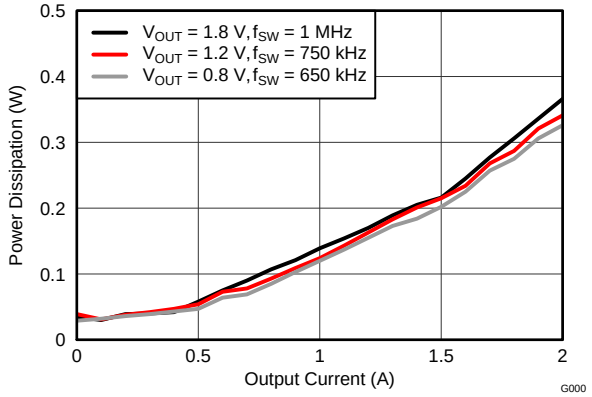


Figure 8. Power Dissipation vs. Output Current

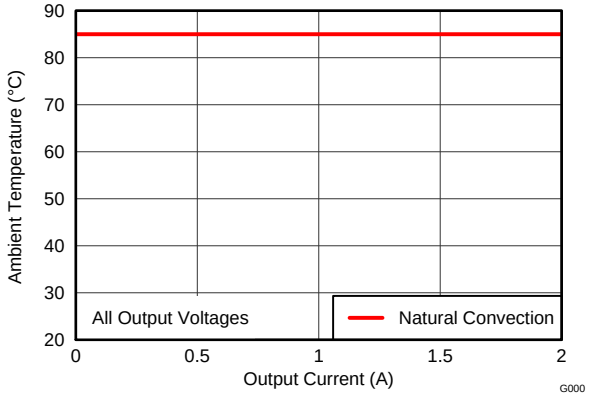


Figure 9. Safe Operating Area

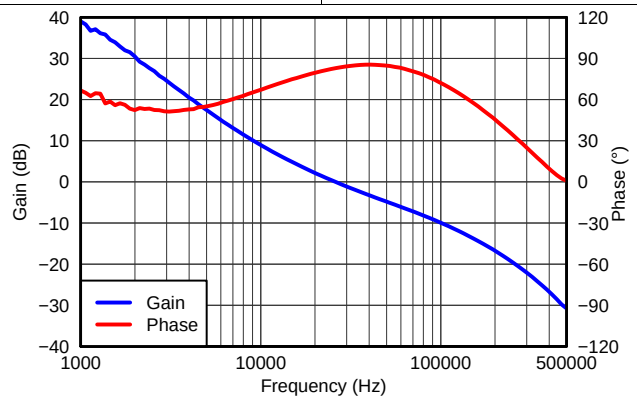
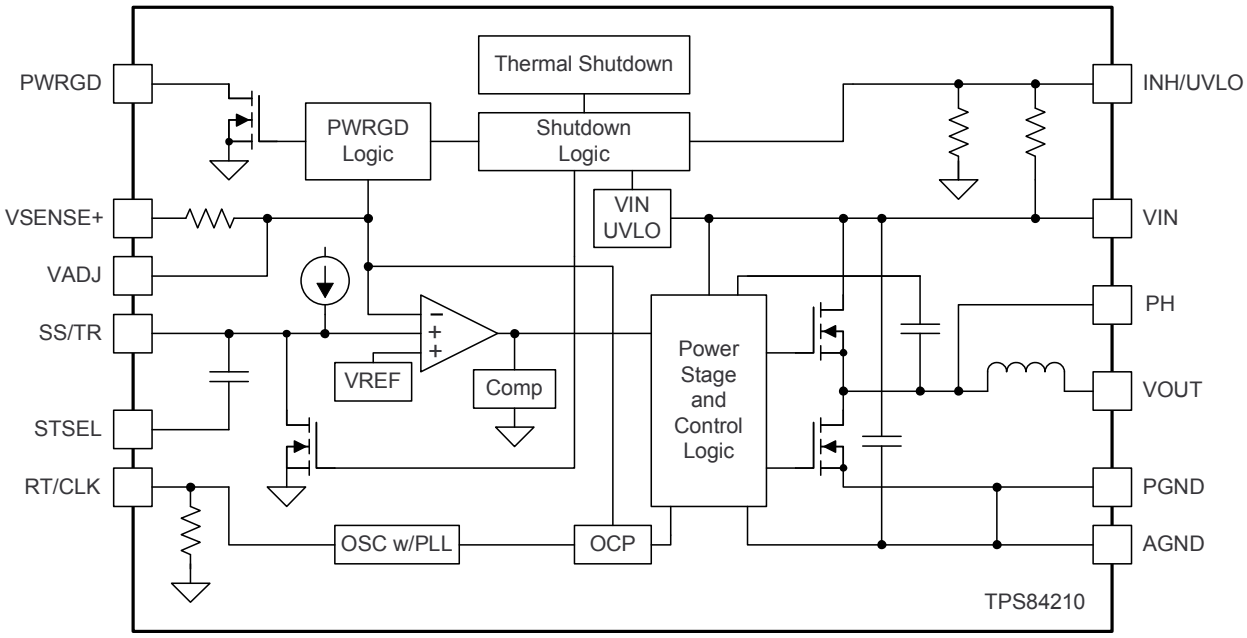


Figure 10. V_{OUT}= 1.8 V, I_{OUT}= 2 A, C_{OUT1}= 47 µF ceramic, C_{OUT2}= 100 µF POSCAP, f_{SW}= 1 MHz

6.8 Functional Block Diagram



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7 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Application Information

7.1.1 Adjusting The Output Voltage

The VADJ control sets the output voltage of the TPS84210. The output voltage adjustment range is from 0.8V to 3.6V. The adjustment method requires the addition of R_{SET}, which sets the output voltage, the connection of SENSE+ to VOUT, and in some cases R_{RT} which sets the switching frequency. The R_{SET} resistor must be connected directly between the VADJ (pin 35) and AGND (pin 33 & 34). The SENSE+ pin (pin 36) must be connected to VOUT either at the load for improved regulation or at VOUT of the module. The R_{RT} resistor must be connected directly between the RT/CLK (pin 4) and AGND (pins 33 & 34).

Table 1 gives the standard external R_{SET} resistor for a number of common bus voltages, along with the recommended R_{RT} resistor for that output voltage.

Table 1. Standard R_{SET} Resistor Values for Common Output Voltages

RESISTORS	OUTPUT VOLTAGE V_{OUT} (V)					
	0.8	1.2	1.5	1.8	2.5	3.3
R_{SET} (kΩ)	open	2.87	1.65	1.15	0.673	0.459
R_{RT} (kΩ)	1200	715	348	348	174	174

For other output voltages, the value of the required resistor can either be calculated using the following formula, or simply selected from the range of values given in Table 2.

$$R_{SET} = \frac{1.43}{\left(\left(\frac{V_{OUT}}{0.803}\right) - 1\right)} \ (k\Omega) \quad (1)$$

Table 2. Standard R_{SET} Resistor Values

V_{OUT} (V)	R_{SET} (kΩ)	R_{RT}(kΩ)	f_{SW}(kHz)	V_{OUT} (V)	R_{SET} (kΩ)	R_{RT}(kΩ)	f_{SW}(kHz)
0.8	open	1200	650	2.3	0.768	174	1500
0.9	11.8	1200	650	2.4	0.715	174	1500
1.0	5.83	1200	650	2.5	0.673	174	1500
1.1	3.83	1200	650	2.6	0.634	174	1500
1.2	2.87	715	750	2.7	0.604	174	1500
1.3	2.32	715	750	2.8	0.576	174	1500
1.4	1.91	715	750	2.9	0.549	174	1500
1.5	1.65	348	1000	3.0	0.523	174	1500
1.6	1.43	348	1000	3.1	0.499	174	1500
1.7	1.27	348	1000	3.2	0.475	174	1500
1.8	1.15	348	1000	3.3	0.459	174	1500
1.9	1.05	348	1000	3.4	0.442	174	1500
2.0	0.953	174	1500	3.5	0.422	174	1500
2.1	0.845	174	1500	3.6	0.412	174	1500
2.2	0.825	174	1500				

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7.2 Capacitor Recommendations For The TPS84210 Power Supply

7.2.1 Capacitor Technologies

7.2.1.1 Electrolytic, Polymer-Electrolytic Capacitors

When using electrolytic capacitors, high-quality, computer-grade electrolytic capacitors are recommended. Polymer-electrolytic type capacitors are recommended for applications where the ambient operating temperature is less than 0°C. The Sanyo OS-CON capacitor series is suggested due to the lower ESR, higher rated surge, power dissipation, ripple current capability, and small package size. Aluminum electrolytic capacitors provide adequate decoupling over the frequency range of 2 kHz to 150 kHz, and are suitable when ambient temperatures are above 0°C.

7.2.1.2 Ceramic Capacitors

The performance of aluminum electrolytic capacitors is less effective than ceramic capacitors above 150 kHz. Multilayer ceramic capacitors have a low ESR and a resonant frequency higher than the bandwidth of the regulator. They can be used to reduce the reflected ripple current at the input as well as improve the transient response of the output.

7.2.1.3 Tantalum, Polymer-Tantalum Capacitors

Polymer-tantalum type capacitors are recommended for applications where the ambient operating temperature is less than 0°C. The Sanyo POSCAP series and Kemet T530 capacitor series are recommended rather than many other tantalum types due to their lower ESR, higher rated surge, power dissipation, ripple current capability, and small package size. Tantalum capacitors that have no stated ESR or surge current rating are not recommended for power applications.

7.2.2 Input Capacitor

The TPS84210 requires a minimum input capacitance of 47 µF of ceramic capacitance. An additional 220 µF polymer-tantalum capacitor is recommended for applications with transient load requirements. The combined ripple current rating of the input capacitors must be at least 1000 mArms. Table 5 includes a preferred list of capacitors by vendor. For applications where the ambient operating temperature is less than 0°C, an additional 1 µF, X5R or X7R ceramic capacitor placed between VIN and AGND is recommended.

7.2.3 Output Capacitor

The required output capacitance is determined by the output voltage of the TPS84210. See Table 3 for the amount of required capacitance. The required output capacitance must include at least one 47 µF ceramic capacitor. For applications where the ambient operating temperature is less than 0°C, an additional 100 µF polymer-tantalum capacitor is recommended. When adding additional non-ceramic bulk capacitors, low-ESR devices like the ones recommended in Table 5 are required. The required capacitance above the minimum is determined by actual transient deviation requirements. See Table 4 for typical transient response values for several output voltage, input voltage and capacitance combinations. Table 5 includes a preferred list of capacitors by vendor.

Table 3. Required Output Capacitance

V_{OUT} RANGE (V)		MINIMUM REQUIRED C_{OUT} (µF)
MIN	MAX	
0.8	< 1.8	147 (1)
1.8	< 3.3	100 (2)
3.3	3.6	47 (2)

(1) Minimum required must include at least 1 × 47 µF ceramic capacitor plus 1 × 100 µF polymer-tantalum capacitor.
(2) Minimum required must include at least 47 µF of ceramic capacitance.

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Table 4. Output Voltage Transient Response

CIN1 = 1 × 47 µF CERAMIC, C_{IN2} = 220 µF POLYMER-TANTALUM, LOAD STEP = 1 A, 1 A/µs						
V_{OUT} (V)	V_{IN} (V)	C_{OUT1} Ceramic	C_{OUT2} BULK	VOLTAGE DEVIATION (mV)	PEAK-PEAK (mV)	RECOVERY TIME (µs)
0.8	3.3	47 µF	100 µF	30	55	70
		47 µF	330 µF	20	35	70
	5	47 µF	100 µF	30	50	65
		47 µF	330 µF	20	35	65
1.2	3.3	47 µF	100 µF	35	65	65
		47 µF	330 µF	25	50	80
	5	47 µF	100 µF	35	70	65
		47 µF	330 µF	25	45	75
1.8	3.3	47 µF	100 µF	45	80	70
		47 µF	330 µF	35	65	90
	5	47 µF	100 µF	40	65	70
		47 µF	330 µF	35	65	90
2.5	5	47 µF	100 µF	60	100	70
		2 × 47 µF	-	75	140	75
3.3	5	47 µF	100 µF	70	130	80
		47 µF	-	90	180	90

Table 5. Recommended Input/Output Capacitors(1)

VENDOR	SERIES	PART NUMBER	CAPACITOR CHARACTERISTICS		
			WORKING VOLTAGE (V)	CAPACITANCE (µf)	ESR(2) (mΩ)
Murata	X5R	GRM32ER61C476K	16	47	2
TDK	X5R	C3225X5R0J107M	6.3	100	2
Murata	X5R	GRM32ER60J107M	6.3	100	2
TDK	X5R	C3225X5R0J476K	6.3	47	2
Murata	X5R	GRM32ER60J476M	6.3	47	2
Sanyo	POSCAP	10TPE220ML	10	220	25
Kemet	T520	T520V107M010ASE025	10	100	25
Sanyo	POSCAP	6TPE100MPB	6.3	100	25
Sanyo	POSCAP	2R5TPE220M7	2.5	220	7
Kemet	T530	T530D227M006ATE006	6.3	220	6
Kemet	T530	T530D337M006ATE010	6.3	330	10
Sanyo	POSCAP	2TPF330M6	2.0	330	6
Sanyo	POSCAP	6TPE330MFL	6.3	330	15

(1) **Capacitor Supplier Verification**
Please verify availability of capacitors identified in this table.
RoHS, Lead-free and Material Details
Please consult capacitor suppliers regarding material composition, RoHS status, lead-free status, and manufacturing process requirements.
(2) Maximum ESR @ 100 kHz, 25°C.

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7.3 Transient Response

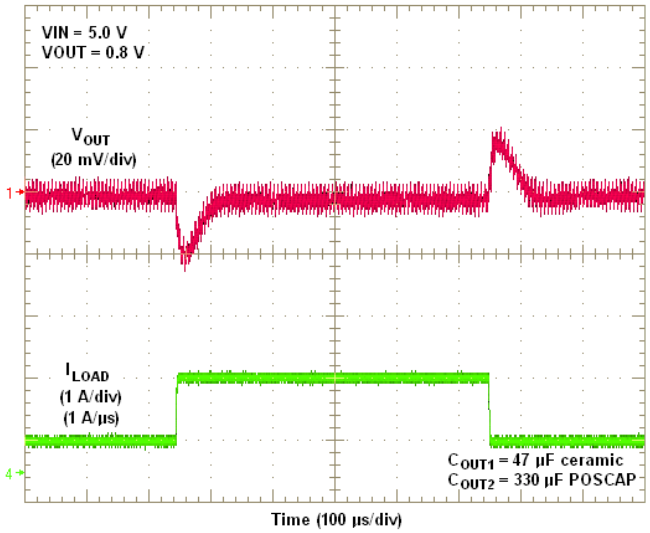


Figure 11. VIN = 5 V, VOUT = 0.8 V, 1 A Load Step

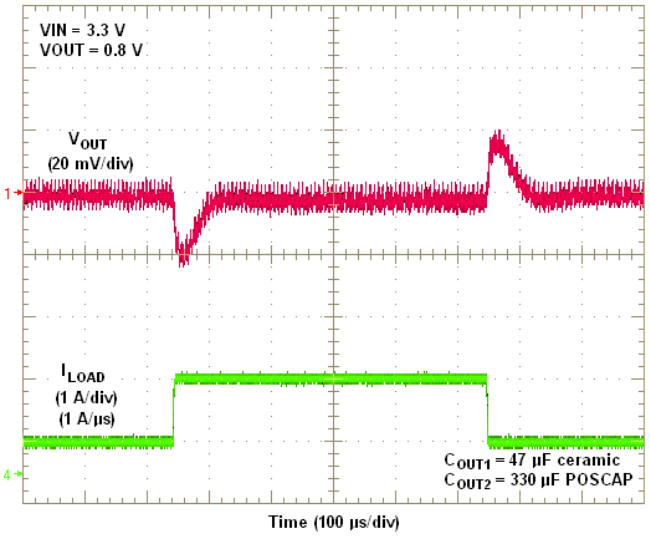


Figure 12. VIN = 3.3 V, VOUT = 0.8 V, 1 A Load Step

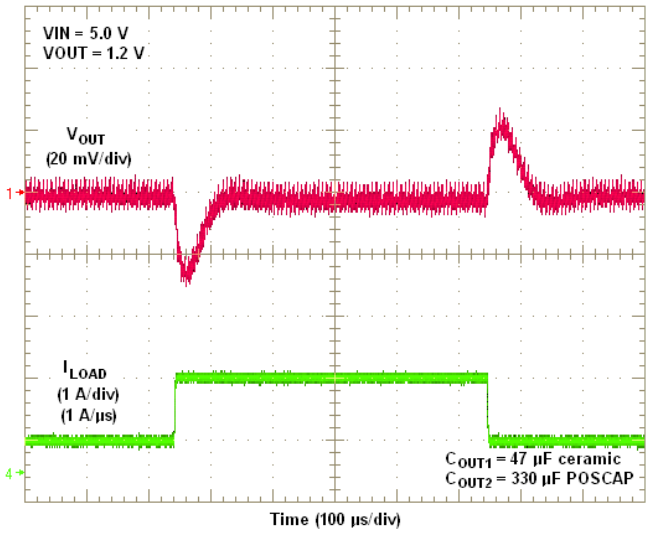


Figure 13. VIN = 5V, VOUT = 1.2V, 1A Load Step

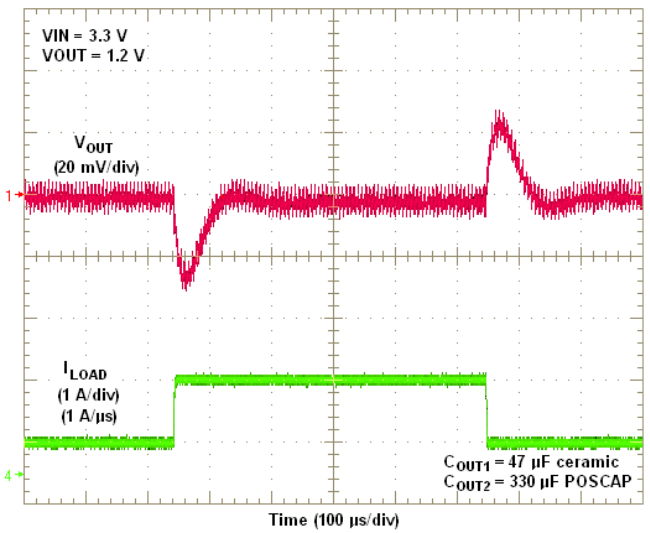


Figure 14. VIN = 3.3V, VOUT = 1.2V, 1A Load Step

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Transient Response (continued)

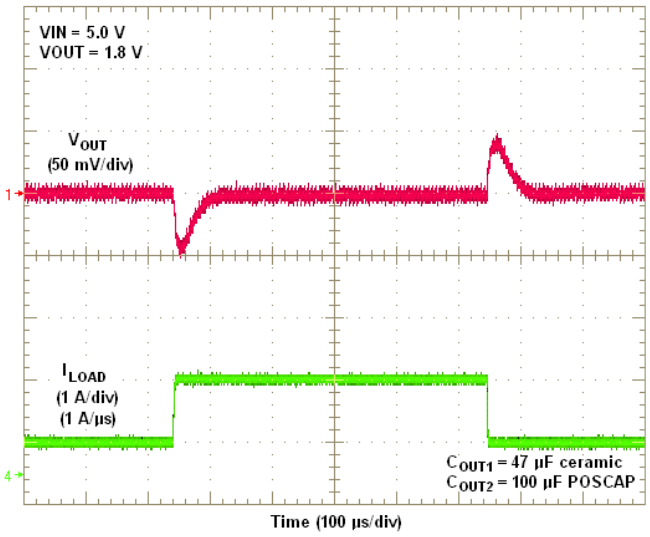


Figure 15. VIN = 5V, VOUT = 1.8V, 1A Load Step

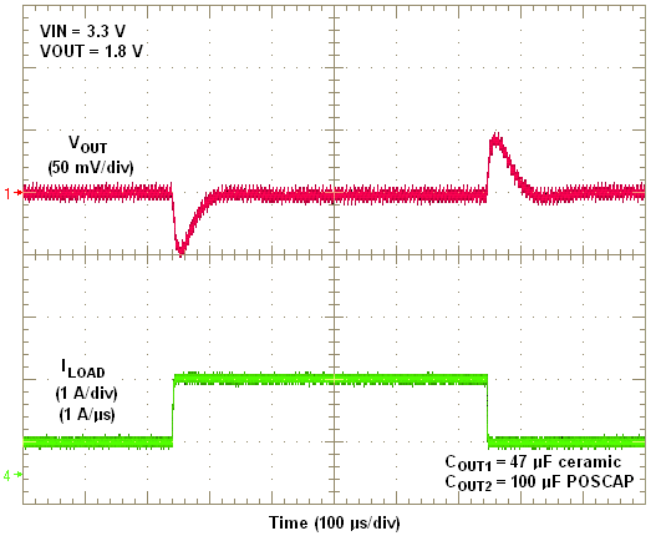


Figure 16. VIN = 3.3V, VOUT = 1.8V, 1A Load Step

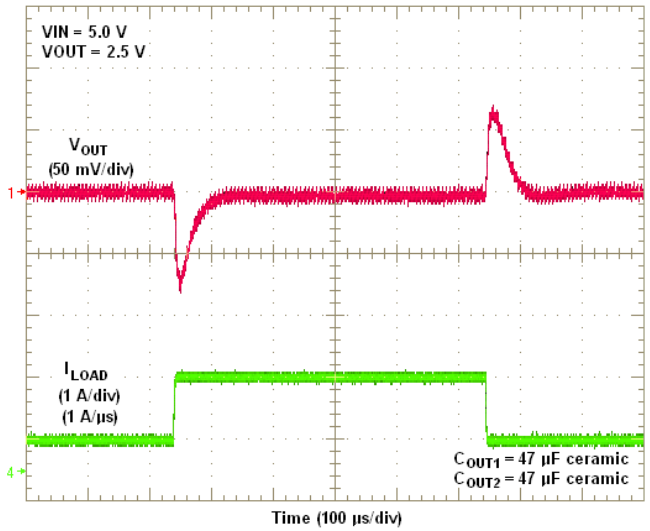


Figure 17. VIN = 5V, VOUT = 2.5V, 1A Load Step

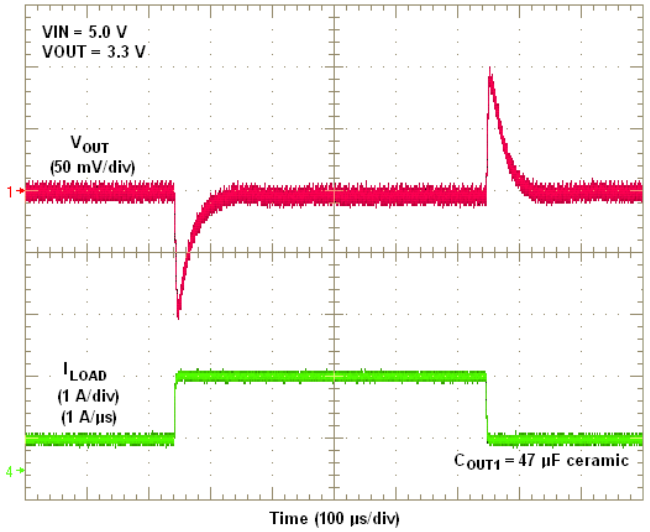


Figure 18. VIN = 5V, VOUT = 3.3V, 1A Load Step

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7.4 Application Schematics

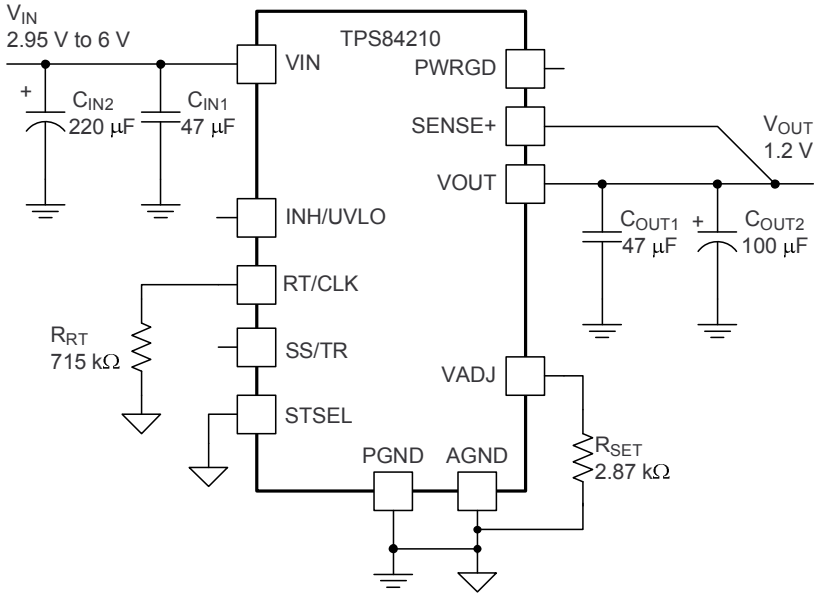


Figure 19. Typical Schematic
VIN = 2.95 V to 6.0 V, VOUT = 1.2 V

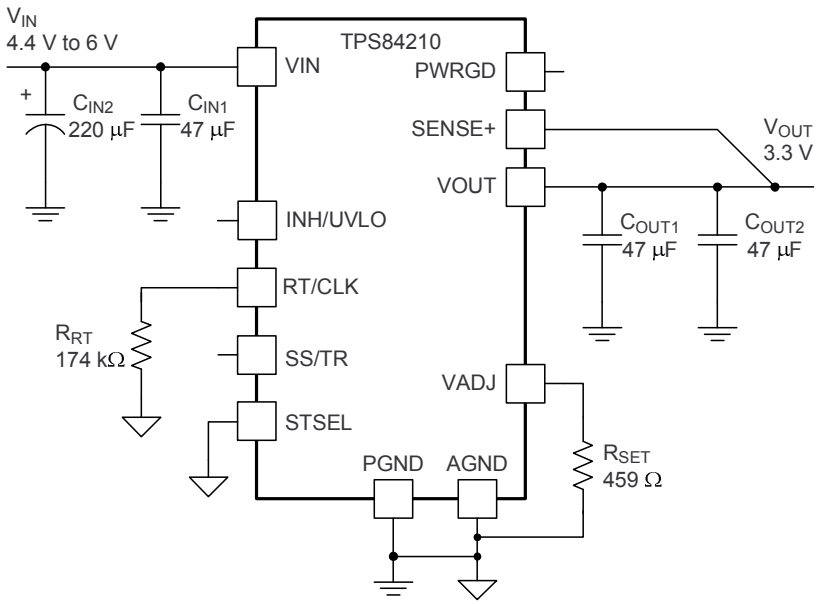


Figure 20. Typical Schematic
VIN = 4.4 V to 6.0 V, VOUT = 3.3 V

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7.5 Power Good (PWRGD)

The PWRGD pin is an open drain output. Once the voltage on the SENSE+ pin is between 93% and 105% of the set voltage, the PWRGD pin pull-down is released and the pin floats. The recommended pull-up resistor value is between 10 kΩ and 100 kΩ to a voltage source that is 6 V or less. The PWRGD pin is in a defined state once VIN is greater than 1.2 V, but with reduced current sinking capability. The PWRGD pin achieves full current sinking capability once the VIN pin is above 2.95V. Figure 21 shows the PWRGD waveform during power-up. The PWRGD pin is pulled low when the voltage on SENSE+ is lower than 91% or greater than 107% of the nominal set voltage. Also, the PWRGD pin is pulled low if the input UVLO or thermal shutdown is asserted, or if the INH pin is pulled low.

7.6 Power-Up Characteristics

When configured as shown in the front page schematic, the TPS84210 produces a regulated output voltage following the application of a valid input voltage. During the power-up, internal soft-start circuitry slows the rate that the output voltage rises, thereby limiting the amount of in-rush current that can be drawn from the input source. The soft-start circuitry introduces a short time delay from the point that a valid input voltage is recognized. Figure 21 shows the start-up waveforms for a TPS84210, operating from a 5-V input and with the output voltage adjusted to 1.8 V. The waveform is measured with a 2-A constant current load.

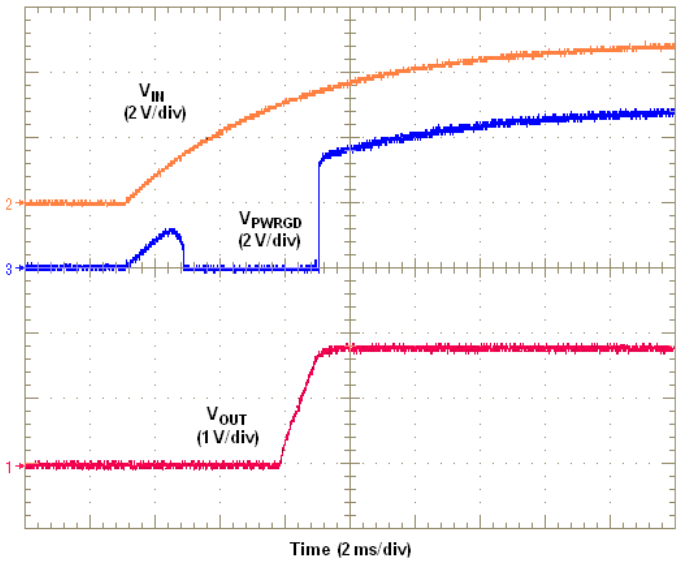


Figure 21. Start-Up Waveforms

7.7 Remote Sense

The SENSE+ pin must be connected to V_{OUT} at the load, or at the device pins.

Connecting the SENSE+ pin to V_{OUT} at the load improves the load regulation performance of the device by allowing it to compensate for any I-R voltage drop between its output pins and the load. An I-R drop is caused by the high output current flowing through the small amount of pin and trace resistance. This should be limited to a maximum of 300 mV.

NOTE

The remote sense feature is not designed to compensate for the forward drop of nonlinear or frequency dependent components that may be placed in series with the converter output. Examples include OR-ing diodes, filter inductors, ferrite beads, and fuses. When these components are enclosed by the SENSE+ connection, they are effectively placed inside the regulation control loop, which can adversely affect the stability of the regulator.

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7.8 Output On/Off Inhibit (INH)

The INH pin provides electrical on/off control of the device. Once the INH pin voltage exceeds the threshold voltage, the device starts operation. If the INH pin voltage is pulled below the threshold voltage, the regulator stops switching and enters low quiescent current state.

The INH pin has an internal pull-up current source, allowing the user to float the INH pin for enabling the device. If an application requires controlling the INH pin, use an open drain/collector device, or a suitable logic gate to interface with the pin. Do not place an external pull-up resistor on this pin. Figure 22 shows the typical application of the inhibit function.

Turning Q1 on applies a low voltage to the inhibit control (INH) pin and disables the output of the supply, as shown in Figure 23. If Q1 is turned off, the supply executes a soft-start power-up sequence, as shown in Figure 24. The waveforms were measured with a 2-A constant current load.

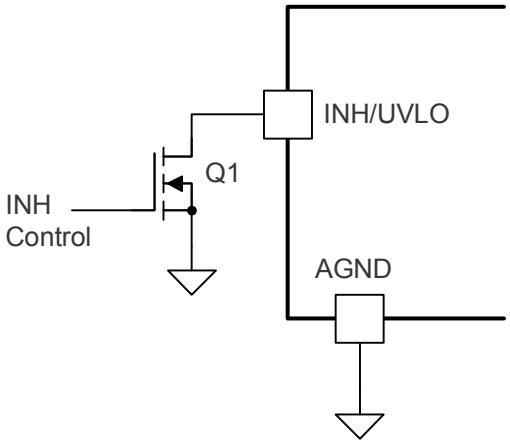


Figure 22. Typical Inhibit Control

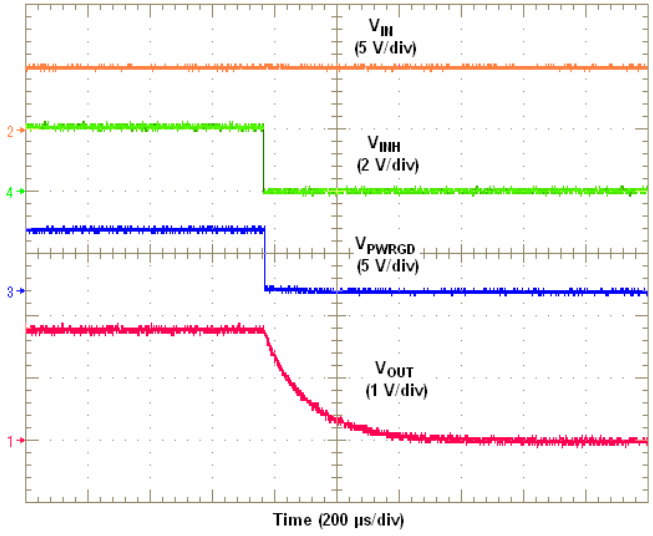


Figure 23. Inhibit Turn-Off

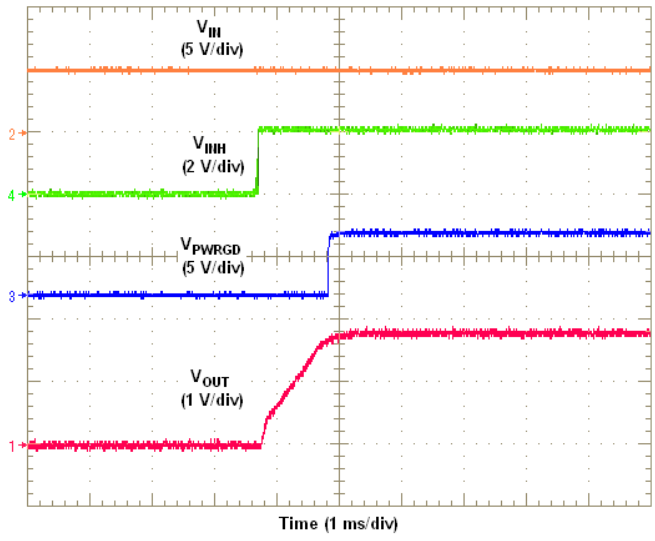


Figure 24. Inhibit Turn-On

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7.9 Slow Start (SS/TR)

Connecting the STSEL pin to AGND and leaving SS/TR pin open enables the internal SS capacitor with a slow start interval of approximately 1.1 ms. Adding additional capacitance between the SS pin and AGND increases the slow start time. Table 6 shows an additional SS capacitor connected to the SS/TR pin and the STSEL pin connected to AGND. See Table 6 below for SS capacitor values and timing interval.

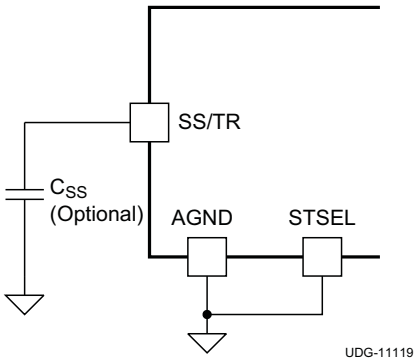


Figure 25. Slow-Start Capacitor (C_{SS}) and STSEL Connection

Table 6. Slow-Start Capacitor Values and Slow-Start Time

C_{SS} (pF)	open	2200	4700	10000	15000	22000	25000
SS Time (msec)	1.1	1.9	2.8	4.6	6.4	8.8	9.8

7.10 Overcurrent Protection

For protection against load faults, the TPS84210 uses current limiting. The device is protected from overcurrent conditions by cycle-by-cycle current limiting and frequency foldback. During an overcurrent condition the output current is limited and the output voltage is reduced, as shown in Figure 26. When the overcurrent condition is removed, the output voltage returns to the established voltage, as shown in Figure 27.

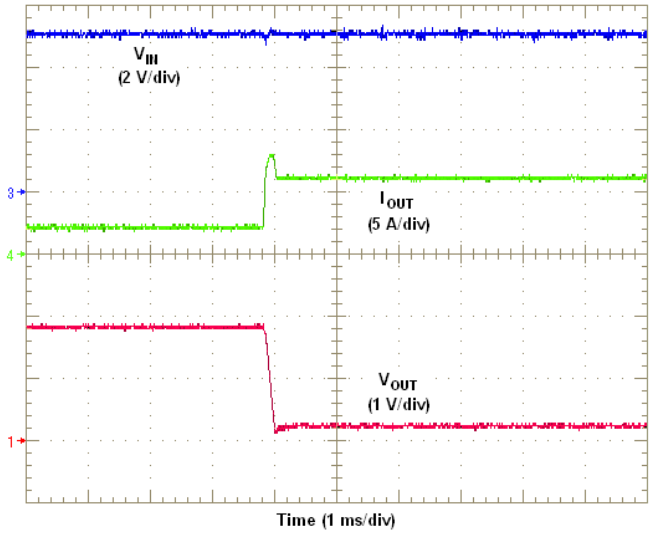


Figure 26. Overcurrent Limiting

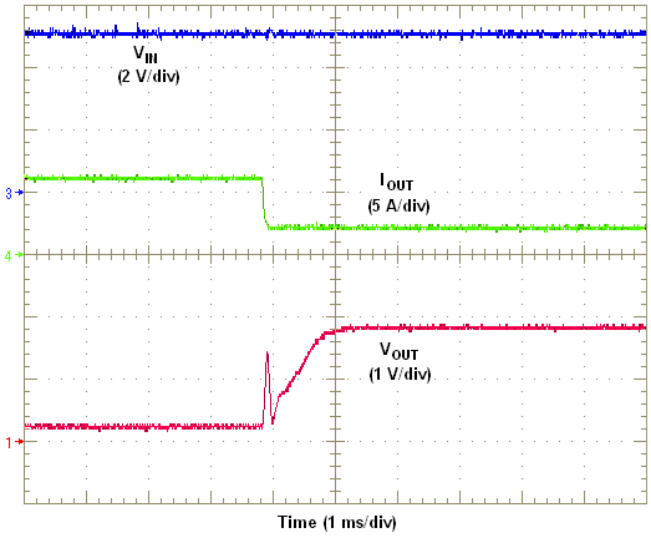


Figure 27. Removal of Overcurrent Condition

7.11 Synchronization (CLK)

An internal phase locked loop (PLL) has been implemented to allow synchronization between 500 kHz and 2 MHz, and to easily switch from RT mode to CLK mode. To implement the synchronization feature, connect a square wave clock signal to the RT/CLK pin with a minimum pulse width of 75 ns. The maximum clock pulse width must be calculated using Equation 2. The clock signal amplitude must transition lower than 0.4 V and higher than 2.2 V. The start of the switching cycle is synchronized to the falling edge of RT/CLK pin. In applications where both RT mode and CLK mode are needed, the device can be configured as shown in Figure 28.

Before the external clock is present, the device works in RT mode and the switching frequency is set by RT resistor (R_{RT}). When the external clock is present, the CLK mode overrides the RT mode. The device switches from RT mode to CLK mode and the RT/CLK pin becomes high impedance as the PLL starts to lock onto the frequency of the external clock. The device will lock to the external clock frequency approximately 15 µs after a valid clock signal is present. It is not recommended to switch from CLK mode back to RT mode because the internal switching frequency drops to a lower frequency before returning to the switching frequency set by the RT resistor.

$$CLK_PW_{MAX} = \frac{0.75 \times \left(1 - \frac{V_{OUT}}{V_{IN(min)}}\right)}{f_{SW}} \quad (2)$$

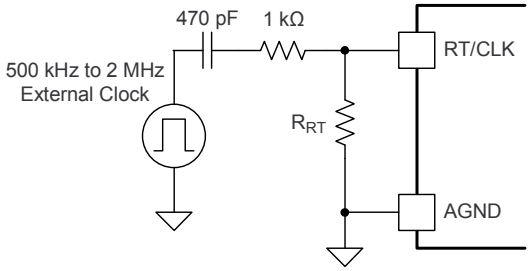


Figure 28. CLK/RT Configuration

The synchronization frequency must be selected based on the output voltages of the devices being synchronized. Table 7 shows the allowable frequencies for a given range of output voltages based on a resistive load. 5-V input applications requiring 1.5 A or less can synchronize to a wider frequency range. For the most efficient solution, always synchronize to the lowest allowable frequency. For example, an application requires synchronizing three TPS84210 devices with output voltages of 1.2V@1.7A, 1.8@1.1AV and 3.3V@ 1.0A, all powered from VIN = 5V. Table 7 shows that all three output voltages can be synchronized to any frequency between 700 kHz to 1 MHz. For best efficiency, choose 700 kHz as the sychronization frequency.

Table 7. Synchronization Frequency vs Output Voltage

SYNCHRONIZATION FREQUENCY (kHz)	R_{RT} (kΩ)	VIN = 5 V				VIN = 3.3 V	
		I_{OUT} ≤ 1.5 A		I_{OUT} > 1.5 A		All I_{OUT}	
		V_{OUT} RANGE (V)		V_{OUT} RANGE (V)		V_{OUT} RANGE (V)	
		MIN	MAX	MIN	MAX	MIN	MAX
500	open	0.8	1.4	0.8	0.8	0.8	1.1
550	3400	0.8	1.6	0.8	0.9	0.8	1.2
600	1800	0.8	1.9	0.8	1.1	0.8	2.0
650	1200	0.8	2.4	0.8	1.2	0.8	2.2
700	887	0.8	3.6	0.8	1.3	0.8	2.4
750	715	0.9	3.6	0.9	1.5	0.8	2.5
800	590	0.9	3.6	0.9	1.7	0.8	2.5
900	511	1.0	3.6	1.0	2.2	0.8	2.5
1000	348	1.2	3.6	1.2	2.5	0.8	2.5
1250	232	1.4	3.6	1.4	3.3	1.0	2.5
1500	174	1.7	3.6	1.7	3.6	1.1	2.5
1750	137	2.0	3.6	2.0	3.6	1.3	2.4

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Table 7. Synchronization Frequency vs Output Voltage (continued)

SYNCHRONIZATION FREQUENCY (kHz)	R_{RT} (kΩ)	VIN = 5 V				VIN = 3.3 V	
		I_{OUT} ≤ 1.5 A		I_{OUT} > 1.5 A		All I_{OUT}	
		V_{OUT} RANGE (V)		V_{OUT} RANGE (V)		V_{OUT} RANGE (V)	
		MIN	MAX	MIN	MAX	MIN	MAX
2000	113	2.3	3.6	2.3	3.6	1.5	2.3

7.12 Sequencing (SS/TR)

Many of the common power supply sequencing methods can be implemented using the SS/TR, INH and PWRGD pins. The sequential method is illustrated in Figure 29 using two TPS84210 devices. The PWRGD pin of the first device is coupled to the INH pin of the second device which enables the second power supply once the primary supply reaches regulation. Do not place a pull-up resistor on PWRGD in this configuration. Figure 30 shows sequential turn-on waveforms of two TPS84210 devices.

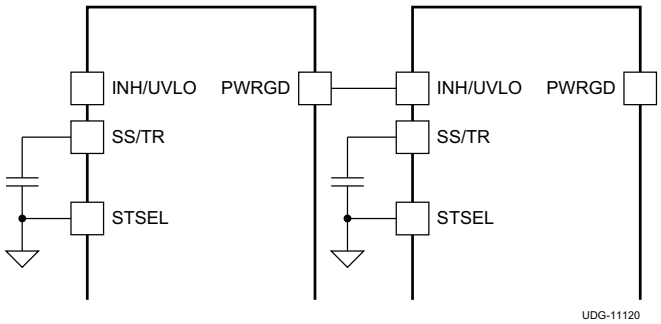


Figure 29. Sequencing Schematic

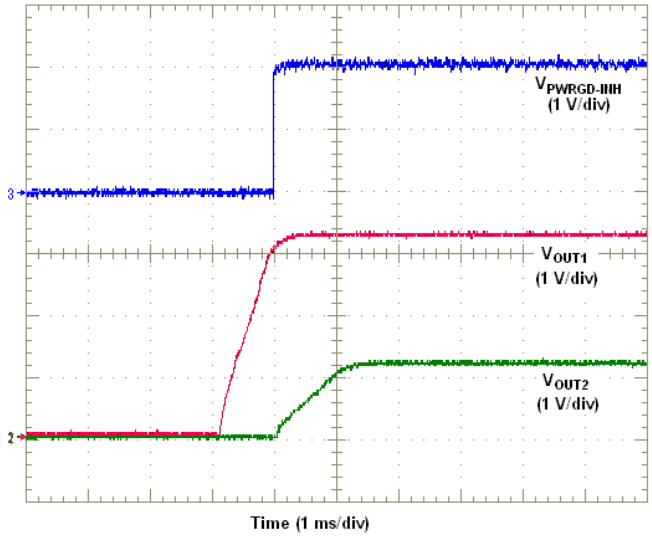


Figure 30. Sequencing Waveforms

Simultaneous power supply sequencing can be implemented by connecting the resistor network of R1 and R2 shown in Figure 31 to the output of the power supply that needs to be tracked or to another voltage reference source. Figure 32 shows simultaneous turn-on waveforms of two TPS84210 devices. Use Equation 3 and Equation 4 to calculate the values of R1 and R2.

$$R1 = \frac{(V_{OUT2} \times 12.6)}{0.803} \ (k\Omega) \quad (3)$$

$$R2 = \frac{0.803 \times R1}{(V_{OUT2} - 0.803)} \ (k\Omega) \quad (4)$$

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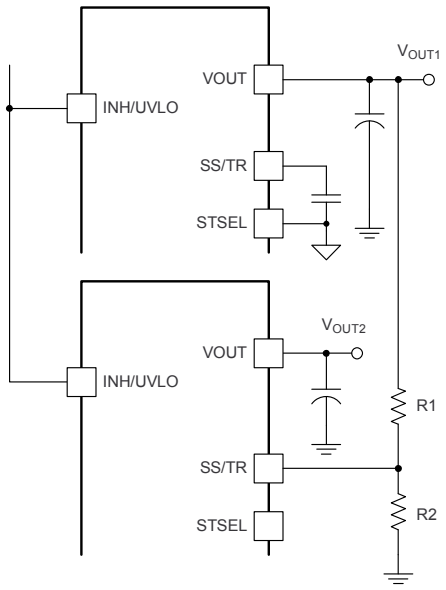


Figure 31. Simultaneous Tracking Schematic

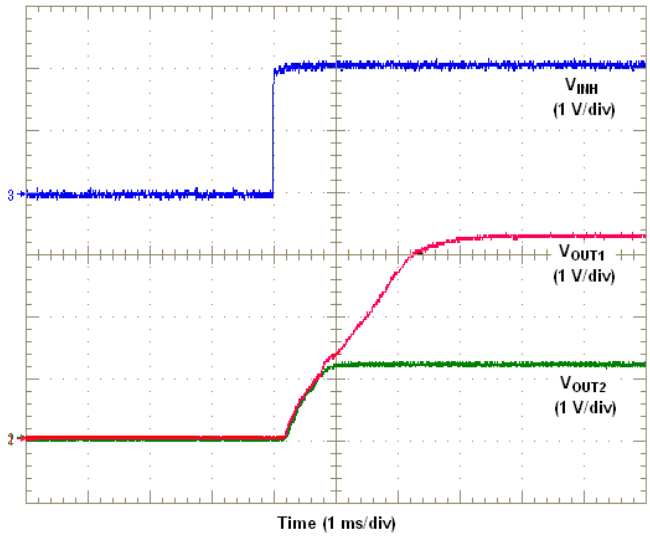


Figure 32. Simultaneous Tracking Waveforms

7.13 Programmable Undervoltage Lockout (UVLO)

The TPS84210 implements internal UVLO circuitry on the VIN pin. The device is disabled when the VIN pin voltage falls below the internal VIN UVLO threshold. The internal VIN UVLO rising threshold is 3.135 V (max) with a typical hysteresis of 300 mV.

If an application requires a higher UVLO threshold on the VIN pin, the UVLO pin can be configured as shown in Figure 33. Table 8 lists standard values for R_{UVLO} to adjust the VIN UVLO voltage up.

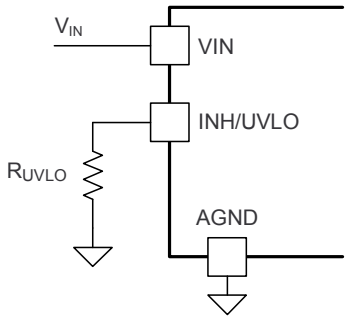


Figure 33. Adjustable VIN UVLO

Table 8. Standard Resistor values for Adjusting VIN UVLO

VIN UVLO (V) (typ)	3.25	3.5	3.75	4.0	4.25	4.5	4.75
R_{UVLO} (kΩ)	294	133	86.6	63.4	49.9	42.2	35.7
Hysteresis (mV)	325	335	345	355	365	375	385

7.14 Thermal Shutdown

The internal thermal shutdown circuitry forces the device to stop switching if the junction temperature exceeds 175°C typically. The device reinitiates the power up sequence when the junction temperature drops below 160°C typically.

7.15 Layout Guidelines

To achieve optimal electrical and thermal performance, an optimized PCB layout is required. Figure 34, shows a typical PCB layout. Some considerations for an optimized layout are:

- Use large copper areas for power planes (VIN, VOUT, and PGND) to minimize conduction loss and thermal stress.
- Place ceramic input and output capacitors close to the module pins to minimize high frequency noise.
- Locate additional output capacitors between the ceramic capacitor and the load.
- Place a dedicated AGND copper area beneath the TPS84210.
- Connect the AGND and PGND copper area at one point; directly at the pin 37 PowerPad using multiple vias.
- Place R_{SET}, R_{RT}, and C_{SS} as close as possible to their respective pins.
- Use multiple vias to connect the power planes to internal layers.

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7.16 Layout Example

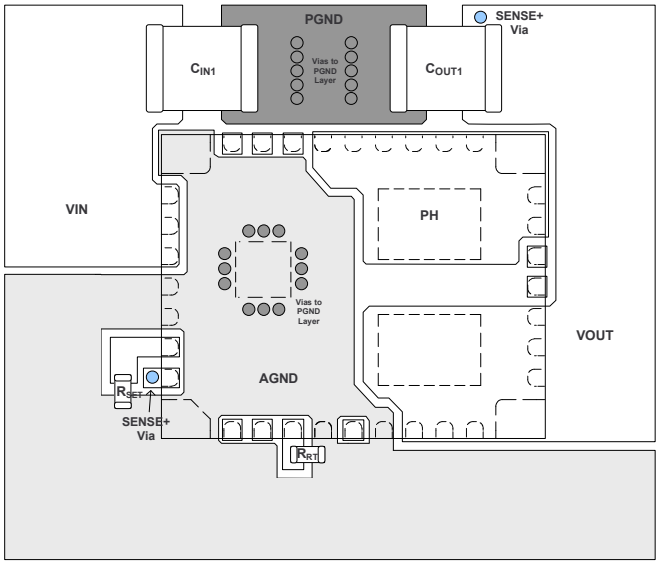


Figure 34. Typical Top-Layer Recommended Layout

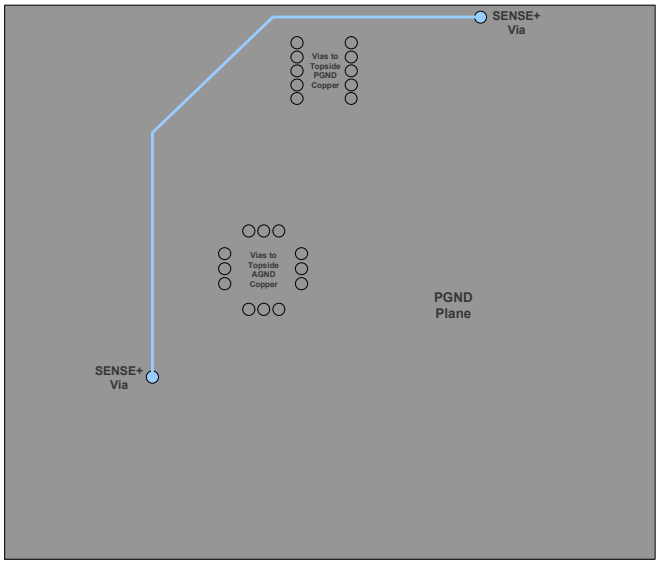


Figure 35. Typical PGND-Layer Recommended Layout

7.17 EMI

The TPS84210 is compliant with EN55022 Class B radiated emissions. Figure 36 and Figure 37 show typical examples of radiated emissions plots for the TPS84210 operating from 5V and 3.3V respectively. Both graphs include the plots of the antenna in the horizontal and vertical positions.

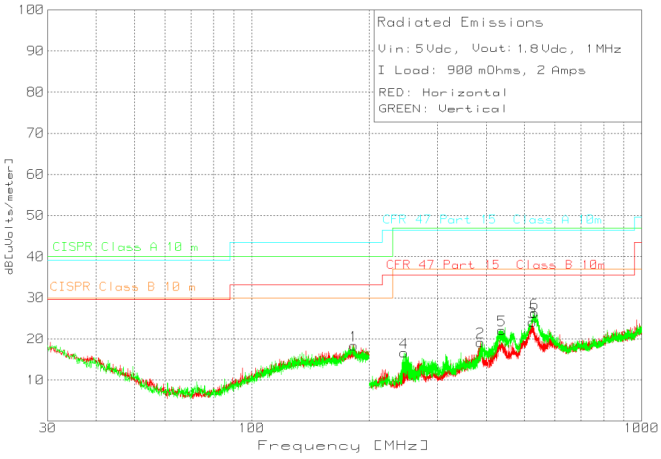


Figure 36. Radiated Emissions 5-V Input, 1.8-V Output, 2-A Load (EN55022 Class B)

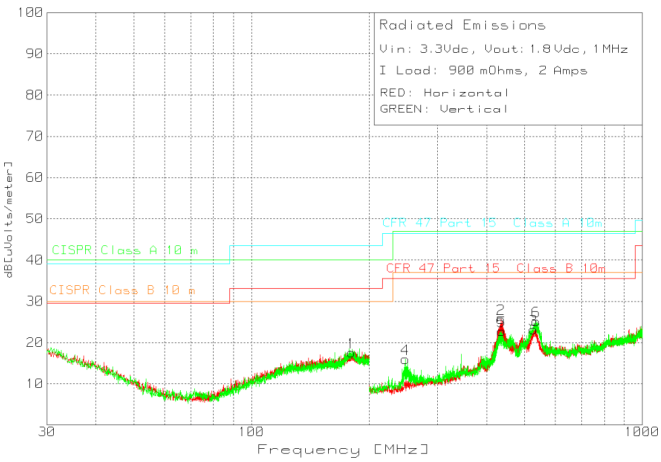


Figure 37. Radiated Emissions 3.3-V Input, 1.8-V Output, 2-A Load (EN55022 Class B)

8 Device and Documentation Support

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

8.3 Trademarks

E2E is a trademark of Texas Instruments.

8.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

SLYZ022 — *TI Glossary*.

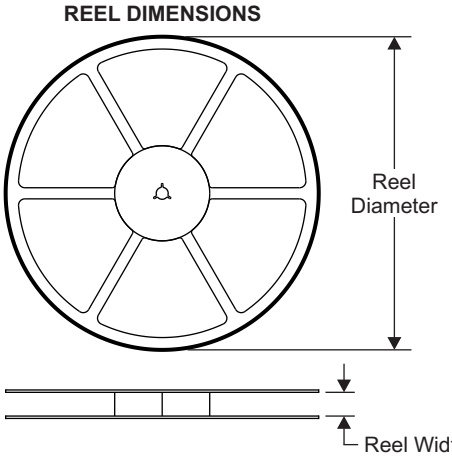
This glossary lists and explains terms, acronyms, and definitions.

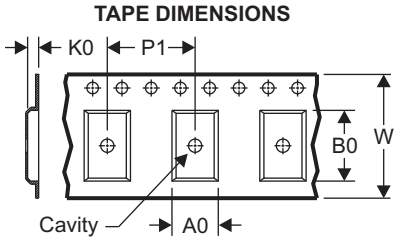
9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

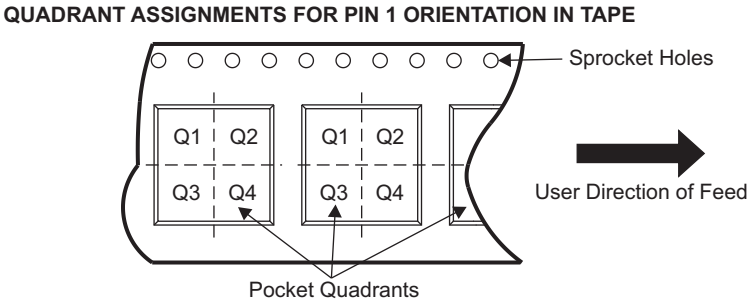
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9.1 Tape and Reel Information





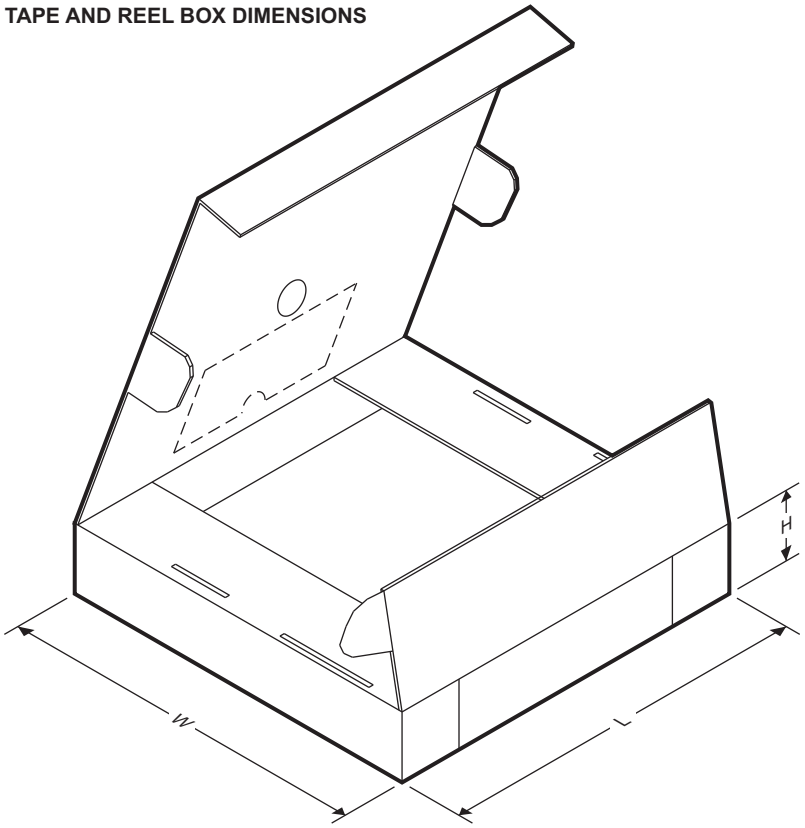
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS84210RKGR	B1FQN	RKG	39	500	330.0	24.4	9.35	11.35	3.1	16.0	24.0	Q1
TPS84210RKGT	B1QFN	RKG	39	250	330.0	24.4	9.35	11.35	3.1	16.0	24.0	Q1

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TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS84210RKGR	B1FQN	RKG	39	500	383.0	353.0	58.0
TPS84210RKGT	B1QFN	RKG	39	250	383.0	353.0	58.0

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS84210RKGR	ACTIVE	B1QFN	RKG	39	500	RoHS Exempt & Green	NIPDAU	Level-3-250C-168 HR	-40 to 85	TPS84210	Samples
TPS84210RKGT	ACTIVE	B1QFN	RKG	39	250	RoHS Exempt & Green	NIPDAU	Level-3-250C-168 HR	-40 to 85	TPS84210	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

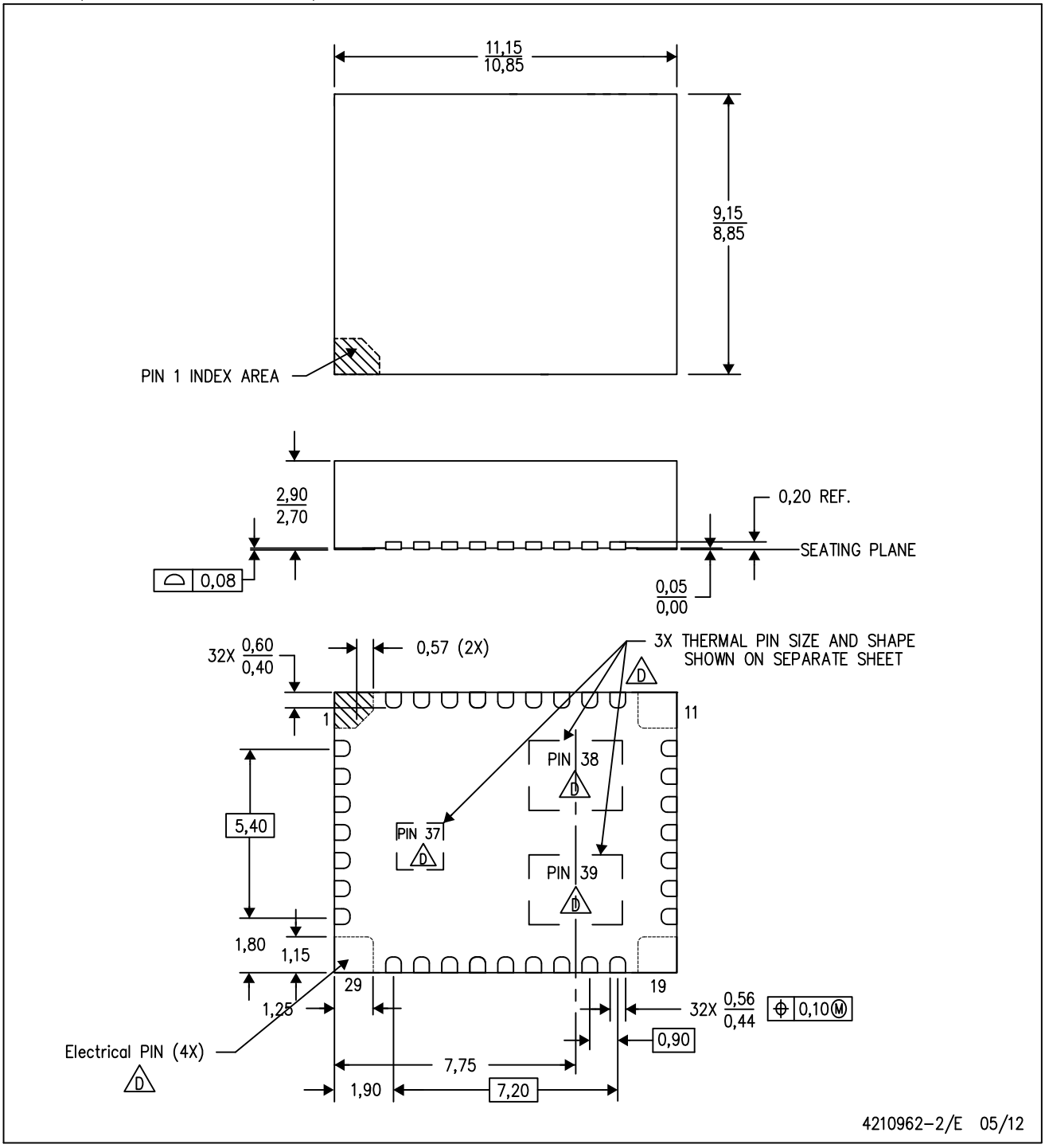
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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RKG (R–PB1QFN–N39) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane.

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