MP4653

Real LIPS CC/CV Mode LLC TV LED Driver

DESCRIPTION

The MP4653 is a CC/CV mode LLC TV LED driver for LED backlighting, especially for large size TV LED backlighting. Powered by 9V to 30V input supplies, the MP4653 outputs two 180 degree phase shifted driving signals for the external power stages. Its enhanced 9V gate driver provides adequate driving capability and can directly drive the external MOSFETs through an external gate driving transformer.

The MP4653 integrates a constant current control loop for the LED current regulation and also a constant voltage control loop for the DC bus voltage, which is used to generate system power supplies like 12V/5V with other DC/DC converters. The CC/CV control loop programs the operating frequency of the LLC power stage and thus regulates the LED current and also the bus voltage.

The MP4653 incorporates both analog dimming and PWM dimming to the LED current. A driving signal is output to directly drive the dimming MOSFET, which helps to achieve fast and high contrast ratio PWM dimming.

The PWM dimming signal is also used for the CC/CV mode control. At PWM on interval, the CC mode is effective and the LED current is regulated; at PWM off interval, the CV mode is effective and the DC bus voltage is regulated. The gate driving signal and thus the energy through the power stage are continuous at both the PWM on interval and the PWM off interval. This helps to eliminate the system audible noise at PWM dimming.

The MP4653 features sufficient and smart protection to increase system reliability. It protects the fault condition at both the DC bus stage and the LED driver stage.

The protection for the DC bus stage includes the over voltage protection and over current protection (short protection).

The protection for the LED driver stage includes the open LED protection, short LED protection, over LED current protection and any point of LED string short to ground protection.

Thermal protection is integrated in MP4653. The MP4653 is available in SOIC20 package.

FEATURES

- Secondary Side “Real LIPS” LLC Controller
- CC/CV Frequency Control Loop
- Audible Noise Elimination
- Continuous driving signal at PWM dimming and LED fault condition
- 9V to 30V Input Voltage Range
- Analog and PWM Dimming
- Input Under Voltage Lockout
- DC Bus Output Over Voltage Protection
- DC Bus Short Protection
- System Auto-recovery and Hiccup Timer
- LED Open, Short Protection
- LED Output Over Voltage, Over LED Current Protection
- Any Point of LED String Short to GND Protection
- Available in SOIC 20 Package

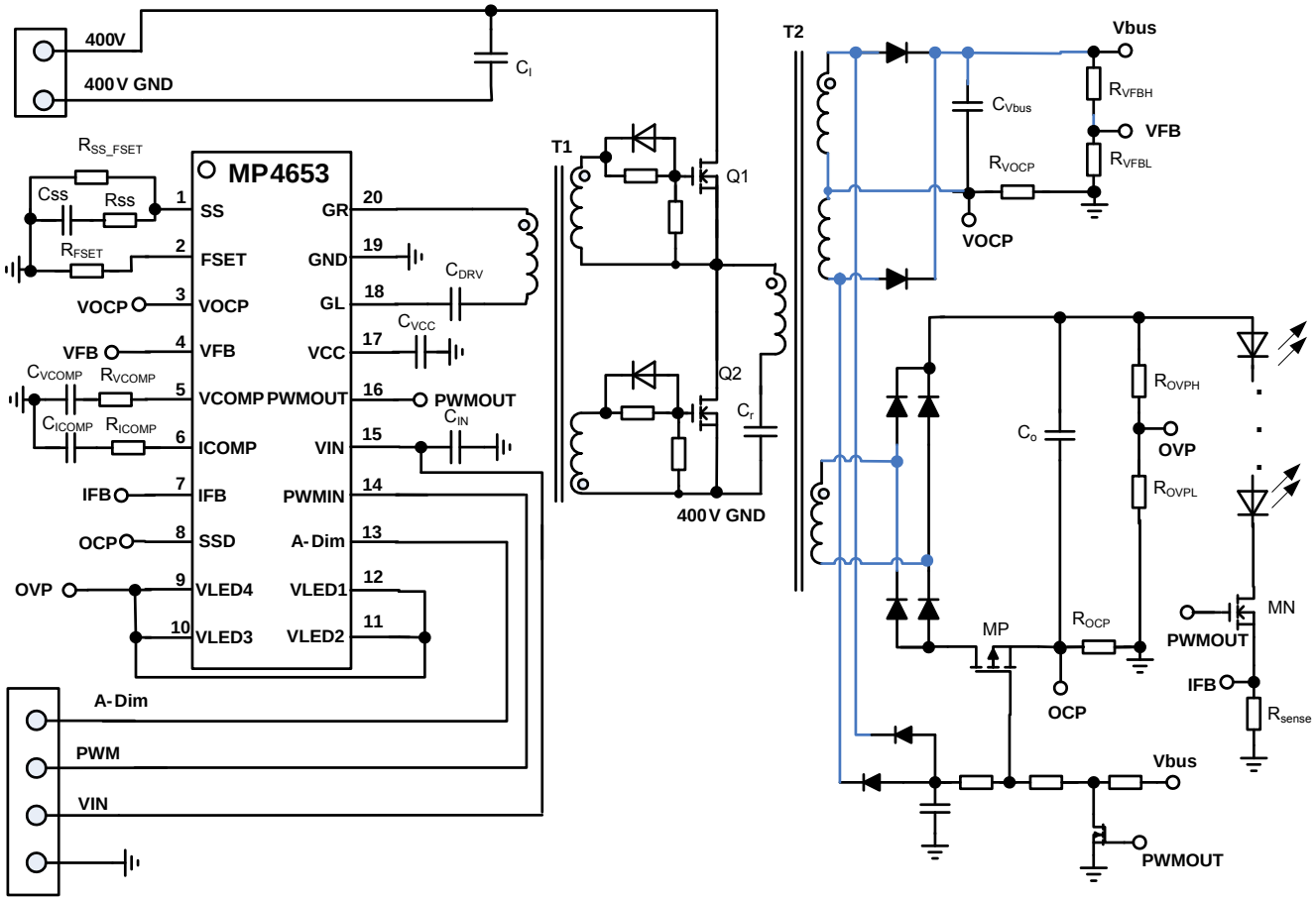
APPLICATIONS

- LCD TVs and Monitors
- Desktop LCD Flat Panel Displays
- Flat Panel Video Displays
- Street Lighting

All MPS parts are lead-free and adhere to the RoHS directive. For MPS green status, please visit MPS website under Products, Quality Assurance “MPS” and “The Future of Analog IC Technology” are Registered Trademarks of Monolithic Power Systems, Inc.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2012 MPS. All Rights Reserved.

TYPICAL APPLICATION



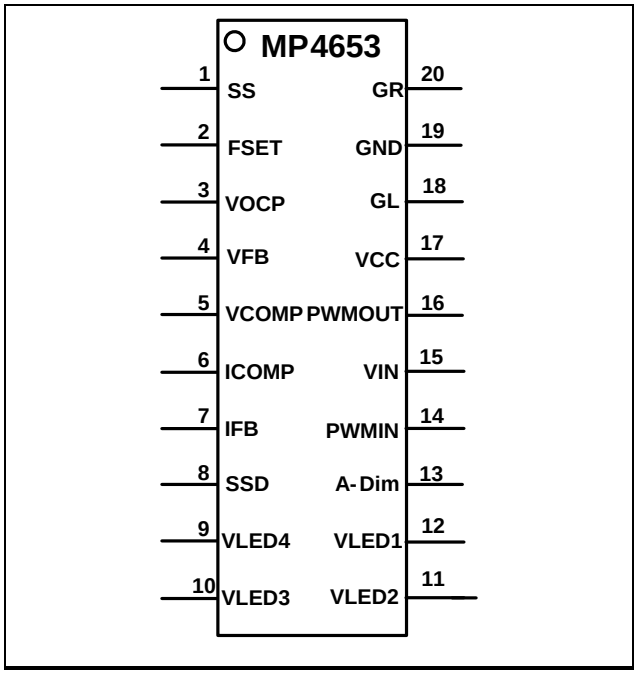
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2012 MPS. All Rights Reserved.

ORDERING INFORMATION

Part Number*	Package	Top Marking
MP4653GY	SOIC20	MP4653

* For Tape & Reel, add suffix –Z (eg. MP4653GY–Z);

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage V_{in} ..... -0.3V to +38V
GL,GR,VCC, PWMOUT ..... -0.5V to 10.7V
SSD, VOCP ..... -6.5V to + 4V
Other pins ..... -0.5V to +7V
Junction Temperature ..... 150°C
Continuous Power Dissipation (T_A = +25°C) (2) ..... 1.7 W
Storage Temperature ..... -65°C to +150°C
Operating frequency 300kHz

Recommended Operating Conditions (3)

Supply Voltage V_{in} ..... -0.3V to +30V
operating frequency ..... 20kHz to 250kHz
Operating Junction Temp ..... -40°C to +125°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}
SOIC20	72	30 °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2012 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_A = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Gate driver GL, GR						
Gate Pull-Down	R_{GD}	Igate = 20mA		2		Ω
Gate Pull-Up	R_{GU}	Igate = 20mA		7.5		Ω
Output Source Current	I_{SOURCE}	With 1nF load		1 [5]		A
Output Sink Current	I_{SINK}	With 1nF load		2 [5]		A
Dead time	t_{dead}		600	750	900	ns
Gate Driver Supply Voltage (VCC)						
Voltage	V_{VCC}	I_{VCC}=0mA	9	9.4	9.8	V
		I_{VCC}=30mA	8.8	9.3		V
Current	I_{VCC}			20	50	mA
Vin UVLO threshold	$V_{TH_UVLO_VIN}$	VCC rising	4.2	4.35	4.5	V
VCC UVLO Hysteresis	$V_{TH_VIN_HYST}$			240		mV
Brightness Dimming Control Range						
Analog Dimming Full Scale	$V_{A\text{-}dim}$	Analog dimming	1.13	1.18	1.23	V
PWM Logic Input Threshold	$V_{TH\text{-}PWM}$	PWM dimming	1.6	1.9	2.2	V
PWM Logic Input Hysteresis	$V_{TH\text{-}PWM\text{-}Hyst}$	PWM dimming		0.5		V
Supply Current						
Supply Current	I_{IN}	No driver output		1.6	2.5	mA
Operating Frequency						
Minimum Frequency Set Voltage	V_{FSET}		0.95	1	1.05	V
SS pin voltage	Vss	At normal operation	1.45	1.49	1.53	V
Minimum operating frequency	F_{min_op}	RFSET=R_{SS_FSET}=40kΩ, IFB=0.1V(ICOMP=2.2V), PWMIN=high	35.6	38.6	41.6	kHz
Maximum Operating Frequency	F_{max_op}	RFSET=R_{SS_FSET}=40kΩ,, IFB=0.21V(ICOMP=1V), PWMIN=high	2.2	2.5	2.8	Fmin
Output PWM Dimming Signal for LED (PWMOUT)						
Logic High Voltage	$V_{H\text{-}PWMOUT}$	Normal Operation	9V	9.4	9.8	V
Logic Low Voltage	$V_{L\text{-}PWMOUT}$	At Fault Condition, or PWMIN=0			0.3	V
Output PWM Source Current	I_{SOURCE_PWMOUT}	100pF on PWMOUT pin		5		mA
Output PWM Sink Current	I_{SINK_PWMOUT}	100pF on PWMOUT pin		100		mA
LED Current Feedback (IFB)						
Magnitude	$\|V_{IFB}\|$		0.192	0.2	0.208	V
LED Short Threshold for Immediate action	V_{IFBS}		540	600	660	mV
LED short detection blanking time	T_{blank}		100	140	180	ns

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2012 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_A = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
LED short threshold for slow action	V_{IFBSC}		270	300	330	mV
Delay time for slow action	T_{delay_IFB}	300mV<V_{IFB}<600mV	100	200	350	µs
Internal Current Loop Compensation Transconductance Opamp (ICOMP)						
Gain Bandwidth product	GB_I	75pF on ICOMP		1.0[6]		MHz
Open Loop DC Gain	A_{V_I}	ICOMP open	60[6]			dB
Input Common-mode range	V_{CM_I}		-0.3[6]		4[6]	V
Transconductance	Gm_I			830		µA/V
Saturated output current	I_{sat_I}		35	50	65	µA
Low level clamp voltage	VICOMP_L	Normal operation	0.95	1	1.05	V
High level clamp votlage	VICOMP_H	Normal operation	2.15	2.2	2.25	V
DC Bus Voltage Feedback (VFB)						
Sampling Delay Time	T_{dealy_sample}	PWM falling edge			100[6]	ns
Minimum clamp voltage	$V_{min_clamp_VFB}$		1.1	1.2	1.3	V
Maximum clamp voltage	$V_{max_clamp_VFB}$		1.9	2	2.1	V
Internal Voltage Loop Compensation Transconductance Opamp (VCOMP)						
Gain Bandwidth product	GB_V	75pF on VCOMP		1.0[6]		MHz
Open Loop DC Gain	A_{V_V}	VCOMP open	60[6]			dB
Low level clamp voltage	VVCOMP_L	Normal operation	0.95	1	1.05	V
High level clamp votlage	VVCOMP_H	Normal operation	2.15	2.2	2.25	V
Transconductance	Gm_V			160		µA/V
Saturated output current	I_{sat_V}		35	50	65	µA
Over LED Voltage Protection (VLED1~VLED4)						
Over LED Voltage Protection Threshold	$V_{TH(OVP_LED)}$		2.25	2.40	2.55	V
Over LED voltage delay time	T_{delay_VLED}		1.7	2.3	2.9	µs
Gain of differential voltage			14.7	16.3	17.9	
Internal resistance	R_{VLED}		19	23	27	kΩ
Hiccup mode fault delay timer(ICOMP, VCOMP)						
ICOMP Valley Threshold	$V_{th_low(ICOMP)}$		0.35	0.45	0.55	V
ICOMP Peak Threshold	$V_{th_peak(ICOMP)}$		2.7	3	3.3	V
ICOMP charging current at hiccup mode	$I_{charge_fault(ICOMP)}$		1.6	2	2.4	µA
ICOMP discharging current at hiccup mode	$I_{discharge_fault(ICOMP)}$		1.6	2	2.4	µA
VCOMP Valley Threshold	$V_{th_low(VCOMP)}$		0.35	0.45	0.55	V

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2012 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_A = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
VCOMP Peak Threshold	$V_{th_peak(VCOMP)}$		2.7	3	3.3	V
VCOMP charging current at hiccup mode	$I_{charge_fault(VCOMP)}$		1.6	2	2.4	μA
VCOMP discharging current at hiccup mode	$I_{discharge_fault(VCOMP)}$		1.6	2	2.4	μA
Burst mode (Pulse Skipping) threshold (VCOMP, ICOMP,VFB, IFB)						
VCOMP threshold for burst mode	$V_{TH_burst_VCOMP}$	VFB>1.1V_{SH}	1.05	1.1	1.15	V
VCOMP hysteresis for burst mode			70	90	110	mV
VFB threshold for burst mode	$V_{TH_burst_VFB}$		1	1.1	1.2	V_{SH}
VFB reset threshold for burst mode	$V_{TH_reset_burst_VFB}$			1		V_{SH}
ICOMP threshold for burst mode	$V_{TH_burst_ICOMP}$	V_{IFB}>1.1V_{IFB_REF}	1.05	1.1	1.15	V
ICOMP hysteresis for burst mode			70	90	110	mV
IFB threshold for burst mode	$V_{TH_burst_IFB}$		1	1.1	1.2	V_{IFB_REF}
IFB reset threshold for burst mode	$V_{TH_reset_burst_IFB}$			1		V_{IFB_REF}
Over Bus Voltage Protection (VFB)						
Over bus Voltage Protection Threshold	$V_{TH(OVP_VFB)}$		2.25	2.40	2.55	V
Delay Time		VFB>2.4V	1.7	2.3	2.9	μs
Short LED stage Detection (SSD)						
SSD Threshold	V_{TH_SSD}		-225	-200	-175	mV
SSD Detection Delay Time	T_{D_SSD}	SSD<-200mV	1.8	2.4	3	μs
Short Bus Stage Detection (OCP)						
OCP detection threshold	V_{TH_OCP}		-120	-100	-80	mV
OCP delay time	T_{D_OCP}	OCP<-100mV	1.8	2.4	3	μs

*: For design reference, not test parameter.

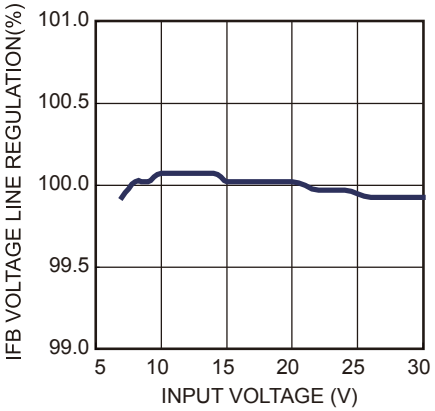
[5]: for bench evaluation only

[6]: for design only, not to be test

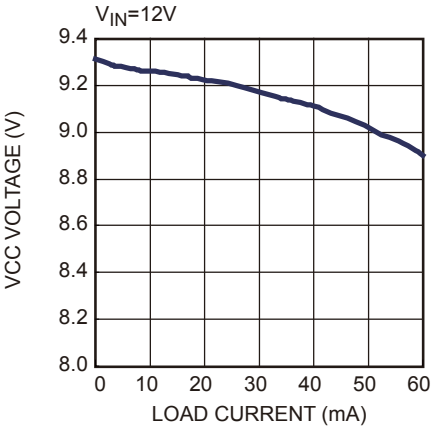
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2012 MPS. All Rights Reserved.

TYPICAL CHARACTERISTICS

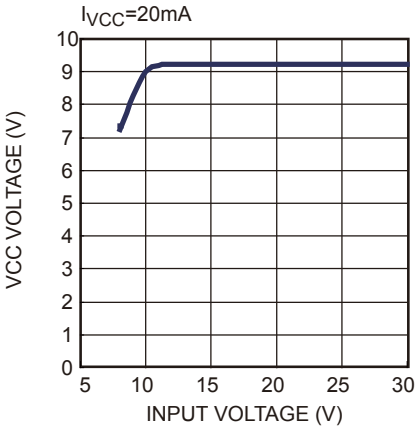
IFB Voltage Line Regulation



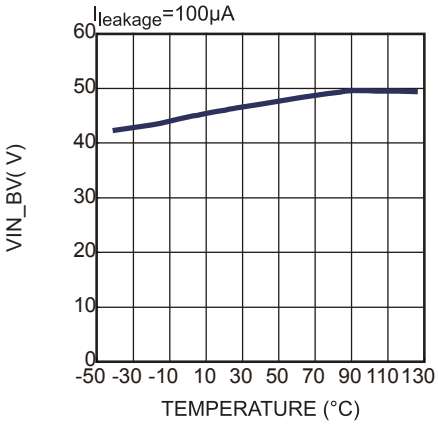
VCC Load Regulation



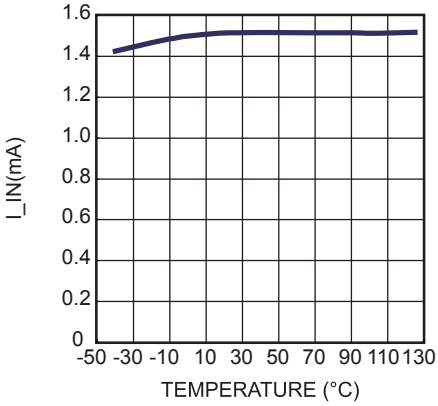
VCC Line Regulation



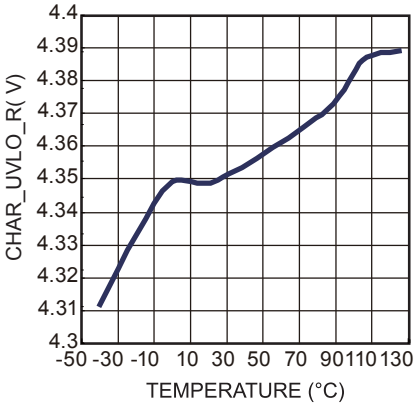
Break Down Voltage vs. Temperature



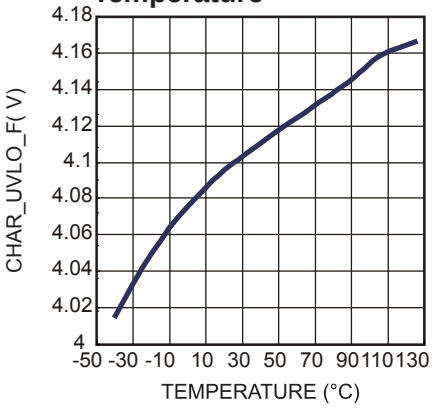
Supply Current vs. Temperature



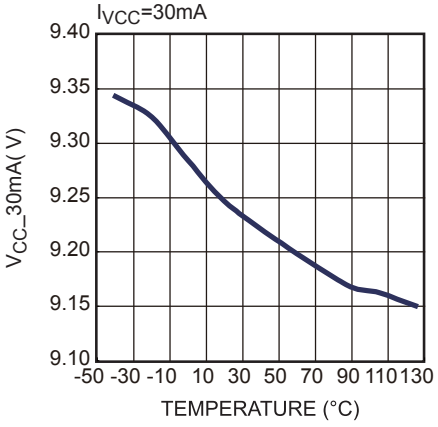
V_{UVLO_rising} vs. Temperature



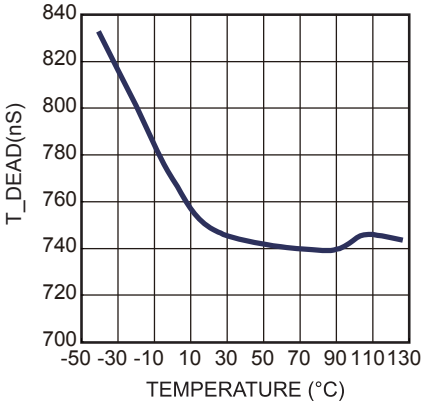
$V_{UVLO_falling}$ vs. Temperature



V_{CC} vs. Temperature



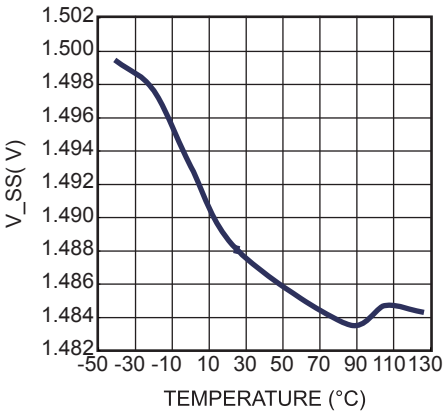
Dead Time vs. Temperature



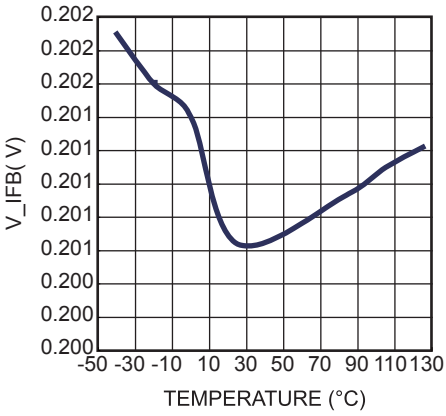
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2012 MPS. All Rights Reserved.

TYPICAL CHARACTERISTICS *(continued)*

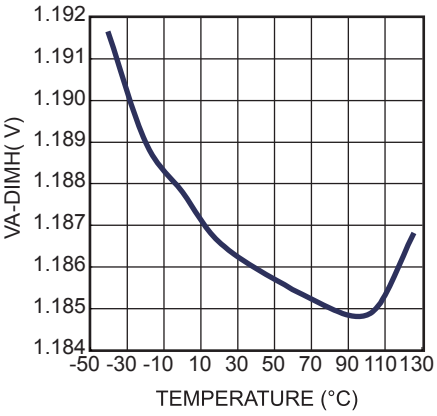
VSS vs. Temperature



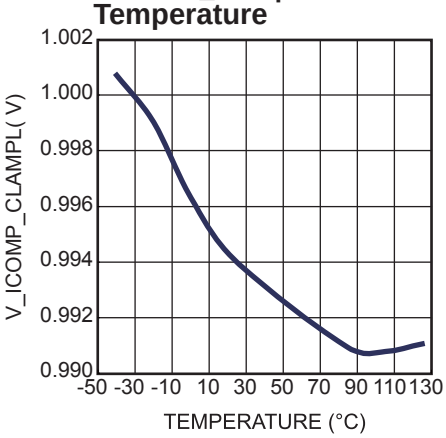
V_{IFB} vs. Temperature



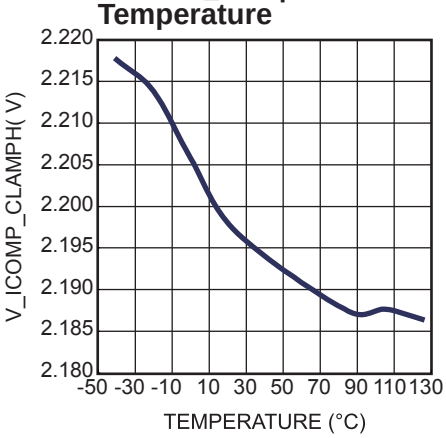
$V_{A\text{-}dim}$ vs. Temperature



V_{ICOMP_clampL} vs. Temperature

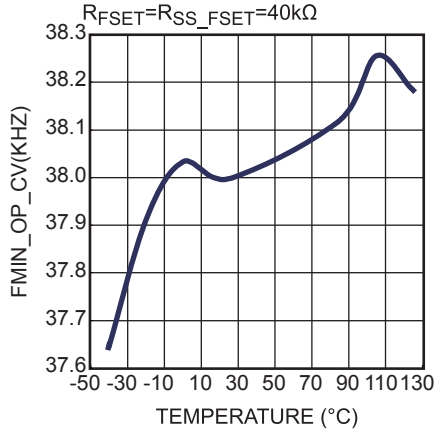


V_{ICOMP_clampH} vs. Temperature

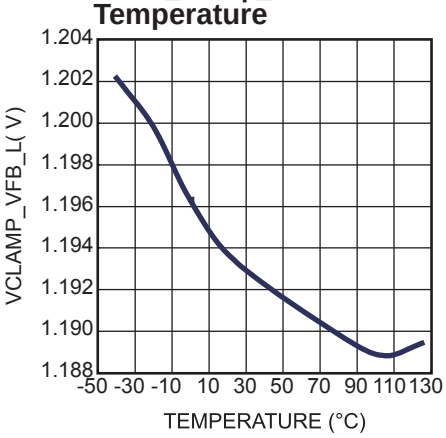


Fmin vs. Temperature

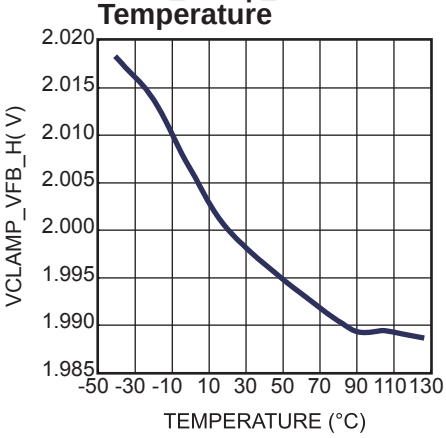
$R_{FSET}=R_{SS_FSET}=40k\Omega$



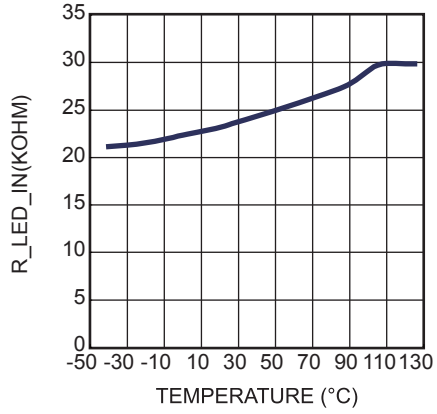
$V_{VFB_clamp_L}$ vs. Temperature



$V_{VFB_clamp_H}$ vs. Temperature



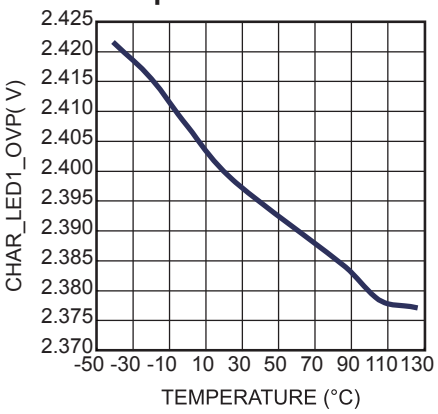
R_{VLED} vs. Temperature



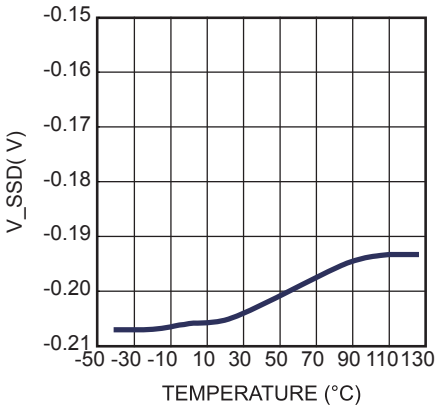
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2012 MPS. All Rights Reserved.

TYPICAL CHARACTERISTICS *(continued)*

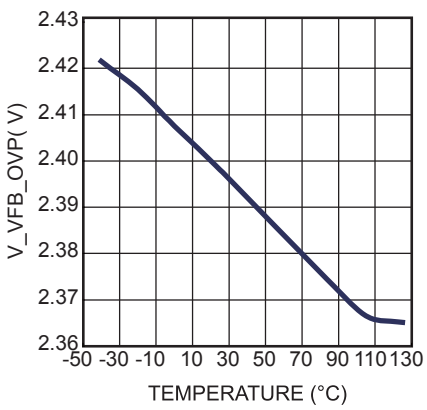
V_{VLED_OVP} vs. Temperature



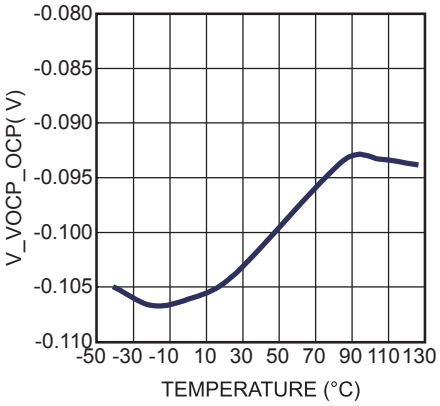
V_{SSD} vs. Temperature



V_{VFB_OVP} vs. Temperature



V_{VOCP_OCP} vs. Temperature

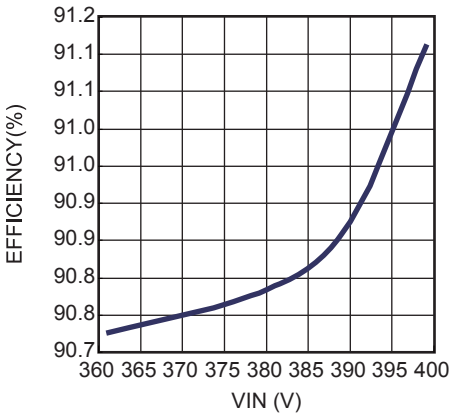


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2012 MPS. All Rights Reserved.

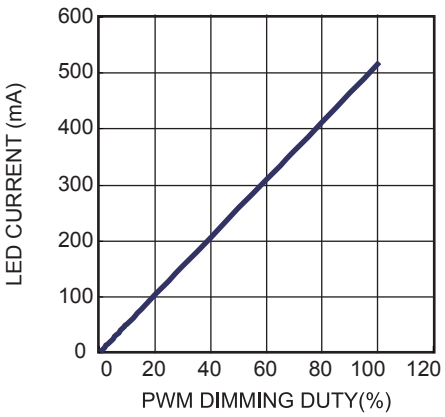
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board of the Design Example section. V_{IN} = 12V, 400V_bus=380V, V_{LED} = 120V, ILED=130mA*4 strings, DC/DC output=12V/1.5A, T_A = 25°C, unless otherwise noted.

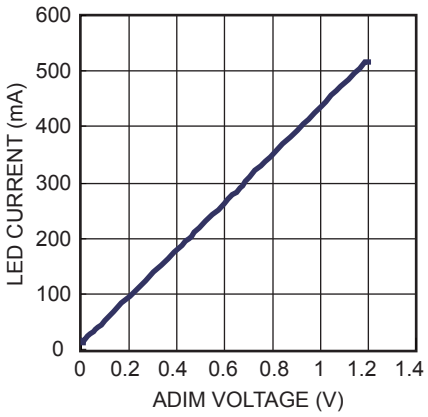
Efficiency vs. V400V_bus



PWM Dimming Curve



Analog dimming curve

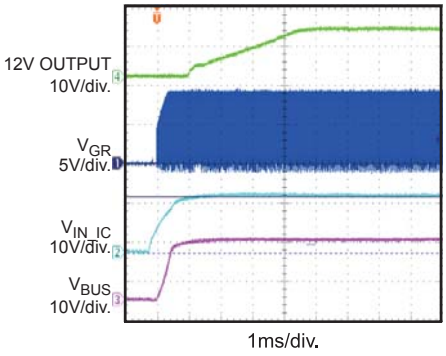


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2012 MPS. All Rights Reserved.

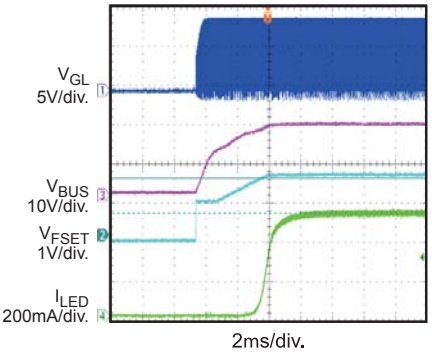
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board of the Design Example section. V_{IN} = 12V, 400V_bus=380V, V_{LED} = 120V, ILED=130mA*4 strings, DC/DC output=12V/1.5A, T_A = 25°C, unless otherwise noted.

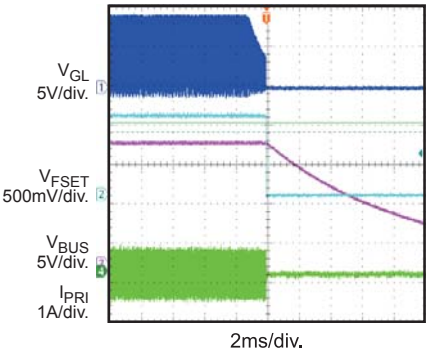
Start Up with CV Mode



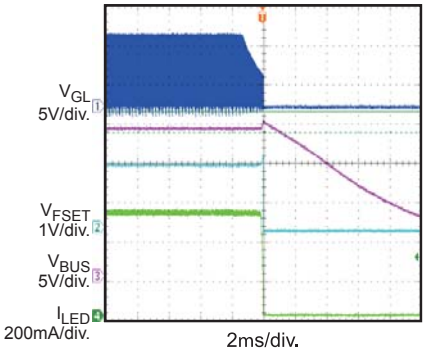
Start Up with CC Mode



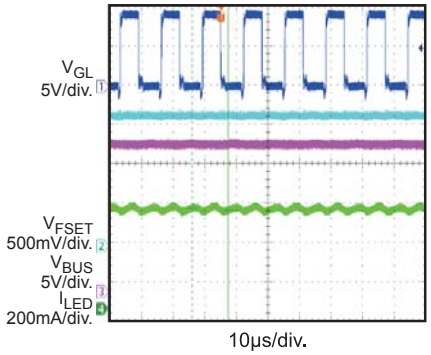
Shut Down at CV Mode



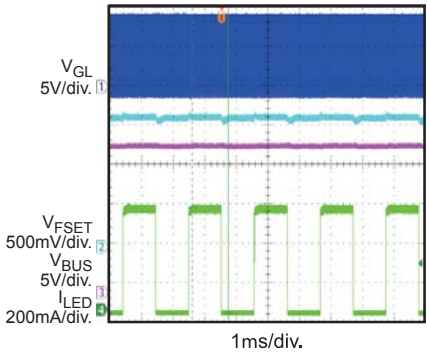
Shut Down at CC Mode



Steady State

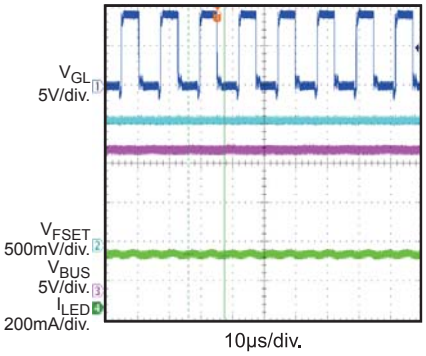


PWM Dimming, 50%, 480Hz

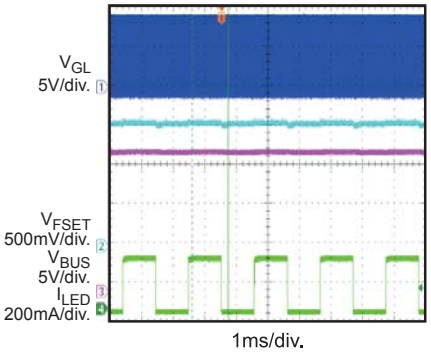


Analog Dimming

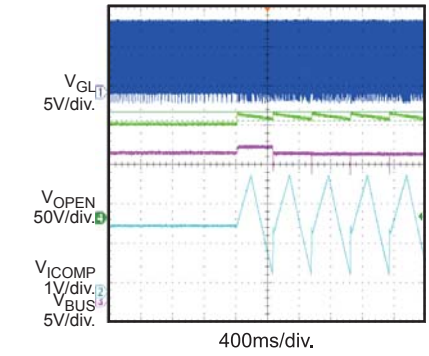
ADIM=0.655V



PWM Dimming+ Analog Dimming



Open LED Protection

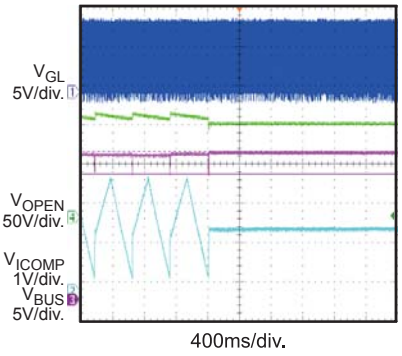


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2012 MPS. All Rights Reserved.

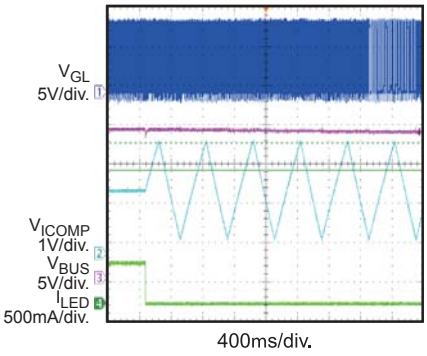
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board of the Design Example section. V_{IN} = 12V, 400V_bus=380V, V_{LED} = 120V, ILED=130mA*4 strings, DC/DC output=12V/1.5A, T_A = 25°C, unless otherwise noted.

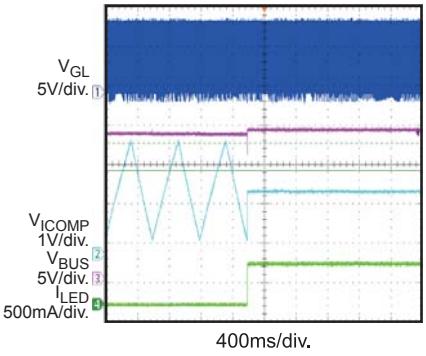
Open LED Protection Recovery



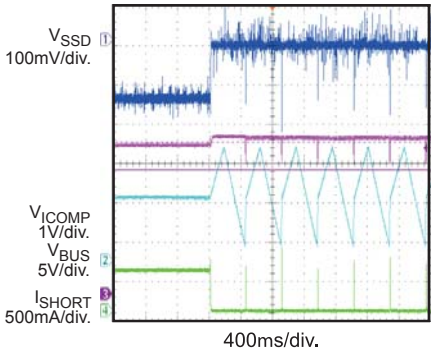
Short LED+ to LED- Protection



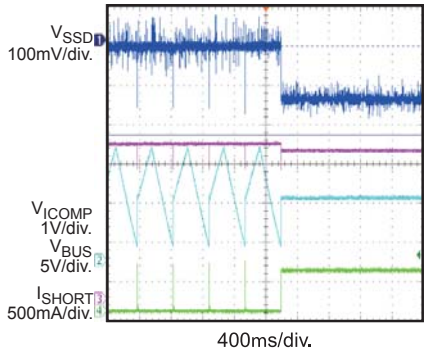
Short LED+ to LED- Recover



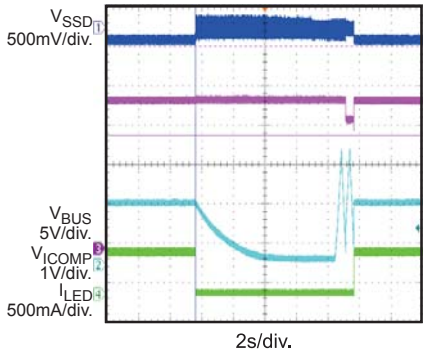
Short LED- to GND Protection



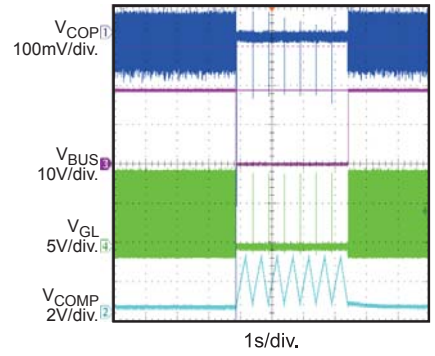
Short LED- to GND Recover



Short LED+ to GND Protection and Recovery



Short DC bus to GND Protection and Recover



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2012 MPS. All Rights Reserved.

PIN FUNCTIONS

Pin #	Name	Description
1	SS	Soft Start. This pin functions soft start and also sets the operating frequency together with FSET pin. Connect a resistor (R_{SS_FSET}) in parallel with a resistor (Rss) and a capacitor (Css) in series to this pin. The sourcing current of this pin together with the sourcing current of FSET pin determines the operating frequency. The resistor R_{SS_FSET} together with the resistor on FSET pin sets the operating frequency; the resistor Rss and the capacitor Css functions the soft start. The normal voltage on this pin is 1.49V and is pulled low to 0V at bus voltage stage fault condition. The Rss and Css network sets the start up operating frequency and the soft start time.
2	FSET	Frequency Set. Connect a resistor from this pin to GND. The operating frequency is determined by the sourcing current through this pin and SS pin. The voltage of FSET pin is programmed by the current control loop and the voltage control loop, and so does the operating frequency.
3	VOCP	Over current protection of bus stage. This pin senses the secondary current of the bus stage, when the VOCP voltage is lower than -100mV, IC triggers bus stage protection.
4	VFB	Bus voltage feedback. This pin feeds back the bus voltage for regulation. MP4653 automatically samples the VFB voltage at PWM ON interval and uses it as the reference voltage of the bus voltage control loop at PWM OFF interval. The voltage on VFB pin is also used for over voltage protection of bus voltage stage. When the voltage on VFB pin exceeds 2.4V, the over voltage protection of bus voltage stage is triggered.
5	VCOMP	Feedback Compensation Node of voltage control loop. Connect a compensation capacitor or a R-C network from this pin to GND. VCOMP pin is also used as the hiccup timer for the fault protection of the Bus voltage stage. When fault condition occurs in the bus voltage stage, the VCOMP is disconnected from the internal voltage loop and the hiccup timer for the voltage bus voltage stage starts. An internal current source charges VCOMP until 3V and then discharges it to 0.45V.
6	ICOMP	Feedback Compensation Node of current control loop. Connect a compensation capacitor or a R-C network from this pin to GND. ICOMP pin is also used as the hiccup timer for the LED stage protection. When fault condition of the LED stage occurs, the ICOMP pin is disconnected from the internal amplifier and LED stage hiccup timer starts. An internal current source charges ICOMP until 3V and then discharges it to 0.45V.
7	IFB	LED Current Feedback Input. This pin feeds back the LED current through a sensing resistor. The internal error amplifier sinks a current from the ICOMP pin proportional to the absolute value of the voltage at this pin. The average voltage at this pin is regulated to the reference voltage (controlled by the A-dim voltage, 0.2V when A-dim is high). The voltage on this pin is also used for over LED current detection. When the voltage on this pin gets higher than 0.3V for 200μs or when the voltage gets higher than 0.6V, the IC triggers the LED stage protection.
8	SSD	Short string protection. This pin feeds back the secondary side current of the LED driver stage. When the voltage on this pin is less than -200mV, IC triggers the LED driver stage protection.
9	VLED4	Voltage feedback of LED string4.
10	VLED3	Voltage feedback of LED string3.
11	VLED2	Voltage feedback of LED string2.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2012 MPS. All Rights Reserved.

PIN FUNCTIONS *(continued)*

Pin #	Name	Description
12	VLED1	Voltage feedback of LED string1. VLED1, VLED2, VLED3 and VLED4 corporate for the protection of the LED driver stage. The maximum voltage of these pins and the voltage difference among these pins are detected for LED stage protection. If the number of LED strings is less than 4, connect the left pins together with others.
13	A-Dim	Analog dimming input. 0~1.18V sets the LED current from 0 to 100%. If not used pull it high to VCC through a 100kΩ resistor.
14	PWMIN	PWM Dimming control Input. Apply a 100Hz to 2kHz PWM signal to this pin for PWM dimming
15	VIN	Supply Input. Bypass this pin with a ceramic capacitor larger than 0.1μF.
16	PWMOUT	Output of the driving signal for the dimming MOSFET.
17	VCC	Power Supply for the gate driver and internal circuit. Bypass this pin with a ceramic capacitor larger than 1μF.
18	GL	Driving signal output, 180 degree phase shifted of GR
19	GND	Ground Reference.
20	GR	Driving signal output, 180 degree phase shifted of GL

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2012 MPS. All Rights Reserved.

FUNCTION BLOCK DIAGRAM

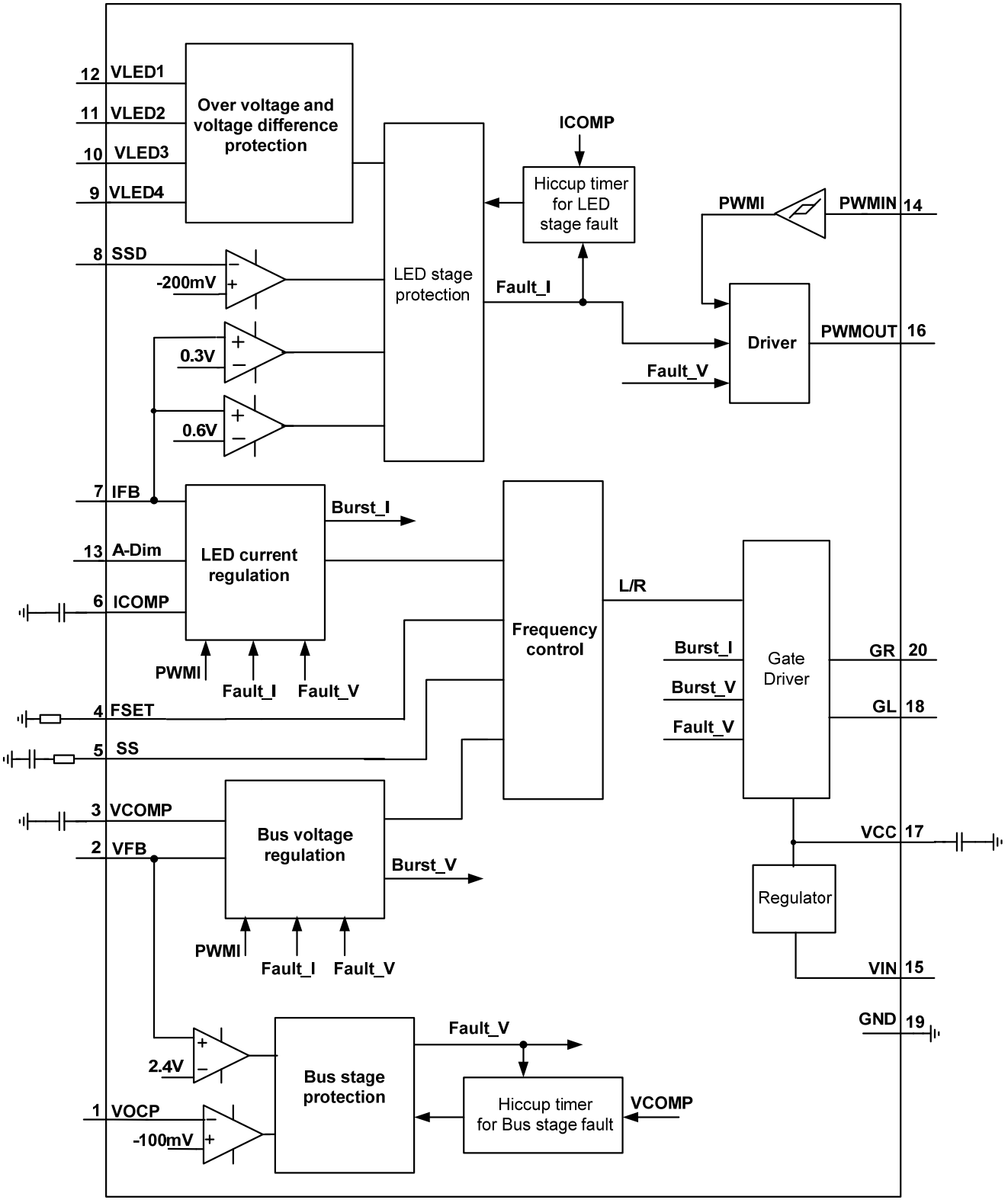


Figure 1—MP4653 Function Block Diagram

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2012 MPS. All Rights Reserved.

OPERATION

The MP4653 is a CC/CV mode LLC TV LED driver, especially designed for the real LIPS structure for the large size TV LED backlighting. Powered by 9V to 30V input supplies, the MP4653 outputs two 180 degree phase shifted driving signals for the external power stages. Its enhanced 9V gate driver provides adequate driving capability and can directly drive the external MOSFETs through an external gate driving transformer.

The MP4653 employs frequency control for the LLC power stage. Both the LED current and the bus voltage are controlled. Figure 1 shows the block diagram of MP4653.

Internal Regulator

The MP4653 includes an internal linear regulator VCC. It is the supply voltage for the gate driver and also for the internal circuit. The MP4653 features Under Voltage Lockout. The chip is disabled until VCC exceeds the UVLO threshold.

System Startup

When the MP4653 is powered up, the VCC is charged up, and when it passes the UVLO threshold, IC starts up. It resets the voltage control loop, the current control loop and discharges the soft start capacitor. The MP4653 enjoys a soft start up.

The MP4653 gets a 4.35V input UVLO threshold, and it can start up directly from the system 5V standby power supply. Please refer to figure 2.

The PWM dimming signal controls the start up of the LED driver stage. The system operates in constant voltage mode and the DC bus voltage is controlled before PWM signal applied.

CC/CV Mode Operation

The MP4653 integrates a constant voltage control loop (CV) and a constant current control loop (CC). Both the LED current of the LED stage and the bus voltage of the bus voltage stage are controlled. The PWM dimming signal is used to distinguish these two modes. At PWM on interval, the current control loop is effective (CC mode) and the LED current is regulated. At PWM off interval, the voltage control loop is effective and the DC bus voltage is controlled (CV mode).

For the current control loop for the LED current regulation, the LED current is fed back to IFB pin. The internal error amplifier regulates the average value of IFB signal to the internal 200mV reference voltage. Its output is connected to the external current-loop compensation network on ICOMP pin through an inner switch S1. At PWM on interval, S1 is on, and the output of the error amplifier is connected to the external compensation network on ICOMP pin. The LED current is regulated by this control loop. At PWM off interval, S1 is turned off, and the compensation network on ICOMP is disconnected from the error amplifier and holds its value until next PWM on interval. The output of the error amplifier is pulled low at PWM off interval.

MP4653 integrates burst mode for the LED current regulation. When IFB voltage is higher than 1.1 times of its reference voltage and the ICOMP voltage is sufficiently low (which means a highest operating frequency), the IC skips some switching cycles until IFB voltage decreases sufficiently.

For the voltage control loop for the bus voltage regulation, the bus voltage is fed back on VFB pin. MP4653 automatically samples the VFB voltage at PWM on interval and uses it as the reference for the voltage control loop. The internal voltage-loop error amplifier regulates the average value of the VFB voltage to this reference voltage at PWM off interval. Its output is connected to the external voltage-loop compensation network on VCOMP pin through an inner switch S2. At PWM off interval, S2 is on, and the output of the voltage-loop error amplifier is connected to the external compensation network on VCOMP pin. The bus voltage is regulated by this control loop. At PWM on interval, S2 is turned off, and the compensation network on VCOMP is disconnected from the error amplifier and holds its value until next PWM off interval. The output

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2012 MPS. All Rights Reserved.

of the voltage-loop error amplifier is pulled low at PWM on interval.

MP4653 also integrates burst mode for the voltage regulation. When VFB voltage is higher than 1.1 times of the reference voltage and the VCOMP voltage is sufficiently low (which means a highest operating frequency), the IC skips some switching cycles until VFB voltage decreases sufficiently.

The operating frequency is controlled by the larger one of the outputs of the current-loop error amplifier and the voltage-loop error amplifier. A high compensation output voltage gets a low operating frequency.

Dimming Control

The MP4653 provides two dimming methods: PWM Dimming Mode and Analog Dimming Mode. Applying a digital PWM signal on the PWMIN pin allows the PWM dimming. The brightness of the LED string is proportional to the duty cycle of the external PWM signal. A driving signal on PWMOUT pin is output to directly drive the dimming MOSFET, which helps to achieve fast and high contrast ratio PWM dimming.

MP4653 achieves 500:1 PWM dimming ratio (0.2% minimum PWM dimming duty) at 200Hz PWM dimming frequency. The PWM dimming ratio may decrease with a higher PWM dimming frequency.

A DC analog signal from 0V to 1.18V on A-Dim pin dims the LED current amplitude from 0 to 100%.

For PWM and analog dimming control, apply the PWM dimming signal on PWMIN pin and apply the analog dimming signal on A-dim pin.

Bus Voltage Stage Protection

The MP4653 features rich and smart protection to increase system reliability. It protects the fault condition at both the DC bus voltage stage and the LED driver stage.

The protection for the DC bus voltage stage includes the over voltage protection and over current protection (short protection).

The VFB pin senses the bus stage voltage for voltage regulation and also for over voltage protection. When the VFB pin voltage gets higher than 2.4V for 2us, IC triggers the Bus Voltage Stage Protection.

The secondary side current of bus voltage stage is sensed on VOCP pin. When VOCP voltage gets lower than -100mV, IC triggers the Bus Voltage Stage Protection.

At Bus Voltage Stage Protection, the whole gate driving signals are disabled and no power is delivered to the output, including both the DC bus voltage stage and the LED driver stage. The current loop compensation node ICOMP pin and the soft start SS pin are pulled low. The hiccup timer for the bus voltage stage starts. The voltage-loop compensation node VCOMP pin is disconnected from the internal amplifier and holds its value until the fault condition disappears. A 2μA current source charges the VCOMP pin capacitor till VCOMP voltage hits 3V, and then a 2μA current source discharges VCOMP pin until 0.45V and then the system recovers.

LED Driver Stage Protection

The fault protection for the LED driver stage includes the open LED protection, short LED protection, over LED current protection and any point of LED string short to ground protection.

The voltage of the LED strings are sensed on VLED1~VLED4 pins. The maximum value of VLED1~VLED4 and their voltage difference are used for protection. When the maximum value of VLED1~VLED4 gets higher than 2.4V or their voltage difference get larger than 150mV (this value can be adjusted by the external input resistance on VLED# pins), IC triggers the LED Driver Stage Protection.

The LED current feedback IFB is also used for over LED current protection. When IFB voltage gets higher than 300mV for 200us or when IFB voltage gets higher than 600mV, IC triggers the LED Driver Stage Protection.

The secondary side current of the LED driver stage is sensed on SSD pin. When SSD pin voltage gets lower than -200mV for 2us, IC triggers the LED Driver Stage Protection.

At the LED Driver Stage Protection, the driving signal for the dimming MOSFET is disabled to

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2012 MPS. All Rights Reserved.

turn off the dimming MOSFET and also to disconnect the LED driver stage from the power stage. The current loop compensation node ICOMP is disconnected from the internal amplifier and holds its value until the fault condition on the LED driver stage disappears. A 2μA current source charges the ICOMP pin capacitor till ICOMP voltage hits 3V, and then a 2μA current source discharges ICOMP pin until 0.45V and then the LED driver stage recovers.

The gate driving signals for the MOSFETs in the power stage are continuous and the DC bus voltage is regulated at the fault condition of LED driver stage. Therefore, the system power supplies are not influenced by the fault protection of the LED driver stage.

Thermal protection is integrated in MP4653.

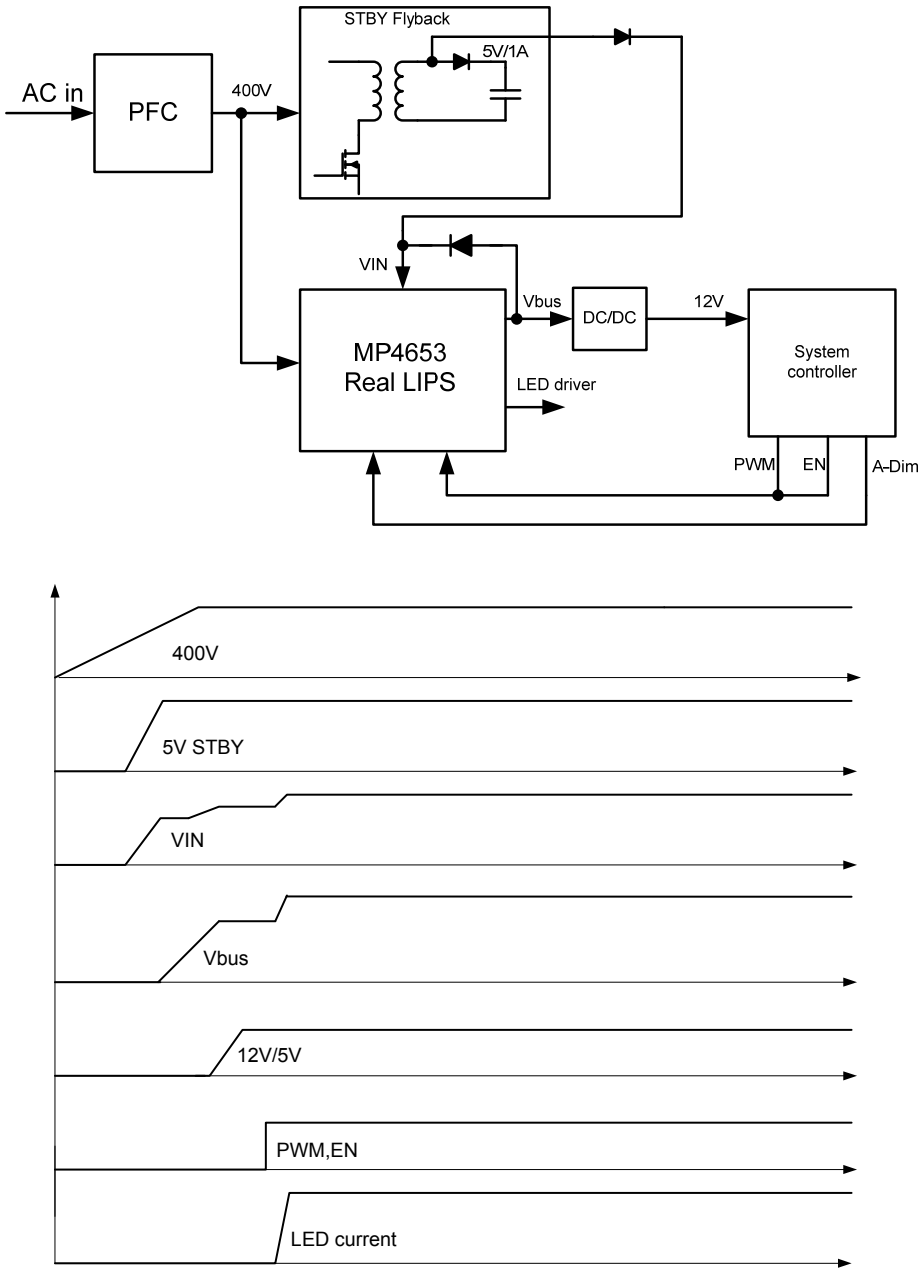


Figure 2—Real LIPS Power System and Start Up Sequence

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2012 MPS. All Rights Reserved.

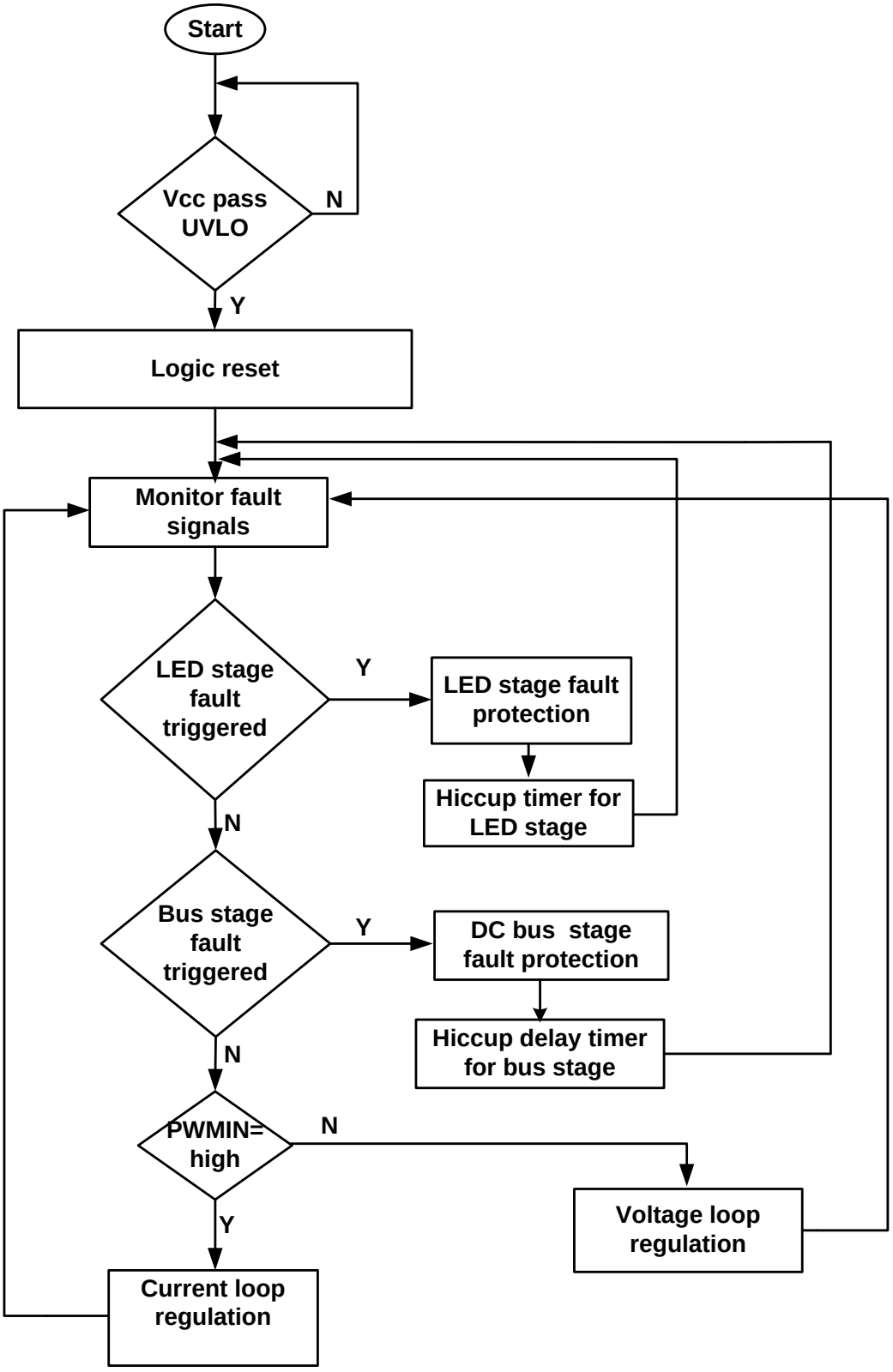


Figure 3—System Operation Flow Chart

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2012 MPS. All Rights Reserved.

APPLICATION INFORMATION

Setting the LED Current (Pin7, IFB)

The external LED current sensing resistor sets the maximum LED current (refer to TYPICAL APPLICATION CIRCUIT) and value can be determined using the equation:

$$Rsense = \frac{0.2V}{I_{LED}}$$

The ILED is the total current of the LED strings.

It is recommended a 1k resistor between the IFB pin and the current sensing resistor for short proteciton.

Setting the minimum/maximum operating frequency (Pin1 SS, Pin2 FSET)

The operating frequency of MP4653 is determined by the sourcing current through SS pin and FSET pin.

$$f_{op} = (\frac{2\times1.49V}{R_{SS_FSET}} - \frac{V_{FSET}}{R_{FSET}})\times1.98\times10^9$$

The V_{FSET} voltage is the larger value of the outputs of internal amplifiers for voltage loop and current loop. It is in range of 1~2.2V.

The minimum operating frequency is set by:

$$f_{min} = (\frac{2\times1.49V}{R_{SS_FSET}} - \frac{2.2V}{R_{FSET}})\times1.98\times10^9$$

The maximum operating frequency is set by:

$$f_{max} = (\frac{2\times1.49V}{R_{SS_FSET}} - \frac{1V}{R_{FSET}})\times1.98\times10^9$$

Setting the Soft Start up Frequency and Soft Start Time (Pin1 SS)

The soft start up frequency is:

$$f_{s_start} = (\frac{2\times1.49V\times(R_{SS_FSET}+R_{SS})}{R_{SS_FSET}*R_{SS}} - \frac{1V}{R_{FSET}})\times1.98\times10^9$$

Usually, the soft start up frequency could be 1.5 to 3 times of the maximum operating frequency.

The soft start time is determined by the RC Constant of Rss and C_{SS}. The soft start time could be estimated with 3 times of the RC Constant:

$$T_{SS} \approx 3\times R_{SS}\times C_{SS}$$

Setting the Voltage Loop Feedback (Pin4 VFB)

The voltage on VFB pin should between 1.2V and 2V at normal operation. Set the voltage feedback divider (R_{VFBH} and R_{VFBL}) and make sure the feedback voltage is in this range at normal operation.

$$1.2V < V_{VFB} = \frac{R_{VFBL}}{R_{VFBH}+R_{VFBL}}\times V_{bus} < 2V$$

The VFB pin also functions as the over voltage protection for the bus stage. When the voltage on VFB gets higher than 2.4V, IC triggers bus stage protection.

Setting Over-Voltage Protection of the LED Stage (Pin9,10,11,12)

The voltage divider sets the over-voltage protection point (refer to TYPICAL APPLICATION CIRCUIT) through the equation:

$$V_{OVP} = \frac{R_{OVPH}+R_{OVPL}}{R_{OVPL}}\times2.4V$$

Normally, the OVP point is setting about 10%-30% higher than the maximum LED voltage.

Setting the Voltage Difference Protection of the LED Strings (Pin9,10,11,12)

MP4653 implements the protection when LED string voltage is different from each other, in order to protect the condition that several LEDs in a string are shorted. It is used only for multiple-strings application. The protection point of the voltage difference between LED strings is set by:

$$\Delta V_{pro} = \frac{R_{OVPH}+R_{OVPL}}{R_{OVPL}}\times2.4V\times\frac{23k+R_{input}}{16\times23k}$$

Where R_{input} is the input resistance of the LED# pin. Adjust the input resistance to program the protection point.

Application can add a resistor R_X between the voltage divider and LED# pins to adjust the input resistance.

$$R_{input} = \frac{R_{OVPH}\times R_{OVPL}}{R_{OVPL}+R_{OVPH}} + R_X$$

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2012 MPS. All Rights Reserved.

Setting the Over Current Protection for the bus stage (Pin3 VOCP)

This pin implements the over current protection for the bus stage. The current of the bus stage is sensed to this pin with a negative polarity. When the voltage on this pin is lower than -100mV, the IC triggers the bus stage protection.

$$I_{OCP_Bus} = \frac{100mV}{R_{VOCP}}$$

Usually, the protection point is around 1.5 to 3 times of the normal current of the bus stage.

Setting the Over Current Protection for the LED stage (Pin8 SSD)

This pin detects the current through the LED stage with a negative polarity. When the voltage on this pin gets lower than -200mV, IC triggers LED stage protection.

$$I_{OCP_LED} = \frac{200mV}{R_{OCP}}$$

The over current protection point for the LED stage could usually set at around 1.5 to 2 times of the total current through the LED strings.

Setting the Voltage loop compensation (Pin5 VCOMP)

This pin is connected to the output of the inner error amplifier for the voltage control loop through an internal switch. Place a RC (R_{VCOMP}, C_{VCOMP}) network on this pin for compensating the voltage control loop.

Usually, a ceramic capacitor in range of 47nF to 470nF and a resistor in range of 2kΩ to 200kΩ is recommended for the compensation.

This pin is also used as the hiccup mode fault timer. When fault condition in the bus stage occurs, the inner switch which connects this pin to the output of error amplifier for voltage control loop turns off and a 2μA current source will charge this pin to 3V and then discharge it to 0.45V. IC auto recovers after the hiccup timer.

The hiccup delay time is:

$$T_{hiccup_V} = \frac{C_{VCOMP} \times (3V - V_{VCOMP})}{2\mu A} + \frac{C_{VCOMP} \times 2.5V}{2\mu A}$$

Setting the current loop compensation (Pin6 ICOMP)

This pin is connected to the output of the inner error amplifier for the current control loop through an internal switch. Place a RC (R_{ICOMP}, C_{ICOMP}) network on this pin for the current control loop compensation.

Usually, a ceramic capacitor in range of 47nF to 470nF and a resistor in range of 200Ω to 5kΩ is recommended for the compensation.

This pin is also used as the hiccup mode fault timer for the LED stage. When fault condition occurs in the LED stage, the inner switch which connects this pin to the output of the error amplifier for current control loop turns off and a current source will charge this pin to 3V and then discharge it to 0.45V. The control for the LED stage auto recovers after this hiccup timer.

The hiccup delay time is:

$$T_{hiccup_I} = \frac{C_{ICOMP} \times (3V - V_{ICOMP0})}{2\mu A} + \frac{C_{ICOMP} \times 2.5V}{2\mu A}$$

Analog Dimming (Pin 13, A-Dim)

This pin is for analog dimming. Applying a voltage in range of 0V to 1.18V dims the LED current from 0 to 100%. It has positive polarity for the analog dimming. A ceramic capacitor is recommended on this pin to bypass it.

PWM Dimming input (Pin 14, PWMIN)

This pin is for PWM dimming input. Applying a PWM dimming signal with frequency in range of 100Hz to 2kHz on this pin. It has positive polarity for the PWM dimming.

At PWM on interval, the LED current is regulated and at PWM off interval, the voltage control loop for the DC bus functions. The DC bus voltage is regulated at the value of that in PWM on interval.

Supply Input (Pin 15, VIN)

This pin is the supply input voltage for the IC. Bypass this pin with a 0.1uF or larger ceramic capacitor.

IC starts to work when the VIN voltage is applied. If PWMIN pin is high, the LED current control loop is effective and if the PWMIN pin is low, the voltage control loop for the DC bus control is effective. If an “Enable” signal is required to

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2012 MPS. All Rights Reserved.

control the starting operation of the IC, use this "Enable" signal to control this supply input voltage with following circuit in figure 4.

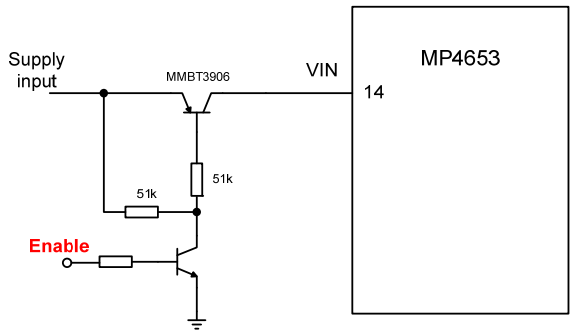


Figure 4—MP4653 Enable control circuit

PWM dimming signal output (Pin 16, PWMOUT)

This pin outputs a PWM dimming signal to drive the external dimming MOSFET (MN) in series with the LED string, and achieves fast PWM dimming. Connect a resistor in series with this pin to adjust the driving speed.

The PWMOUT signal is also used to control the external P-MOS (MP) for protection, as shown in figure 5A. Figure 5B shows the operating scheme of this driving circuit. A negative voltage source (-Vbus) is generated from the secondary winding of DC bus stage. A pulse waveform at "V_X" is generated through the PWMOUT signal. By summing the negative voltage source and V_X, a pulse waveform with a negative magnitude is generated on "P_Drive" (the P-MOS gate) and is used to drive the P-MOS.

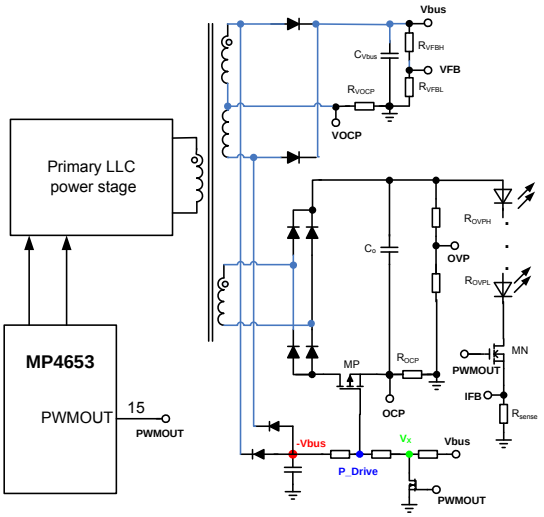


Figure 5A—PWMOUT for the P_MOS Driver

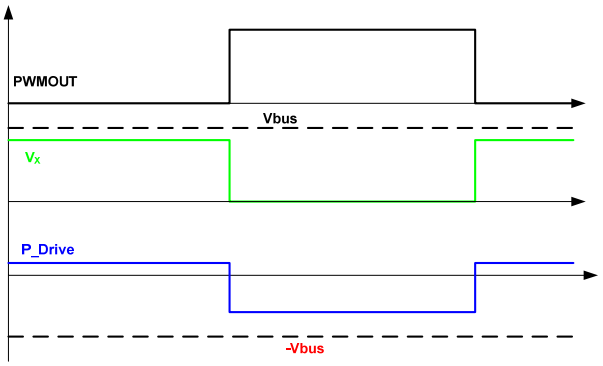


Figure 5B—Scheme of the PWMOUT Driving the P_MOS

Gate Driver Supply (Pin 17, VCC)

This pin supplies the gate drive signals GL,GR and PWMOUT. Bypass this pin with a 1uF or larger ceramic capacitor. This pin could also be used to supply an external circuit.

Gate Drive Signals (Pin 18,20 GL,GR)

GL and GR provide the driving signal for the power stage. GL and GR are 180 degree phase shifted gate drive signals. With the enhanced drive capability, GL and GR can directly drive the external MOSFET in the power stage through a gate driving transformer.

The gate driving transformer also isolates the primary power stage and the secondary control circuit. Place a 2.2nF Y cap between the power stage ground and the reference ground for the control circuit to improve the EMI performance.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2012 MPS. All Rights Reserved.

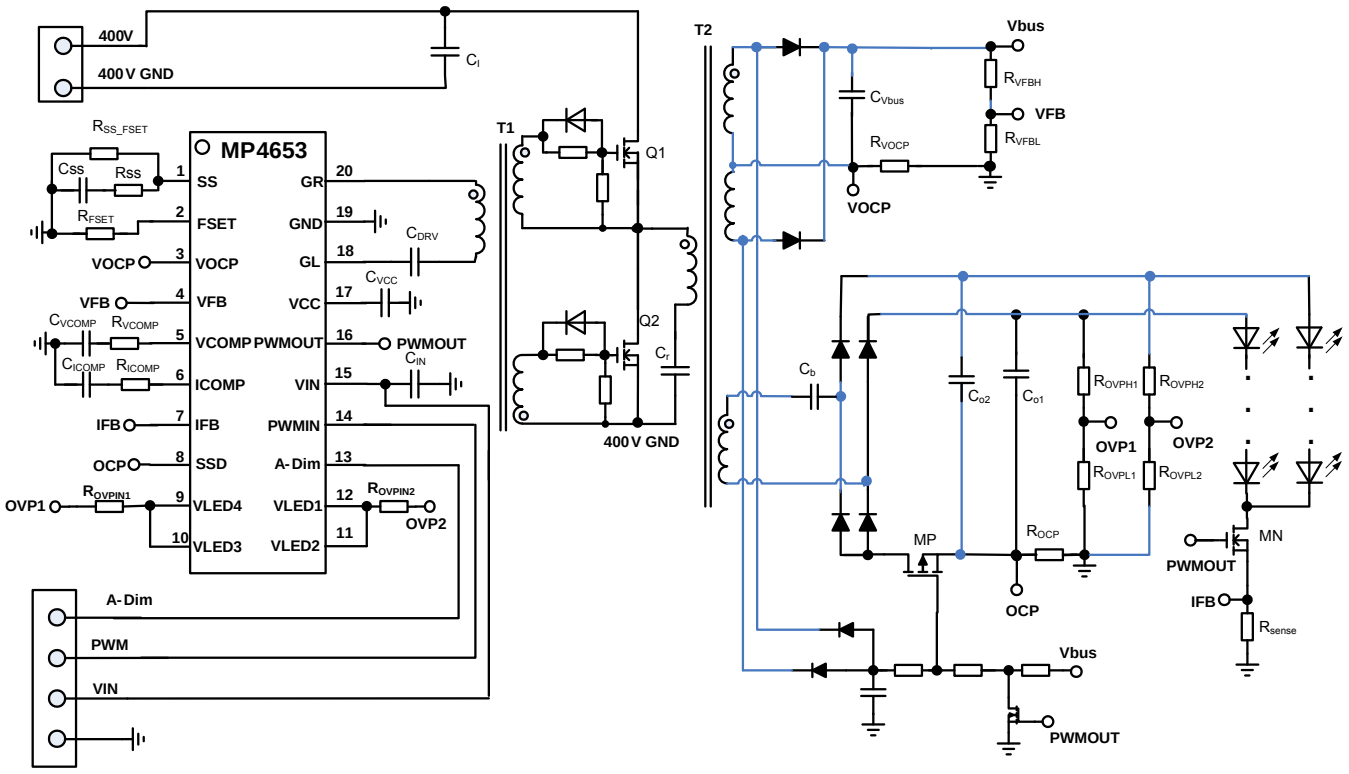


Figure 6—MP4653 Based LED Driver for 2 Strings

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2012 MPS. All Rights Reserved.

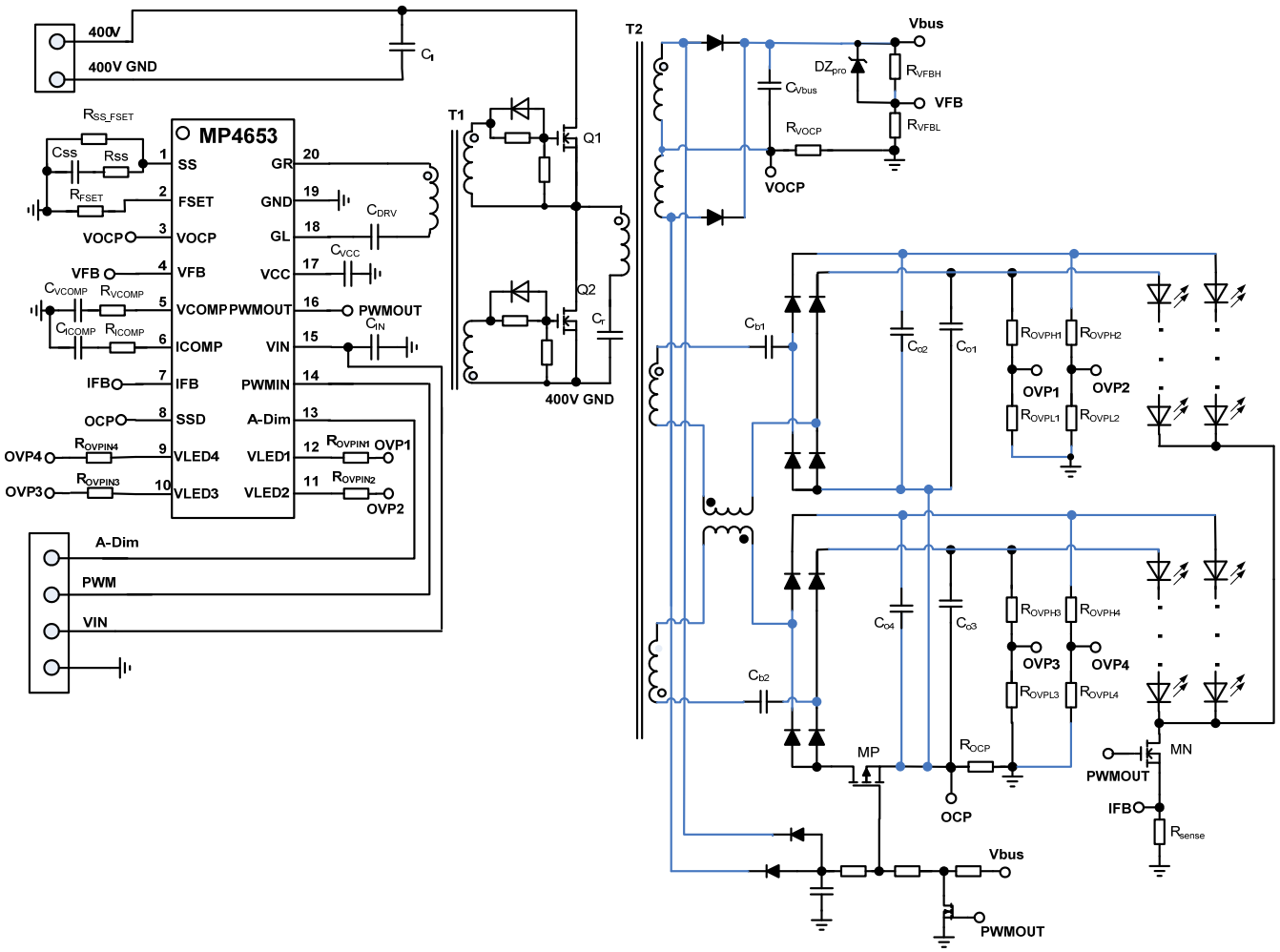


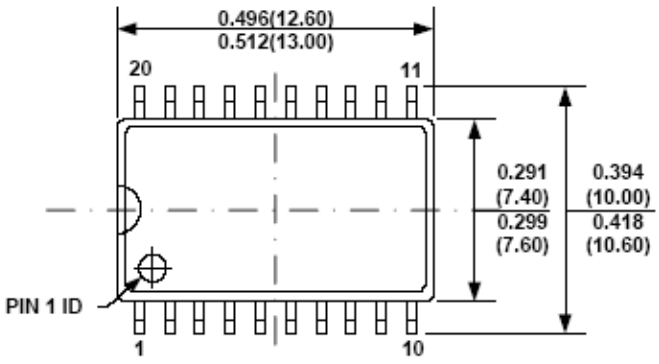
Figure 7—MP4653 Based LED Driver for 4 Strings

Please refer to MP4653 application note for the design procedure and example.

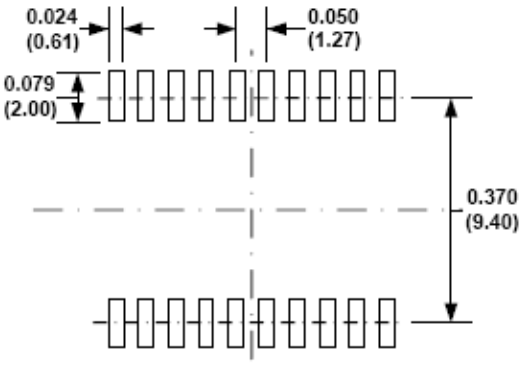
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2012 MPS. All Rights Reserved.

PACKAGE INFORMATION

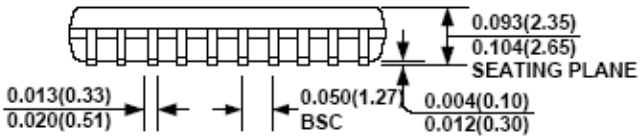
SOIC20



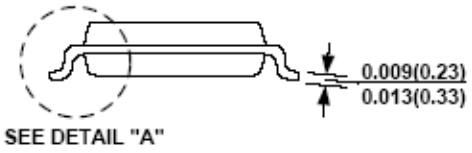
TOP VIEW



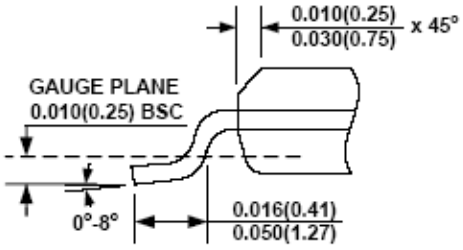
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MS-013, VARIATION AC.
6) DRAWING IS NOT TO SCALE.

NOTICE: The information in this document is subject to change without notice. Users should warrant and guarantee that third party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2012 MPS. All Rights Reserved.