DS250DF810 25 Gbps Multi-Rate 8-Channel Retimer

1 Features

- Octal-channel multi-rate retimer with integrated signal conditioning
- All channels lock independently from 20.2752 to 25.8 Gbps (including sub-rates like 10.3125 Gbps, 12.5 Gbps, and more)
- Ultra-low latency: <500 ps typical for 25.78125 Gbps data rate
- Single power supply, no low-jitter reference clock required, and integrated ac coupling capacitors to reduce board routing complexity and BOM cost
- Integrated 2×2 cross point
- Adaptive continuous time linear equalizer (CTLE)
- Adaptive decision feedback equalizer (DFE)
- Low-jitter transmitter with 3-Tap FIR filter
- Combined equalization supporting 35+ dB channel loss at 12.9 GHz
- Adjustable transmit amplitude: 205 mVppd to 1225 mVppd (typical)
- On-chip eye opening monitor (EOM), PRBS pattern checker/generator small 8 mm × 13 mm BGA package with easy flow-through routing
- Unique pinout allows routing high-speed signals underneath the package
- Pin-compatible repeater available

2 Applications

- Backplane/mid-plane reach extension
- Jitter cleaning for front-port optical
- IEEE802.3bj 100GbE, Infiniband EDR, and OIF-CEI-25G-LR/MR/SR/VSR electrical interfaces
- SFP28, QSFP28, CFP2/CFP4, CDFP

3 Description

The DS250DF810 is an eight-channel multi-rate Retimer with integrated signal conditioning. It is used to extend the reach and robustness of long, lossy, crosstalk-impaired high-speed serial links while achieving a bit error rate (BER) of 10^{-15} or less.

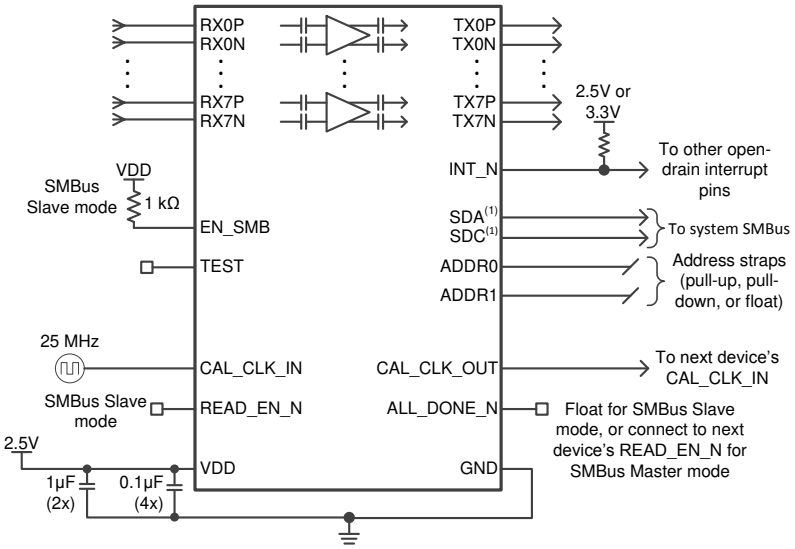
Each channel of the DS250DF810 independently locks to serial data rates in a continuous range from 20.6 Gbps to 25.8 Gbps or to any supported sub-rate (÷2 and ÷4), including key data rates such as 10.3125 Gbps and 12.5 Gbps, which allows the DS250DF810 to support individual lane Forward Error Correction (FEC) pass-through.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DS250DF810	135-pin fcBGA (135)	8.0 mm × 13.0 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Simplified Schematic



(1) SMBus signals need to be pulled up elsewhere in the system.

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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5 Revision History

Changes from Revision B (June 2019) to Revision C	Page
• Initial Public Release	1

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6 Description (continued)

Integrated physical AC coupling capacitors (TX and RX) eliminate the need for external capacitors on the PCB. The DS250DF810 has a single power supply and minimal need for external components. These features reduce PCB routing complexity and BOM cost.

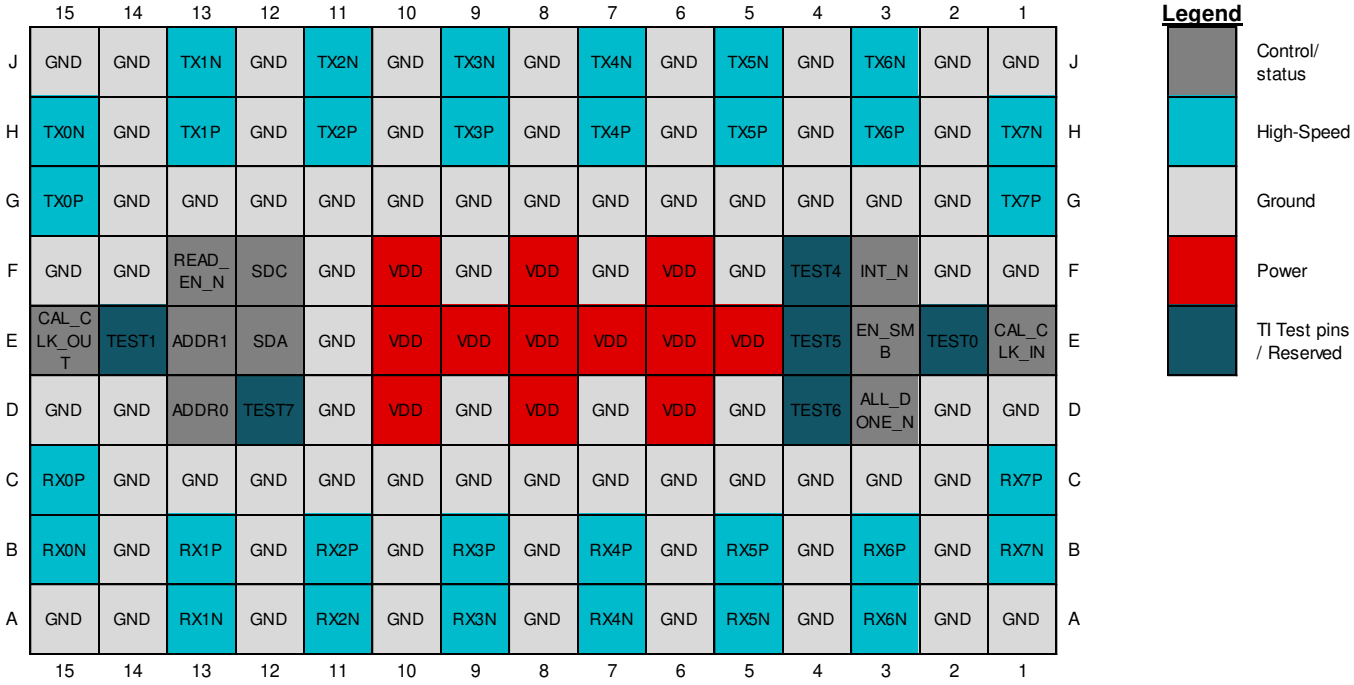
The advanced equalization features of the DS250DF810 include a low-jitter 3-tap transmit finite impulse response (FIR) filter, an adaptive continuous-time linear equalizer (CTLE), and an adaptive decision feedback equalizer (DFE). This enables reach extension for lossy interconnect and backplanes with multiple connectors and crosstalk. The integrated CDR function is ideal for front-port optical module applications to reset the jitter budget and retime the high-speed serial data. The DS250DF810 implements 2x2 cross-point on each channel pair, providing the host with both lane crossing and fanout options.

The DS250DF810 can be configured either via the SMBus or through an external EEPROM. Up to 16 devices can share a single EEPROM. A non-disruptive on-chip eye monitor and a PRBS generator/checker allow for in-system diagnostics.

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7 Pin Configuration and Functions

135-pin fcBGA, 0.8mm BGA pin pitch
Top View



Pin Functions

PIN		TYPE	INTERNAL PULL-UP/ PULL-DOWN	DESCRIPTION
NAME	NO.			
HIGH SPEED DIFFERENTIAL I/Os				
RX0P	C15	Input	None	Inverting and non-inverting differential inputs to the equalizer. An on-chip 100-Ω termination resistor connects RXP to RXN. These inputs are AC coupled on-chip with physical 220nF capacitors.
RX0N	B15	Input	None	
RX1P	B13	Input	None	Inverting and non-inverting differential inputs to the equalizer. An on-chip 100-Ω termination resistor connects RXP to RXN. These inputs are AC coupled on-chip with physical 220nF capacitors.
RX1N	A13	Input	None	
RX2P	B11	Input	None	Inverting and non-inverting differential inputs to the equalizer. An on-chip 100-Ω termination resistor connects RXP to RXN. These inputs are AC coupled on-chip with physical 220nF capacitors.
RX2N	A11	Input	None	
RX3P	B9	Input	None	Inverting and non-inverting differential inputs to the equalizer. An on-chip 100-Ω termination resistor connects RXP to RXN. These inputs are AC coupled on-chip with physical 220nF capacitors.
RX3N	A9	Input	None	
RX4P	B7	Input	None	Inverting and non-inverting differential inputs to the equalizer. An on-chip 100-Ω termination resistor connects RXP to RXN. These inputs are AC coupled on-chip with physical 220nF capacitors.
RX4N	A7	Input	None	
RX5P	B5	Input	None	Inverting and non-inverting differential inputs to the equalizer. An on-chip 100-Ω termination resistor connects RXP to RXN. These inputs are AC coupled on-chip with physical 220nF capacitors.
RX5N	A5	Input	None	
RX6P	B3	Input	None	Inverting and non-inverting differential inputs to the equalizer. An on-chip 100-Ω termination resistor connects RXP to RXN. These inputs are AC coupled on-chip with physical 220nF capacitors.
RX6N	A3	Input	None	
RX7P	C1	Input	None	Inverting and non-inverting differential inputs to the equalizer. An on-chip 100-Ω termination resistor connects RXP to RXN. These inputs are AC coupled on-chip with physical 220nF capacitors.
RX7N	B1	Input	None	
TX0P	G15	Output	None	Inverting and non-inverting 50Ω driver outputs. These outputs are AC coupled on-chip with physical 220nF capacitors.
TX0N	H15	Output	None	

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Pin Functions (continued)

PIN		TYPE	INTERNAL PULL-UP/ PULL-DOWN	DESCRIPTION
NAME	NO.			
TX1P	H13	Output	None	Inverting and non-inverting 50Ω driver outputs. These outputs are AC coupled on-chip with physical 220nF capacitors.
TX1N	J13	Output	None	
TX2P	H11	Output	None	Inverting and non-inverting 50Ω driver outputs. These outputs are AC coupled on-chip with physical 220nF capacitors.
TX2N	J11	Output	None	
TX3P	H9	Output	None	Inverting and non-inverting 50Ω driver outputs. These outputs are AC coupled on-chip with physical 220nF capacitors.
TX3N	J9	Output	None	
TX4P	H7	Output	None	Inverting and non-inverting 50Ω driver outputs. These outputs are AC coupled on-chip with physical 220nF capacitors.
TX4N	J7	Output	None	
TX5P	H5	Output	None	Inverting and non-inverting 50Ω driver outputs. These outputs are AC coupled on-chip with physical 220nF capacitors.
TX5N	J5	Output	None	
TX6P	H3	Output	None	Inverting and non-inverting 50Ω driver outputs. These outputs are AC coupled on-chip with physical 220nF capacitors.
TX6N	J3	Output	None	
TX7P	G1	Output	None	Inverting and non-inverting 50Ω driver outputs. These outputs are AC coupled on-chip with physical 220nF capacitors.
TX7N	H1	Output	None	
CALIBRATION CLOCK PINS				
CAL_CLK_IN	E1	Input, 2.5V CMOS	None	25 MHz (±100 PPM) 2.5 V single-ended clock from external oscillator. No stringent phase noise or jitter requirements on this clock. Used to calibrate VCO frequency range. This clock is not used to recover data.
CAL_CLK_OUT	E15	Output, 2.5V CMOS	None	2.5 V buffered replica of calibration clock input (pin E1) for connecting multiple devices in a daisy-chained fashion.
SYSTEM MANAGEMENT BUS (SMBUS) PINS				
ADDR0	D13	Input, 4-level	None	4-level strap pins used to set the SMBus address of the device. The pin state is read on power-up. The multi-level nature of these pins allows for 16 unique device addresses. The four strap options include: 0: 1 kΩ to GND R: 10 kΩ to GND F: Float 1: 1 kΩ to VDD
ADDR1	E13	Input, 4-level	None	
EN_SMB	E3	Input, 4-level	None	Four-level 2.5 V input used to select between SMBus master mode (float) and SMBus slave mode (high). The four defined levels are: 0: 1 kΩ to GND - RESERVED R: 10 kΩ to GND - RESERVED, TI test mode F: Float - SMBus Master Mode 1: 1 kΩ to VDD - SMBus Slave Mode
SDA	E12	I/O, 3.3V LVCMOS, Open Drain	None	SMBus data input / open drain output. External 2 kΩ to 5 kΩ pull-up resistor is required as per SMBus interface standard. This pin is 3.3 V LVCMOS tolerant.
SDC	F12	I/O, 3.3V LVCMOS, Open Drain	None	SMBus clock input / open drain clock output. External 2 kΩ to 5 kΩ pull-up resistor is required as per SMBus interface standard. This pin is 3.3 V LVCMOS tolerant.
SMBUS MASTER MODE PINS				
READ_EN_N	F13	Input, 3.3V LVCMOS	weak pull-up	SMBus Master Mode (EN_SMB=Float): When asserted low, initiates the SMBus master mode EEPROM read function. Once EEPROM read is complete (indicated by assertion of ALL_DONE_N low), this pin can be held low for normal device operation. This pin is 3.3 V tolerant. SMBus Slave Mode (EN_SMB=1): When asserted low, this causes the device to be held in reset (I2C state machine reset and register reset). This pin should be pulled high or left floating for normal operation in SMBus Slave Mode. This pin is 3.3 V tolerant.

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Pin Functions (continued)

PIN		TYPE	INTERNAL PULL-UP/ PULL-DOWN	DESCRIPTION
NAME	NO.			
ALL_DONE_N	D3	Output, LVCMOS	None	Indicates the completion of a valid EEPROM register load operation when in SMBus Master Mode (EN_SMB=Float): High = External EEPROM load failed or incomplete Low = External EEPROM load successful and complete When in SMBus slave mode (EN_SMB=1), this output will be high-z until READ_EN_N is driven low, at which point ALL_DONE_N will be driven low.
MISCELLANEOUS PINS				
INT_N	F3	Output, LVCMOS, Open-Drain	None	Open-drain 3.3 V tolerant active-low interrupt output. It pulls low when an interrupt occurs. The events which trigger an interrupt are programmable through SMBus registers. This pin can be connected in a wired-OR fashion with other device's interrupt pin. A single pull-up resistor in the 2 kΩ to 5 kΩ range is adequate for the entire INT_N net.
TEST0	E2	Input, LVCMOS	weak pull-up	Reserved TI test pin. During normal (non-test-mode) operation, these pins are configured as inputs and therefore are not affected by the presence of a signal. These pins may be left floating, tied to GND, or connected to a 2.5V (max) output.
TEST1	E14	Input, LVCMOS	weak pull-up	
TEST4	F4	Input, LVCMOS	None	Reserved TI test pin. During normal (non-test-mode) operation, this pin is configured as an input and therefore is not affected by the presence of a signal. This pin should be tied to GND or left floating to support both the Repeater and Retimer device.
TEST5	E4	Input, LVCMOS	None	Reserved TI test pin. During normal (non-test-mode) operation, this pin is configured as an input and therefore is not affected by the presence of a signal. This pin may be left floating, tied to GND, or connected to a 2.5V (max) output.
TEST6	D4	Input, LVCMOS	None	
TEST7	D12	Input, LVCMOS	None	
POWER				
VDD	D6, D8, D10, E5, E6, E7, E8, E9, E10, F6, F8, F10	Power	None	Power supply, VDD = 2.5 V ±5%. TI recommends connecting at least six de-coupling capacitors between the Retimer's VDD plane and GND as close to the Retimer as possible. For example, four 0.1 μF capacitors and two 1 μF capacitors directly beneath the device or as close to the VDD pins as possible. The VDD pins on this device should be connected through a low-resistance path to the board VDD plane.
GND	A1, A2, A4, A6, A8, A10, A12, A14, A15, B2, B4, B6, B8, B10, B12, B14, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, D1, D2, D5, D7, D9, D11, D14, D15, E11, F1, F2, F5, F7, F9, F11, F14, F15, G2, G3, G4, G5, G6, G7, G8, G9, G10, G11, G12, G13, G14, H2, H4, H6, H8, H10, H12, H14, J1, J2, J4, J6, J8, J10, J12, J14, J15	Power	None	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.

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8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
VDD_{ABSMAX}	Supply voltage (VDD)	-0.5	2.75	V
$VIO_{2.5V,ABSMAX}$	2.5 V I/O voltage (LVCMOS, CMOS and Analog)	-0.5	2.75	V
$VIO_{3.3V,ABSMAX}$	Open Drain Voltage (SDA, SDC, INT_N) and LVCMOS Input Voltage (READ_EN_N)	-0.5	4.0	V
VIN_{ABSMAX}	Signal input voltage (RXnP, RXnN)	-0.5	2.75	V
$VOUT_{ABSMAX}$	Signal output voltage (TXnP, TXnN)	-0.5	2.75	V
TJ_{ABSMAX}	Junction temperature		150	ºC
Tstg	Storage temperature	-40	150	ºC

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

8.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2	kV
	Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±2 kV may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±1 kV may actually have higher performance.

8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
VDD	Supply voltage, VDD to GND. DC plus AC power should not exceed these limits.	2.375	2.625	V
NVDD	Supply noise, DC to < 50 Hz, sinusoidal (1)		250	mVpp
NVDD	Supply noise, 50 Hz to 10 MHz, sinusoidal (1)		20	mVpp
NVDD	Supply noise, >10 MHz, sinusoidal (1)		10	mVpp
$T_{rampVDD}$	VDD supply ramp time, from 0V to 2.375V	150		µs
T_J	Operating junction temperature	-40	110	ºC
T_A	Operating ambient temperature	-40	85 (2)	ºC
$VIO_{2.5V}$	2.5 V I/O voltage (LVCMOS, CMOS and Analog)	2.375	2.625	V
$VIO_{3.3V,INT_N}$	Open Drain LVCMOS I/O voltage (INT_N)		3.6	V
$VIO_{3.3V}$	Open Drain LVCMOS I/O voltage (SDA, SDC)	2.375	3.6	V

(1) Steps must be taken to ensure the combined AC plus DC supply noise meets the specified VDD supply voltage limits.
(2) Steps must be taken to ensure the operating junction temperature range is met.

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8.4 Thermal Information

THERMAL METRIC(1)		CONDITIONS/ ASSUMPTIONS(2)				UNIT
		4-layer JEDEC Board	10-layer 8in x 6in Board	20-layer 8in x 6in Board	30-layer 8in x 6in Board	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	26.4	9.3	8.5	8.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	1.6	-	-	-	
$R_{\theta JB}$	Junction-to-board thermal resistance	9.3	-	-	-	
Ψ_{JT}	Junction-to-top characterization parameter	0.1	0.1	0.1	0.1	
Ψ_{JB}	Junction-to-board characterization parameter	9.3	5	4.9	4.6	

(1) For more information about traditional and new thermal metrics, see the IC Package-Thermal Metrics application report, SPRA953.
(2) No heat sink or airflow was assumed for these estimations. Depending on the application, a heat sink, faster airflow, and/or reduced ambient temperature (<85 C) may be required in order to meet the maximum junction temperature specification per the Recommended Operating Conditions section.

8.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Rbaud	Input data rate	Full-rate	20.2752		25.8	Gbps
Rbaud		Half-rate	10.1376		12.9	Gbps
Rbaud		Quarter-rate	5.0688		6.45	Gbps
t_{EEPROM}	EEPROM configuration load time	Single device reading its configuration from an EEPROM. Common channel configuration. This time scales with the number of devices reading from the same EEPROM.			15(1)	ms
t_{EEPROM}	EEPROM configuration load time	Single device reading its configuration from an EEPROM. Unique channel configuration. This time scales with the number of devices reading from the same EEPROM.			40(1)	ms
t_{POR}	Power-on reset assertion time	Internal power-on reset (PoR) stretch between stable power supply and de-assertion of internal PoR. The SMBus address is latched on the completion of the PoR stretch, and SMBus accesses are permitted.			50	ms

(1) From low assertion of READ_EN_N to low assertion of ALL_DONE_N. Does not include Power-On Reset time.

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Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
$W_{channel}$	Power consumption per active channel	With CTLE, full DFE, Tx FIR, Driver, and Crosspoint enabled. Idle power consumption not included.		241	305	mW
		With CTLE, full DFE, Tx FIR, and Driver enabled; Crosspoint disabled. Idle power consumption not included.		233		mW
		With CTLE, partial DFE (taps 1-2 only), Tx FIR, and Driver enabled; Crosspoint and DFE taps 3-5 disabled. Idle power consumption not included.		220		mW
		With CTLE, Tx FIR, Driver, and Crosspoint enabled; DFE disabled. Idle power consumption not included.		211	290	mW
		Assuming CDR acquiring lock with CTLE, full DFE, Tx FIR, Driver, and Crosspoint enabled. Idle power consumption not included.		365	430	mW
		Assuming CDR acquiring lock with CTLE, Tx FIR, Driver, and Crosspoint enabled; DFE disabled. Idle power consumption not included.		318	393	mW
		PRBS checker power consumption only(2)		220	302	mW
		PRBS generator power power consumption only(2)		230	315	mW
W_{static_total}	Total idle power consumption	Idle/static mode, power supplied, no high-speed data present at inputs, all channels automatically powered down.		658	1050	mW
I_{total}	Active mode total device supply current consumption	With CTLE, full DFE, Tx FIR, Driver, and Crosspoint enabled.		1036	1330	mA
		With CTLE, full DFE, Tx FIR, and Driver enabled; Crosspoint disabled.		1010		mA
		With CTLE, partial DFE (taps 1-2 only), Tx FIR, and Driver enabled; Crosspoint and DFE taps 3-5 disabled.		970		mA
		With CTLE, Tx FIR, Driver, and Crosspoint enabled. DFE disabled.		940	1278	mA
I_{static_total}	Idle mode total device supply current consumption	Idle/static mode. Power supplied, no high-speed data present at inputs, all channels automatically powered down.		263	400	mA
LVCMOS DC SPECIFICATIONS						
V_{IH}	Input high level voltage	2.5 V LVCMOS pins	1.75		VDD	V
		3.3 V LVCMOS pin (READ_EN_N)	1.75		3.6	V
V_{IL}	Input low level voltage	2.5 V LVCMOS pins	GND		0.7	V
		3.3 V LVCMOS pin (READ_EN_N)	GND		0.8	V

(2) To ensure optimal performance, it is recommended to not enable more than two PRBS blocks (checker and/or generator) per channel quad.

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Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{TH}	High level (1) input voltage	4-level pins ADDR0, ADDR1, and EN_SMB		0.95 * VDD		V
	Float level input voltage	4-level pins ADDR0, ADDR1, and EN_SMB		0.67 * VDD		V
	10K to GND input voltage	4-level pins ADDR0, ADDR1, and EN_SMB		0.33 * VDD		V
	Low level (0) input voltage	4-level pins ADDR0, ADDR1, and EN_SMB		0.1		V
V_{OH}	High level output voltage	IOH = 4mA	2			V
V_{OL}	Low level output voltage	IOL = -4mA			0.4	V
I_{IH}	Input high leakage current	Vinput = VDD, Open drain pins			70	µA
I_{IH}	Input high leakage current	Vinput = VDD and CAL_CLK_IN pin			65	µA
I_{IH}	Input high leakage current	Vinput = VDD, ADDR[1:0] and EN_SMB pins			120	µA
I_{IH}	Input high leakage current	Vinput = VDD, READ_EN_N			75	µA
I_{IL}	Input low leakage current	Vinput = 0V, Open drain pins	-15			µA
I_{IL}	Input low leakage current	Vinput = 0V, CAL_CLK_IN pins	-45			µA
I_{IL}	Input low leakage current	Vinput = 0V, ADDR[1:0], READ_EN_N, and EN_SMB pins	-230			µA
RECEIVER INPUTS (RXnP, RXnN)						
V_{IDMax}	Maximum input differential voltage	For normal operation		1225		mVppd
RL_{SDD11}	Differential input return loss, SDD11	Between 50 MHz and 3.69 GHz		<-16		dB
RL_{SDD11}	Differential input return loss, SDD11	Between 3.69 GHz and 12.9 GHz		<-12		dB
RL_{SDC11}	Differential to common-mode input return loss, SDC11	Between 50 MHz and 12.9 GHz		<-23		dB
RL_{SCD11}	Differential to common-mode input return loss, SCD11	Between 50 MHz and 12.9 GHz		<-24		dB
RL_{SCC11}	Common-mode input return loss, SCC11	Between 150 MHz and 10 GHz		<-10		dB
RL_{SCC11}	Common-mode input return loss, SCC11	Between 10 GHz and 12.9 GHz		<-10		dB
V_{SDAT}	AC signal detect assert (ON) threshold level	Minimum input peak-to-peak amplitude level at device pins required to assert signal detect. 25.78125Gbps with PRBS7 pattern and 20dB loss channel		196		mVppd
V_{SDDT}	AC signal detect de-assert (OFF) threshold level	Maximum input peak-to-peak amplitude level at device pins which causes signal detect to de-assert. 25.78125Gbps with PRBS7 pattern and 20dB loss channel		147		mVppd
TRANSMITTER OUTPUTS (TXnP, TXnN)						
VOD	Output differential voltage amplitude	Measured with c(0)=7 setting (Reg_0x3D[6:0]=0x07, Reg_0x3E[6:0]=0x40, REG_0x3F[6:0]=0x40). Differential measurement using an 8T pattern (eight 1s followed by eight 0s) at 25.78125 Gbps with TXPn and TXNn terminated by 50 Ohms to GND.		525		mVppd

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Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOD	Output differential voltage amplitude	Measured with c(0)=31 setting (Reg_0x3D[6:0]=0x1F, Reg_0x3E[6:0]=0x40, REG_0x3F[6:0]=0x40). Differential measurement using an 8T pattern (eight 1s followed by eight 0s) at 25.78125 Gbps with TXPn and TXNn terminated by 50 Ohms to GND.		1225		mVppd
VOD_{idle}	Differential output amplitude with TX disabled			< 11		mVppd
VOD_{res}	Output VOD resolution	Difference in VOD between two adjacent c(0) settings. Applies to VOD in the 525mVppd to 1225mVppd range [c(0)>4].		< 50		mVppd
$V_{cm\text{-}TX\text{-}AC}$	Common-mode AC output noise	With respect to signal ground. Measured with PRBS9 data pattern. Measured with a 33GHz (-3dB) low-pass filter.		6.5		mV, RMS
t_r, t_f	Output transition time	20%-to-80% rise time and 80%-to-20% fall time on a clock-like {11111 00000} data pattern at 25.78125 Gbps. Measured for ~800 mVppd output amplitude and no equalization: Reg_0x3D=+13, Reg_0x3E=0, REG_0x3F=0		17		ps
RL_{SDD22}	Differential output return loss, SDD22	Between 50 MHz and 5 GHz		<-12		dB
RL_{SDD22}	Differential output return loss, SDD22	Between 5 GHz and 12.9 GHz		<-9		dB
RL_{SCD22}	Common-mode to differential output return loss, SCD22	Between 50 MHz and 12.9 GHz		<-22		dB
RL_{SDC22}	Differential-to-common-mode output return loss, SDC22	Between 50 MHz and 12.9 GHz		<-22		dB
RL_{SCC22}	Common-mode output return loss, SCC22	Between 50 MHz and 10 GHz		<-9		dB
RL_{SCC22}	Common-mode output return loss, SCC22	Between 10 GHz and 12.9 GHz		<-9		dB
SMBus ELECTRICAL CHARACTERISTICS (SLAVE MODE)						
V_{IH}	Input high level voltage	SDA and SDC	1.75		3.6	V
V_{IL}	Input low level voltage	SDA and SDC	GND		0.8	V
C_{IN}	Input pin capacitance			15		pF
V_{OL}	Low level output voltage	SDA or SDC, IOL = 1.25 mA			0.4	V
I_{IN}	Input current	SDA or SDC, VINPUT = VIN, VDD, GND	-15		15	µA
T_R	SDA rise time, read operation	Pull-up resistor = 1 kΩ, Cb = 50pF		150		ns
T_F	SDA fall time, read operation	Pull-up resistor = 1 kΩ, Cb = 50pF		4.5		ns

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8.6 Timing Requirements, Retimer Jitter Specifications

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
J_{TJ}	Output Total jitter (TJ)	Measured at 25.78125 Gbps to a probability level of 1E-12 with PRBS11 data pattern an evaluation board traces de-embedded.		0.17		UIpp @ 1E-12
J_{RJ}	Output Random Jitter (RJ)	Measured at 25.78125 Gbps to a probability level of 1E-12 with PRBS11 data pattern an evaluation board traces de-embedded		6		mUI RMS
J_{DCD}	Output Duty Cycle Distortion (DCD)	Measured at 25.78125 Gbps to a probability level of 1E-12 with PRBS11 data pattern an evaluation board traces de-embedded		4		mUIpp
J_{PEAK}	Jitter peaking	Measured at 10.3125 Gbps with PRBS7 data pattern. Peaking frequency in the range of 1 to 6 MHz.		0.8		dB
J_{PEAK}	Jitter peaking	Measured at 25.78125 Gbps with PRBS7 data pattern. Peaking frequency in the range of 1 to 17 MHz.		0.4		dB
BWPLL	PLL bandwidth	Data rate of 10.3125Gbps with PRBS7 pattern		5.3		MHz
BWPLL	PLL bandwidth	Data rate of 25.78125Gbps with PRBS7 pattern		5.5		MHz
J_{TOL}	Input jitter tolerance	Measured at 25.78125 Gbps with SJ frequency = 190 KHz, 30dB input channel loss, PRBS31 data pattern, 800 mVppd launch amplitude, and 0.078 UIpp total uncorrelated output jitter in addition to the applied SJ. BER < 1E-12.		9		UIpp
J_{TOL}	Input jitter tolerance	Measured at 25.78125 Gbps with SJ frequency = 940 KHz, 30dB input channel loss, PRBS31 data pattern, 800 mVppd launch amplitude, and 0.078 UIpp total uncorrelated output jitter in addition to the applied SJ. BER < 1E-12.		1		UIpp
J_{TOL}	Input jitter tolerance	Measured at 25.78125 Gbps with SJ frequency > 15MHz, 30dB input channel loss, PRBS31 data pattern, 800 mVppd launch amplitude, and 0.078 UIpp total uncorrelated output jitter in addition to the applied SJ. BER < 1E-12.		0.3		UIpp

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8.7 Timing Requirements, Retimer Specifications

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_D	Input-to-output latency (propagation delay) through a channel	No crosspoint; CDR enabled and locked.		3.5UI + 125ps		ps
t_D	Input-to-output latency (propagation delay) through a channel	Crosspoint enabled; CDR enabled and locked.		3.5UI + 145ps		ps
t_D	Input-to-output latency (propagation delay) through a channel	No crosspoint; CDR in raw mode. 25.78125 Gbps data rate.		< 145		ps
t_{SK}	Channel-to-channel interpair skew	Latency difference between channels at full-rate. 25.78125 Gbps data rate		< 30		ps
t_{lock}	CDR lock acquisition time	Measured at 25.78125 Gbps, Adapt Mode = 1 (Reg_0x31[6:5]=0x1), EOM timer = 0x5 (Reg_0x2A[7:4]=0x5).		< 100		ms
t_{lock}	CDR lock acquisition time	Measured at 10.3125 Gbps, Adapt Mode = 1 (Reg_0x31[6:5]=0x1), EOM timer = 0x5 (Reg_0x2A[7:4]=0x5).		< 100		ms

8.8 Timing Requirements, Recommended Calibration Clock Specifications

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CLK_f	Calibration clock frequency			25		MHz
CLK_{PPM}	Calibration clock PPM tolerance		-100		100	PPM
CLK_{IDC}	Recommended/tolerable input duty cycle		40%	50%	60%	
CLK_{ODC}	Intrinsic calibration clock duty cycle distortion	Intrinsic duty cycle distortion of chip calibration clock output at the CAL_CLK_OUT pin, assuming 50% duty cycle on CAL_CLK_IN pin.	45%		55%	
CLKnum	Number of devices which can be cascaded from CAL_CLK_OUT to CAL_CLK_IN	Assumes worst-case 60%/40% input duty cycle on the first device. CAL_CLK_OUT from first devuce connects to CAL_CLK_IN of second device, and so on until the last device.		20		N/A

8.9 Recommended SMBus Switching Characteristics (Slave Mode)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SDC}	SDC clock frequency		10	100	400	kHz
t_{HD-DAT}	Data hold time			0.75		ns
t_{SU-DAT}	Data setup time			100		ns

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8.10 Recommended SMBus Switching Characteristics (Master Mode)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SDC}	SDC clock frequency		260	303	346	kHz
T_{LOW}	SDC low period		1.66	1.90	2.21	µs
T_{HIGH}	SDC high period		1.22	1.40	1.63	µs
T_{HD-STA}	Hold time start operation			0.6		µs
T_{SU-STA}	Setup time start operation			0.6		µs
T_{HD-DAT}	Data hold time			0.9		µs
T_{SD-DAT}	Data setup time			0.1		µs
T_{SU-STO}	Stop condition setup time			0.6		µs
T_{BUF}	Bus free time between Stop-Start			1.3		µs
T_R	SDC rise time	Pull-up resistor = 1 kΩ		300		ns
T_F	SDC fall time	Pull-up resistor = 1 kΩ		300		ns

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8.11 Typical Characteristics

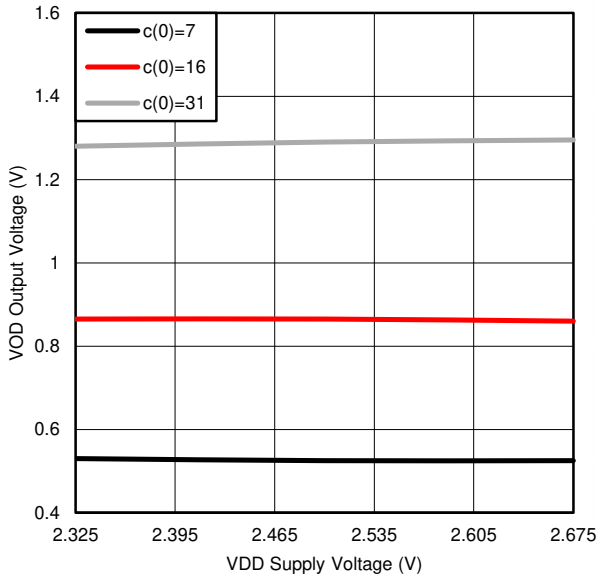


Figure 1. Typical VOD versus Supply Voltage

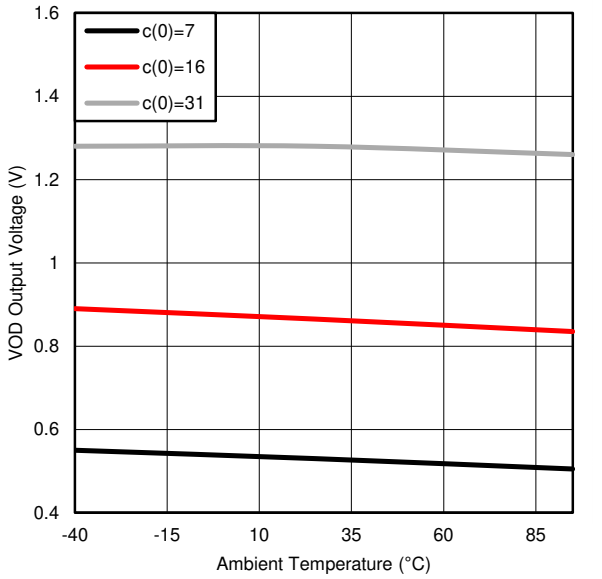


Figure 2. Typical VOD versus Temperature

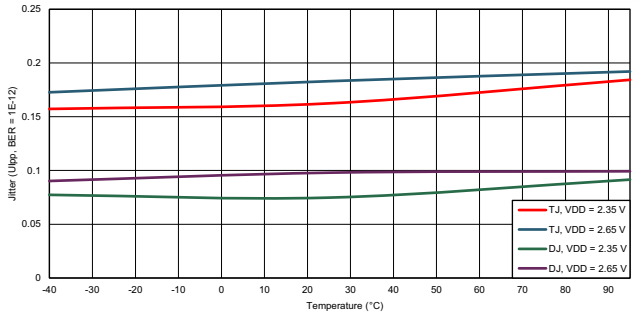


Figure 3. Typical VOD versus FIR Main-Cursor

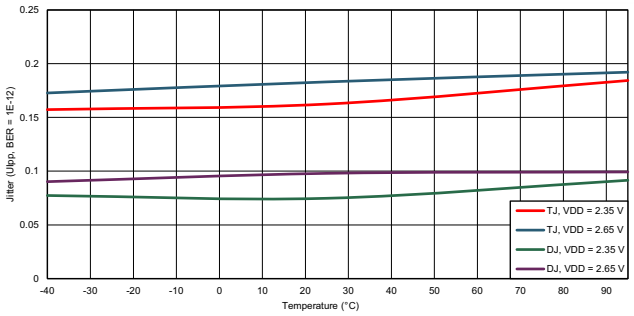


Figure 4. Typical Output Jitter versus Temperature at 25.78125Gbps

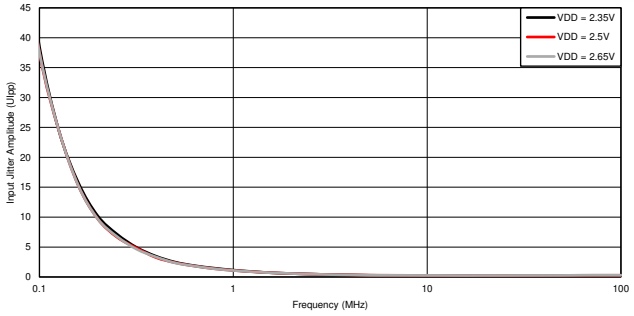


Figure 5. Typical Sinusoidal Input Jitter Tolerance for 30dB channel at 25.78125Gbps for 0.1MHz to 100MHz with Input Random Jitter = 0.078UIpp, T = 25C

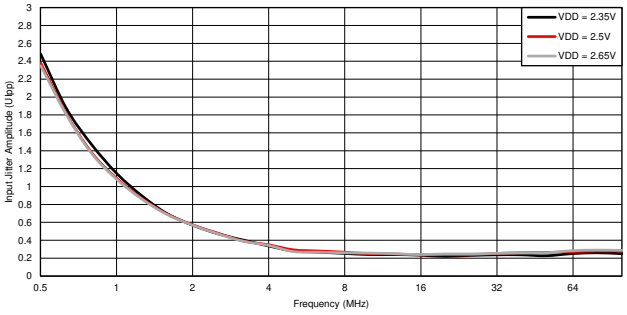


Figure 6. Typical Input Jitter Tolerance for 30dB channel at 25.78125Gbps for 0.5MHz to 100MHz with Input Random Jitter = 0.078UIpp, T = 25C

9 Detailed Description

9.1 Overview

The DS250DF810 is an eight-channel multi-rate retimer with integrated signal conditioning. Each of the eight channels operates independently. Each channel includes a continuous-time linear equalizer (CTLE) and a Decision Feedback Equalizer (DFE), which together compensate for the presence of a dispersive transmission channel between the source transmitter and the DS250DF810 receiver. The CTLE and DFE are self-adaptive.

Each channel includes an independent voltage-controlled oscillator (VCO) and phase-locked loop (PLL) which produce a clean clock that is frequency-locked to the clock embedded in the input data stream. The high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially-reduced jitter. This clean clock is used to re-time the incoming data, removing high-frequency jitter from the data stream and reproducing the data on the output with significantly-reduced jitter.

Each channel of the DS250DF810 features an output driver with adjustable differential output voltage and output equalization in the form of a three-tap finite impulse response (FIR) filter. The output FIR compensates for dispersion in the transmission channel at the output of the DS250DF810.

All transmit and receive channels on the DS250DF810 are AC-coupled with physical AC-coupling capacitors (220 nF +/- 20%) on the package substrate. This ensures common mode voltage compatibility with all link partners and eliminates the need for AC coupling capacitors on the system PCB, thereby saving cost and greatly reducing PCB routing complexity.

Between each group of two adjacent channels (e.g. between channels 0 and 1, 2 and 3, 4 and 5, and 6 and 7) is a full 2x2 cross-point switch. This allows multiplexing and de-multiplexing/fanout applications for fail-over redundancy, as well as cross-over applications to aid PCB routing.

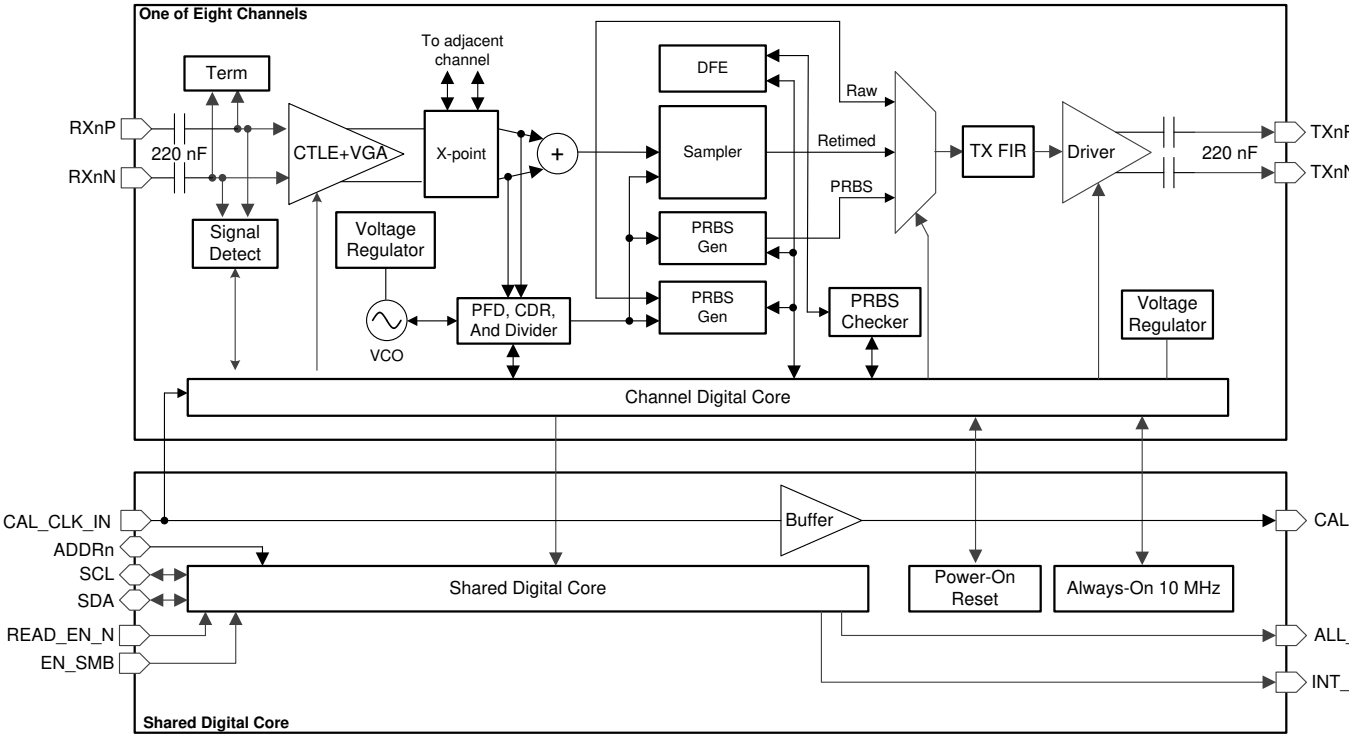
Each channel also includes diagnostic features such as a Pseudo Random Bit Sequence (PRBS) pattern generator and checker, as well as a non-destructive eye opening monitor (EOM). The EOM can be used to plot the post-equalized eye at the input to the decision slicer or simply to read the horizontal eye opening (HEO) and vertical eye opening (VEO).

The DS250DF810 is configurable through a single SMBus port. The DS250DF810 can also act as an SMBus master to configure itself from an EEPROM. Up to sixteen DS250DF810 devices can share a single SMBus.

The sections which follow describe the functionality of various circuits and features within the DS250DF810. For more information about how to program or operate these features, consult the DS250DF810 Programming Guide.

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9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Device Data Path Operation

The DS250DF810 data path consists of several key blocks as shown in the functional block diagram. These key circuits are:

- *AC-Coupled Receiver and Transmitter*
- *Signal Detect*
- *Continuous Time Linear Equalizer (CTLE)*
- *Variable Gain Amplifier (VGA)*
- *Cross-Point Switch*
- *Decision Feedback Equalizer (DFE)*
- *Clock and Data Recovery (CDR)*
- *Calibration Clock*
- *Differential Driver with FIR Filter*

9.3.2 AC-Coupled Receiver and Transmitter

The differential receiver for each DS250DF810 channel contains on-chip AC coupling capacitors. The differential transmitter for each DS250DF810 channel also implement on-chip AC coupling capacitors. Value is 220nF +/- 20% for all AC coupling capacitors.

9.3.3 Signal Detect

The DS250DF810 receiver contains a signal detect circuit. The signal detect circuit monitors the energy level on the receiver inputs and powers on or off the rest of the high-speed data path if a signal is detected or not. By default, each channel allows the signal detect circuit to automatically power on or off the rest of the high speed data path depending on the presence of an input signal. The signal detect block can be manually controlled in the SMBus channel registers. This can be useful if it is desired to manually force channels to be disabled. For information on how to manually operate the signal detect circuit refer to the DS250DF810 Programming Guide.

9.3.4 Continuous Time Linear Equalizer (CTLE)

The CTLE in the DS250DF810 is a fully-adaptive equalizer. The CTLE adapts according to a Figure of Merit (FOM) calculation during the lock acquisition process. The FOM calculation is based upon the horizontal eye opening (HEO) and vertical eye opening (VEO). Once the CDR locks and the CTLE adapts, the CTLE boost level is frozen until a manual re-adapt command is issued or until the CDR re-enters the lock acquisition state. The CTLE can be re-adapted by resetting the CDR.

The CTLE consists of 4 stages, with each stage having 2-bit boost control. This allows for 256 different boost combinations. The CTLE adaption algorithm allows the CTLE to adapt through 16 of these boost combinations. These 16 boost combinations comprise the EQ Table in the channel registers. See channel registers 0x40 through 0x4F. This EQ Table can be reprogrammed to support up to 16 of the 256 boost settings.

The boost levels can be set between 8 dB and 25 dB (at 14GHz.)

9.3.5 Variable Gain Amplifier (VGA)

The DS250DF810 receiver implements a VGA. The VGA assists in the recovery of extremely small signals, working in conjunction with the CTLE to equalize and scale amplitude. The VGA has 1-bit control via Register 0x8E[0], and the VGA is enabled by default. In addition to the VGA, the CTLE implements its own gain control via register 0x13[5] to adjust the DC amplitude similar to the VGA. For more information on how to configure the VGA refer to the DS250DF810 Programming Guide.

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Feature Description (continued)

9.3.6 Cross-Point Switch

Each group of two adjacent channels in the DS250DF810 has a 2×2 cross-point that may be enabled to implement a 2-to-1 mux, a 1-to-2 fanout, or an A-to-B/B-to-A lane cross. A cross-point exists between the following channel pairs:

- Channel 0 and Channel 1
- Channel 2 and Channel 3
- Channel 4 and Channel 5
- Channel 6 and Channel 7

9.3.7 Decision Feedback Equalizer (DFE)

A 5-tap DFE can be enabled within the data path of each channel to assist with reducing the effects of cross talk, reflections, or post cursor inter-symbol interference (ISI). The DFE must be manually enabled, regardless of the selected adapt mode. Once the DFE has been enabled it can be configured to adapt only during lock acquisition or to adapt continuously. The DFE can also be manually configured to specified tap polarities and tap weights. However, when the DFE is configured manually the DFE auto-adaption should be disabled. For many applications with lower insertion loss (i.e. < 30 dB) lower crosstalk, and/or lower reflections, part or all of the DFE can be disabled to reduce power consumption. The DFE can either be fully enabled (taps 1-5), partially enabled (taps 1-2 only), or fully disabled (no taps).

The DFE taps are all feedback taps with 1UI spacing. Each tap has a specified boost weight range and polarity bit.

Table 1. DFE Tap Weights

DFE PARAMETER	DECIMAL (REGISTER VALUE)	VALUE (mV) (TYP)
Tap 1 Weight Range	0 - 31	0 – 217
Tap 2-5 Weight Range	0 - 15	0 – 105
Tap Weight Step Size	NA	7
Polarity	0: (+) positive; feedback value creates a low-pass filter response, thus providing attenuation to correct for negative-sign post-cursor ISI 1: (-) negative; Feedback value creates a high-pass filter response, thus providing boost to correct for positive-sign post-cursor ISI.	

9.3.8 Clock and Data Recovery (CDR)

The CDR consists of a Phase Locked Loop (PLL), PPM counter, and Input and Output Data Multiplexers (mux) allowing for retimed data, un-retimed data, PRBS generator and output muted modes.

By default, the equalized data is fed into the CDR for clock and data recovery. The recovered data is then output to the FIR filter and differential driver together with the recovered clock which has been cleaned of any high-frequency jitter outside the bandwidth of the CDR clock recovery loop. The bandwidth of the CDR defaults to 5.5 MHz (typ) in full-rate (divide-by-1) mode and 5.3 MHz (typ) in sub-rate mode. The CDR bandwidth is adjustable. Refer to the DS250DF810 Programming Guide for more information on adjusting the CDR bandwidth. Users can configure the CDR data to route the recovered clock and data to the PRBS checker. Users also have the option of configuring the output of the CDR to send raw non-retimed data, or data from the pattern generator.

The CDR requires the following in order to be properly configured:

- 25 MHz calibration clock to run the PPM counter (CAL_CLK_IN).
- Expected data rates must be programmed into the CDR either through the rate table or entered manually with the corrected divider settings. Refer to the Programming Guide for more information on configuring the CDR for different data rates.

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9.3.9 Calibration Clock

The calibration clock is not part of the CDR's PLL and thus is not used for clock and data recovery. The calibration clock is connected only to the PPM counter for each CDR. The PPM counter constrains the allowable lock ranges of the CDR according to the programmed values in the rate table or the manually entered data rates. The host should provide an input calibration clock signal of 25 MHz frequency. Because this clock is not used for clock and data recovery, there are no stringent jitter requirements placed on this 25 MHz calibration clock.

9.3.10 Differential Driver with FIR Filter

The DS250DF810 output driver has a three-tap finite impulse response (FIR) filter which allows for pre- and post-cursor equalization to compensate for a wide variety of output channel media. The filter consists of a weighted sum of three consecutive retimed bits as shown in the following diagram. C[0] can take on values in the range [-31, +31]. C[-1] and C[+1] can take on values in the range [-15, 15].

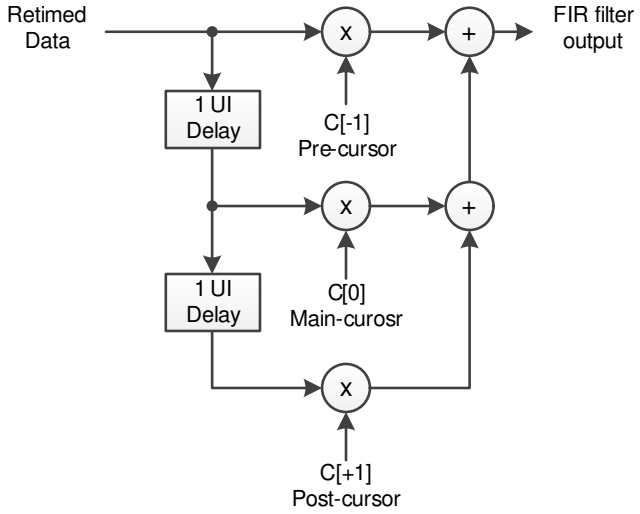


Figure 7. FIR Filter Functional Model

When utilizing the FIR filter, it is important to abide by the following general rules:

- |C[-1]|+|C[0]|+|C[+1]| ≤ 31; the FIR tap coefficients absolute sum must be less or equal to 31)
- sgn(C[-1])=sgn(C[+1]) ≠ sgn(C[0]), for high-pass filter effect; the sign for the pre-cursor and/or post-cursor tap must be different from main-cursor tap to realize boost effect
- sgn(C[-1])=sgn(C[+1]) = sgn(C[0]), for low-pass filter effect; the sign for the pre-cursor and/or post-cursor tap must be equal to the main-cursor tap to realize attenuation effect

The FIR filter is used to pre-distort the transmitted waveform in order to compensate for frequency-dependant loss in the output channel. The most common way of pre-distorting the signal is to accentuate the transitions and de-emphasize the non-transitions. The bit before a transition is accentuated via the pre-cursor tap, and the bit after the transition is accentuated via the post-cursor tap. The figures below give a conceptual illustration of how the FIR filter affects the output waveform. The following characteristics can be derived from the example waveforms.

- $VOD_{pk\text{-}pk} = v_7 - v_8$
- $VOD_{low\text{-}frequency} = v_2 - v_5$
- $Rpre_{dB} = 20 * \log_{10} (v_3 / v_2)$
- $Rpst_{dB} = 20 * \log_{10} (v_1 / v_2)$

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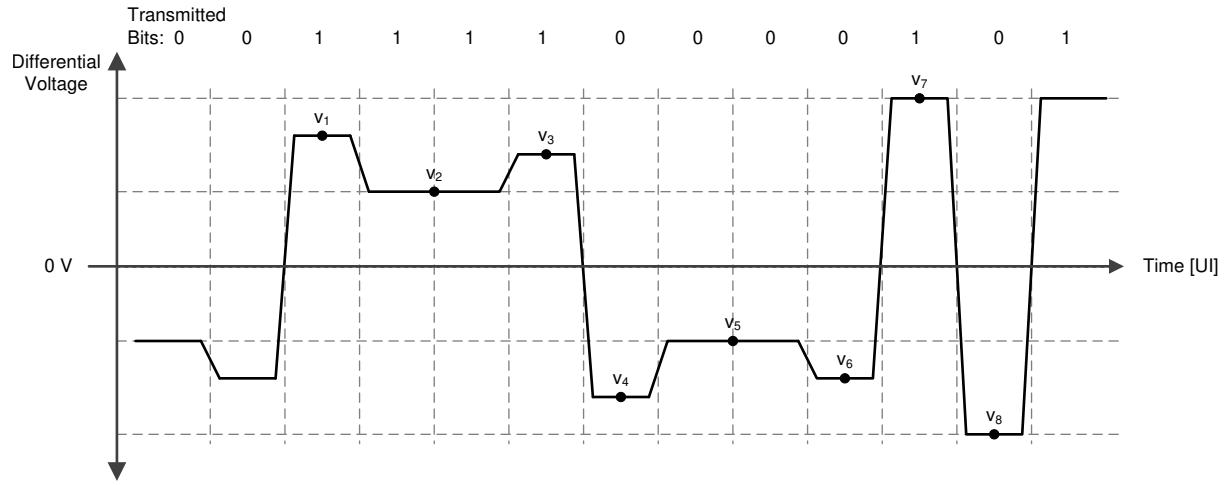


Figure 8. Conceptual FIR Waveform With Post-Cursor Only

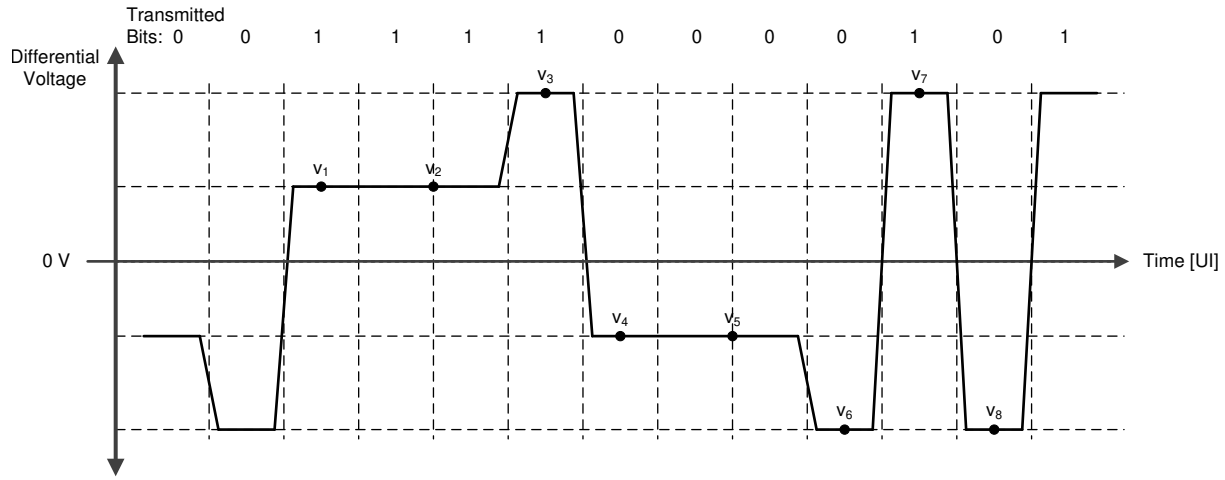


Figure 9. Conceptual FIR Waveform With Pre-Cursor Only

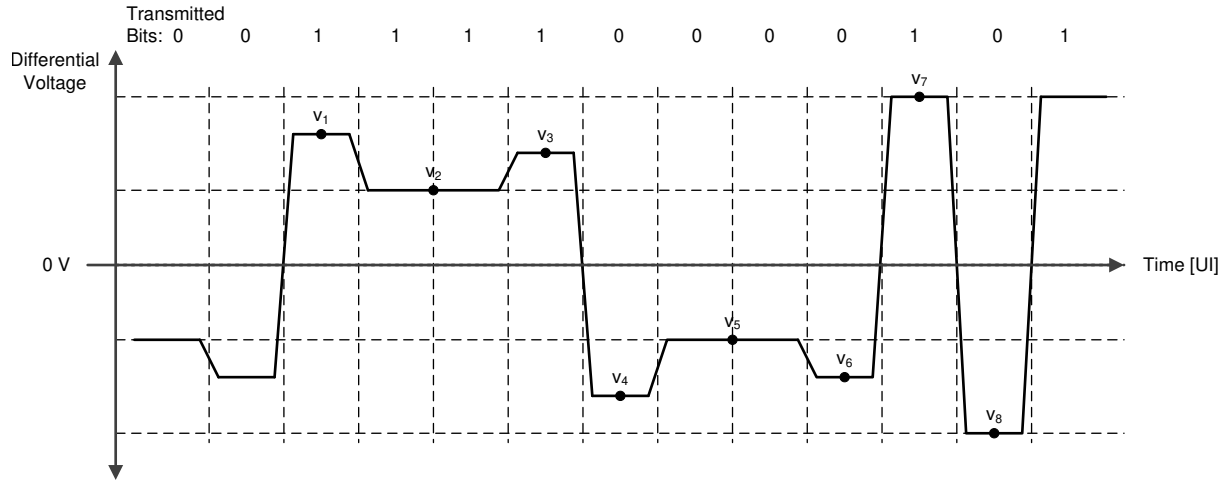


Figure 10. Conceptual FIR Waveform With Both Pre- And Post-Cursor

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9.3.11 Setting the Output V_{OD}

The output differential voltage (V_{OD}) of the driver is controlled by manipulating the FIR tap settings. The main cursor tap is the primary knob for amplitude adjustment. The pre and post cursor FIR tap settings can then be adjusted to provide equalization. To maintain a constant peak-to-peak VOD, the user should adjust the main cursor tap value relative to the pre/post tap changes so as to maintain a constant absolute sum of the FIR tap values. The table below shows various settings for V_{OD} settings ranging from 205 mVpp to 1225 mVpp (typical). Note that the output peak-to-peak amplitude is a function of the sum of the absolute values of the taps, whereas the low-frequency amplitude is purely a function of the main-cursor value.

Table 2. Typical VOD and FIR Values

FIR SETTINGS			Peak-to Peak VOD(V)	RPRE(dB)	RPST(dB)
PRE-CURSOR: REG_0x3E[6:0]	MAIN-CURSOR: REG_0x3D[6:0]	POST-CURSOR: REG_0x3F[6:0]			
0	0	0	0.205	NA	NA
0	+1	0	0.260	NA	NA
0	+2	0	0.305	NA	NA
0	+3	0	0.355	NA	NA
0	+4	0	0.395	NA	NA
0	+5	0	0.440	NA	NA
0	+6	0	0.490	NA	NA
0	+7	0	0.525	NA	NA
0	+8	0	0.565	NA	NA
0	+9	0	0.610	NA	NA
0	+10	0	0.650	NA	NA
0	+11	0	0.685	NA	NA
0	+12	0	0.720	NA	NA
0	+13	0	0.760	NA	NA
0	+14	0	0.790	NA	NA
0	+15	0	0.825	NA	NA
0	+16	0	0.860	NA	NA
0	+17	0	0.890	NA	NA
0	+18	0	0.925	NA	NA
0	+19	0	0.960	NA	NA
0	+20	0	0.985	NA	NA
0	+21	0	1.010	NA	NA
0	+22	0	1.040	NA	NA
0	+23	0	1.075	NA	NA
0	+24	0	1.095	NA	NA
0	+25	0	1.125	NA	NA
0	+26	0	1.150	NA	NA
0	+27	0	1.165	NA	NA
0	+28	0	1.190	NA	NA
0	+29	0	1.205	NA	NA
0	+30	0	1.220	NA	NA
0	+31	0	1.225	NA	NA
0	+18	-1	0.960	NA	2.1
0	+17	-2	0.960	NA	2.5
0	+16	-3	0.960	NA	3.1
0	+15	-4	0.960	NA	3.8
0	+14	-5	0.960	NA	4.7

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Table 2. Typical VOD and FIR Values (continued)

FIR SETTINGS			Peak-to Peak VOD(V)	RPRE(dB)	RPST(dB)
PRE-CURSOR: REG_0x3E[6:0]	MAIN-CURSOR: REG_0x3D[6:0]	POST-CURSOR: REG_0x3F[6:0]			
0	+13	-6	0.960	NA	5.8
0	+12	-7	0.960	NA	7.2
0	+11	-8	0.960	NA	9.0
0	+10	-9	0.960	NA	11.6
-1	18	0	0.960	1.0	NA
-2	17	0	0.960	1.6	NA
-3	16	0	0.960	2.4	NA
-4	15	0	0.960	3.3	NA
0	26	-1	1.165	NA	1.1
0	25	-2	1.165	NA	1.3
0	24	-3	1.165	NA	1.8
0	23	-4	1.165	NA	2.2
0	22	-5	1.165	NA	2.7
0	21	-6	1.165	NA	3.3
0	20	-7	1.165	NA	3.9
0	19	-8	1.165	NA	4.7
0	18	-9	1.165	NA	5.7
0	17	-10	1.165	NA	6.9
0	16	-11	1.165	NA	8.4
0	15	-12	1.165	NA	10.1
-1	26	0	1.165	0.7	NA
-2	25	0	1.165	1.2	NA
-3	24	0	1.165	1.5	NA
-4	23	0	1.165	2.0	NA
-5	22	0	1.165	2.6	NA
-6	21	0	1.165	3.2	NA
-7	20	0	1.165	4.0	NA

The recommended pre-cursor and post-cursor settings for a given channel will depend on the channel characteristics (mainly insertion loss) as well as the equalization capabilities of the downstream receiver. The DS250DF810 receiver, with its highly-capable CTLE and DFE, does not require a significant amount of pre- or post-cursor. The figures below give general recommendations for pre- and post-cursor for different channel loss conditions. The insertion loss (IL) in these plots refers to the total loss between the link partner transmitter and the DS250DF810 receiver.

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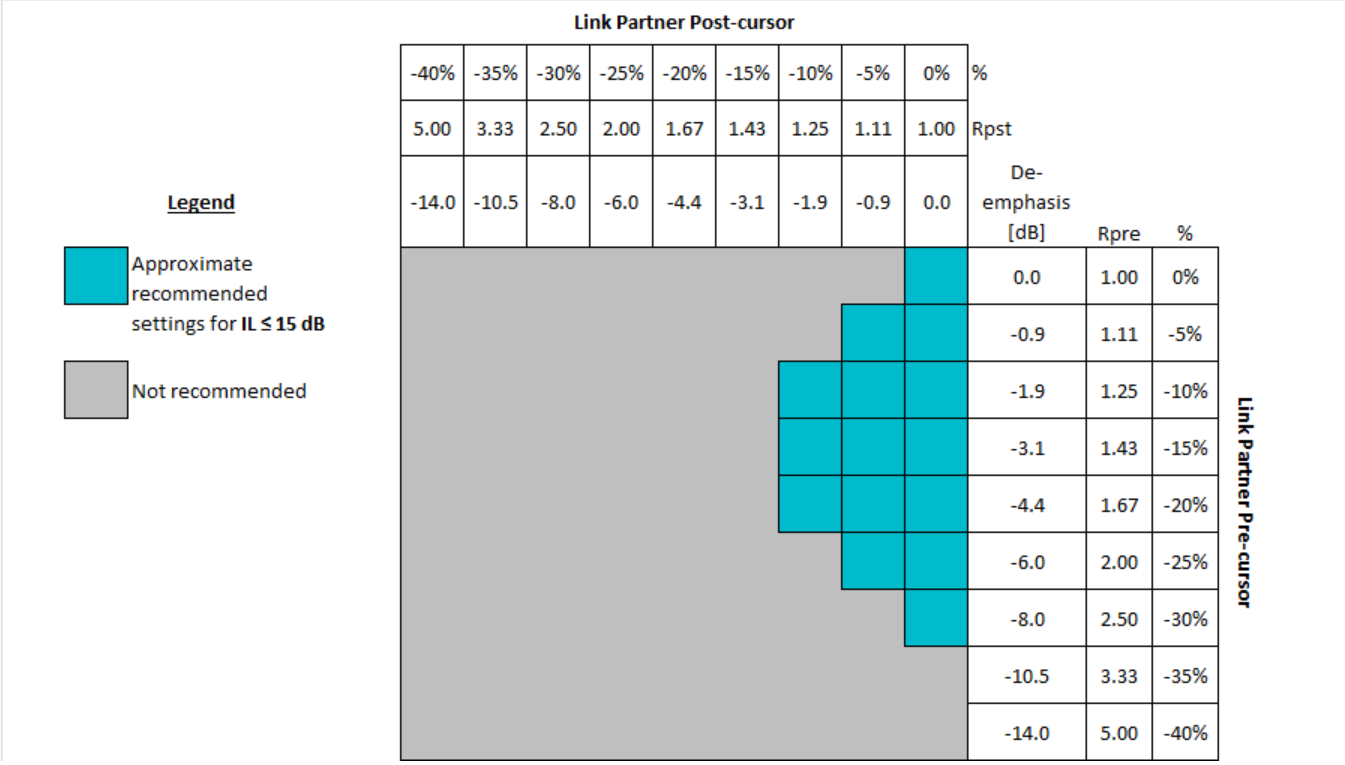


Figure 11. Guideline for link partner FIR settings when IL ≤ 15dB

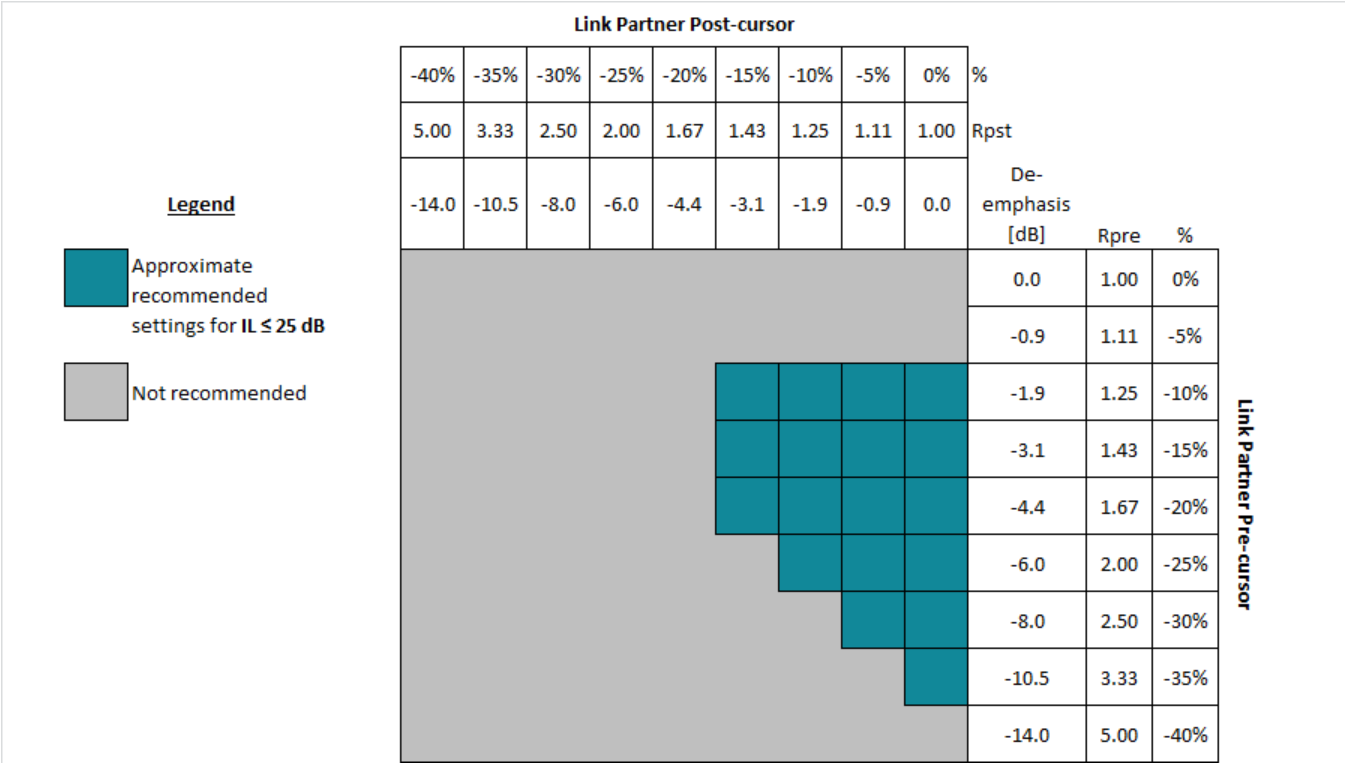


Figure 12. Guideline for link partner FIR settings when IL ≤ 25dB

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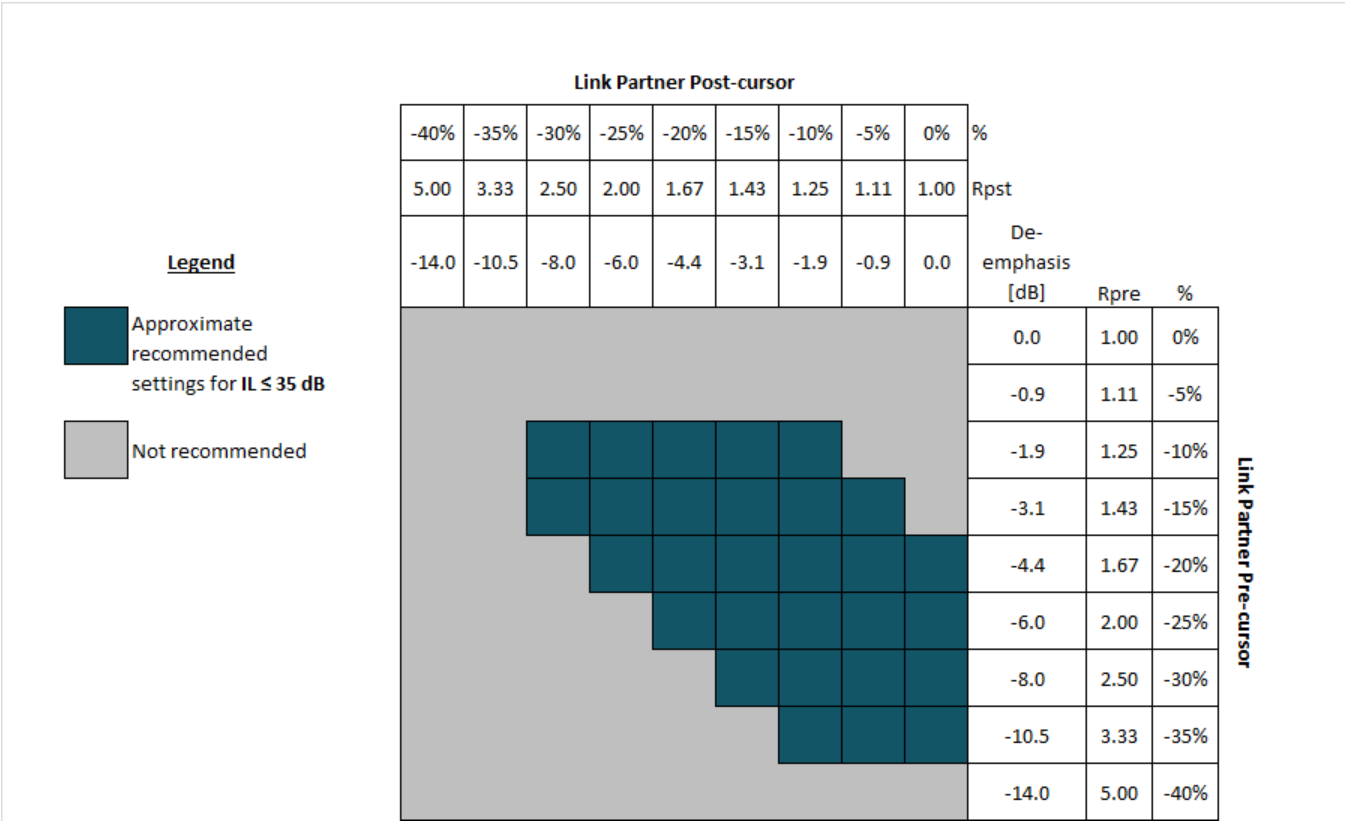


Figure 13. Guideline for link partner FIR settings when IL ≤ 35dB

9.3.12 Output Driver Polarity Inversion

In some applications, it may be necessary to invert the polarity of the data transmitted from the retimer. To invert the polarity of the data, read back the FIR polarity settings for the pre, main and post cursor taps and then invert these bits.

9.3.13 Debug Features

9.3.13.1 Pattern Generator

Each channel in the DS250DF810 can be configured to generate a 16-bit user-defined data pattern or a pseudo random bit sequence (PRBS). The user defined pattern can also be set to automatically invert every other 16-bit symbol for DC balancing purposes. The DS250DF810 pattern generator supports the following PRBS sequences:

- PRBS – 2^7 - 1
- PRBS – 2^9 - 1
- PRBS – 2^{11} - 1
- PRBS – 2^{15} - 1
- PRBS – 2^{23} - 1
- PRBS – 2^{31} - 1
- PRBS – 2^{58} - 1
- PRBS – 2^{63} - 1

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9.3.13.2 Pattern Checker

The pattern checker can be manually set to look for specific PRBS sequences and polarities or it can be set to automatically detect the incoming pattern and polarity. The PRBS checker supports the same set of PRBS patterns as the PRBS generator.

The pattern checker consists of an 11-bit error counter. The pattern checker uses 32- bit words, but every bit in the word is checked for error, so the error count represents the count of single bit errors.

In order to read out the bit and error counters, the pattern checker must first be frozen. Continuous operation with simultaneous read out of the bit and error counters is not supported in this implementation. Once the bit and error counter is read, they can be un-frozen to continue counting.

9.3.13.3 Eye Opening Monitor

The DS250DF810's Eye Opening Monitor (EOM) measures the internal data eye at the input of the decision slicer and can be used for 2 functions:

1. Horizontal Eye Opening (HEO) and Vertical Eye Opening (VEO) measurement
2. Full Eye Diagram Capture

The HEO measurement is made at the 0V crossing and is read in channel register 0x27. The VEO measurement is made at the 0.5 UI mark and is read in channel register 0x28. The HEO and VEO registers can be read from channel registers 0x27 and 0x28 at any time while the CDR is locked. The following equations are used to convert the contents of channel registers 0x27 and 0x28 into their appropriate units:

- HEO [UI] = ch reg 0x27 ÷ 32
- VEO [mV] = ch reg 0x28 x 3.125

A full eye diagram capture can be performed when the CDR is locked. The eye diagram is constructed within a 64 x 64 array, where each cell in the matrix consists of an 16-bit word representing the total number of hits recorded at that particular phase and voltage offset. Users can manually adjust the vertical scaling of the EOM or allow the state machine to control the scaling which is the default option. The horizontal scaling controlled by the state machine and is always directly proportional to the data rate.

When a full eye diagram plot is captured, the retimer will shift out four 16-bit words of junk data that should be discarded followed by 4096 16-bit words that make up the 64 × 64 eye plot. The first actual word of the eye plot from the retimer is for (X, Y) position (0,0), which is the earliest position in time and the most negative position in voltage. Each time the eye plot data is read out the voltage position is incremented. Once the voltage position has incremented to position 63 (the most positive voltage), the next read will cause the voltage position to reset to 0 (the most negative voltage) and the phase position to increment. This process will continue until the entire 64 × 64 matrix is read out. Figure 14 below shows the EOM read out sequence overlaid on top of a simple eye opening plot. In this plot any hits are shown in green. This type of plot is helpful for quickly visualizing the HEO and VEO. Users can apply different algorithms to the output data to plot density or color gradients to the output data.

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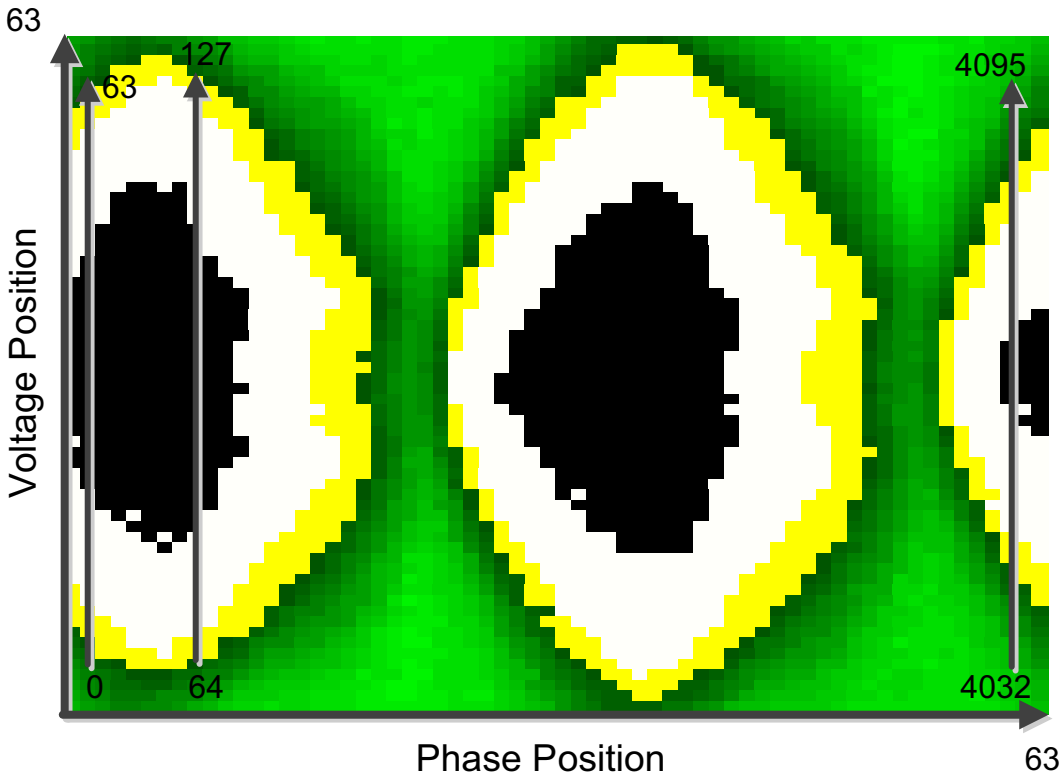


Figure 14. EOM Full Eye Capture Readout

To manually control the EOM vertical range, remove scaling control from the state machine then select the desired range:

Channel Reg 0x2C[6] → 0 (see Table 3).

Table 3. Eye Opening Monitor Vertical Range Settings

CH REG 0x11[7:6] VALUE	EOM VERTICAL RANGE [mV]
2'b00	±100
2'b01	±200
2'b10	±300
2'b11	±400

The EOM operates as an under-sampled circuit. This allows the EOM to be useful in identifying over equalization, ringing and other gross signal conditioning issues. However, the EOM cannot be correlated to a bit error rate.

The EOM can be accessed in two ways to read out the entire eye plot:

- Multi-byte reads can be used such that data is repeatedly latched out from channel register 0x25.
- With single byte reads, the MSB are located in register 0x25 and the LSB are located in register 0x26. In this mode, the device must be addressed each time a new byte is read.

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To perform a full eye capture with the EOM, follow these steps below within the desired channel register set:

Table 4. Eye Opening Monitor Full Eye Capture Instructions

STEP	REGISTER [bits]	OPERATION	VALUE	DESCRIPTION
1	0x67[5]	Write	0	Disable lock EOM lock monitoring
2	0x2C[6]	Write	0	Set the desired EOM vertical range
	0x11[7:6]	Write	2'b--	
3	0x11[5]	Write	0	Power on the EOM
4	0x24[7]	Write	1	Enable fast EOM
5	0x24[0] 0x25 0x26	Read	1	Begin read out of the 64 x 64 array, discard first 4 words Ch reg 0x24[0] is self-clearing.
				0x25 is the MSB of the 16-bit word
				0x26 is the LSB of the 16-bit word
6	0x25	Read		Continue reading information until the 64 x 64 array is complete.
	0x26			
7	0x67[5]	Write	1	Return the EOM to its original state. Undo steps 1-4
	0x2C[6]	Write	1	
	0x11[5]	Write	1	
	0x24[7,1]	Write	0	

9.3.14 Interrupt Signals

The DS250DF810 can be configured to report different events as interrupt signals. These interrupt signals do not impact the operation of the device, but merely report that the selected event has occurred. The interrupt bits in the register sets are all sticky bits. This means that when an event triggers an interrupt the status bit for that interrupt is set to logic HIGH. This interrupt status bit will remain at logic HIGH until the bit has been read. Once the bit has been read it will be automatically cleared, which allows for new interrupts to be detected. The DS250DF810 will report the occurrence of an interrupt through the INT_N pin. The INT_N pin is an open drain output that will pull the line low when an interrupt signal is triggered.

Note that all available interrupts are disabled by default. Users must activate the various interrupts before they can be used.

The interrupts available in the DS250DF810 are:

- CDR loss of lock
- CDR locked
- Signal detect loss
- Signal detected
- PRBS pattern checker bit error detected
- HEO/VEO threshold violation

When an interrupt occurs, share register 0x08 reports which channel generated the interrupt request. Users can then select the channel(s) that generated the interrupt request and service the interrupt by reading the appropriate interrupt status bits in the corresponding channel registers. For more information on reading interrupt status, refer to the DS250DF810 Programming Guide.

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9.4 Device Functional Modes

9.4.1 Supported Data Rates

The DS250DF810 supports a wide range of input data rates, including divide-by-2 and divide-by-4 sub-rates. The supported data rates are listed in Table 5. Refer to the DS250DF810 Programming Guide for information on configuring the DS250DF810 for different data rates.

Table 5. Supported Data Rates

DATA RATE RANGE		DIVIDER	CDR MODE	COMMENT
MIN	MAX			
≥ 20.2752 Gbps	≤ 25.8 Gbps	1	Enabled	
≥ 10.1376 Gbps	≤ 12.9 Gbps	2	Enabled	
> 6.45 Gbps	< 10.3 Gbps	N/A	Disabled	Output jitter will be higher with CDR disabled.
≥ 5.0688 Gbps	≤ 6.45 Gbps	4	Enabled	
≥ 1.25 Gbps	< 5.15 Gbps	N/A	Disabled	Output jitter will be higher with CDR disabled.

9.4.2 SMBus Master Mode

SMBus master mode allows the DS250DF810 to program itself by reading directly from an external EEPROM. When using the SMBus master mode, the DS25DF810 will read directly from specific location in the external EEPROM. When designing a system for using the external EEPROM, the user needs to follow these specific guidelines:

- Maximum EEPROM size is 2048 Bytes
- Minimum EEPROM size for a single DS250DF810 with individual channel configuration is 595 Bytes (3 base header bytes + 12 address map bytes + 8 x 72 channel register bytes + 2x2 share register bytes; bytes are defined to be 8-bits)
- Set ENSMB = Float, for SMBus master mode
- The external EEPROM device address byte must be 0xA0
- The external EEPROM device must support 400kHz operation at 2.5V or 3.3V supply
- Set the SMBus address of the DS250DF810 by configuring the ADDR0 and ADDR1 pins

When loading multiple DS250DF810 devices from the same EEPROM, use these guidelines to configure the devices:

- Configure the SMBus addresses for each DS250DF810 to be sequential. The first device in the sequence must have an address of 0x30
- Daisy chain READ_EN_N and ALL_DONE_N from one device to the next device in the sequence so that they do not compete for the EEPROM at the same time.
- If all of the DS250DF810 devices share the same EEPROM channel and share register settings, configure the common channel bit in the base header to 1. With common channel configuration enabled, each DS250DF810 device will configure all 8 channels with the same settings.

When loading a single DS250DF810 from an EEPROM, use these guidelines to configure the device:

- Set the common channel bit to 0 to allow for individual channel configuration, or set the common channel bit to 1 to load the same configuration settings to all channels.
- When configuring individual channels, a 1024 or 2048 Byte EEPROM must be used.
- If there are more than three DS250DF810 devices on a PCB that require individual channel configuration, then each device must have its own EEPROM.

9.4.3 Device SMBus Address

The DS250DF810's SMBus slave address is strapped at power up using the ADDR[1:0] pins. The pin state is read on power up, after the internal power-on reset signal is de-asserted. The ADDR[1:0] pins are four-level LVCMOS IOs, which provides for 16 unique SMBus addresses. The four levels are achieved by pin strap options as follows:

- 0: 1 kΩ to GND

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- R: 10 kΩ to GND
- F: Float
- 1: 1 kΩ to VDD

Table 6. SMBus Address Map

8-BIT WRITE ADDRESS [HEX]	REQUIRED ADDRESS PIN STRAP VALUE	
	ADDR1	ADDR0
0x30	0	0
0x32	0	R
0x34	0	F
0x36	0	1
0x38	R	0
0x3A	R	R
0x3C	R	F
0x3E	R	1
0x40	F	0
0x42	F	R
0x44	F	F
0x46	F	1
0x48	1	0
0x4A	1	R
0x4C	1	F
0x4E	1	1

9.5 Programming

9.5.1 Bit Fields in the Register Set

Many of the registers in the DS250DF810 are divided into bit fields. This allows a single register to serve multiple purposes which may be unrelated. Often, configuring the DS250DF810 requires writing a bit field that makes up only part of a register value while leaving the remainder of the register value unchanged. The procedure for accomplishing this task is to read in the current value of the register to be written, modify only the desired bits in this value, and write the modified value back to the register. Of course, if the entire register is to be changed, rather than just a bit field within the register, it is not necessary to read in the current value of the register first. In all register configuration procedures described in the following sections, this procedure should be kept in mind. In some cases, the entire register is to be modified. When only a part of the register is to be changed, however, the procedure described above should be used.

Most register bits can be read or written to. However, some register bits are constrained to specific interface instructions.

Register bits can have the following interface constraints:

- R - Read only
- RW - Read/Write
- RWSC - Read/Write, self-clearing

9.5.2 Writing to and Reading from the Global/Shared/Channel Registers

The DS250DF810 has 3 types of registers:

1) Global Registers – These registers can be accessed at any time and are used to select individual channel registers, the shared registers or to read back the TI ID and version information.

2) Shared Registers – These registers are used for device-level configuration, status read back or control.

3) Channel Registers – These registers are used to control and configure specific features for each individual channel. All channels have the same channel register set and can be configured independent of each other.

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Programming (continued)

The global registers can be accessed at any time, regardless of whether the shared or channel register set is selected. The DS250DF1810 global registers are located on addresses 0xEF-0xFF. The function of the global registers falls into the following categories:

- Channel selection and share enabling – Registers 0xFC and 0xFF
- Device and version information – Registers 0xEF-0xF3
- Reserved/unused registers – all other addresses

Register 0xFF[5:4] is used to select the share registers of either Quad 0 (channels 0-3) or Quad 1 (channels 4-7).

Register 0xFC is used to select the channel registers to be written to. To select a channel, write a 1 to its corresponding bit in register 0xFC. Note that more than one channel may be written to by setting multiple bits in register 0xFC. However, when performing an SMBus read transaction only one channel can be selected at a time. If multiple channels are selected when attempting to perform an SMBus read, the device will return 0x00.

Register 0xFF bit 1 can be used to perform broadcast register writes to all channels. A single channel read-modify broadcast write type commands can be accomplished by setting register 0xFF to 0x03 and selecting a single channel in register 0xFC. This type of configuration allows for the reading of a single channel's register information and then writing to all channels with the modified value. Register 0xFF bit 0 is used to select the shared register page or the channel register page for the channels selected in register 0xFC.

TI repeaters/retimers have a vendor ID register (0xFE) which will always read back 0x03. In addition, there are three device ID registers (0xF0, 0xF1, and 0xF3). These are useful to verify that there is a good SMBus connection between the SMBus master and the DS250DF810.

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9.6 Register Maps

Table 7. Global Registers

ADDRESS (HEX)	BITS	DEFAULT VALUE (HEX)	MODE	EEPROM	FIELD NAME	DESCRIPTION
EF	7	0	R	N	SPARE	
	6	0	R	N	SPARE	
	5	0	R	N	SPARE	
	4	0	R	N	SPARE	
	3	1	R	N	CHAN_CONFIG_ID[3]	
	2	1	R	N	CHAN_CONFIG_ID[2]	
	1	0	R	N	CHAN_CONFIG_ID[1]	
	0	0	R	N	CHAN_CONFIG_ID[0]	
F0	7	0	R	N	VERSION[7]	
	6	0	R	N	VERSION[6]	
	5	1	R	N	VERSION[5]	
	4	1	R	N	VERSION[4]	
	3	0	R	N	VERSION[3]	
	2	0	R	N	VERSION[2]	
	1	1	R	N	VERSION[1]	
	0	0	R	N	VERSION[0]	
F1	7	0	R	N	DEVICE_ID[7]	Full device ID
	6	0	R	N	DEVICE_ID[6]	
	5	0	R	N	DEVICE_ID[5]	
	4	1	R	N	DEVICE_ID[4]	
	3	0	R	N	DEVICE_ID[3]	
	2	0	R	N	DEVICE_ID[2]	
	1	0	R	N	DEVICE_ID[1]	
	0	0	R	N	DEVICE_ID[0]	
F3	7	0	R	N	CHAN_VERSION[3]	Digital Channel Version
	6	0	R	N	CHAN_VERSION[2]	
	5	0	R	N	CHAN_VERSION[1]	
	4	0	R	N	CHAN_VERSION[0]	
	3	0	R	N	SHARE_VERSION[3]	Digital Share Version
	2	0	R	N	SHARE_VERSION[2]	
	1	0	R	N	SHARE_VERSION[1]	
	0	0	R	N	SHARE_VERSION[0]	
FB	7	0	RW	N	RESERVED	
	6	0	RW	N	RESERVED	
	5	0	RW	N	RESERVED	
	4	0	RW	N	RESERVED	
	3	0	RW	N	RESERVED	
	2	1	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	0	RW	N	RESERVED	
FC	7	0	RW	N	EN_CH7	Select channel 7
	6	0	RW	N	EN_CH6	Select channel 6
	5	0	RW	N	EN_CH5	Select channel 5
	4	0	RW	N	EN_CH4	Select channel 4

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Register Maps (continued)

Table 7. Global Registers (continued)

ADDRESS (HEX)	BITS	DEFAULT VALUE (HEX)	MODE	EEPROM	FIELD NAME	DESCRIPTION
	3	0	RW	N	EN_CH3	Select channel 3
	2	0	RW	N	EN_CH2	Select channel 2
	1	0	RW	N	EN_CH1	Select channel 1
	0	0	RW	N	EN_CH0	Select channel 0
FD	7	0	RW	N	RESERVED	
	6	0	RW	N	RESERVED	
	5	0	RW	N	RESERVED	
	4	0	RW	N	RESERVED	
	3	0	RW	N	RESERVED	
	2	0	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	0	RW	N	RESERVED	
FE	7	0	R	N	VENDOR_ID[7]	TI vendor ID
	6	0	R	N	VENDOR_ID[6]	
	5	0	R	N	VENDOR_ID[5]	
	4	0	R	N	VENDOR_ID[4]	
	3	0	R	N	VENDOR_ID[3]	
	2	0	R	N	VENDOR_ID[2]	
	1	1	R	N	VENDOR_ID[1]	
	0	1	R	N	VENDOR_ID[0]	
FF	7	0	RW	N	RESERVED	
	6	0	RW	N	RESERVED	
	5	1	RW	N	EN_SHARE_Q1	Select shared registers for quad 1
	4	0	RW	N	EN_SHARE_Q0	Select shared registers for quad 0
	3	0	RW	N	RESERVED	
	2	0	RW	N	RESERVED	
	1	0	RW	N	WRITE_ALL_CH	Allows customer to write to all channels as if they are the same, but only allows read back from the channel specified in 0xFC and 0xFD. Note: en_ch_SMB must be = 1 or else this function is invalid.
	0	0	RW	N	EN_CH_SMB	1: Enables SMBUS access to the channels specified in register 0xFC 0: The shared registers are selected, see 0xFF[5:4]

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Table 8. Shared Registers

ADDRESS (HEX)	BITS	DEFAULT VALUE (HEX)	MODE	EEPROM	FIELD NAME	DESCRIPTION
0	7	1	R	N	SMBus_Addr3	SMBus Address
	6	1	R	N	SMBus_Addr2	Strapped 7-bit addres is 0x18 + SMBus_Addr[3:0]
	5	0	R	N	SMBus_Addr1	
	4	0	R	N	SMBus_Addr0	
	3:0	0			RESERVED	
1	7	1	R	N	RESERVED	
	6	0	R	N	RESERVED	
	5	1	R	N	RESERVED	
	4	1	R	N	RESERVED	
	3	0	R	N	RESERVED	
	2	0	R	N	RESERVED	
	1	0	R	N	RESERVED	
	0	1	R	N	RESERVED	
2	7:0	0	RW	N	RESERVED	
3	7:0	0	RW	N	RESERVED	
4	7	0	RW	N	RESERVED	
	6	0	RW	N	RST_SMB_REGS	1: Resets share registers.
	5	0	RWSC	N	RST_SMB_MAS	1: Reset for SMBus Master Mode
	4	0	RW	N	rc_eeprm_rd	1: Force EEPROM Configuration
	3	1	RW	Y	RESERVED	
	2	0	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	1	RW	N	RESERVED	
5	7	0	RW	N	disab_eeprm_cfg	Disable Master Mode EEPROM Configuration
	6:5	0	RW	N	RESERVED	
	4	1	R	N	EEPROM_READ_DONE	This bit is set to 1 when read from EEPROM is done
	3	0	RW	N	RESERVED	
	2	0	RW	Y	RESERVED	
	1	0	RW	Y	RESERVED	
	0	1	RW	Y	RESERVED	
6	7:0	0	RW	N	RESERVED	
8	7	0	R	N	RESERVED	
	6	0	R	N	RESERVED	
	5	0	R	N	RESERVED	
	4	0	R	N	RESERVED	
	3	0	R	N	int_q0c3	Interrupt from channel3 of quad0
	2	0	R	N	int_q0c2	Interrupt from channel2 of quad0
	1	0	R	N	int_q0c1	Interrupt from channel1 of quad0
	0	0	R	N	int_q0c0	Interrupt from channel0 of quad0
A	7:1	0	R	Y	RESERVED	
	0	0	RW	Y	dis_refclk_out	1: Disable REFCLK_OUT (high-Z) 0: Enable REFCLK_OUT
B	7	0	RW	N	RESERVED	

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Table 8. Shared Registers (continued)

ADDRESS (HEX)	BITS	DEFAULT VALUE (HEX)	MODE	EEPROM	FIELD NAME	DESCRIPTION
	6	0	R	N	refclk_det	High level when ref_clk has been detected
	5	0	RW	N	RESERVED	
	4	0	RW	N	RESERVED	
	3	0	RW	N	mr_refclk_det_dis	
	2	0	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	0	RW	N	RESERVED	
C	7:0	0	RW	N	RESERVED	
D	7:0	0	R	N	RESERVED	
E	7:2	0	RW	N	RESERVED	
	1:0	0	R	N	RESERVED	
F	7:0	0	RW	N	RESERVED	
10	7	1	RW	N	RESERVED	
	6	1	RW	N	RESERVED	
	5	1	RW	N	RESERVED	
	4	1	RW	N	RESERVED	
	3	1	RW	Y	RESERVED	
	2	1	RW	Y	RESERVED	
	1	1	RW	Y	RESERVED	
	0	1	RW	Y	RESERVED	
11	7	0	R	N	eecfg_cmplt	11: Not valid 10: EEPROM load completed successfully 01: EEPROM load failed after 64 attempts 00: EEPROM load in progress
	6	0	R	N	eecfg_fail	
	5	0	R	N	eecfg_atmpt[5]	Number of attempts made to load EEPROM image
	4	0	R	N	eecfg_atmpt[4]	
	3	0	R	N	eecfg_atmpt[3]	
	2	0	R	N	eecfg_atmpt[2]	
	1	0	R	N	eecfg_atmpt[1]	
	0	0	R	N	eecfg_atmpt[0]	
12	7	1	RW	N	reg_i2c_fast	1: EEPROM load uses Fast I2C Mode (400 kHz) 0: EEPROM load uses Standard I2C Mode (100 kHz)
	6	0	RW	N	RESERVED	
	5	0	RW	N	RESERVED	
	4	1	RW	N	RESERVED	
	3	0	RW	N	RESERVED	
	2	0	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	1	RW	N	RESERVED	

Table 9. Channel Select Global Register Definition

ADDRESS (HEX)	BITS	DESCRIPTION
0xFC	7	Select register set for channel 7

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Table 9. Channel Select Global Register Definition (continued)

ADDRESS (HEX)	BITS	DESCRIPTION
	6	Select register set for channel 6
	5	Select register set for channel 5
	4	Select register set for channel 4
	3	Select register set for channel 3
	2	Select register set for channel 2
	1	Select register set for channel 1
	0	Select register set for channel 0

Table 10. Device/Vendor ID Global Register Definition

ADDRESS (HEX)	BITS	DESCRIPTION
0xF0		TI Device ID. Contains 0x32.
0xF1		TI Device ID. Contains 0x10.
0xF3		TI Device ID. Contains 0x00.
0xFE		TI Vendor ID. Read-only register. Contains value 0x03.

Table 11. Register Page Select Definition

ADDRESS (HEX)	BITS	DESCRIPTION
0xFF	5	1: Selects shared registers for channels 4 -7 0: Normal operation
	4	1: Selects shared registers for channels 0-3 0: Normal operation
	1	1: Broadcast write to all channels, 0xFF[0] must be set to 1. Select a single channel in 0xFC. 0: Normal operation, select channel register as defined in 0xFC.
	0	1: Select Channel Registers 0: Select Share Registers

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Table 12. Channel Registers, 0 to 39

ADDRESS (HEX)	BITS	DEFAULT VALUE (HEX)	MODE	EEPROM	FIELD NAME	DESCRIPTION
0	7	0	RW	N	RESERVED	RESERVED
	6	0	RW	N	RESERVED	RESERVED
	5	0	RW	N	RESERVED	RESERVED
	4	0	RW	N	RESERVED	RESERVED
	3	0	RW	N	RST_CORE	1: Reset the 10M core clock domain. This is the main clock domain for all the state machines 0: Normal operation
	2	0	RW	N	RST_REGS	1: Reset channel registers to power-up defaults. 0: Normal operation
	1	0	RW	N	RST_VCO	1: Resets the CDR S2P clock domain, includes PPM counter, EOM counter. 0: Normal operation
	0	0	RW	N	RST_REFCLK	1: Resets the 25MHz reference clock domain, includes PPM counter. Does not work if 25MHz clock is not present. 0: Normal operation
1	7	0	R	N	sigdet	Raw Signal Detect observation
	6	0	R	N	pol_inv_det	Indicates PRBS checker detected polarity inversion in the locked data sequence.
	5	0	R	N	CDR_LOCK_LOSS_INT	1: Indicates loss of CDR lock after having acquired it. Bit clears on read. Feature must be enabled with reg_31[1]
	4	0	R	N	prbs_seq_det[3]	Indicates the pattern detected on the input serial stream
	3	0	R	N	prbs_seq_det[2]	0xxx: No detect 1000: 7 bits PRBS sequence 1001: 9 bits PRBS sequence 1010: 11 bits PRBS sequence 1011: 15 bits PRBS sequence 1100: 23 bits PRBS sequence 1101: 31 bits PRBS sequence 1110: 58 bits PRBS sequence 1111: 63 bits PRBS sequence
	2	0	R	N	prbs_seq_det[1]	
	1	0	R	N	prbs_seq_det[0]	
	0	0	R	N	SIG_DET_LOSS_INT	Loss of signal indicator, set once signal is acquired and then lost. Clears on read. Feature must be enabled with reg_31[0]
2	7	0	R	N	CDR_STATUS[7]	"This register is used to read the status of internal signal. Select what is observable on this bus using Reg_0x0C[7:4]"
	6	0	R	N	CDR_STATUS[6]	
	5	0	R	N	CDR_STATUS[5]	
	4	0	R	N	CDR_STATUS[4]	
	3	0	R	N	CDR_STATUS[3]	
	2	0	R	N	CDR_STATUS[2]	
	1	0	R	N	CDR_STATUS[1]	
	0	0	R	N	CDR_STATUS[0]	

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Table 12. Channel Registers, 0 to 39 (continued)

ADDRESS (HEX)	BITS	DEFAULT VALUE (HEX)	MODE	EEPROM	FIELD NAME	DESCRIPTION
3	7	0	RW	Y	EQ_BST0[1]	This register can be used to force an EQ boost setting if used in conjunction with channel register 0x2D[3].
	6	0	RW	Y	EQ_BST0[0]	
	5	0	RW	Y	EQ_BST1[1]	
	4	0	RW	Y	EQ_BST1[0]	
	3	0	RW	Y	EQ_BST2[1]	
	2	0	RW	Y	EQ_BST2[0]	
	1	0	RW	Y	EQ_BST3[1]	
	0	0	RW	Y	EQ_BST3[0]	
4	7	0	RW	N	RESERVED	RESERVED
	6	0	RW	N	RESERVED	RESERVED
	5	0	RW	N	RESERVED	RESERVED
	4	0	RW	N	RESERVED	RESERVED
	3	0	RW	N	RESERVED	RESERVED
	2	0	RW	N	RESERVED	RESERVED
	1	0	RW	N	RESERVED	RESERVED
	0	1	RW	N	RESERVED	RESERVED
5	7	0	RW	N	RESERVED	RESERVED
	6	0	RW	N	RESERVED	RESERVED
	5	0	RW	N	RESERVED	RESERVED
	4	0	RW	N	RESERVED	RESERVED
	3	0	RW	N	RESERVED	RESERVED
	2	0	RW	N	RESERVED	RESERVED
	1	0	RW	N	RESERVED	RESERVED
	0	1	RW	N	RESERVED	RESERVED
6	7	0	RW	N	RESERVED	RESERVED
	6	0	RW	N	RESERVED	RESERVED
	5	0	RW	N	RESERVED	RESERVED
	4	0	RW	N	RESERVED	RESERVED
	3	0	RW	N	RESERVED	RESERVED
	2	0	RW	N	RESERVED	RESERVED
	1	0	RW	N	RESERVED	RESERVED
	0	1	RW	N	RESERVED	RESERVED
7	7	0	RW	N	RESERVED	RESERVED
	6	0	RW	N	RESERVED	RESERVED
	5	0	RW	N	RESERVED	RESERVED
	4	0	RW	N	RESERVED	RESERVED
	3	0	RW	N	RESERVED	RESERVED
	2	0	RW	N	RESERVED	RESERVED
	1	0	RW	N	RESERVED	RESERVED
	0	1	RW	N	RESERVED	RESERVED

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Table 12. Channel Registers, 0 to 39 (continued)

ADDRESS (HEX)	BITS	DEFAULT VALUE (HEX)	MODE	EEPROM	FIELD NAME	DESCRIPTION
8	7	0	RW	Y	RESERVED	RESERVED
	6	1	RW	Y	RESERVED	RESERVED
	5	1	RW	Y	RESERVED	RESERVED
	4	1	RW	Y	RESERVED	RESERVED
	3	0	RW	Y	RESERVED	RESERVED
	2	0	RW	Y	RESERVED	RESERVED
	1	1	RW	Y	RESERVED	RESERVED
	0	1	RW	Y	RESERVED	RESERVED
9	7	0	RW	Y	REG_VCO_CAP_OV	Enable bit to override cap_cnt with value in register and 0B[4:0]
	6	0	RW	Y	REG_SET_CP_LVL_LPF_OV	Enable bit to override lpf_dac_val with value in register 1F[4:0]
	5	0	RW	Y	REG_BYPASS_PFD_OV	Enable bit to override sel_retimedD_loopthru and sel_rawD_loopthru with values in reg1E[7:5]
	4	0	RW	Y	REG_EN_FD_PD_VCO_PDIQ_OV	Enable bit to override en_fd, pd_pd, pd_vco, pd_pdiq with reg1E[0], reg1E[2], reg1C[0], reg1C[1]
	3	0	RW	Y	REG_EN_PD_CP_OV	Enable bit to override pd_fd_cp and pd_pd_cp with value in register 1B[1:0]
	2	0	RW	Y	REG_DIVSEL_OV	Enable bit to override divsel with value in register 18[6:4]
	1	0	RW	Y	RESERVED	RESERVED
	0	0	RW	Y	REG_PFD_LOCK_MODE_SM	Enable fd in lock state
A	7	0	RW	Y	RESERVED	RESERVED
	6	0	RW	Y	REG_EN_IDAC_PD_CP_OV AND_REG_EN_IDAC_FD_CP_OV	Enable bit to override phase detector charge pump settings with reg1C[7:5] Enable bit to override frequency detector charge pump settings with reg1C[4:2]"
	5	0	RW	Y	REG_DAC_LPF_HIGH_PHASE_OV _AND_REG_DAC_LPF_LOW_PHASE_OV	Enable bit to loop filter comparator trip voltages with reg16[7:0]
	4	0	RW	Y	RESERVED	RESERVED
	3	0	RW	N	REG_CDR_RESET_OV	Enable CDR Reset override with reg0A[2]
	2	0	RW	N	REG_CDR_RESET_SM	CDR Reset override bit
	1	0	RW	N	REG_CDR_LOCK_OV	Enable CDR lock signal override with reg0A[0]
	0	0	RW	N	REG_CDR_LOCK	CDR lock signal override bit
B	7	0	RW	Y	RESERVED	RESERVED
	6	1	RW	Y	RESERVED	RESERVED
	5	1	RW	Y	RESERVED	RESERVED
	4	0	RW	Y	RESERVED	RESERVED
	3	0	RW	Y	RESERVED	RESERVED
	2	0	RW	Y	RESERVED	RESERVED
	1	1	RW	Y	RESERVED	RESERVED
	0	1	RW	Y	RESERVED	RESERVED

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Table 12. Channel Registers, 0 to 39 (continued)

ADDRESS (HEX)	BITS	DEFAULT VALUE (HEX)	MODE	EEPROM	FIELD NAME	DESCRIPTION
C	7	0	RW	N	RESERVED	RESERVED
	6	0	RW	N	RESERVED	RESERVED
	5	0	RW	N	RESERVED	RESERVED
	4	0	RW	N	RESERVED	RESERVED
	3	0	RW	N	RESERVED	RESERVED
	2	0	RW	N	RESERVED	RESERVED
	1	0	RW	N	RESERVED	RESERVED
	0	0	RW	N	RESERVED	RESERVED
D	7	1	RW	N	DES_PD	"1: De-serializer (for PRBS checker) is powered down 0: De-serializer (for PRBS checker) is enabled"
	6	0	RW	N	RESERVED	RESERVED
	5	0	RW	Y	RESERVED	RESERVED
	4	0	RW	Y	RESERVED	RESERVED
	3	0	RW	Y	RESERVED	RESERVED
	2	0	RW	Y	RESERVED	RESERVED
	1	0	RW	N	RESERVED	RESERVED
	0	0	RW	N	RESERVED	RESERVED
E	7	1	RW	N	RESERVED	RESERVED
	6	0	RW	N	RESERVED	RESERVED
	5	0	RW	N	RESERVED	RESERVED
	4	1	RW	N	RESERVED	RESERVED
	3	0	RW	N	RESERVED	RESERVED
	2	0	RW	N	RESERVED	RESERVED
	1	1	RW	N	RESERVED	RESERVED
	0	1	RW	N	RESERVED	RESERVED
F	7	0	RW	N	RESERVED	RESERVED
	6	1	RW	N	RESERVED	RESERVED
	5	1	RW	N	RESERVED	RESERVED
	4	0	RW	N	RESERVED	RESERVED
	3	1	RW	N	RESERVED	RESERVED
	2	0	RW	N	RESERVED	RESERVED
	1	0	RW	N	RESERVED	RESERVED
	0	1	RW	N	RESERVED	RESERVED
10	7	0	RW	N	RESERVED	RESERVED
	6	0	RW	N	RESERVED	RESERVED
	5	0	RW	N	RESERVED	RESERVED
	4	0	RW	N	RESERVED	RESERVED
	3	0	RW	N	RESERVED	RESERVED
	2	0	RW	N	RESERVED	RESERVED
	1	0	RW	N	RESERVED	RESERVED
	0	0	RW	N	RESERVED	RESERVED

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Table 12. Channel Registers, 0 to 39 (continued)

ADDRESS (HEX)	BITS	DEFAULT VALUE (HEX)	MODE	EEPROM	FIELD NAME	DESCRIPTION
11	7	0	RW	Y	EOM_SEL_VRANGE[1]	Manually set the EOM vertical range, used with channel register 0x2C[6]: 00: ±100 mV 01: ±200 mV 10: ±300 mV 11: ±400 mV
	6	0	RW	Y	EOM_SEL_VRANGE[0]	
	5	1	RW	Y	EOM_PD	1: Normal operation
	4	0	RW	N	RESERVED	
	3	0	RW	Y	DFE_TAP2_POL	Bit forces DFE tap 2 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	2	0	RW	Y	DFE_TAP3_POL	Bit forces DFE tap 3 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	1	0	RW	Y	DFE_TAP4_POL	Bit forces DFE tap 4 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	0	0	RW	Y	DFE_TAP5_POL	Bit forces DFE tap 5 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
12	7	1	RW	Y	DFE_TAP1_POL	Bit forces DFE tap 1 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	6	0	RW	N	RESERVED	
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	DFE_WT1[4]	Bits force DFE tap 1 weight. Manual DFE operation required to take effect by setting 0x15[7]=1.
	3	0	RW	Y	DFE_WT1[3]	
	2	0	RW	Y	DFE_WT1[2]	
	1	1	RW	Y	DFE_WT1[1]	
	0	1	RW	Y	DFE_WT1[0]	
13	7	1	RW	N	eq_PD_PeakDetect	
	6	0	RW	Y	eq_PD_SD	
	5	1	RW	Y	eq_hi_gain	
	4	1	RW	Y	eq_en_dc_off	
	3	0	RW	Y	RESERVED	
	2	0	RW	Y	eq_limit_en	1: Configures the final stage of the equalizer to be a limiting stage. 0: Normal operation, final stage of the equalizer is configured to be a linear stage.
	1	0	RW	Y	RESERVED	
	0	0	RW	Y	RESERVED	

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Table 12. Channel Registers, 0 to 39 (continued)

ADDRESS (HEX)	BITS	DEFAULT VALUE (HEX)	MODE	EEPROM	FIELD NAME	DESCRIPTION
14	7	0	RW	Y	EQ_SD_PRESET	1: Forces signal detect HIGH, and force enables the channel. Should not be set if bit 6 is set. 0: Normal Operation.
	6	0	RW	Y	EQ_SD_RESET	1: Forces signal detect LOW and force disables the channel. Should not be set if bit 7 is set. 0: Normal Operation.
	5	0	RW	Y	EQ_REFA_SEL1	Controls the signal detect assert levels.
	4	0	RW	Y	EQ_REFA_SEL0	
	3	0	RW	Y	EQ_REFD_SEL1	Controls the signal detect de-assert levels.
	2	1	RW	Y	EQ_REFD_SEL0	
	1	0	RW	N	RESERVED	RESERVED
	0	0	RW	N	RESERVED	RESERVED
15	7	0	RW	Y	DFE_FORCE_EN	1: Enables manual DFE tap settings 0: Normal operation
	6	0	RW	N	RESERVED	
	5	0	RW	N	RESERVED	
	4	1	RW	Y	RESERVED	
	3	0	RW	Y	DRV_PD	1: Powers down the high speed driver 0: Normal operation
	2	0	RW	Y	RESERVED	
	1	0	RW	Y	RESERVED	
	0	0	RW	Y	RESERVED	
16	7	0	RW	Y	RESERVED	RESERVED
	6	1	RW	Y	RESERVED	RESERVED
	5	1	RW	Y	RESERVED	RESERVED
	4	1	RW	Y	RESERVED	RESERVED
	3	1	RW	Y	RESERVED	RESERVED
	2	0	RW	Y	RESERVED	RESERVED
	1	1	RW	Y	RESERVED	RESERVED
	0	0	RW	Y	RESERVED	RESERVED
17	7	0	RW	Y	RESERVED	RESERVED
	6	0	RW	Y	RESERVED	RESERVED
	5	1	RW	Y	RESERVED	RESERVED
	4	1	RW	Y	RESERVED	RESERVED
	3	0	RW	Y	RESERVED	RESERVED
	2	1	RW	Y	RESERVED	RESERVED
	1	1	RW	Y	RESERVED	RESERVED
	0	0	RW	Y	RESERVED	RESERVED

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Table 12. Channel Registers, 0 to 39 (continued)

ADDRESS (HEX)	BITS	DEFAULT VALUE (HEX)	MODE	EEPROM	FIELD NAME	DESCRIPTION
18	7	0	RW	N	RESERVED	
	6	1	RW	Y	PDIQ_SEL_DIV2	These bits will force the divider setting if 0x09[2] is set. 000: Divide by 1 001: Divide by 2 010: Divide by 4 011: Divide by 8 100: Divide by 16 All other values are reserved.
	5	0	RW	Y	PDIQ_SEL_DIV1	
	4	0	RW	Y	PDIQ_SEL_DIV0	
	3	0	RW	N	RESERVED	
	2	0	RW	Y	RESERVED	
	1	0	RW	N	RESERVED	
	0	0	RW	N	RESERVED	
19	7	0	RW	N	RESERVED	RESERVED
	6	0	RW	N	RESERVED	RESERVED
	5	1	RW	Y	RESERVED	RESERVED
	4	0	RW	Y	RESERVED	RESERVED
	3	0	RW	Y	RESERVED	RESERVED
	2	0	RW	Y	RESERVED	RESERVED
	1	0	RW	Y	RESERVED	RESERVED
	0	0	RW	Y	RESERVED	RESERVED
1A	7	0	RW	Y	RESERVED	RESERVED
	6	1	RW	Y	RESERVED	RESERVED
	5	0	RW	Y	RESERVED	RESERVED
	4	1	RW	Y	RESERVED	RESERVED
	3	1	RW	Y	RESERVED	RESERVED
	2	0	RW	Y	RESERVED	RESERVED
	1	0	RW	N	RESERVED	RESERVED
	0	0	RW	N	RESERVED	RESERVED
1B	7	0	RW	N	RESERVED	RESERVED
	6	0	RW	N	RESERVED	RESERVED
	5	0	RW	N	RESERVED	RESERVED
	4	0	RW	N	RESERVED	RESERVED
	3	0	RW	N	RESERVED	RESERVED
	2	0	RW	N	RESERVED	RESERVED
	1	1	RW	Y	CP_EN_CP_PD	1: Normal operation, phase detector charge pump enabled
	0	1	RW	Y	CP_EN_CP_FD	1: Normal operation, frequency detector charge pump enabled
1C	7	1	RW	Y	EN_IDAC_PD_CP2	Phase detector charge pump setting. Override bit required for these bits to take effect
	6	0	RW	Y	EN_IDAC_PD_CP1	
	5	0	RW	Y	EN_IDAC_PD_CP0	
	4	1	RW	Y	EN_IDAC_FD_CP2	Frequency detector charge pump setting. Override bit required for these bits to take effect
	3	0	RW	Y	EN_IDAC_FD_CP1	
	2	0	RW	Y	EN_IDAC_FD_CP0	
	1	0	RW	Y	RESERVED	RESERVED
	0	0	RW	Y	RESERVED	RESERVED

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Table 12. Channel Registers, 0 to 39 (continued)

ADDRESS (HEX)	BITS	DEFAULT VALUE (HEX)	MODE	EEPROM	FIELD NAME	DESCRIPTION
1D	7	0	RW	N	RESERVED	RESERVED
	6	0	RW	N	RESERVED	RESERVED
	5	0	RW	N	RESERVED	RESERVED
	4	0	RW	N	RESERVED	RESERVED
	3	0	RW	N	RESERVED	RESERVED
	2	0	RW	N	RESERVED	RESERVED
	1	0	RW	N	RESERVED	RESERVED
	0	0	RW	N	RESERVED	RESERVED
1E	7	1	RW	Y	PFD_SEL_DATA_MUX2	For these values to take effect, register 0x09[5] must be set to 1. 000: Raw Data* 001: Retimed Data 100: Pattern Generator 111: Mute All other values are reserved.
	6	1	RW	Y	PFD_SEL_DATA_MUX1	
	5	1	RW	Y	PFD_SEL_DATA_MUX0	
	4	0	RW	N	SER_EN	1: Enable PRBS Generator
	3	1	RW	Y	DFE_PD	This bit must be cleared for the DFE to be functional in any adapt mode. 0: DFE enabled 1: DFE disabled
	2	0	RW	Y	PFD_PD_PD	PFD phase detector power down override
	1	0	RW	Y	EN_PARTIAL_DFE	0: (Default) Disable DFE taps 3-5. 1: Enable DFE taps 3-5. DFE_PD must also be set to 0.
	0	1	RW	Y	PFD_EN_FD	PFD enable frequency detector override
1F	7	0	RW	N	RESERVED	RESERVED
	6	0	RW	N	RESERVED	RESERVED
	5	0	RW	N	RESERVED	RESERVED
	4	0	RW	Y	RESERVED	RESERVED
	3	1	RW	Y	MR_LPF_AUTO_ADJST_EN	"1: Allow LPF to tune to optimum value during fast-cap search routine 0: Otherwise LPF value is determined by the Reg_0x9D"
	2	0	RW	Y	RESERVED	RESERVED
	1	1	RW	Y	RESERVED	RESERVED
	0	1	RW	Y	RESERVED	RESERVED
20	7	0	RW	Y	DFE_WT5[3]	Bits force DFE tap 5 weight, manual DFE operation required to take effect by setting 0x15[7]=1.
	6	0	RW	Y	DFE_WT5[2]	
	5	0	RW	Y	DFE_WT5[1]	
	4	0	RW	Y	DFE_WT5[0]	
	3	0	RW	Y	DFE_WT4[3]	Bits force DFE tap 4 weight, manual DFE operation required to take effect by setting 0x15[7]=1.
	2	0	RW	Y	DFE_WT4[2]	
	1	0	RW	Y	DFE_WT4[1]	
	0	0	RW	Y	DFE_WT4[0]	

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Table 12. Channel Registers, 0 to 39 (continued)

ADDRESS (HEX)	BITS	DEFAULT VALUE (HEX)	MODE	EEPROM	FIELD NAME	DESCRIPTION
21	7	0	RW	Y	DFE_WT3[3]	Bits force DFE tap 3 weight, manual DFE operation required to take effect by setting 0x15[7]=1.
	6	0	RW	Y	DFE_WT3[2]	
	5	0	RW	Y	DFE_WT3[1]	
	4	0	RW	Y	DFE_WT3[0]	
	3	0	RW	Y	DFE_WT2[3]	Bits force DFE tap 2 weight, manual DFE operation required to take effect by setting 0x15[7]=1.
	2	0	RW	Y	DFE_WT2[2]	
	1	0	RW	Y	DFE_WT2[1]	
	0	0	RW	Y	DFE_WT2[0]	
22	7	0	RW	N	EOM_OV	"1: Override enable for EOM manual control 0: Normal operation"
	6	0	RW	N	EOM_SEL_RATE_OV	"1: Override enable for EOM rate selection 0: Normal operation"
	5	0	RW	N	RESERVED	RESERVED
	4	0	RW	N	RESERVED	RESERVED
	3	0	RW	N	RESERVED	RESERVED
	2	0	RW	N	RESERVED	RESERVED
	1	0	RW	N	RESERVED	RESERVED
	0	0	RW	N	RESERVED	RESERVED
23	7	0	RW	N	EOM_GET_HEO_VEO_OV	"1: Override enable for manual control of the HEO/VEO trigger 0: Normal operation"
	6	1	RW	Y	DFE_OV	1: Normal operation; DFE must be enabled in Reg_0x1E[3]
	5	0	RW	N	RESERVED	RESERVED
	4	0	RW	N	RESERVED	RESERVED
	3	0	RW	N	RESERVED	RESERVED
	2	0	RW	N	RESERVED	RESERVED
	1	0	RW	N	RESERVED	RESERVED
	0	0	RW	N	RESERVED	RESERVED

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Table 12. Channel Registers, 0 to 39 (continued)

ADDRESS (HEX)	BITS	DEFAULT VALUE (HEX)	MODE	EEPROM	FIELD NAME	DESCRIPTION
24	7	0	RW	N	FAST_EOM	1: Enables fast EOM for full eye capture. In this mode the phase DAC and voltage DAC or the EOM are automatically incremented through a 64 x 64 matrix. Values for each point are stored in Reg_0x25 and Reg_0x26. 0: Normal operation
	6	0	R	N	DFE_EQ_ERROR_NO_LOCK	DFE/CTLE SM quit due to loss of lock
	5	0	R	N	GET_HEO_VEO_ERROR_NO_HITS	get_heo_veo sees no hits at zero crossing
	4	0	R	N	GET_HEO_VEO_ERROR_NO_OPENING	get_heo_veo cannot see a vertical eye opening
	3	0	RW	N	RESERVED	RESERVED
	2	0	RWSC	N	DFE_ADAPT	1: Manually start DFE adaption (self-clearing) 0: Normal operation
	1	0	R	N	EOM_GET_HEO_VEO	1: Manually triggers HEO/VEO measurement; feature must be enabled with Reg_0x23[7]; the HEO/VEO values are read from Reg_0x27, Reg_0x28
	0	0	RWSC	N	EOM_START	Starts EOM counter, self-clearing
25	7	0	R	N	EOM_COUNT15	MSBs of EOM counter
	6	0	R	N	EOM_COUNT14	
	5	0	R	N	EOM_COUNT13	
	4	0	R	N	EOM_COUNT12	
	3	0	R	N	EOM_COUNT11	
	2	0	R	N	EOM_COUNT10	
	1	0	R	N	EOM_COUNT9	
	0	0	R	N	EOM_COUNT8	
26	7	0	R	N	EOM_COUNT7	LSBs of EOM counter
	6	0	R	N	EOM_COUNT6	
	5	0	R	N	EOM_COUNT5	
	4	0	R	N	EOM_COUNT4	
	3	0	R	N	EOM_COUNT3	
	2	0	R	N	EOM_COUNT2	
	1	0	R	N	EOM_COUNT1	
	0	0	R	N	EOM_COUNT0	
27	7	0	R	N	HEO7	HEO value, requires CDR to be locked for valid measurement
	6	0	R	N	HEO6	
	5	0	R	N	HEO5	
	4	0	R	N	HEO4	
	3	0	R	N	HEO3	
	2	0	R	N	HEO2	
	1	0	R	N	HEO1	
	0	0	R	N	HEO0	

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Table 12. Channel Registers, 0 to 39 (continued)

ADDRESS (HEX)	BITS	DEFAULT VALUE (HEX)	MODE	EEPROM	FIELD NAME	DESCRIPTION
28	7	0	R	N	VEO7	VEO value, requires CDR to be locked for valid measurement
	6	0	R	N	VEO6	
	5	0	R	N	VEO5	
	4	0	R	N	VEO4	
	3	0	R	N	VEO3	
	2	0	R	N	VEO2	
	1	0	R	N	VEO1	
	0	0	R	N	VEO0	
29	7	0	RW	N	RESERVED	RESERVED
	6	0	R	N	EOM_VRANGE_SETTING[1]	"Read the currently set Eye Monitor Voltage Range: 11 - +/-400mV 10 - +/- 300mV 01 - +/- 200mV 00 - +/- 100mV"
	5	0	R	N	EOM_VRANGE_SETTING[0]	
	4	0	RW	N	RESERVED	RESERVED
	3	0	RW	N	RESERVED	RESERVED
	2	0	RW	N	RESERVED	RESERVED
	1	0	R	N	VEO[8]	VEO MSB value
	0	0	R	N	HEO[8]	HEO MSB value
2A	7	0	RW	Y	EOM_TIMER_THR[3]	The value of eom_timer_thr[7:0] controls the amount of time the Eye Monitor samples each point in the eye for. The total counter bit width is 16b, this register representing the upper 8b. Therefore, the count value is equal to {eom_timer_thr[7:0],8'h0}. The counter counts in 32b words. Therefore, the total number of bits counted is 32 times this value.
	6	1	RW	Y	EOM_TIMER_THR[2]	
	5	0	RW	Y	EOM_TIMER_THR[1]	
	4	1	RW	Y	EOM_TIMER_THR[0]	
	3	1	RW	Y	VEO_MIN_REQ_HITS[3]	Whenever the Eye Monitor is used to measure HEO and VEO, the data is sampled for some number of bits, set by Reg_0x2A[7:3]. This register sets the number of hits within that sample size that is required before the EOM will indicate a hit has occurred. This filtering only affects the VEO measurement.
	2	0	RW	Y	VEO_MIN_REQ_HITS[2]	
	1	1	RW	Y	VEO_MIN_REQ_HITS[1]	
	0	0	RW	Y	VEO_MIN_REQ_HITS[0]	
2B	7	0	RW	N	RESERVED	RESERVED
	6	0	RW	N	RESERVED	RESERVED
	5	0	RW	Y	RESERVED	RESERVED
	4	0	RW	Y	RESERVED	RESERVED
	3	1	RW	Y	EOM_MIN_REQ_HITS[3]	Whenever the Eye Monitor is used to measure HEO and VEO, the data is sampled for some number of bits, set by Reg_0x2A[7:3]. This register sets the number of hits within that sample size that is required before the EOM will indicate a hit has occured. This filtering only affects the HEO measurement.
	2	0	RW	Y	EOM_MIN_REQ_HITS[2]	
	1	1	RW	Y	EOM_MIN_REQ_HITS[1]	
	0	0	RW	Y	EOM_MIN_REQ_HITS[0]	

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Table 12. Channel Registers, 0 to 39 (continued)

ADDRESS (HEX)	BITS	DEFAULT VALUE (HEX)	MODE	EEPROM	FIELD NAME	DESCRIPTION
2C	7	1	RW	N	reload_dfe_taps	Causes DFE taps to load from last adapted values
	6	1	RW	Y	VEO_SCALE	Scale VEO based on EOM vrange
	5	1	RW	Y	DFE_SM_FOM1	This register defines the Figure of Merit used when adapting the DFE: 00: not valid 01: SM uses only HEO 10: SM uses only VEO 11: SM uses both HEO and VEO Additionally, if Register 0x6E[6] is set to '1', the Alternate FOM is used. This bit takes precedence over DFE_SM_FOM
	4	1	RW	Y	DFE_SM_FOM0	
	3	0	RW	Y	DFE_ADAPT_COUNTER3	DFE look-beyond count.
	2	1	RW	Y	DFE_ADAPT_COUNTER2	
	1	1	RW	Y	DFE_ADAPT_COUNTER1	
	0	0	RW	Y	DFE_ADAPT_COUNTER0	
2D	7	0	RW	Y	RESERVED	RESERVED
	6	0	RW	Y	RESERVED	RESERVED
	5	1	RW	Y	RESERVED	RESERVED
	4	1	RW	Y	RESERVED	RESERVED
	3	0	RW	Y	REG_EQ_BST_OV	Allow override control of the EQ setting by writing to Reg_0x03
	2	0	RW	Y	RESERVED	RESERVED
	1	0	RW	Y	RESERVED	RESERVED
	0	0	RW	Y	RESERVED	RESERVED
2E	7	0	RW	N	RESERVED	RESERVED
	6	0	RW	N	RESERVED	RESERVED
	5	0	R	N	EQ_BST3_2_TO_ANALOG	Read-back of eq_BST3[2] going to analog
	4	0	RW	N	RESERVED	RESERVED
	3	0	RW	N	RESERVED	RESERVED
	2	0	RW	N	PRBS_PATTERN_SEL[2]	MSB for the PRBS_PATTERN_SEL field. Lower bits are found on register 0x30[1:0]. Refer to the register 0x30 description on this table.
	1	0	RW	N	RESERVED	RESERVED
	0	0	RW	N	RESERVED	RESERVED

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Table 12. Channel Registers, 0 to 39 (continued)

ADDRESS (HEX)	BITS	DEFAULT VALUE (HEX)	MODE	EEPROM	FIELD NAME	DESCRIPTION
2F	7	0	RW	Y	RESERVED	RESERVED
	6	1	RW	Y	RATE[2]	Configure PPM register and divider for a standard data rate. Refer to Programming Guide.
	5	0	RW	Y	RATE[1]	Configure PPM register and divider for a standard data rate. Refer to Programming Guide.
	4	1	RW	Y	RATE[0]	Configure PPM register and divider for a standard data rate. Refer to Programming Guide.
	3	0	RW	Y	INDEX_OV	If this bit is 1, then Reg_0x39 is to be used as 4-bit index to the [15:0] array of EQ settings. The EQ setting at that index is loaded to the EQ boost registers going to the analog and is used as the starting point for adaption.
	2	1	RW	Y	EN_PPM_CHECK	Enable the PPM to be used as a qualifier when performing Lock Detect
	1	0	RW	Y	RESERVED	RESERVED
	0	0	RWSC	N	CTLE_ADAPT	Starts CTLE adaptation, self-clearing

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Table 12. Channel Registers, 0 to 39 (continued)

ADDRESS (HEX)	BITS	DEFAULT VALUE (HEX)	MODE	EEPROM	FIELD NAME	DESCRIPTION
30	7	0	RW	N	FREEZE_PPM_CNT	Freeze the PPM counter to allow safe read asynchronously
	6	0	RW	Y	EQ_SEARCH_OV_EN	Enables the EQ 'search" bit to be forced by Reg_0x13[2]
	5	0	RW	N	EN_PATT_INV	Enable automatic pattern inversion of successive 16 bit words when using the "Fixed Pattern" generator option.
	4	0	RW	N	RELOAD_PRBS_CHKR	Force reload of seed into PRBS checker LFSR without holding the checker in reset.
	3	0	RW	N	PRBS_EN_DIG_CLK	This bit enables the clock to operate the PRBS generator and/or the PRBS checher. Toggling this bit is the primary method to reset the PRBS pattern generator and PRBS checker.
	2	0	RW	N	PRBS_PROGPATT_EN	"Enable a fixed data pattern output. Requires that serializer is enabled with Reg_0x1E[4]. PRBS generator and checker should be disabled, Reg_0x30[3]. The fixed data pattern is set by Reg_0x7C and Reg_0x97. Enable inversion of the pattern every 16 bits with Reg_0x30[5]".
	1	0	RW	N	PRBS_PATTERN_SEL[1]	"Selects the pattern output when using the PRBS generator. Requires the pattern generator to be configured properly. The MSB for the PRBS_PATTERN_SEL field is in Reg_0x2E[2]. Use Reg_0x30[3] to enable the PRBS generator. 000: 2^7-1 bits PRBS sequence 001: 2^9-1 bits PRBS sequence 010: 2^11-1 bits PRBS sequence 011: 2^15-1 bits PRBS sequence 100: 2^23-1 bits PRBS sequence 101: 2^31-1 bits PRBS sequence 110: 2^58-1 bits PRBS sequence 111: 2^63-1 bits PRBS sequence"
	0	0	RW	N	PRBS_PATTERN_SEL[0]	

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Table 12. Channel Registers, 0 to 39 (continued)

ADDRESS (HEX)	BITS	DEFAULT VALUE (HEX)	MODE	EEPROM	FIELD NAME	DESCRIPTION
31	7	0	RW	N	prbs_int_en	1: Enables interrupt for detection of PRBS errors. The PRBS checker must be properly configured for this feature to work
	6	0	RW	Y	ADAPT_MODE1	00: no adaption 01: adapt CTLE only 10: adapt CTLE until optimal, then DFE, then CTLE again 11: adapt CTLE until lock, then DFE, then EQ until optimal Note: for ADAPT_MODE=2 or 3, the DFE must be enabled by setting Reg_0x1E[3]=0 and Reg_0x1E[1]=1.
	5	1	RW	Y	ADAPT_MODE0	
	4	0	RW	Y	EQ_SM_FOM1	00: not valid 01: SM uses HEO only 10: SM uses VEO only 11: SM uses both HEO and VEO
	3	0	RW	Y	EQ_SM_FOM0	
	2	0	RW	N	RESERVED	
	1	0	RW	Y	cdr_lock_loss_int_en	Enable for CDR Lock Loss Interrupt. Observable in reg_1[5]
	0	0	RW	Y	signal_det_loss_int_en	Enable for Signal Detect Loss Interrupt. Observable in reg_1[0]
32	7	0	RW	Y	HEO_INT_THRESH3	These bits set the threshold for the HEO and VEO interrupt. Each threshold bit represents 8 counts of HEO or VEO.
	6	0	RW	Y	HEO_INT_THRESH2	
	5	0	RW	Y	HEO_INT_THRESH1	
	4	1	RW	Y	HEO_INT_THRESH0	
	3	0	RW	Y	VEO_INT_THRESH3	
	2	0	RW	Y	VEO_INT_THRESH2	
	1	0	RW	Y	VEO_INT_THRESH1	
	0	1	RW	Y	VEO_INT_THRESH0	
33	7	1	RW	Y	HEO_THRESH3	In adapt mode 3, the register sets the minimum HEO and VEO required for CTLE adaption, before starting DFE adaption. This can be a max of 15.
	6	0	RW	Y	HEO_THRESH2	
	5	0	RW	Y	HEO_THRESH1	
	4	0	RW	Y	HEO_THRESH0	
	3	1	RW	Y	VEO_THRESH3	
	2	0	RW	Y	VEO_THRESH2	
	1	0	RW	Y	VEO_THRESH1	
	0	0	RW	Y	VEO_THRESH0	

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Table 12. Channel Registers, 0 to 39 (continued)

ADDRESS (HEX)	BITS	DEFAULT VALUE (HEX)	MODE	EEPROM	FIELD NAME	DESCRIPTION
34	7	0	R	N	PPM_ERR_RDY	1: Indicates that a PPM error count is read to be read from channel register 0x3B and 0x3C
	6	0	RW	Y	LOW_POWER_MODE_DISABLE	By default, all blocks (except signal detect) power down after 100 ms after signal detect goes low. After achieving lock, the CDR continues to monitor the lock criteria. If the lock criteria fail, the lock is checked for a total of N number of times before declaring an out of lock condition, where N is set by this the value in these registers, with a max value of +3, for a total of 4. If during the N lock checks, lock is regained, then the lock condition is left HI, and the counter is reset back to zero.
	5	1	RW	Y	LOCK_COUNTER1	
	4	1	RW	Y	LOCK_COUNTER0	
	3	1	RW	Y	DFE_MAX_TAP2_5[3]	These four bits are used to set the maximum value by which DFE taps 2-5 are able to adapt with each subsequent adaptation. Same used for both polarities.
	2	1	RW	Y	DFE_MAX_TAP2_5[2]	
	1	1	RW	Y	DFE_MAX_TAP2_5[1]	
	0	1	RW	Y	DFE_MAX_TAP2_5[0]	
35	7	0	RW	Y	DATA_LOCK_PPM1	Modifies the value of the ppm delta tolerance from channel register 0x64: 00 - ppm_delta[7:0] =1 x ppm_delta[7:0] 01 - ppm_delta[7:0] =1 x ppm_delta[7:0] + ppm_delta[3:1] 10 - ppm_delta[7:0] =2 x ppm_delta[7:0] 11 - ppm_delta[7:0] =2 x ppm_delta[7:0] + ppm_delta[3:1]
	6	0	RW	Y	DATA_LOCK_PPM0	
	5	0	RW	N	GET_PPM_ERROR	Get ppm error from ppm_count - clears when done. Normally updates continuously, but can be manually triggered with read value from channel register0x3B and 0x3C Determines max tap limit for DFE tap 1
	4	0	RW	Y	DFE_MAX_TAP1[4]	
	3	1	RW	Y	DFE_MAX_TAP1[3]	
	2	1	RW	Y	DFE_MAX_TAP1[2]	
	1	1	RW	Y	DFE_MAX_TAP1[1]	
	0	1	RW	Y	DFE_MAX_TAP1[0]	
36	7	0	RW	N	RESERVED	
	6	0	RW	Y	HEO_VEO_INT_EN	1: Enable HEO/VEO interrupt capability
	5	1	RW	Y	REF_MODE1	11: Normal Operation
	4	1	RW	Y	REF_MODE0	
	3	0	RW	N	RESERVED	
	2	0	RW	Y	RESERVED	
	1	0	RW	N	RESERVED	
	0	0	RW	N	RESERVED	

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Table 12. Channel Registers, 0 to 39 (continued)

ADDRESS (HEX)	BITS	DEFAULT VALUE (HEX)	MODE	EEPROM	FIELD NAME	DESCRIPTION
37	7	0	R	N	CTLE_STATUS7	Feature is reserved for future use
	6	0	R	N	CTLE_STATUS6	
	5	0	R	N	CTLE_STATUS5	
	4	0	R	N	CTLE_STATUS4	
	3	0	R	N	CTLE_STATUS3	
	2	0	R	N	CTLE_STATUS2	
	1	0	R	N	CTLE_STATUS1	
	0	0	R	N	CTLE_STATUS0	
38	7	0	R	N	DFE_STATUS7	Feature is reserved for future use
	6	0	R	N	DFE_STATUS6	
	5	0	R	N	DFE_STATUS5	
	4	0	R	N	DFE_STATUS4	
	3	0	R	N	DFE_STATUS3	
	2	0	R	N	DFE_STATUS2	
	1	0	R	N	DFE_STATUS1	
	0	0	R	N	DFE_STATUS0	
39	7	0	RW	N	RESERVED	RESERVED
	6	1	RW	Y	MR_EOM_RATE1	With eom_ov = 1, these bits control the Eye Monitor Rate: 11: Use for full rate, fastest 10: Use for 1/2 Rate All other values are reserved
	5	1	RW	Y	MR_EOM_RATE0	
	4	0	RW	Y	RESERVED	RESERVED
	3	0	RW	Y	START_INDEX[3]	Start index for EQ adaptation
	2	0	RW	Y	START_INDEX[2]	
	1	0	RW	Y	START_INDEX[1]	
	0	0	RW	Y	START_INDEX[0]	

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Table 13. Channel Registers, 3A to A9

ADDRESS (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
3A	7	0	RW	Y	FIXED_EQ_BST0[1]	During adaptation, if the divider setting is >2, then a fixed EQ setting from this register will be used. However, if channel register 0x6F[7] is enabled, then an EQ adaptation will be performed instead
	6	0	RW	Y	FIXED_EQ_BST0[0]	
	5	0	RW	Y	FIXED_EQ_BST1[1]	
	4	0	RW	Y	FIXED_EQ_BST1[0]	
	3	0	RW	Y	FIXED_EQ_BST2[1]	
	2	0	RW	Y	FIXED_EQ_BST2[0]	
	1	0	RW	Y	FIXED_EQ_BST3[1]	
	0	0	RW	Y	FIXED_EQ_BST3[0]	
3B	7	0	R	N	ppm_count[15]	PPM count MSB
	6	0	R	N	ppm_count[14]	
	5	0	R	N	ppm_count[13]	
	4	0	R	N	ppm_count[12]	
	3	0	R	N	ppm_count[11]	
	2	0	R	N	ppm_count[10]	
	1	0	R	N	ppm_count[9]	
	0	0	R	N	ppm_count[8]	
3C	7	0	R	N	ppm_count[7]	PPM count LSB
	6	0	R	N	ppm_count[6]	
	5	0	R	N	ppm_count[5]	
	4	0	R	N	ppm_count[4]	
	3	0	R	N	ppm_count[3]	
	2	0	R	N	ppm_count[2]	
	1	0	R	N	ppm_count[1]	
	0	0	R	N	ppm_count[0]	
3D	7	0	RW	Y	EN_FIR_CURSOR	1: Enable Pre- and Post-cursor FIR 0: Disable Pre- and Post-cursor FIR (lower power)
	6	0	RW	Y	FIR_C0_SGN	Main-cursor sign bit 0: positive 1: negative
	5	0	RW	Y	RESERVED	RESERVED
	4	1	RW	Y	FIR_C0[4]	Main-cursor magnitude
	3	1	RW	Y	FIR_C0[3]	Main-cursor magnitude
	2	0	RW	Y	FIR_C0[2]	Main-cursor magnitude
	1	1	RW	Y	FIR_C0[1]	Main-cursor magnitude
	0	0	RW	Y	FIR_C0[0]	Main-cursor magnitude
3E	7	0	RW	Y	FIR_PD_TX	
	6	1	RW	Y	FIR_CN1_SGN	Pre-cursor sign bit 1: negative 0: positive
	5	0	RW	Y	RESERVED	RESERVED
	4	0	RW	Y	RESERVED	RESERVED
	3	0	RW	Y	FIR_CN1[3]	Pre-cursor magnitude
	2	0	RW	Y	FIR_CN1[2]	Pre-cursor magnitude
	1	0	RW	Y	FIR_CN1[1]	Pre-cursor magnitude
	0	0	RW	Y	FIR_CN1[0]	Pre-cursor magnitude

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Table 13. Channel Registers, 3A to A9 (continued)

ADDRESS (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
3F	7	0	RW	Y	RESERVED	
	6	1	RW	Y	FIR_CP1_SGN	Post-cursor sign bit 1: negative 0: positive
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	FIR_CP1[3]	Post-cursor magnitude
	2	0	RW	Y	FIR_CP1[2]	Post-cursor magnitude
	1	0	RW	Y	FIR_CP1[1]	Post-cursor magnitude
	0	0	RW	Y	FIR_CP1[0]	Post-cursor magnitude
40	7	0	RW	Y	EQ_ARRAY_INDEX_0_BST0[1]	
	6	0	RW	Y	EQ_ARRAY_INDEX_0_BST0[0]	
	5	0	RW	Y	EQ_ARRAY_INDEX_0_BST1[1]	
	4	0	RW	Y	EQ_ARRAY_INDEX_0_BST1[0]	
	3	0	RW	Y	EQ_ARRAY_INDEX_0_BST2[1]	
	2	0	RW	Y	EQ_ARRAY_INDEX_0_BST2[0]	
	1	0	RW	Y	EQ_ARRAY_INDEX_0_BST3[1]	
	0	0	RW	Y	EQ_ARRAY_INDEX_0_BST3[0]	
41	7	0	RW	Y	EQ_ARRAY_INDEX_1_BST0[1]	
	6	1	RW	Y	EQ_ARRAY_INDEX_1_BST0[0]	
	5	0	RW	Y	EQ_ARRAY_INDEX_1_BST1[1]	
	4	0	RW	Y	EQ_ARRAY_INDEX_1_BST1[0]	
	3	0	RW	Y	EQ_ARRAY_INDEX_1_BST2[1]	
	2	0	RW	Y	EQ_ARRAY_INDEX_1_BST2[0]	
	1	0	RW	Y	EQ_ARRAY_INDEX_1_BST3[1]	
	0	0	RW	Y	EQ_ARRAY_INDEX_1_BST3[0]	
42	7	0	RW	Y	EQ_ARRAY_INDEX_2_BST0[1]	
	6	1	RW	Y	EQ_ARRAY_INDEX_2_BST0[0]	
	5	0	RW	Y	EQ_ARRAY_INDEX_2_BST1[1]	
	4	1	RW	Y	EQ_ARRAY_INDEX_2_BST1[0]	
	3	0	RW	Y	EQ_ARRAY_INDEX_2_BST2[1]	
	2	0	RW	Y	EQ_ARRAY_INDEX_2_BST2[0]	
	1	0	RW	Y	EQ_ARRAY_INDEX_2_BST3[1]	
	0	0	RW	Y	EQ_ARRAY_INDEX_2_BST3[0]	
43	7	1	RW	Y	EQ_ARRAY_INDEX_3_BST0[1]	
	6	0	RW	Y	EQ_ARRAY_INDEX_3_BST0[0]	
	5	0	RW	Y	EQ_ARRAY_INDEX_3_BST1[1]	
	4	0	RW	Y	EQ_ARRAY_INDEX_3_BST1[0]	
	3	0	RW	Y	EQ_ARRAY_INDEX_3_BST2[1]	
	2	0	RW	Y	EQ_ARRAY_INDEX_3_BST2[0]	
	1	0	RW	Y	EQ_ARRAY_INDEX_3_BST3[1]	
	0	0	RW	Y	EQ_ARRAY_INDEX_3_BST3[0]	

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Table 13. Channel Registers, 3A to A9 (continued)

ADDRESS (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
44	7	1	RW	Y	EQ_ARRAY_INDEX_4_BST0[1]	
	6	0	RW	Y	EQ_ARRAY_INDEX_4_BST0[0]	
	5	0	RW	Y	EQ_ARRAY_INDEX_4_BST1[1]	
	4	1	RW	Y	EQ_ARRAY_INDEX_4_BST1[0]	
	3	0	RW	Y	EQ_ARRAY_INDEX_4_BST2[1]	
	2	0	RW	Y	EQ_ARRAY_INDEX_4_BST2[0]	
	1	0	RW	Y	EQ_ARRAY_INDEX_4_BST3[1]	
	0	0	RW	Y	EQ_ARRAY_INDEX_4_BST3[0]	
45	7	1	RW	Y	EQ_ARRAY_INDEX_5_BST0[1]	
	6	1	RW	Y	EQ_ARRAY_INDEX_5_BST0[0]	
	5	0	RW	Y	EQ_ARRAY_INDEX_5_BST1[1]	
	4	0	RW	Y	EQ_ARRAY_INDEX_5_BST1[0]	
	3	0	RW	Y	EQ_ARRAY_INDEX_5_BST2[1]	
	2	0	RW	Y	EQ_ARRAY_INDEX_5_BST2[0]	
	1	0	RW	Y	EQ_ARRAY_INDEX_5_BST3[1]	
	0	0	RW	Y	EQ_ARRAY_INDEX_5_BST3[0]	
46	7	1	RW	Y	EQ_ARRAY_INDEX_6_BST0[1]	
	6	1	RW	Y	EQ_ARRAY_INDEX_6_BST0[0]	
	5	0	RW	Y	EQ_ARRAY_INDEX_6_BST1[1]	
	4	1	RW	Y	EQ_ARRAY_INDEX_6_BST1[0]	
	3	0	RW	Y	EQ_ARRAY_INDEX_6_BST2[1]	
	2	0	RW	Y	EQ_ARRAY_INDEX_6_BST2[0]	
	1	0	RW	Y	EQ_ARRAY_INDEX_6_BST3[1]	
	0	0	RW	Y	EQ_ARRAY_INDEX_6_BST3[0]	
47	7	1	RW	Y	EQ_ARRAY_INDEX_7_BST0[1]	
	6	1	RW	Y	EQ_ARRAY_INDEX_7_BST0[0]	
	5	0	RW	Y	EQ_ARRAY_INDEX_7_BST1[1]	
	4	1	RW	Y	EQ_ARRAY_INDEX_7_BST1[0]	
	3	0	RW	Y	EQ_ARRAY_INDEX_7_BST2[1]	
	2	0	RW	Y	EQ_ARRAY_INDEX_7_BST2[0]	
	1	0	RW	Y	EQ_ARRAY_INDEX_7_BST3[1]	
	0	1	RW	Y	EQ_ARRAY_INDEX_7_BST3[0]	
48	7	1	RW	Y	EQ_ARRAY_INDEX_8_BST0[1]	
	6	1	RW	Y	EQ_ARRAY_INDEX_8_BST0[0]	
	5	0	RW	Y	EQ_ARRAY_INDEX_8_BST1[1]	
	4	1	RW	Y	EQ_ARRAY_INDEX_8_BST1[0]	
	3	0	RW	Y	EQ_ARRAY_INDEX_8_BST2[1]	
	2	1	RW	Y	EQ_ARRAY_INDEX_8_BST2[0]	
	1	0	RW	Y	EQ_ARRAY_INDEX_8_BST3[1]	
	0	1	RW	Y	EQ_ARRAY_INDEX_8_BST3[0]	

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Table 13. Channel Registers, 3A to A9 (continued)

ADDRESS (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
49	7	1	RW	Y	EQ_ARRAY_INDEX_9_BST0[1]	
	6	1	RW	Y	EQ_ARRAY_INDEX_9_BST0[0]	
	5	0	RW	Y	EQ_ARRAY_INDEX_9_BST1[1]	
	4	1	RW	Y	EQ_ARRAY_INDEX_9_BST1[0]	
	3	1	RW	Y	EQ_ARRAY_INDEX_9_BST2[1]	
	2	0	RW	Y	EQ_ARRAY_INDEX_9_BST2[0]	
	1	0	RW	Y	EQ_ARRAY_INDEX_9_BST3[1]	
	0	0	RW	Y	EQ_ARRAY_INDEX_9_BST3[0]	
4A	7	1	RW	Y	EQ_ARRAY_INDEX_10_BST0[1]	
	6	1	RW	Y	EQ_ARRAY_INDEX_10_BST0[0]	
	5	1	RW	Y	EQ_ARRAY_INDEX_10_BST1[1]	
	4	0	RW	Y	EQ_ARRAY_INDEX_10_BST1[0]	
	3	1	RW	Y	EQ_ARRAY_INDEX_10_BST2[1]	
	2	0	RW	Y	EQ_ARRAY_INDEX_10_BST2[0]	
	1	1	RW	Y	EQ_ARRAY_INDEX_10_BST3[1]	
	0	0	RW	Y	EQ_ARRAY_INDEX_10_BST3[0]	
4B	7	1	RW	Y	EQ_ARRAY_INDEX_11_BST0[1]	
	6	1	RW	Y	EQ_ARRAY_INDEX_11_BST0[0]	
	5	1	RW	Y	EQ_ARRAY_INDEX_11_BST1[1]	
	4	1	RW	Y	EQ_ARRAY_INDEX_11_BST1[0]	
	3	0	RW	Y	EQ_ARRAY_INDEX_11_BST2[1]	
	2	1	RW	Y	EQ_ARRAY_INDEX_11_BST2[0]	
	1	1	RW	Y	EQ_ARRAY_INDEX_11_BST3[1]	
	0	1	RW	Y	EQ_ARRAY_INDEX_11_BST3[0]	
4C	7	1	RW	Y	EQ_ARRAY_INDEX_12_BST0[1]	
	6	1	RW	Y	EQ_ARRAY_INDEX_12_BST0[0]	
	5	1	RW	Y	EQ_ARRAY_INDEX_12_BST1[1]	
	4	1	RW	Y	EQ_ARRAY_INDEX_12_BST1[0]	
	3	1	RW	Y	EQ_ARRAY_INDEX_12_BST2[1]	
	2	1	RW	Y	EQ_ARRAY_INDEX_12_BST2[0]	
	1	0	RW	Y	EQ_ARRAY_INDEX_12_BST3[1]	
	0	1	RW	Y	EQ_ARRAY_INDEX_12_BST3[0]	
4D	7	1	RW	Y	EQ_ARRAY_INDEX_13_BST0[1]	
	6	1	RW	Y	EQ_ARRAY_INDEX_13_BST0[0]	
	5	1	RW	Y	EQ_ARRAY_INDEX_13_BST1[1]	
	4	0	RW	Y	EQ_ARRAY_INDEX_13_BST1[0]	
	3	1	RW	Y	EQ_ARRAY_INDEX_13_BST2[1]	
	2	1	RW	Y	EQ_ARRAY_INDEX_13_BST2[0]	
	1	1	RW	Y	EQ_ARRAY_INDEX_13_BST3[1]	
	0	0	RW	Y	EQ_ARRAY_INDEX_13_BST3[0]	

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Table 13. Channel Registers, 3A to A9 (continued)

ADDRESS (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
4E	7	1	RW	Y	EQ_ARRAY_INDEX_14_BST0[1]	
	6	1	RW	Y	EQ_ARRAY_INDEX_14_BST0[0]	
	5	1	RW	Y	EQ_ARRAY_INDEX_14_BST1[1]	
	4	0	RW	Y	EQ_ARRAY_INDEX_14_BST1[0]	
	3	1	RW	Y	EQ_ARRAY_INDEX_14_BST2[1]	
	2	1	RW	Y	EQ_ARRAY_INDEX_14_BST2[0]	
	1	1	RW	Y	EQ_ARRAY_INDEX_14_BST3[1]	
	0	1	RW	Y	EQ_ARRAY_INDEX_14_BST3[0]	
4F	7	1	RW	Y	EQ_ARRAY_INDEX_15_BST0[1]	
	6	1	RW	Y	EQ_ARRAY_INDEX_15_BST0[0]	
	5	1	RW	Y	EQ_ARRAY_INDEX_15_BST1[1]	
	4	1	RW	Y	EQ_ARRAY_INDEX_15_BST1[0]	
	3	1	RW	Y	EQ_ARRAY_INDEX_15_BST2[1]	
	2	1	RW	Y	EQ_ARRAY_INDEX_15_BST2[0]	
	1	1	RW	Y	EQ_ARRAY_INDEX_15_BST3[1]	
	0	1	RW	Y	EQ_ARRAY_INDEX_15_BST3[0]	
50	7	1	RW	N	RESERVED	
	6	0	RW	N	RESERVED	
	5	0	RW	N	RESERVED	
	4	0	RW	N	RESERVED	
	3	1	RW	N	RESERVED	
	2	0	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	0	RW	N	RESERVED	
51	7	1	RW	N	RESERVED	
	6	0	RW	N	RESERVED	
	5	0	RW	N	RESERVED	
	4	0	RW	N	RESERVED	
	3	0	RW	N	RESERVED	
	2	0	RW	N	RESERVED	
	1	1	RW	N	RESERVED	
	0	0	RW	N	RESERVED	
52	7	1	RW	N	RESERVED	
	6	0	RW	N	RESERVED	
	5	1	RW	N	RESERVED	
	4	0	RW	N	RESERVED	
	3	0	RW	N	RESERVED	
	2	0	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	0	RW	N	RESERVED	

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Table 13. Channel Registers, 3A to A9 (continued)

ADDRESS (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
53	7	0	RW	N	RESERVED	
	6	1	RW	N	RESERVED	
	5	0	RW	N	RESERVED	
	4	0	RW	N	RESERVED	
	3	0	RW	N	RESERVED	
	2	1	RW	N	RESERVED	
	1	1	RW	N	RESERVED	
	0	0	RW	N	RESERVED	
54	7	0	RW	N	RESERVED	
	6	1	RW	N	RESERVED	
	5	0	RW	N	RESERVED	
	4	1	RW	N	RESERVED	
	3	0	RW	N	RESERVED	
	2	0	RW	N	RESERVED	
	1	1	RW	N	RESERVED	
	0	0	RW	N	RESERVED	
55	7	1	RW	N	RESERVED	
	6	0	RW	N	RESERVED	
	5	0	RW	N	RESERVED	
	4	0	RW	N	RESERVED	
	3	1	RW	N	RESERVED	
	2	1	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	0	RW	N	RESERVED	
56	7	1	RW	N	RESERVED	
	6	0	RW	N	RESERVED	
	5	1	RW	N	RESERVED	
	4	1	RW	N	RESERVED	
	3	0	RW	N	RESERVED	
	2	0	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	0	RW	N	RESERVED	
57	7	1	RW	N	RESERVED	
	6	1	RW	N	RESERVED	
	5	0	RW	N	RESERVED	
	4	0	RW	N	RESERVED	
	3	1	RW	N	RESERVED	
	2	0	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	0	RW	N	RESERVED	

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Table 13. Channel Registers, 3A to A9 (continued)

ADDRESS (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
58	7	0	RW	N	RESERVED	
	6	1	RW	N	RESERVED	
	5	0	RW	N	RESERVED	
	4	1	RW	N	RESERVED	
	3	0	RW	N	RESERVED	
	2	1	RW	N	RESERVED	
	1	1	RW	N	RESERVED	
	0	1	RW	N	RESERVED	
59	7	0	RW	N	RESERVED	
	6	1	RW	N	RESERVED	
	5	0	RW	N	RESERVED	
	4	1	RW	N	RESERVED	
	3	1	RW	N	RESERVED	
	2	1	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	1	RW	N	RESERVED	
5A	7	0	RW	N	RESERVED	
	6	1	RW	N	RESERVED	
	5	1	RW	N	RESERVED	
	4	0	RW	N	RESERVED	
	3	1	RW	N	RESERVED	
	2	0	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	1	RW	N	RESERVED	
5B	7	0	RW	N	RESERVED	
	6	1	RW	N	RESERVED	
	5	1	RW	N	RESERVED	
	4	1	RW	N	RESERVED	
	3	0	RW	N	RESERVED	
	2	1	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	1	RW	N	RESERVED	
5C	7	1	RW	N	RESERVED	
	6	1	RW	N	RESERVED	
	5	0	RW	N	RESERVED	
	4	1	RW	N	RESERVED	
	3	0	RW	N	RESERVED	
	2	1	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	1	RW	N	RESERVED	

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Table 13. Channel Registers, 3A to A9 (continued)

ADDRESS (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
5D	7	1	RW	N	RESERVED	
	6	0	RW	N	RESERVED	
	5	0	RW	N	RESERVED	
	4	1	RW	N	RESERVED	
	3	1	RW	N	RESERVED	
	2	0	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	1	RW	N	RESERVED	
5E	7	1	RW	N	RESERVED	
	6	0	RW	N	RESERVED	
	5	0	RW	N	RESERVED	
	4	1	RW	N	RESERVED	
	3	0	RW	N	RESERVED	
	2	1	RW	N	RESERVED	
	1	1	RW	N	RESERVED	
	0	0	RW	N	RESERVED	
5F	7	1	RW	N	RESERVED	
	6	0	RW	N	RESERVED	
	5	1	RW	N	RESERVED	
	4	0	RW	N	RESERVED	
	3	0	RW	N	RESERVED	
	2	1	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	1	RW	N	RESERVED	
60	7	0	RW	Y	GRP0_OV_CNT7	Group 0 count LSB
	6	0	RW	Y	GRP0_OV_CNT6	
	5	0	RW	Y	GRP0_OV_CNT5	
	4	0	RW	Y	GRP0_OV_CNT4	
	3	0	RW	Y	GRP0_OV_CNT3	
	2	0	RW	Y	GRP0_OV_CNT2	
	1	0	RW	Y	GRP0_OV_CNT1	
	0	0	RW	Y	GRP0_OV_CNT0	
61	7	0	RW	Y	CNT_DLTA_OV_0	Override enable for group 0 manual data rate selection
	6	0	RW	Y	GRP0_OV_CNT14	Group 0 count MSB
	5	0	RW	Y	GRP0_OV_CNT13	
	4	0	RW	Y	GRP0_OV_CNT12	
	3	0	RW	Y	GRP0_OV_CNT11	
	2	0	RW	Y	GRP0_OV_CNT10	
	1	0	RW	Y	GRP0_OV_CNT9	
	0	0	RW	Y	GRP0_OV_CNT8	

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Table 13. Channel Registers, 3A to A9 (continued)

ADDRESS (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
62	7	0	RW	Y	GRP1_OV_CNT7	Group 1 count LSB
	6	0	RW	Y	GRP1_OV_CNT6	
	5	0	RW	Y	GRP1_OV_CNT5	
	4	0	RW	Y	GRP1_OV_CNT4	
	3	0	RW	Y	GRP1_OV_CNT3	
	2	0	RW	Y	GRP1_OV_CNT2	
	1	0	RW	Y	GRP1_OV_CNT1	
	0	0	RW	Y	GRP1_OV_CNT0	
63	7	0	RW	Y	CNT_DLTA_OV_1	Override enable for group 1 manual data rate selection
	6	0	RW	Y	GRP1_OV_CNT14	Group 1 count MSB
	5	0	RW	Y	GRP1_OV_CNT13	
	4	0	RW	Y	GRP1_OV_CNT12	
	3	0	RW	Y	GRP1_OV_CNT11	
	2	0	RW	Y	GRP1_OV_CNT10	
	1	0	RW	Y	GRP1_OV_CNT9	
	0	0	RW	Y	GRP1_OV_CNT8	
64	7	0	RW	Y	GRP0_OV_DLTA3	Sets the PPM delta tolerance for the PPM counter lock check for group 0. Must also program channel register 0x67[7].
	6	0	RW	Y	GRP0_OV_DLTA2	
	5	0	RW	Y	GRP0_OV_DLTA1	
	4	0	RW	Y	GRP0_OV_DLTA0	
	3	0	RW	Y	GRP1_OV_DLTA3	Sets the PPM delta tolerance for the PPM counter lock check for group 1. Must also program channel register 0x67[6].
	2	0	RW	Y	GRP1_OV_DLTA2	
	1	0	RW	Y	GRP1_OV_DLTA1	
	0	0	RW	Y	GRP1_OV_DLTA0	
65	7	0	RW	N	RESERVED	RESERVED
	6	0	RW	N	RESERVED	RESERVED
	5	0	RW	N	RESERVED	RESERVED
	4	0	RW	N	RESERVED	RESERVED
	3	0	RW	N	RESERVED	RESERVED
	2	0	RW	N	RESERVED	RESERVED
	1	0	RW	N	RESERVED	RESERVED
	0	0	RW	N	RESERVED	RESERVED
66	7	0	RW	N	RESERVED	RESERVED
	6	0	RW	N	RESERVED	RESERVED
	5	0	RW	N	RESERVED	RESERVED
	4	0	RW	N	RESERVED	RESERVED
	3	0	RW	N	RESERVED	RESERVED
	2	0	RW	N	RESERVED	RESERVED
	1	0	RW	N	RESERVED	RESERVED
	0	0	RW	N	RESERVED	RESERVED

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Table 13. Channel Registers, 3A to A9 (continued)

ADDRESS (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
67	7	0	RW	Y	GRP0_OV_DLTA[4]	
	6	0	RW	Y	GRP1_OV_DLTA[4]	
	5	1	RW	Y	HV_LOCKMON_EN	1: Enable periodic monitoring of HEO/VEO for lock qualification. 0: Disable periodic HEO/VEO monitoring for lock qualification.
	4	0	RW	N	RESERVED	RESERVED
	3	0	RW	N	RESERVED	RESERVED
	2	0	RW	N	RESERVED	RESERVED
	1	0	RW	N	RESERVED	RESERVED
	0	0	RW	N	RESERVED	RESERVED
68	7	0	RW	N	RESERVED	RESERVED
	6	0	RW	N	RESERVED	RESERVED
	5	0	RW	N	RESERVED	RESERVED
	4	0	RW	N	RESERVED	RESERVED
	3	0	RW	N	RESERVED	RESERVED
	2	0	RW	N	RESERVED	RESERVED
	1	0	RW	N	RESERVED	RESERVED
	0	0	RW	N	RESERVED	RESERVED
69	7	0	RW	N	RESERVED	RESERVED
	6	0	RW	N	RESERVED	RESERVED
	5	0	RW	N	RESERVED	RESERVED
	4	0	RW	N	RESERVED	RESERVED
	3	1	RW	Y	RESERVED	RESERVED
	2	0	RW	Y	RESERVED	RESERVED
	1	1	RW	Y	RESERVED	RESERVED
	0	0	RW	Y	RESERVED	RESERVED
6A	7	0	RW	Y	VEO_LCK_THRSH3	VEO threshold to meet before lock is established. The LSB step size is 4 counts of VEO.
	6	0	RW	Y	VEO_LCK_THRSH2	
	5	1	RW	Y	VEO_LCK_THRSH1	
	4	0	RW	Y	VEO_LCK_THRSH0	
	3	0	RW	Y	HEO_LCK_THRSH3	HEO threshold to meet before lock is established. The LSB step size is 4 counts of VEO.
	2	0	RW	Y	HEO_LCK_THRSH2	
	1	1	RW	Y	HEO_LCK_THRSH1	
	0	0	RW	Y	HEO_LCK_THRSH0	
6B	7	0	RW	Y	RESERVED	RESERVED
	6	1	RW	Y	FOM_A6	Alternate Figure of Merit variable A. Max value for this register is 128.
	5	0	RW	Y	FOM_A5	
	4	0	RW	Y	FOM_A4	
	3	0	RW	Y	FOM_A3	
	2	0	RW	Y	FOM_A2	
	1	0	RW	Y	FOM_A1	
	0	0	RW	Y	FOM_A0	

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Table 13. Channel Registers, 3A to A9 (continued)

ADDRESS (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
6C	7	0	RW	Y	FOM_B7	HEO adjustment for Alternate FoM, variable B
	6	0	RW	Y	FOM_B6	
	5	0	RW	Y	FOM_B5	
	4	0	RW	Y	FOM_B4	
	3	0	RW	Y	FOM_B3	
	2	0	RW	Y	FOM_B2	
	1	0	RW	Y	FOM_B1	
	0	0	RW	Y	FOM_B0	
6D	7	0	RW	Y	FOM_C7	VEO adjustment for Alternate FoM, variable C
	6	0	RW	Y	FOM_C6	
	5	0	RW	Y	FOM_C5	
	4	0	RW	Y	FOM_C4	
	3	0	RW	Y	FOM_C3	
	2	0	RW	Y	FOM_C2	
	1	0	RW	Y	FOM_C1	
	0	0	RW	Y	FOM_C0	
6E	7	0	RW	Y	EN_NEW_FOM_CTLE	1: CTLE adaption state machine will use the alternate FoM HEO_ALT = (HEO-B)*A*2VEO_ALT = (VEO-C)*(1-A)*2 The values of A,B,C are set in channel register 0x6B, 0x6C, and 0x6D. The value of A is equal to the register value divided by 128. The Alternate FoM = (HEOB)*A*2 + (VEO-C)*(1-A)*2
	6	0	RW	Y	EN_NEW_FOM_DFE	1: DFE adaption state machine will use the alternate FoM. HEO_ALT = (HEO-B)*A*2VEO_ALT = (VEO-C)*(1-A)*2 The values of A,B,C are set in channel register 0x6B, 0x6C, and 0x6D. The value of A is equal to the register value divided by 128 The Alternate FoM = (HEOB)*A*2 + (VEO-C)*(1-A)*2
	5	0	RW	N	RESERVED	RESERVED
	4	0	RW	N	RESERVED	RESERVED
	3	0	RW	N	RESERVED	RESERVED
	2	0	RW	N	RESERVED	RESERVED
	1	0	RW	N	RESERVED	RESERVED
	0	0	RW	N	RESERVED	RESERVED

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Table 13. Channel Registers, 3A to A9 (continued)

ADDRESS (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
6F	7	0	RW	Y	MR_EN_LOW_DIVSEL_EQ	Normally, during adaptation, if the divider setting is >2, then a fixed EQ setting, from Reg_0x3A will be used. However, if Reg_0x6F[7]=1, then an EQ adaptation will be performed instead.
	6	0	RW	Y	RESERVED	RESERVED
	5	0	RW	Y	RESERVED	RESERVED
	4	0	RW	N	RESERVED	RESERVED
	3	0	RW	N	RESERVED	RESERVED
	2	0	RW	N	RESERVED	RESERVED
	1	0	RW	N	RESERVED	RESERVED
	0	0	RW	N	RESERVED	RESERVED
70	7	0	RW	N	RESERVED	RESERVED
	6	0	RW	N	RESERVED	RESERVED
	5	0	RW	N	RESERVED	RESERVED
	4	0	RW	N	RESERVED	RESERVED
	3	0	RW	Y	EQ_LB_CNT[3]	CTLE look-beyond count for adaptation
	2	1	RW	Y	EQ_LB_CNT[2]	
	1	0	RW	Y	EQ_LB_CNT[1]	
	0	1	RW	Y	EQ_LB_CNT[0]	
71	7	0	R	N	PRBS_INT	When enabled by Reg_0x31[7], goes HI if a PRBS stream is detected. Clears on reading. PRBS checker must be enabled with Reg_0x30[3]. Once cleared, if a PRBS error occurs, then the interrupt will again go HI. Clears on reading. If signal detect is lost, this is considered a PRBS error, and the interrupt will go HI. Clears on reading.
	6	0	R	N	RESERVED	RESERVED
	5	0	R	N	DFE_POL_1_OBS	DFE tap 1 polarity observation
	4	0	R	N	DFE_WT1_OBS[4]	DFE tap 1 weight observation
	3	0	R	N	DFE_WT1_OBS[3]	
	2	0	R	N	DFE_WT1_OBS[2]	
	1	0	R	N	DFE_WT1_OBS[1]	
	0	0	R	N	DFE_WT1_OBS[0]	
72	7	0	R	N	RESERVED	RESERVED
	6	0	R	N	RESERVED	RESERVED
	5	0	R	N	RESERVED	RESERVED
	4	0	R	N	DFE_POL_2_OBS	Primary observation point for DFE tap 2 polarity
	3	0	R	N	DFE_WT2_OBS3	Primary observation point for DFE tap 2 weight
	2	0	R	N	DFE_WT2_OBS2	
	1	0	R	N	DFE_WT2_OBS1	
	0	0	R	N	DFE_WT2_OBS0	

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Table 13. Channel Registers, 3A to A9 (continued)

ADDRESS (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
73	7	0	R	N	RESERVED	RESERVED
	6	0	R	N	RESERVED	RESERVED
	5	0	R	N	RESERVED	RESERVED
	4	0	R	N	DFE_POL_3_OBS	Primary observation point for DFE tap 3 polarity
	3	0	R	N	DFE_WT3_OBS3	Primary observation point for DFE tap 3 weight
	2	0	R	N	DFE_WT3_OBS2	
	1	0	R	N	DFE_WT3_OBS1	
	0	0	R	N	DFE_WT3_OBS0	
74	7	0	R	N	RESERVED	RESERVED
	6	0	R	N	RESERVED	RESERVED
	5	0	R	N	RESERVED	RESERVED
	4	0	R	N	DFE_POL_4_OBS	Primary observation point for DFE tap 4 polarity
	3	0	R	N	DFE_WT4_OBS3	Primary observation point for DFE tap 4 weight
	2	0	R	N	DFE_WT4_OBS2	
	1	0	R	N	DFE_WT4_OBS1	
	0	0	R	N	DFE_WT4_OBS0	
75	7	0	R	N	RESERVED	RESERVED
	6	0	R	N	RESERVED	RESERVED
	5	0	R	N	RESERVED	RESERVED
	4	0	R	N	DFE_POL_5_OBS	Primary observation point for DFE tap 5 polarity
	3	0	R	N	DFE_WT5_OBS3	Primary observation point for DFE tap 5 weight
	2	0	R	N	DFE_WT5_OBS2	
	1	0	R	N	DFE_WT5_OBS1	
	0	0	R	N	DFE_WT5_OBS0	
76	7	0	RW	Y	post_lock_veo_thr[3]	VEO threshold after LOCK is established
	6	0	RW	Y	post_lock_veo_thr[2]	
	5	1	RW	Y	post_lock_veo_thr[1]	
	4	0	RW	Y	post_lock_veo_thr[0]	
	3	0	RW	Y	post_lock_heo_thr[3]	HEO threshold after LOCK is established
	2	0	RW	Y	post_lock_heo_thr[2]	
	1	0	RW	Y	post_lock_heo_thr[1]	
	0	1	RW	Y	post_lock_heo_thr[0]	
77	7	0	RW	N	PRBS_GEN_POL_EN	1: Force polarity inversion on generated PRBS data
	6	0	RW	Y	RESERVED	
	5	0	RW	Y	RESERVED	
	4	1	RW	Y	RESERVED	
	3	1	RW	Y	RESERVED	
	2	0	RW	Y	RESERVED	
	1	1	RW	Y	RESERVED	
	0	0	RW	N	RESERVED	

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Table 13. Channel Registers, 3A to A9 (continued)

ADDRESS (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
78	7	0	R	N	RESERVED	
	6	0	R	N	RESERVED	
	5	0	R	N	SD_STATUS	Primary observation point forsignal detect status
	4	0	R	N	CDR_LOCK_STATUS	Primary observation point forCDR lock status
	3	0	R	N	CDR_LOCK_INT	Requires that channel register 0x79[1] be set. 1: Indicates CDR has achieved lock, lock goes from LOW to HIGH. This bit is cleared after reading. This bit will stay set until it has been cleared by reading.
	2	0	R	N	SD_INT	Requires that channel register 0x79[0] be set. 1: Indicates signal detect status has changed. This will trigger when signal detect goes from LOW to HIGH or HIGH to LOW. This bit is cleared after reading. This bit will stay set until it has been cleared by reading.
	1	0	R	N	EOM_VRANGE_LIMIT_ERROR	Goes high if GET_HEO_VEO indicates high during adaptation
	0	0	R	N	HEO_VEO_INT	Requires that channel register 0x36[6] be set. 1: Indicates that HEO/VEO dropped below the limits set in channel register 0x76 This bit is cleared after reading. This bit will stay set until it has been cleared by reading.
79	7	0	RW	N	RESERVED	
	6	0	RW	N	PRBS_CHKR_EN	1: Enable the PRBS checker. 0: Disable the PRBS checker
	5	0	RW	N	PRBS_GEN_EN	1: Enable the pattern generator 0: Disable the pattern generator
	4	1	RW	N	PRBS_LCKUP_EXIT_EN	0: Turn off lock up detection in PRBS checker/generator Used for debug purposes only.
	3	0	RW	N	RESERVED	
	2	0	RW	N	RESERVED	
	1	0	RW	Y	CDR_LOCK_INT_EN	1: Enable CDR lock interrupt, observable in channel register 0x78[3] 0: Disable CDR lock interrupt
	0	0	RW	Y	SD_INT_EN	1: Enable signal detect interrupt, observable in channel register 0x78[3] 0: Disable signal detect interrupt

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Table 13. Channel Registers, 3A to A9 (continued)

ADDRESS (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
7A	7	0	RW	N	RESERVED	
	6	0	RW	N	RESERVED	
	5	0	RW	N	RESERVED	
	4	0	RW	N	RESERVED	
	3	0	RW	N	RESERVED	
	2	0	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	0	RW	N	RESERVED	
7B	7	0	RW	N	RESERVED	
	6	0	RW	N	RESERVED	
	5	0	RW	N	RESERVED	
	4	0	RW	N	RESERVED	
	3	0	RW	N	RESERVED	
	2	0	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	0	RW	N	RESERVED	
7C	7	0	R	N	PRBS_FIXED7	Pattern generator user defined pattern LSB. MSB located at channel register 0x97.
	6	0	R	N	PRBS_FIXED6	
	5	0	R	N	PRBS_FIXED5	
	4	0	R	N	PRBS_FIXED4	
	3	0	R	N	PRBS_FIXED3	
	2	0	R	N	PRBS_FIXED2	
	1	0	R	N	PRBS_FIXED1	
	0	0	R	N	PRBS_FIXED0	
7D	7	0	RW	Y	CONT_ADAPT_HEO_CHNG_THRS3	Limit for HEO change before triggering a DFE adaption while continuous DFE adaption is enabled.
	6	1	RW	Y	CONT_ADAPT_HEO_CHNG_THRS2	
	5	0	RW	Y	CONT_ADAPT_HEO_CHNG_THRS1	
	4	0	RW	Y	CONT_ADAPT_HEO_CHNG_THRS0	
	3	1	RW	Y	CONT_ADAPT_VEO_CHNG_THRS3	Limit for VEO change before triggering a DFE adaption while continuous DFE adaption is enabled
	2	0	RW	Y	CONT_ADAPT_VEO_CHNG_THRS2	
	1	0	RW	Y	CONT_ADAPT_VEO_CHNG_THRS1	
	0	0	RW	Y	CONT_ADAPT_VEO_CHNG_THRS0	

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Table 13. Channel Registers, 3A to A9 (continued)

ADDRESS (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
7E	7	0	RW	Y	CONT_ADPT_TAP_INCR3	Limit for allowable tap increase from the previous base point
	6	0	RW	Y	CONT_ADPT_TAP_INCR2	
	5	0	RW	Y	CONT_ADPT_TAP_INCR1	
	4	1	RW	Y	CONT_ADPT_TAP_INCR0	
	3	0	RW	Y	CONT_ADPT_FOM_CHNG_THRS 3	Bits define by how much the FOM can change before triggering DFE adapt
	2	0	RW	Y	CONT_ADPT_FOM_CHNG_THRS 2	
	1	1	RW	Y	CONT_ADPT_FOM_CHNG_THRS 1	
	0	1	RW	Y	CONT_ADPT_FOM_CHNG_THRS 0	
7F	7	0	RW	N	EN_OBS_ALT_FOM	1: Allows for alternate FoM 7Fcalculation to be shown in channel registers 0x27, 0x28 and 0x29 instead of HEO and VEO
	6	0	RW	N	RESERVED	
	5	1	RW	Y	DIS_HV_CHK_FOR_CONT_ADAP T	1: Ignore HEO/VEO lock condition checks during continuous adaption. Normal operation for continuous DFE adaption
	4	0	RW	Y	EN_DFE_CONT_ADAPT	1: Continuous DFE adaption is enabled 0: DFE adapts only during lock and then freezes
	3	1	RW	Y	CONT_ADPT_CMP_BOTH	1: If continuous DFE adaption is enabled, a DFE adaption will trigger if either HEO orVEO degrades
	2	0	RW	Y	CONT_ADPT_COUNT2	Limit for number of weights the DFE can look ahead in continuous adaption
	1	1	RW	Y	CONT_ADPT_COUNT1	
	0	0	RW	Y	CONT_ADPT_COUNT0	
80	7	0	R	N	RESERVED	
	6	0	R	N	RESERVED	
	5	0	R	N	RESERVED	
	4	0	R	N	RESERVED	
	3	0	R	N	RESERVED	
	2	0	R	N	RESERVED	
	1	0	R	N	RESERVED	
	0	0	R	N	RESERVED	
81	7	1	R	N	RESERVED	RESERVED
	6	1	R	N	RESERVED	RESERVED
	5	1	R	N	RESERVED	RESERVED
	4	0	R	N	RESERVED	RESERVED
	3	0	R	N	RESERVED	RESERVED
	2	1	R	N	RESERVED	RESERVED
	1	0	R	N	RESERVED	RESERVED
	0	0	R	N	RESERVED	RESERVED

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Table 13. Channel Registers, 3A to A9 (continued)

ADDRESS (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
82	7	0	RW	N	FREEZE_PRBS_CNTR	1: Freeze the PRBS error count to allow for readback. 0: Normal operation. Error counters is allowed to increment if the PRBS checker is properly configured
	6	0	RW	N	RST_PRBS_CNTS	1: Reset the PRBS error counter. 0: Normal operation. Error counter is released from reset.
	5	0	RW	N	PRBS_PATT_OV	1: Override PRBS pattern auto-detection. Forces the pattern checker to only lock onto the pattern defined in Reg_0x82[4:2]. 0: Normal operation. Pattern checker will automatically detect the PRBS pattern
	4	0	RW	N	PRBS_PATT[2]	Used with the PRBS checker. Usage is enabled with Reg_0x82[5]. Select PRBS pattern to be checked: 000 - PRBS7 001 - PRBS9 010 - PRBS11 011 - PRBS15 100 - PRBS23 101 - PRBS31 110 - PRBS58 111 - PRBS63
	3	0	RW	N	PRBS_PATT[1]	
	2	0	RW	N	PRBS_PATT[0]	
	1	0	RW	N	PRBS_POL_OV	1: Override PRBS pattern auto polarity detection. Forces the pattern checker to only lock onto the polarity defined in bit 0 of this register. 0: Normal operation, pattern checker will automatically detect the PRBS pattern polarity
	0	0	RW	N	PRBS_POL	Usage is enabled with Reg_0x82[1]=1 0: Forced polarity = true 1: Forced polarity = inverted
83	7	0	R	N	RESERVED	RESERVED
	6	0	R	N	RESERVED	RESERVED
	5	0	R	N	RESERVED	RESERVED
	4	0	R	N	RESERVED	RESERVED
	3	0	R	N	RESERVED	RESERVED
	2	0	R	N	PRBS_ERR_CNT[10]	PRBS checker error count
	1	0	R	N	PRBS_ERR_CNT[9]	PRBS checker error count
	0	0	R	N	PRBS_ERR_CNT[8]	PRBS checker error count
84	7	0	R	N	PRBS_ERR_CNT7	PRBS checker error count
	6	0	R	N	PRBS_ERR_CNT6	
	5	0	R	N	PRBS_ERR_CNT5	
	4	0	R	N	PRBS_ERR_CNT4	
	3	0	R	N	PRBS_ERR_CNT3	
	2	0	R	N	PRBS_ERR_CNT2	
	1	0	R	N	PRBS_ERR_CNT1	
	0	0	R	N	PRBS_ERR_CNT0	

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Table 13. Channel Registers, 3A to A9 (continued)

ADDRESS (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
85	7	0	R	N	RESERVED	
	6	0	R	N	RESERVED	
	5	0	R	N	RESERVED	
	4	0	R	N	RESERVED	
	3	0	R	N	RESERVED	
	2	0	R	N	RESERVED	
	1	0	R	N	RESERVED	
	0	0	R	N	RESERVED	
86	7	0	R	N	RESERVED	
	6	0	R	N	RESERVED	
	5	0	R	N	RESERVED	
	4	0	R	N	RESERVED	
	3	0	R	N	RESERVED	
	2	0	R	N	RESERVED	
	1	0	R	N	RESERVED	
	0	0	R	N	RESERVED	
87	7	0	R	N	RESERVED	
	6	0	R	N	RESERVED	
	5	0	R	N	RESERVED	
	4	0	R	N	RESERVED	
	3	0	R	N	RESERVED	
	2	0	R	N	RESERVED	
	1	0	R	N	RESERVED	
	0	0	R	N	RESERVED	
88	7	0	R	N	RESERVED	
	6	0	R	N	RESERVED	
	5	0	R	N	RESERVED	
	4	0	R	N	RESERVED	
	3	0	R	N	RESERVED	
	2	0	R	N	RESERVED	
	1	0	R	N	RESERVED	
	0	0	R	N	RESERVED	
89	7	0	R	N	RESERVED	
	6	0	R	N	RESERVED	
	5	0	R	N	RESERVED	
	4	0	R	N	RESERVED	
	3	0	R	N	RESERVED	
	2	0	R	N	RESERVED	
	1	0	R	N	RESERVED	
	0	0	R	N	RESERVED	

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Table 13. Channel Registers, 3A to A9 (continued)

ADDRESS (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
8A	7	0	R	N	RESERVED	
	6	0	R	N	RESERVED	
	5	0	R	N	RESERVED	
	4	0	R	N	RESERVED	
	3	0	R	N	RESERVED	
	2	0	R	N	RESERVED	
	1	0	R	N	RESERVED	
	0	0	R	N	RESERVED	
8B	7	0	RW	N	RESERVED	
	6	0	RW	N	RESERVED	
	5	0	RW	N	RESERVED	
	4	0	RW	N	RESERVED	
	3	0	RW	N	RESERVED	
	2	0	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	0	RW	N	RESERVED	
8C	7	0	RW	N	UNCORR_ERR_PATT7	Used in conjunction with register 0x78[7]. This register, register 0x8B and register 0x8C set a 16-bit pattern that is searched for within the data stream. If this pattern is found, the interrupt in register 0x78[7] is set HI.
	6	0	RW	N	UNCORR_ERR_PATT6	
	5	0	RW	N	UNCORR_ERR_PATT5	
	4	0	RW	N	UNCORR_ERR_PATT4	
	3	0	RW	N	UNCORR_ERR_PATT3	
	2	0	RW	N	UNCORR_ERR_PATT2	
	1	0	RW	N	UNCORR_ERR_PATT1	
	0	0	RW	N	UNCORR_ERR_PATT0	
8D	7	0	RW	N	RESERVED	
	6	0	RW	N	RESERVED	
	5	0	RW	N	RESERVED	
	4	0	RW	N	RESERVED	
	3	0	RW	N	RESERVED	
	2	1	RW	N	RESERVED	
	1	1	RW	N	RESERVED	
	0	0	RW	N	RESERVED	
8E	7	0	RW	N	RESERVED	
	6	0	RW	N	RESERVED	
	5	0	RW	N	RESERVED	
	4	0	RW	N	RESERVED	
	3	0	RW	N	RESERVED	
	2	0	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	0	RW	Y	VGA_SEL_GAIN[0]	VGA selection bit (1: on, 0: off)

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Table 13. Channel Registers, 3A to A9 (continued)

ADDRESS (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
8F	7	0	R	N	EQ_BST_TO_ANA7	Primary observation point for the EQ boost setting.
	6	0	R	N	EQ_BST_TO_ANA6	
	5	0	R	N	EQ_BST_TO_ANA5	
	4	0	R	N	EQ_BST_TO_ANA4	
	3	0	R	N	EQ_BST_TO_ANA3	
	2	0	R	N	EQ_BST_TO_ANA2	
	1	0	R	N	EQ_BST_TO_ANA1	
	0	0	R	N	EQ_BST_TO_ANA0	
90	7	0	RW	N	RESERVED	
	6	0	RW	N	RESERVED	
	5	0	RW	N	RESERVED	
	4	0	RW	N	RESERVED	
	3	0	RW	N	RESERVED	
	2	0	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	0	RW	N	RESERVED	
91	7	0	RW	N	RESERVED	
	6	0	RW	N	RESERVED	
	5	0	RW	N	RESERVED	
	4	0	RW	N	RESERVED	
	3	0	RW	N	RESERVED	
	2	0	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	0	RW	N	RESERVED	
92	7:0	0	RW	N	RESERVED	
93	7:0	0	RW	N	RESERVED	
94	7:0	0	RW	N	RESERVED	
95	7:0	0	RW	N	RESERVED	
96	7	0	RW	N	RESERVED	
	6	0	RW	N	RESERVED	
	5	0	RW	N	RESERVED	
	4	0	RW	N	RESERVED	
	3	1	RW	Y	EQ_EN_LOCAL	1: Enable the ebuf for the local output. Can be set independently of other controls.
	2	0	RW	Y	EQ_EN_FANOUT	1: Enable the ebuf for the fanout. Can be set independently of other controls.
	1	0	RW	Y	EQ_SEL_XPNT	1: Indicates to a channel where it is getting its data from. 0 indicates local. 1-indicates from the cross.
	0	0	RW	Y	XPNT_SLAVE	1: Indicates to a channel if it needs to wait for the other channel to complete its lock/adaptation. The need for this condition comes up when input of one channel is routed to the other channel or multiple channels.

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Table 13. Channel Registers, 3A to A9 (continued)

ADDRESS (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
97	7	0	R	N	PRBS_FIXED15	Pattern generator user defined pattern MSB. LSB located at channel register 0x7C.
	6	0	R	N	PRBS_FIXED14	
	5	0	R	N	PRBS_FIXED13	
	4	0	R	N	PRBS_FIXED12	
	3	0	R	N	PRBS_FIXED11	
	2	0	R	N	PRBS_FIXED10	
	1	0	R	N	PRBS_FIXED9	
	0	0	R	N	PRBS_FIXED8	
98	7:6	0	RW	N	RESERVED	
	5:0	0	RW	Y	RESERVED	
99	7	0	RW	Y	RESERVED	
	6	0	RW	Y	RESERVED	
	5	1	RW	Y	RESERVED	
	4	1	RW	Y	RESERVED	
	3	1	RW	Y	RESERVED	
	2	1	RW	Y	RESERVED	
	1	1	RW	Y	RESERVED	
	0	1	RW	Y	RESERVED	
9A	7	0	RW	Y	RESERVED	
	6	0	RW	Y	RESERVED	
	5	1	RW	Y	RESERVED	
	4	1	RW	Y	RESERVED	
	3	1	RW	Y	RESERVED	
	2	1	RW	Y	RESERVED	
	1	1	RW	Y	RESERVED	
	0	1	RW	Y	RESERVED	
9B	7	1	RW	Y	RESERVED	
	6	1	RW	Y	RESERVED	
	5	1	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	RESERVED	
	2	0	RW	Y	RESERVED	
	1	0	RW	N	RESERVED	
	0	0	RW	N	RESERVED	
9C	7	0	RW	N	RESERVED	
	6	0	RW	N	RESERVED	
	5	1	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	RESERVED	
	2	1	RW	Y	RESERVED	
	1	0	RW	Y	RESERVED	
	0	0	RW	Y	RESERVED	

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Table 13. Channel Registers, 3A to A9 (continued)

ADDRESS (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
9D	7	1	RW	N	RESERVED	
	6	0	RW	N	RESERVED	
	5	1	RW	N	RESERVED	
	4	0	RW	N	RESERVED	
	3	0	RW	Y	RESERVED	
	2	1	RW	Y	RESERVED	
	1	0	RW	Y	RESERVED	
	0	1	RW	N	RESERVED	
9E	7	0	RW	Y	cp_en_idac_pd[2]	Phase detector charge pump setting, when override is enabled. See reg_0C for other bits.
	6	1	RW	Y	cp_en_idac_pd[1]	
	5	0	RW	Y	cp_en_idac_pd[0]	
	4	0	RW	Y	cp_en_idac_fd[2]	Frequency detector charge pump setting, when override is enabled. See reg_0C for other bits.
	3	1	RW	Y	cp_en_idac_fd[1]	
	2	0	RW	Y	cp_en_idac_fd[0]	
	1	0	RW	N	RESERVED	
	0	0	RW	N	RESERVED	
9F	7:0	0	R	N	NOT USED	
A0	7:0	0	R	N	NOT USED	
A1	7:0	0	R	N	NOT USED	
A2	7:0	0	R	N	NOT USED	
A3	7:0	0	R	N	NOT USED	
A4	7:0	0	R	N	NOT USED	
A5	7	0	RW	Y	PFD_SEL_DATA_PSTLCK[2]	Post-lock PFD mux select 111 - Mute 110 - N/A 101 - 10M Clock 100 - PRBS Generator or Fixed Pattern Generator Data 011 - N/A 010 - N/A 000 - Raw Data
	6	0	RW	Y	PFD_SEL_DATA_PSTLCK[1]	
	5	1	RW	Y	PFD_SEL_DATA_PSTLCK[0]	
	4	0	RW	N	RESERVED	RESERVED
	3	0	RW	N	RESERVED	RESERVED
	2	0	RW	N	RESERVED	RESERVED
	1	0	RW	N	RESERVED	RESERVED
	0	0	RW	N	RESERVED	RESERVED

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Table 13. Channel Registers, 3A to A9 (continued)

ADDRESS (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
A6	7	0	RW	N	INCR_HIST_TMR	Provides an option to increase EOM timer given by 0x2A[7:4] for histogram collection by +8 for selection values < 8
	6	1	RW	Y	EOM_TMR_ABRT_ON_HIT	Enables faster scan through the eye-matrix by moving on to the next matrix point as soon as hit is observed Note: This bit does not affect when slope measurement are in progress
	5	0	RW	Y	SLP_MIN_REQ_HITS[1]	Minimum required hit count for registering a hit during slope measurements.
	4	0	RW	Y	SLP_MIN_REQ_HITS[0]	
	3	0	RW	Y	LFT_SLP	0: allows slope measurement for the right side of the eye 1: allows slope measurement for the left side of the eye
	2	0	RW	Y	TOP_SLP	0: allows slope measurement for the bottom side of the eye 1: allows slope measurement for the top side of the eye
	1	1	RW	Y	DFE_BATHTUB_FOM	Enables slope-based bathtub FoM for DFE adaptation
	0	1	RW	Y	CTLE_BATHTUB_FOM	Enables slope-based bathtub FoM for CTLE adaptation
A7	7:0	0	R	N	RESERVED	
A8	7:0	0	RW	N	RESERVED	
A9	7:0	0	RW	Y	RESERVED	

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10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The DS250DF810 is a high-speed retimer which extends the reach of differential channels and cleans jitter and other signal impairments in the process. It can be deployed in a variety of different systems from backplanes to front ports to active cable assemblies. The following sections outline typical applications and their associated design considerations.

10.2 Typical Application

The DS250DF810 is typically used in the following main application scenarios:

1. Backplane and mid-plane reach extension
2. Front-port jitter cleaning / retiming for optical applications

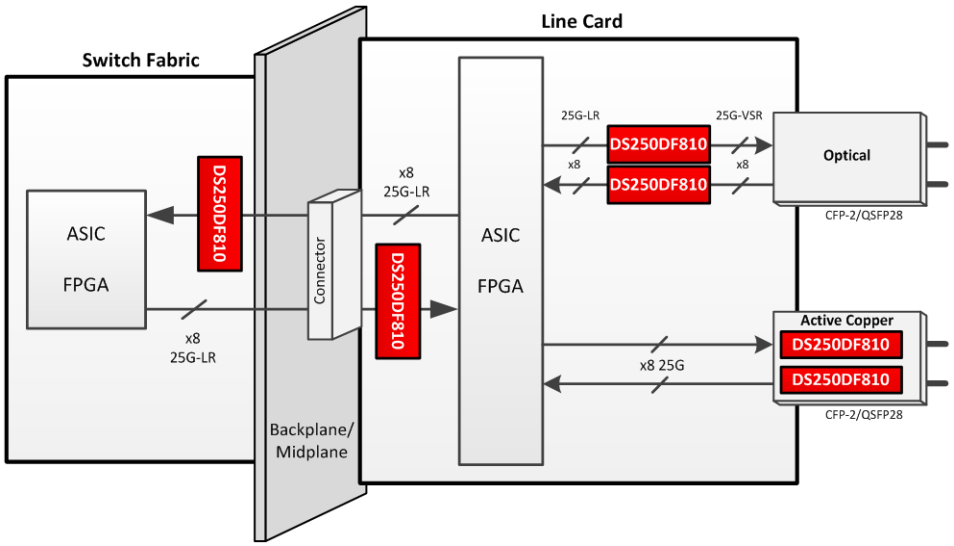


Figure 15. Typical Uses for the DS250DF810 in a System

Typical Application (continued)

10.2.1 Backplane and Mid-Plane Applications

The DS250DF810 has strong equalization capabilities that allow it to recover data over channels up to 35 dB insertion loss. As a result, the optimum placement for the DS250DF810 in a backplane/mid-plane application is with the higher-loss channel segment at the input and the lower-loss channel segment at the output. This reduces the equalization burden on the downstream ASIC/FPGA, as the DS250DF810 is equalizing a majority of the overall channel. This type of asymmetric placement is not a requirement, but when an asymmetric placement is required due to the presence of a passive backplane or mid-plane, then this becomes the recommended placement.

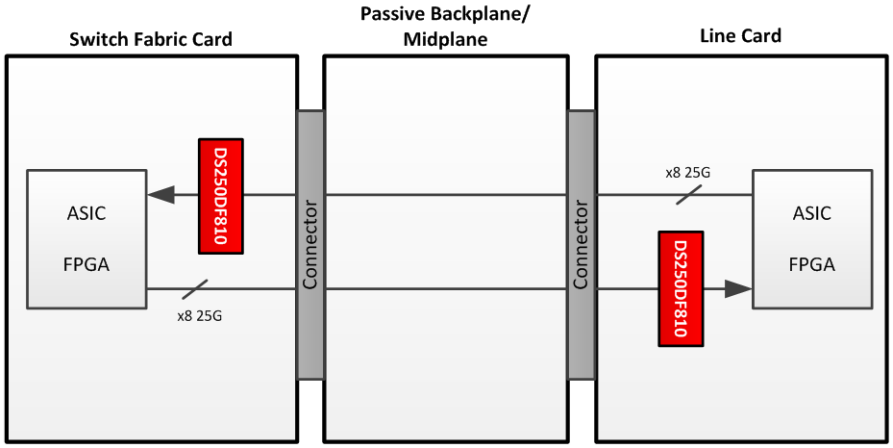
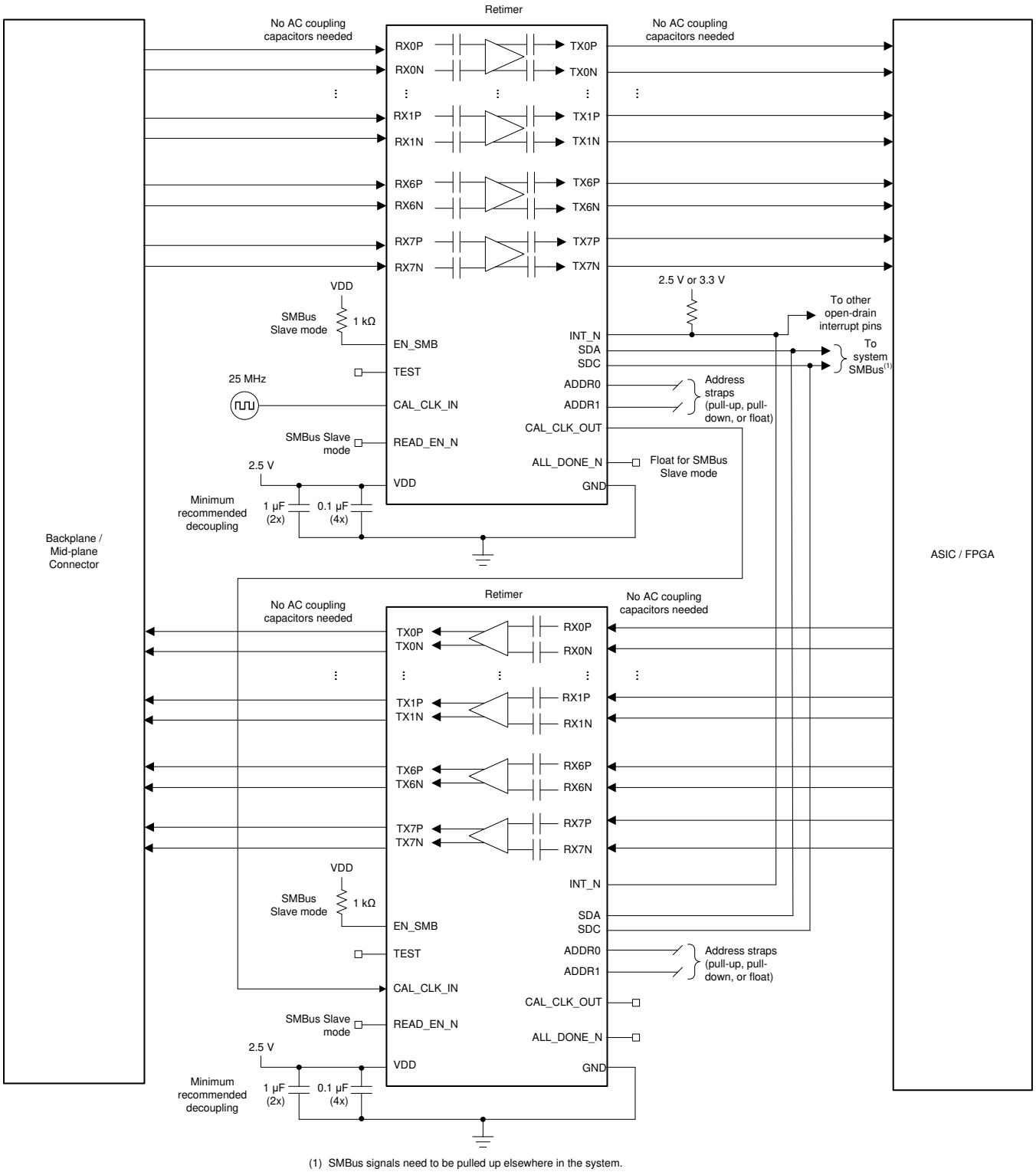


Figure 16. Backplane/Mid-plane Application Block Diagram

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Typical Application (continued)



(1) SMBus signals need to be pulled up elsewhere in the system.

Figure 17. Backplane/Mid-plane Application Schematic

10.2.2 Design Requirements

For this design example, the following guidelines outlined in Table 14 apply.

Typical Application (continued)

Table 14. Backplane/Mid-plane Application Design Guidelines

DESIGN PARAMETER	REQUIREMENT
AC coupling capacitors	Not required. AC coupling capacitors are included in the device package.
Input channel insertion loss	≤ 35 dB at 25.78125 Gbps Nyquist frequency
Output channel insertion loss	Depends on downstream ASIC / FPGA capabilities. The DS250DF810 has a low-jitter output driver with 3-tap FIR filter for equalizing a portion of the output channel.
Link partner TX launch amplitude	800 mVppd to 1200 mVppd
Link partner TX FIR filter	Depends on channel loss

10.2.3 Detailed Design Procedure

The design procedure for backplane/mid-plane applications is as follows:

1. Determine the total number of channels on the board which require a DS250DF810 for signal conditioning. This will dictate the total number of DS250DF810 devices required for the board. It is generally recommended that channels with similar total insertion loss on the board be grouped together in the same DS250DF810 device. This will simplify the device settings, as similar loss channels generally utilize similar settings.
2. Determine the maximum current draw required for all DS250DF810 retimers. This may impact the selection of the regulator for the 2.5 V supply rail. To calculate the maximum current draw, multiply the maximum transient power supply current by the total number of DS250DF810 devices.
3. Determine the maximum operational power consumption for the purpose of thermal analysis. There are two ways to approach this calculation:
   a. Maximum mission-mode operational power consumption is when all channels are locked and retransmitting the data which is received. PRBS pattern checkers/generators are not used in this mode since normal traffic cannot be checked with a PRBS checker. For this calculation, multiply the worst-case power consumption in mission mode by the total number of DS250DF810 devices.
   b. Maximum debug-mode operational power consumption is when all channels are locked and retransmitting the data which is received. At the same time, some channels' PRBS checkers or generators may be enabled. For this calculation, multiply the worst-case power consumption in debug mode by the total number of DS250DF810 devices.
4. Determine the SMBus address scheme needed to uniquely address each DS250DF810 device on the board, depending on the total number of devices identified in step 2. Each DS250DF810 can be strapped with one of 16 unique SMBus addresses. If there are more DS250DF810 devices on the board than the number of unique SMBus addresses which can be assigned, then use an I2C expander like the **TCA/PCA family of I2C/SMBus switches and multiplexers** to split up the SMBus into multiple busses.
5. Determine if the device will be configured from EEPROM (SMBus Master Mode) or from the system I2C bus (SMBus Slave Mode).
   a. If SMBus Master Mode will be used, provisions should be made for an EEPROM on the board with 8-bit SMBus address 0xA0.
   b. If SMBus Slave Mode will be used for all device configurations, an EEPROM is not needed.
6. Make provisions in the schematic and layout for standard decoupling capacitors between the device VDD supply and GND. Refer to the pin function description in *Pin Configuration and Functions* for more details.
7. Make provisions in the schematic and layout for a 25MHz (±100 ppm) single-ended CMOS clock. Each DS250DF810 retimer buffers the clock on the CAL_CLK_IN pin and presents the buffered clock on the CAL_CLK_OUT pin. This allows multiple (up to 20) retimers' calibration clocks to be daisy chained to avoid the need for multiple oscillators on the board. If the oscillator used on the board has a 2.5 V CMOS output, then no AC coupling capacitor or resistor ladder is required at the input to CAL_CLK_IN. No AC coupling or resistor ladder is needed between one retimer's CAL_CLK_OUT output and the next retimer's CAL_CLK_IN input. The final retimer's CAL_CLK_OUT output can be left floating.
8. Connect the INT_N open-drain output to an FPGA or CPU if interrupt monitoring is desired. Note that multiple retimers' INT_N outputs can be connected together since this is an open-drain output. The common INT_N net should be pulled high.

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10.2.4 Application Curves

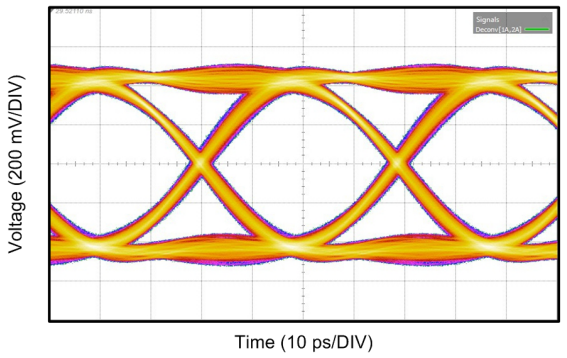


Figure 18. DS250DF810 Operating at 25.78125 Gbps

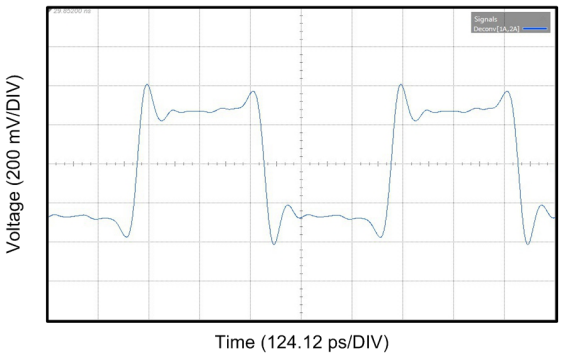


Figure 19. DS250DF810 FIR Transmit Equalization while Operating at 25.78125 Gbps

Figure 18 shows a typical output eye diagram for the DS250DF810 operating at 25.78125 Gbps with PRBS9 pattern using FIR main-cursor of +18, pre-cursor of -1 and post-cursor of +2. All other device settings are left at default.

Figure 19 shows an example of DS250DF810 FIR transmit equalization while operating at 25.78125 Gbps. In this example, the Tx FIR filter main-cursor is set to +15, post-cursor to -3 and pre-cursor to -3. An 8T pattern is used to evaluate the FIR filter, which consists of 0xFF00. All other device settings are left at default.

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11 Power Supply Recommendations

Follow these general guidelines when designing the power supply:

1. The power supply should be designed to provide the recommended operating conditions outlined in *Specifications* in terms of DC voltage, AC noise, and start-up ramp time.
2. The maximum current draw for the DS250DF810 is provided in *Specifications* . This figure can be used to calculate the maximum current the supply must provide. Typical mission-mode current draw can be inferred from the typical power consumption in *Specifications*.
3. The DS250DF810 does not require any special power supply filtering (that is, ferrite bead), provided the recommended operating conditions are met. Only standard supply decoupling is required. Refer to *Pin Configuration and Functions* for details concerning the recommended supply decoupling.

12 Layout

12.1 Layout Guidelines

The following guidelines should be followed when designing the layout:

1. Decoupling capacitors should be placed as close to the VDD pins as possible. Placing them directly underneath the device is one option if the board design permits.
2. High-speed differential signals TXnP/TXnN and RXnP/RXnN should be tightly coupled, skew matched, and impedance controlled.
3. Vias should be avoided when possible on the high-speed differential signals. When vias must be used, care should be taken to minimize the via stub, either by transitioning through most/all layers, or by back drilling.
4. GND relief can be used beneath the high-speed differential signal pads to improve signal integrity by counteracting the pad capacitance.
5. GND vias should be placed directly beneath the device connecting the GND plane attached to the device to the GND planes on other layers. This has the added benefit of improving thermal conductivity from the device to the board
6. BGA landing pads for a 0.8 mm pitch flip-chip BGA are typically 0.4 mm in diameter (exposed). The actual size of the copper pad will depend on whether solder-mask-defined (SMD) or non-solder-mask-defined solder land pads are used. For more information, refer to TI's Surface Mount Technology (SMT) References at http://focus.ti.com/quality/docs under the "Quality & Lead (Pb)-Free Data" menu.
7. If vias are used for the high-speed signals, ground via should be implemented adjacent to the signal via to provide return path and isolation. For differential pair, the typical via configuration is "ground-signal-signal-ground".

12.2 Layout Example

The following example layout demonstrates how all signals can be escaped from the BGA array using stripline routing on a generic 28-layer stackup. This example layout assumes the following:

- Trace width: 0.127 mm (5 mil)
- Trace edge-to-edge spacing: 0.152 mm (6 mil)
- VIA finished hole size (diameter): 0.203 mm (8 mil)
- VIA drilled hole size: 0.254 mm (10 mil)
- VIA-to-VIA spacing: 1.0 mm (39 mil), to enhance PCB manufacturability
- No VIA-in-pad used

Note that many other escape routing options exist using different trace width and spacing combinations. The optimum trace width and spacing will depend on the PCB material, PCB routing density, and other factors.

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Layout Example (continued)

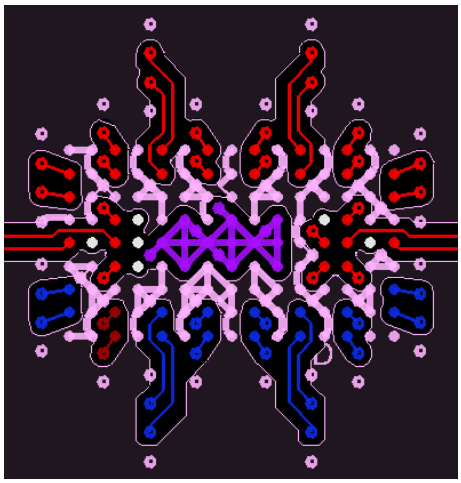


Figure 20. Top Layer

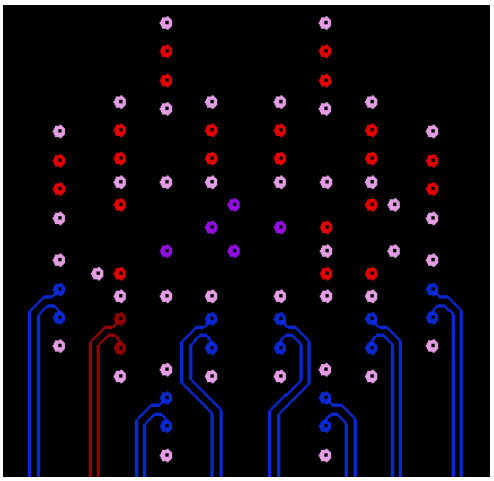


Figure 21. Internal Signal layer 1

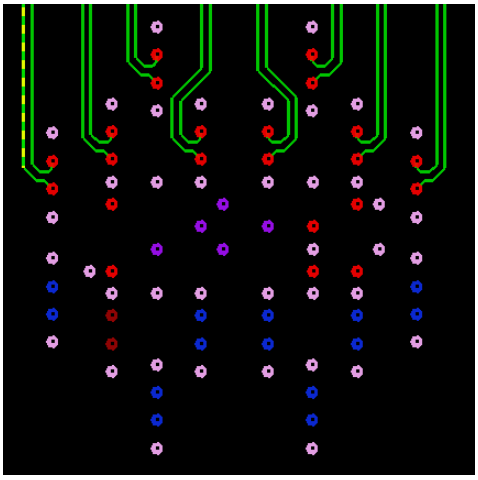


Figure 22. Internal Signal Layer 2

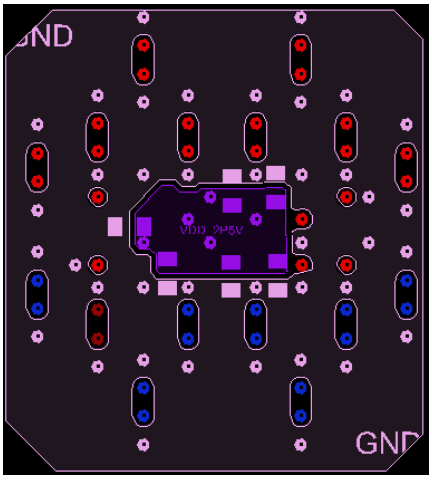


Figure 23. Bottom Layer

13 Device and Documentation Support

13.1 Device Support

13.1.1 Development Support

For additional information, see TI's Surface Mount Technology (SMT) References at:

http://focus.ti.com/quality/docs under the *Quality & Lead (Pb)-Free Data* menu.

13.2 Documentation Support

13.2.1 Related Documentation

For related documentation, see the following:

- *DS2x0DF810, DS250DFx10, DS250DF230 Programmer's Guide* (SNLU182)

Click here to request access to the DS2X0DFX10 IBIS-AMI Model and Programming Guide in the DS250DF810 MySecure folder.

13.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

13.5 Trademarks

E2E is a trademark of Texas Instruments.

13.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS250DF810ABVR	ACTIVE	FCBGA	ABV	135	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-10 to 85	DS250DF8	Samples
DS250DF810ABVT	ACTIVE	FCBGA	ABV	135	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-10 to 85	DS250DF8	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

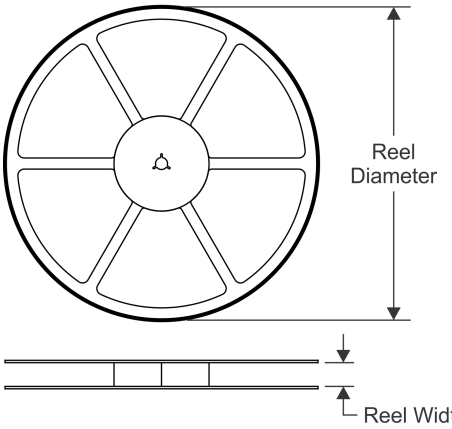
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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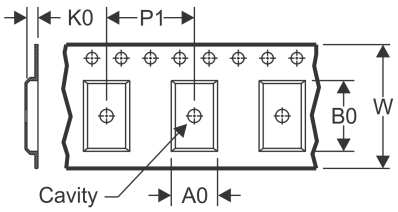
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

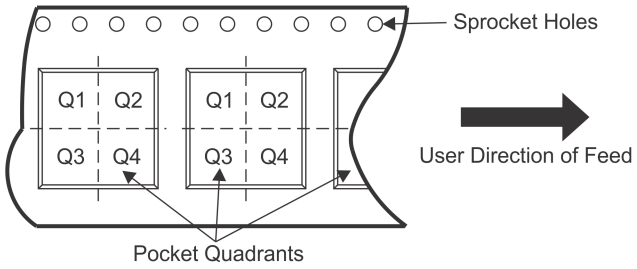


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

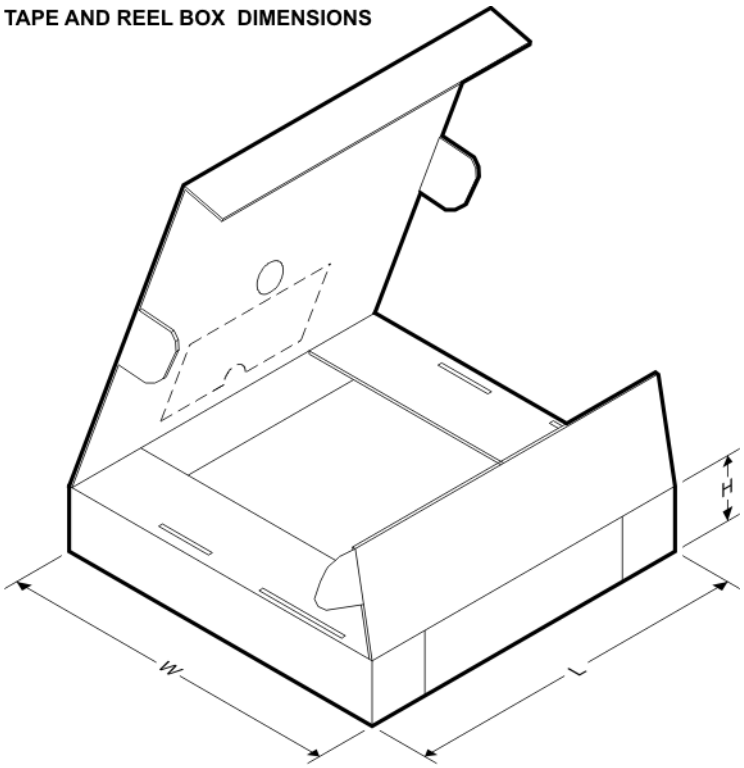
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS250DF810ABVR	FCBGA	ABV	135	1000	330.0	24.4	8.4	13.4	3.0	12.0	24.0	Q2
DS250DF810ABVT	FCBGA	ABV	135	250	178.0	24.4	8.4	13.4	3.0	12.0	24.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

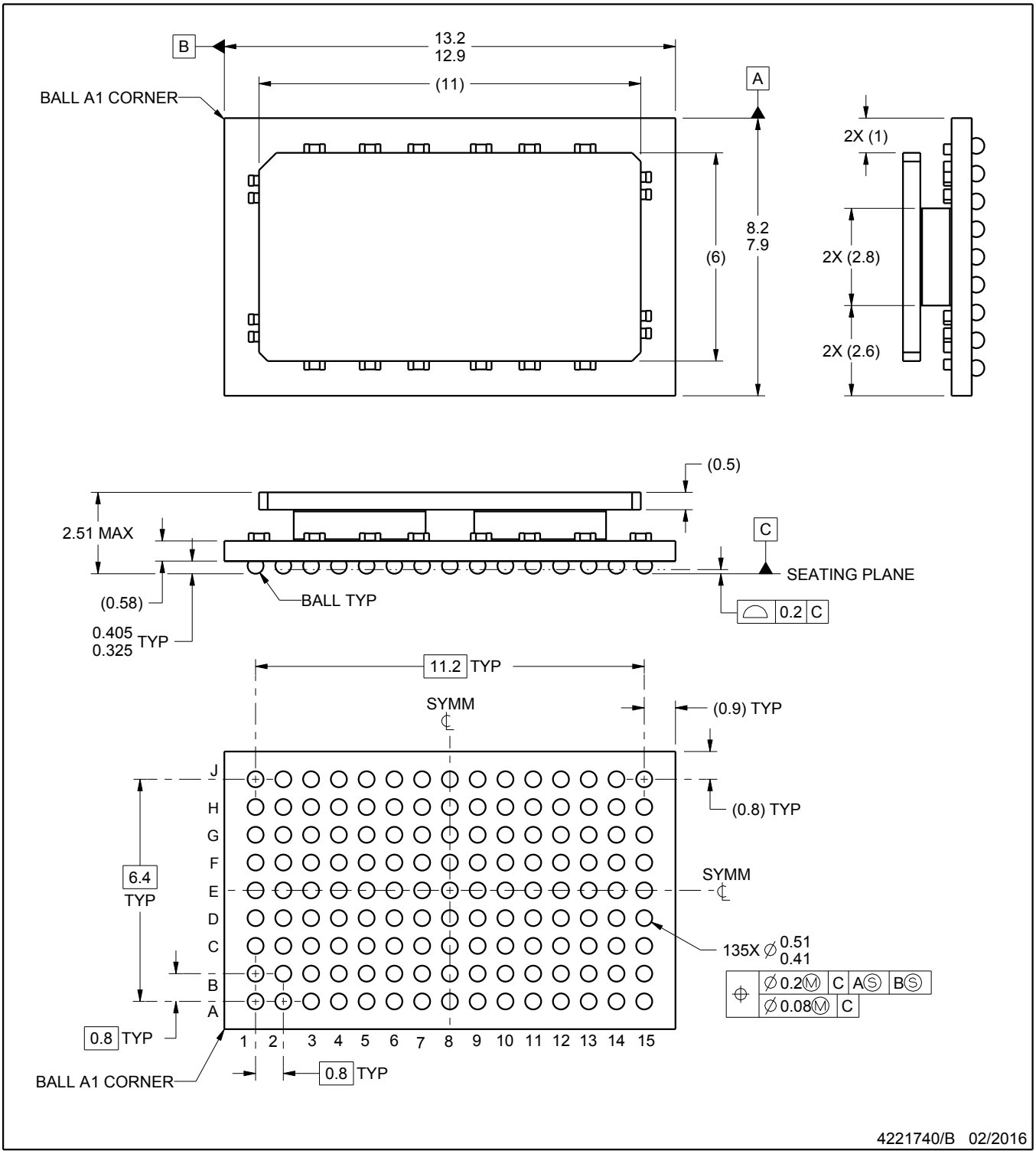
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS250DF810ABVR	FCBGA	ABV	135	1000	367.0	367.0	45.0
DS250DF810ABVT	FCBGA	ABV	135	250	213.0	191.0	55.0

PACKAGE OUTLINE

ABV0135A

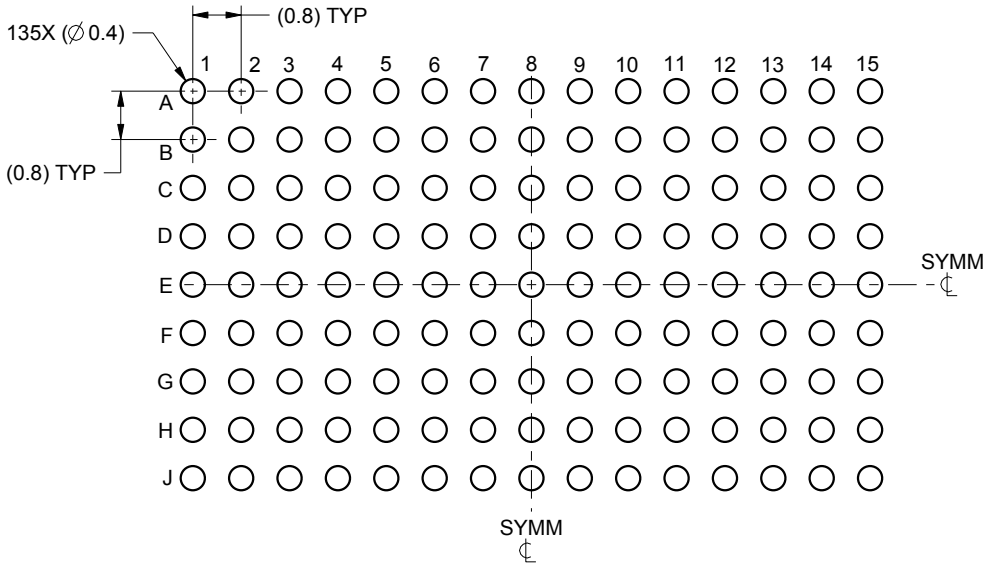
FCBGA - 2.51 mm max height

BALL GRID ARRAY

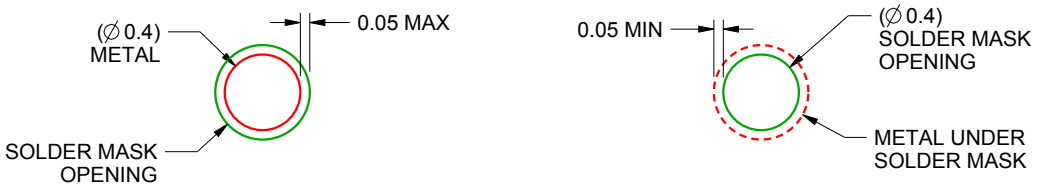


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:8X



NON-SOLDER MASK
DEFINED
(PREFERRED)

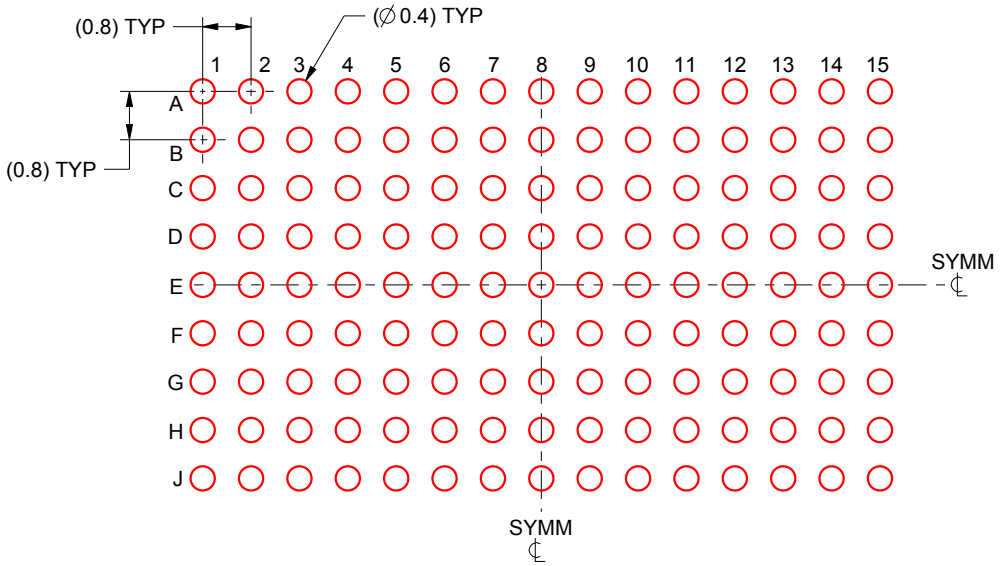
SOLDER MASK
DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

4221740/B 02/2016

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
For information, see Texas Instruments literature number SPRU811 (www.ti.com/lit/spru811).



SOLDER PASTE EXAMPLE
BASED ON 0.15 mm THICK STENCIL
SCALE:8X

4221740/B 02/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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