

PIC18F27/47/57Q43

PIC18F27/47/57Q43 Silicon Errata and Data Sheet Clarifications

The PIC18F27/47/57Q43 devices that you have received conform functionally to the current device data sheet (DS40002147C), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in the table below.

The errata described in this document will be addressed in future revisions of the PIC18F27/47/57Q43 silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

Table 1. Silicon Device Identification

Part Number	Device ID	Revision ID	
Part Number	Device iD	В0	
PIC18F27Q43	0x7480	0xA040	
PIC18F47Q43	0x74A0	0xA040	
PIC18F57Q43	0x74C0	0xA040	



Important: Refer to the **Device/Revision ID** section in the current "**PIC18FXXQ43 Family Programming Specification**" (DS40002079) for more detailed information on Device Identification and Revision IDs for your specific device.

Table 2. Silicon Issue Summary

Module	Feature	Item No.	Issue Summary	Affected Revisions
Module				В0
ADCC	Capacitive Voltage Divider	1.1.1	CVD is only functional on PORTA[2:0] and PORTB[4:0]	X
Oscillator	XT mode	1.2.1	Max. clock frequency limited to 2 MHz for XT mode	Х
Note: Only those issues indicated in the last column apply to the current silicon revision.				

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1. Silicon Errata Issues



Notice: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the bold font in the following tables apply to the current silicon revision.

1.1 Module: Analog-to-Digital Converter with Computation (ADCC)

1.1.1 Capacitive Voltage Divider (CVD)

The CVD feature is only functional on PORTA[2:0] and PORTB[4:0]. This feature is not recommended for use on any other pins.

Work around

None.

Affected Silicon Revisions

В0	
Х	

1.2 Module: Oscillator

1.2.1 Max. Clock Frequency for XT Mode is 2 MHz

The maximum clock frequency for the intermediate gain setting that supports quartz crystal and ceramic resonator operation, XT mode, is being reduced from 4 MHz to 2 MHz.

Work around

For crystal or resonator frequencies above 2 MHz, use HS mode.

Affected Silicon Revisions

В0	
X	

2. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet 40002147C):

Note:

Corrections are shown in bold. Where possible, the original bold text formatting has been removed for clarity.

2.1 Module: Temperature Indicator

2.1.1 Temperature Calculation

Equation 39-1 used to calculate the temperature using the ADC reading of the internal temperature indicator module is incorrect. The corresponding code example, **Example 39-1** is also incorrect. The correct equation and modified code example are shown below.

Equation 39-1: Sensor Temperature (in °C)

$$T_{MEAS} = \frac{\frac{(ADC_{MEAS} \times Gain)}{256} + Offset}{10}$$

Example 39-1: Temperature Calculation (°C)

APPENDIX A: Revision History

3. APPENDIX A: Revision History

Doc Rev.	Date	Comments
С	04/2020	Adding XT mode erratum and Temperature Indicator data sheet clarification.
В	02/2020	Add working pins for CVD.
Α	12/2019	Initial document release.

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