

5-V FULL-DUPLEX RS-485/RS-422 DRIVER AND BALANCED RECEIVER

FEATURES

- Designed for INTERBUS Applications
- Balanced Receiver Thresholds
- 1/2 Unit-Load (up to 64 nodes on the bus)
- Bus-Pin ESD Protection 15 kV HBM
- Bus-Fault Protection of -7V to 12V
- Thermal Shutdown Protection
- Power-Up/Down Glitch-free Bus Inputs and Outputs
- Designed for RS-422 and RS-485 Networks

APPLICATIONS

- Digital Motor Control
- Utility Meters
- Chassis-to-Chassis Interconnections
- Electronic Security Stations
- Industrial, Process, and Building Automation
- Point-of-Sale (POS) Terminals and Networks
- DTE/DCE Interfaces

DESCRIPTION

The SN65HVD179 is a differential line driver and differential-input line receiver that operates with a 5-V power supply. Each driver and receiver has separate input and output pins for full-duplex bus communication designs. They are designed for balanced transmission lines and interoperation with ANSI TIA/EIA-485A, TIA/EIA-422-B, ITU-T v.11, and ISO 8482:1993 standard-compliant devices.

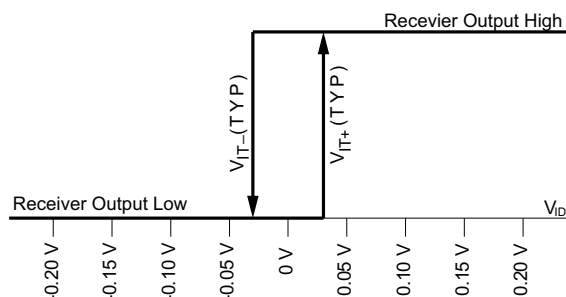
The differential bus driver and receiver are monolithic, integrated circuits designed for full-duplex bi-directional data communication on multipoint bus-transmission lines at signaling rates⁽¹⁾ up to 25 Mbps. The SN65HVD179 is fully enabled with no external enabling pins.

The 1/2 unit load receiver has a high receiver input resistance. This results in lower bus leakage currents over the common-mode voltage range, and reduces the total amount of current that a 485 driver is forced to source or sink when transmitting.

The balanced differential receiver input threshold makes the SN65HVD179 fully compatible with fieldbus requirements that define an external failsafe structure.

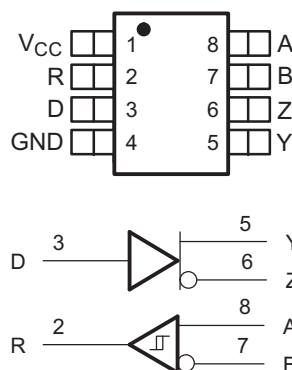
- (1) The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

BALANCED RECEIVER INPUT THRESHOLDS



SN65HVD179

D PACKAGE (TOP VIEW)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

AVAILABLE OPTIONS

SIGNALING RATE	UNIT LOADS	BASE PART NUMBER	SOIC MARKING
25 Mbps	1/2	SN65HVD179	SN65HVD179

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)^{(1) (2)}

		UNIT
V_{CC}	Supply voltage range	−0.3 V to 6 V
V_A, V_B, V_Y, V_Z	Voltage range at any bus terminal (A, B, Y, Z)	−9 V to 14 V
V_{TRANS}	Voltage input, transient pulse through 100 Ω . See Figure 8 (A, B, Y, Z) ⁽³⁾	−50 to 50 V
V_I	Voltage input range (D, DE, $\overline{RE}$)	−0.5 V to 7 V
P_{CONT}	Continuous total power dissipation	Internally limited ⁽⁴⁾
I_O	Output current (receiver output only, R)	11 mA

- (1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
- (3) This tests survivability only and the output state of the receiver is not specified.
- (4) The Thermal shutdown of this device internally limits the continuous total power dissipation. Thermal shutdown typically occurs when the junction temperature reaches 165°C.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5		5.5	V
V_I or V_{IC}	Voltage at any bus terminal (separately or common mode)		−7 ⁽¹⁾		12	
$1/t_{UI}$	Signaling rate				25	Mbps
R_L	Differential load resistance		54	60		Ω
V_{IH}	High-level input voltage	D	2		V_{CC}	V
V_{IL}	Low-level input voltage	D	0		0.8	
V_{ID}	Differential input voltage		−12		12	
I_{OH}	High-level output current	Driver	−60			mA
		Receiver	−8			
I_{OL}	Low-level output current	Driver			60	mA
		Receiver			8	
T_J	Junction temperature ⁽²⁾		−40		150	°C

- (1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.
- (2) See thermal characteristics table for information regarding this specification.

ELECTROSTATIC DISCHARGE PROTECTION

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
Human body model	Bus terminals and GND		±16		kV
Human body model ⁽²⁾	All pins		±4		
Charged-device-model ⁽³⁾	All pins		±1		

- (1) All typical values at 25°C and with a 5-V supply.
- (2) Tested in accordance with JEDEC Standard 22, Test Method A114-A.
- (3) Tested in accordance with JEDEC Standard 22, Test Method C101.

DRIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
$V_{I(K)}$	Input clamp voltage	$I_I = -18$ mA	-1.5			V
$ V_{OD(SS)} $	Steady-state differential output voltage	$I_O = 0$	4		V_{CC}	
		$R_L = 54$ Ω , See Figure 1 (RS-485)	1.7	2.6		
		$R_L = 100$ Ω , See Figure 1 (RS-422)	2.4	3.2		
		$V_{test} = -7$ V to 12 V, See Figure 2	1.6			
$\Delta V_{OD(SS)} $	Change in magnitude of steady-state differential output voltage between states	$R_L = 54$ Ω , See Figure 1 and Figure 2	-0.2		0.2	
$V_{OD(RING)}$	Differential Output Voltage overshoot and undershoot	$R_L = 54$ Ω , $C_L = 50$ pF, See Figure 5 and Figure 3 for definition			10% ⁽²⁾	
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage	See Figure 4		0.5		V
$V_{OC(SS)}$	Steady-state common-mode output voltage		2.2		3.3	
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage		-0.1		0.1	
$I_{Z(Z)}$ or $I_{Y(Z)}$	High-impedance state output current	$V_{CC} = 0$ V, V_Z or $V_Y = 12$ V, Other input at 0 V			90	μ A
		$V_{CC} = 0$ V, V_Z or $V_Y = -7$ V, Other input at 0 V	-10			
$I_{Z(S)}$ or $I_{Y(S)}$	Short Circuit output current ⁽³⁾	V_Z or $V_Y = -7$ V	-250		250	mA
		V_Z or $V_Y = 12$ V	-250		250	
I_I	Input current	$V_I = 0$, $V_I = 2$	0		100	μ A
$C_{(OD)}$	Differential output capacitance			16		pF

(1) All typical values are at 25°C and with a 5-V supply.

(2) 10% of the peak-to-peak Differential Output voltage swing, per TIA/EIA-485.

(3) Under some conditions of short-circuit to negative voltages, output currents exceeding the ANSI TIA/EIA-485-A maximum current of 250 mA may occur. Continuous exposure may affect device reliability.

DRIVER SWITCHING CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	$R_L = 54$ Ω , $C_L = 50$ pF, See Figure 5	4	8	12	ns
t_{PHL}	Propagation delay time, high-to-low-level output					
t_r	Differential output signal rise time		3	6	12	ns
t_f	Differential output signal fall time					
$t_{sk(p)}$	Pulse skew ($ t_{PHL} - t_{PLH} $)			1.4		ns
$t_{sk(pp)}$ ⁽²⁾	Part-to-part skew			1		ns

(1) All typical values are at 25°C and with a 5-V supply.

(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

RECEIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
V_{IT+}	Positive-going differential input threshold voltage	$I_O = -8$ mA			0.2	V
V_{IT-}	Negative-going differential input threshold voltage	$I_O = 8$ mA	-0.2			
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)			50		mV
V_O	Output voltage	$V_{ID} = 200$ mV, $I_O = -8$ mA, See Figure 6	4.0			V
		$V_{ID} = -200$ mV, $I_O = 8$ mA, See Figure 6			0.3	
I_A or I_B	Bus input current	V_A or $V_B = 12$ V		0.20	0.3	mA
		V_A or $V_B = 12$ V, $V_{CC} = 0$ V		0.24	0.4	
		V_A or $V_B = -7$ V	-0.35	-0.19		
		V_A or $V_B = -7$ V, $V_{CC} = 0$ V	-0.25	-0.14		
I_{CC}	Supply current	D at 0 V or V_{CC} and No Load			2.7	mA

(1) All typical values are at 25°C and with a 5-V supply.

RECEIVER SWITCHING CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	$V_I = 0$ V to 3 V, $C_L = 15$ pF, See Figure 7		24	40	ns
t_{PHL}	Propagation delay time, high-to-low-level output					
$t_{sk(p)}$	Pulse skew ($ t_{PHL} - t_{PLH} $)				5	
$t_{sk(pp)}^{(2)}$	Part-to-part skew			5		ns
t_r	Output signal rise time	$C_L = 15$ pF, See Figure 7		2	4	ns
t_f	Output signal fall time			2	4	ns

(1) All typical values are at 25°C and with a 5-V supply

(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

THERMAL CHARACTERISTICS

over operating free-air temperature range unless otherwise noted⁽¹⁾

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
θ_{JA} Junction-to-ambient thermal resistance ⁽²⁾	Low-K board ⁽³⁾ , No airflow		230.8		°C/W
	High-K board ⁽⁴⁾ , No airflow		135.1		
θ_{JB} Junction-to-board thermal resistance	High-K board		44.4		°C/W
θ_{JC} Junction-to-case thermal resistance	No board		43.5		°C/W
P_D Device power dissipation	$R_L = 60\ \Omega$, $C_L = 50\ \text{pF}$, Input to D a 50% duty cycle square wave at indicated signaling rate			420	mW
T_A Ambient air temperature	Low-K board, No airflow	-40		55	°C
	High-K board, No airflow	-40		85	
T_{JSD} Thermal shutdown junction temperature			165		°C

(1) See *Application Information* section for an explanation of these parameters.

(2) The intent of θ_{JA} specification is solely for a thermal performance comparison of one package to another in a standardized environment. This methodology is not meant to and will not predict the performance of a package in an application-specific environment.

(3) In accordance with the Low-K thermal metric definitions of EIA/JESD51-3.

(4) In accordance with the High-K thermal metric definitions of EIA/JESD51-7.

PARAMETER MEASUREMENT INFORMATION

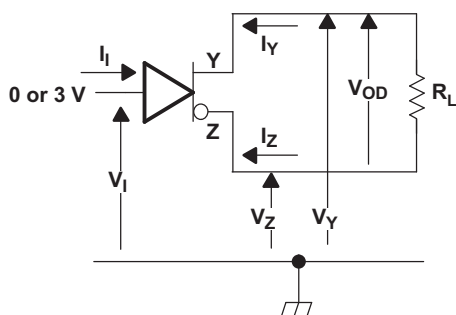


Figure 1. Driver V_{OD} Test Circuit: Voltage and Current Definitions

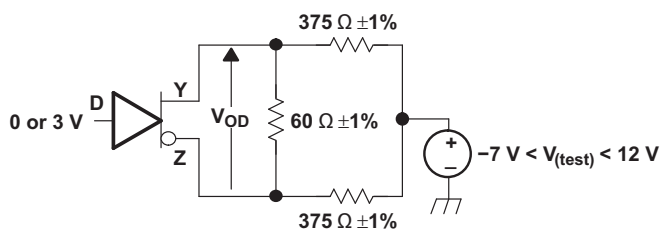


Figure 2. Driver V_{OD} With Common-Mode Loading Test Circuit

$V_{OD(RING)}$ is measured at four points on the output waveform, corresponding to overshoot and undershoot from the $V_{OD(H)}$ and $V_{OD(L)}$ steady state values.

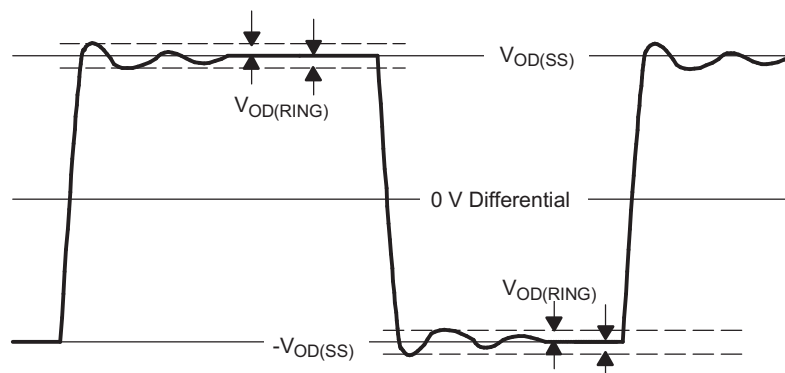


Figure 3. $V_{OD(RING)}$ Waveform and Definitions

PARAMETER MEASUREMENT INFORMATION (continued)

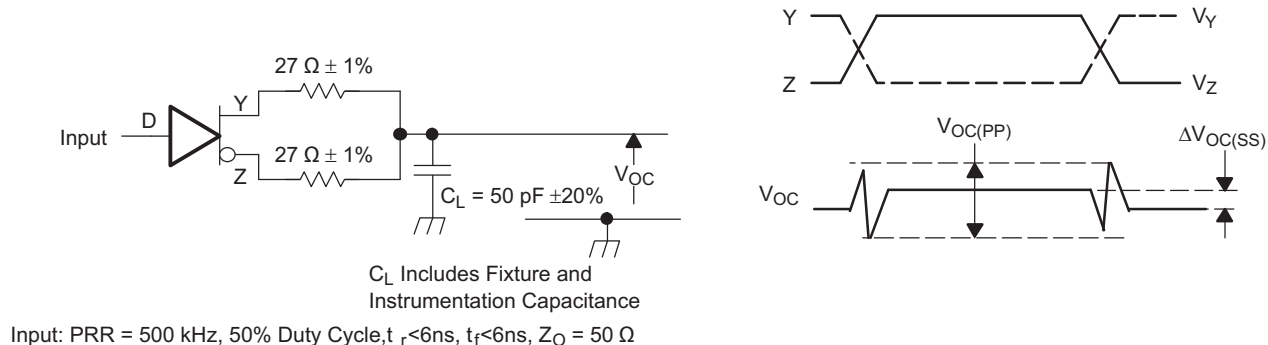


Figure 4. Test Circuit and Definitions for the Driver Common-Mode Output Voltage

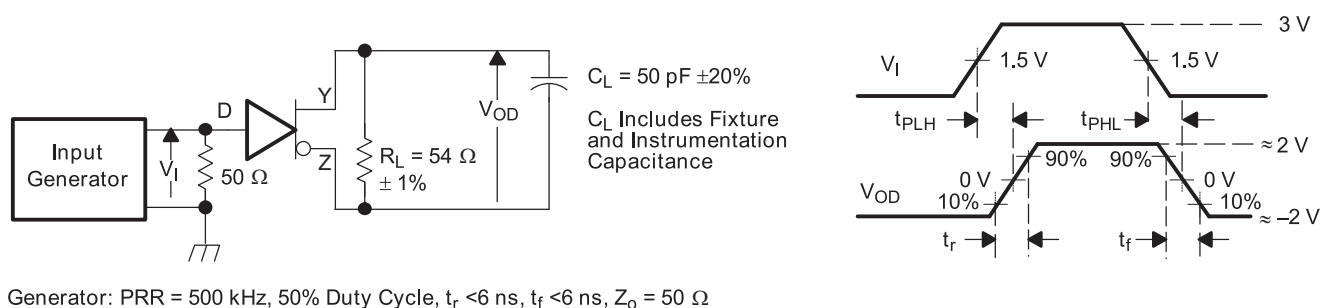


Figure 5. Driver Switching Test Circuit and Voltage Waveforms

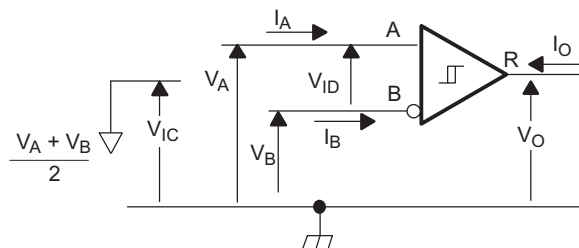


Figure 6. Receiver Voltage and Current Definitions

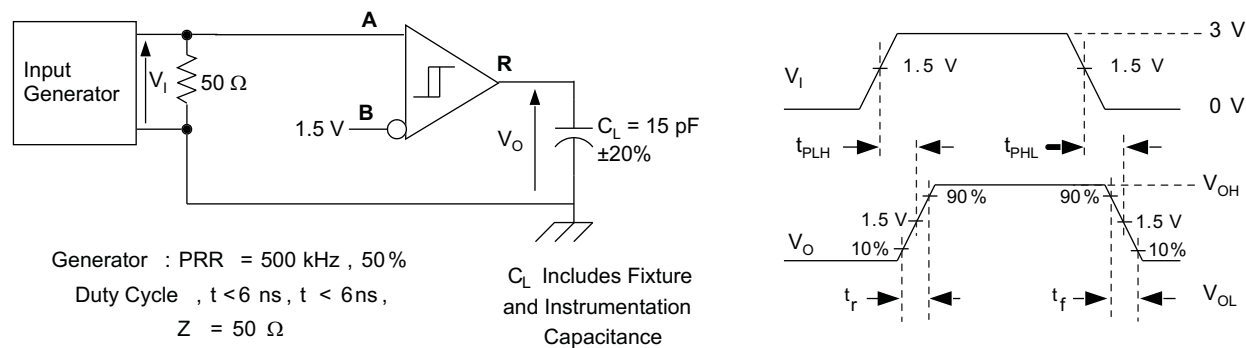


Figure 7. Receiver Switching Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)

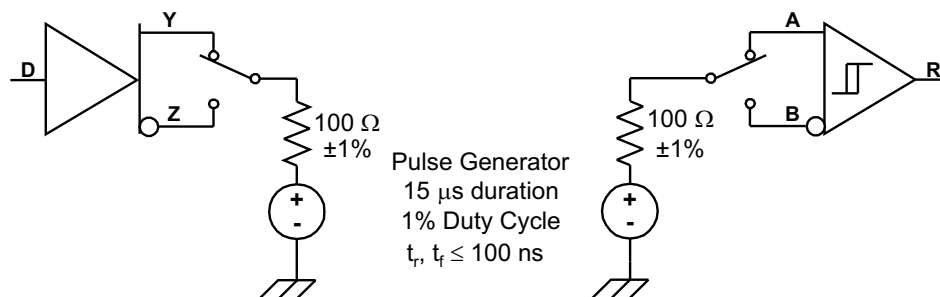
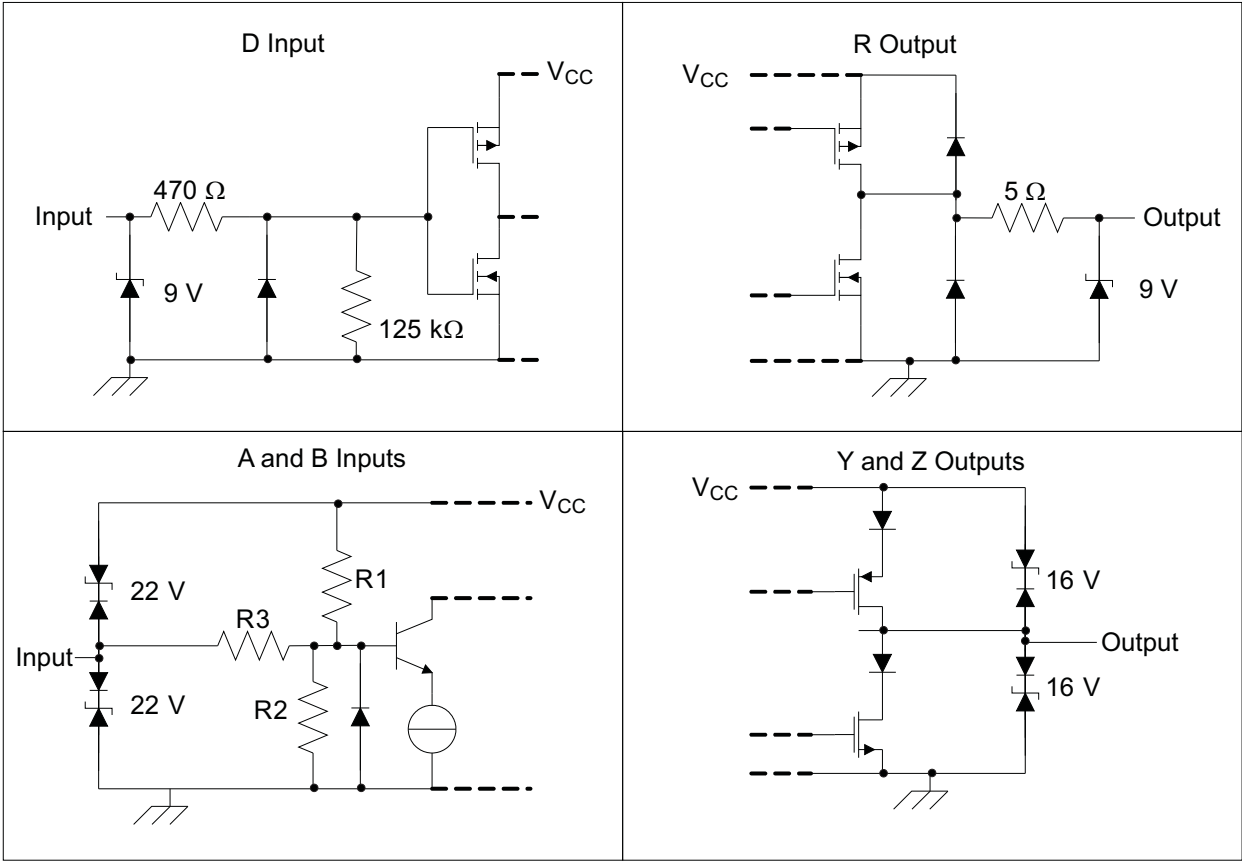


Figure 8. Test Circuit, Transient Overvoltage Test

FUNCTION TABLES

DRIVER			RECEIVER	
INPUT	OUTPUTS		DIFFERENTIAL INPUTS	OUTPUTS
D	Y	Z	$V_{ID} = V_A - V_B$	R
H	H	L	$V_{ID} \leq -0.2$ V	L
L	L	H	-0.2 V $< V_{ID} < 0.2$ V	?
Open	L	H	0.2 V $\leq V_{ID}$	H

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



	R1/R2	R3
SN65HVD179	9 kΩ	45 kΩ

TYPICAL CHARACTERISTICS

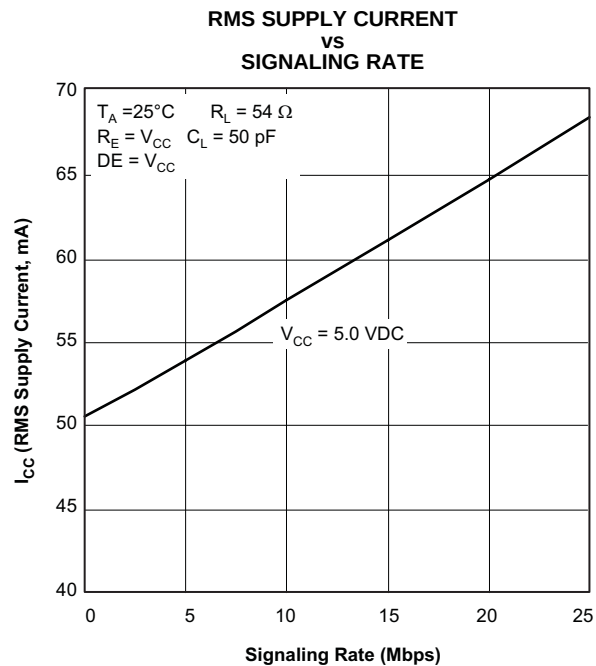


Figure 9.

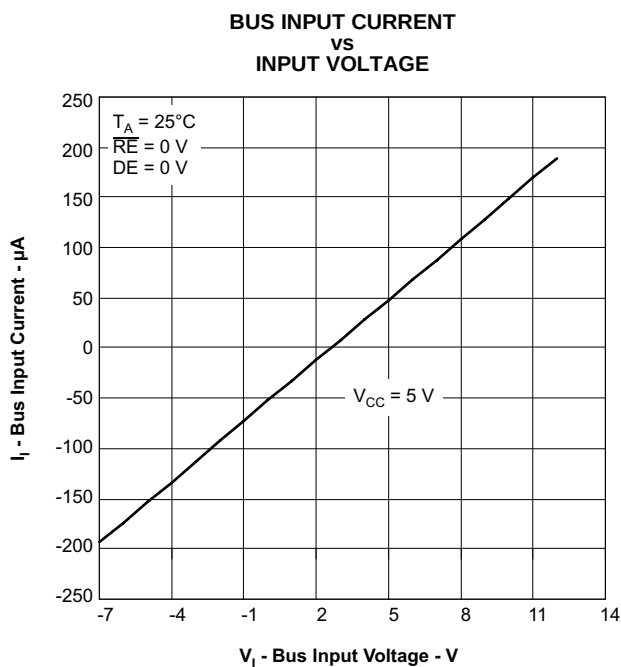


Figure 10.

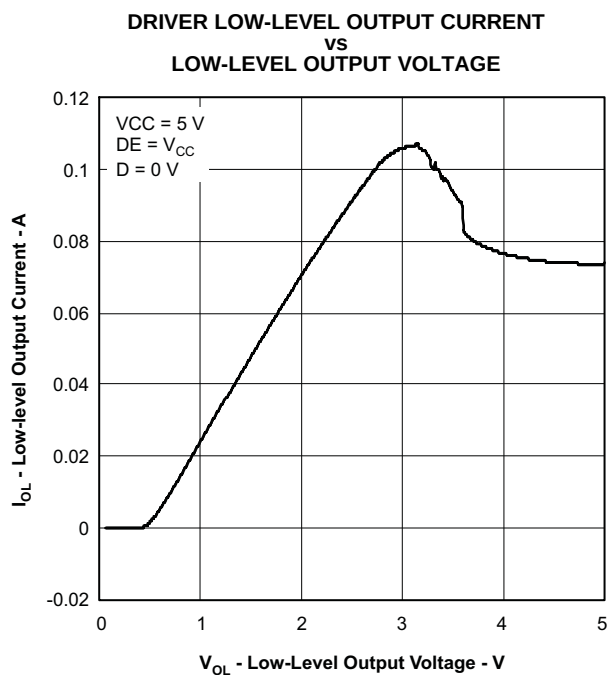


Figure 11.

TYPICAL CHARACTERISTICS (continued)

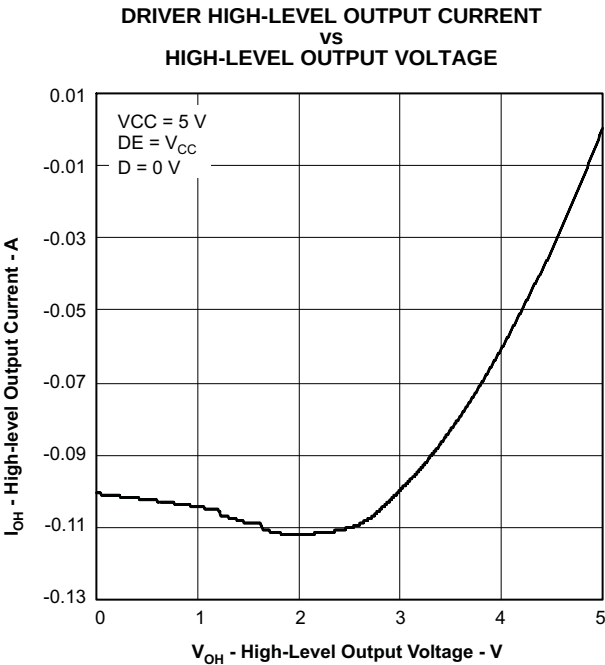


Figure 12.

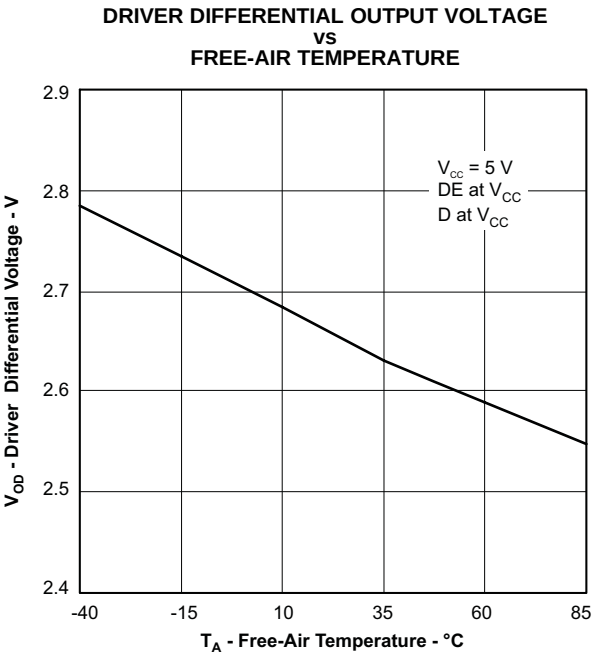


Figure 13.

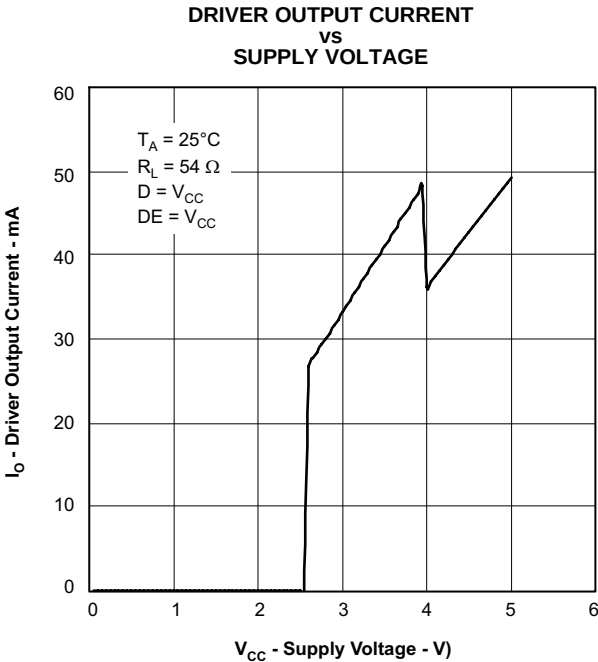


Figure 14.

APPLICATION INFORMATION

THERMAL CHARACTERISTICS OF IC PACKAGES

θ_{JA} (**Junction-to-Ambient Thermal Resistance**) is defined as the difference in junction temperature to ambient temperature divided by the operating power.

θ_{JA} is not a constant and is a strong function of:

- the PCB design (50% variation)
- altitude (20% variation)
- device power (5% variation)

θ_{JA} can be used to compare the thermal performance of packages if the specific test conditions are defined and used. Standardized testing includes specification of PCB construction, test chamber volume, sensor locations, and the thermal characteristics of holding fixtures. θ_{JA} is often misused when it is used to calculate junction temperatures for other installations.

TI uses two test PCBs as defined by JEDEC specifications. The low-K board gives *average* in-use condition thermal performance, and it consists of a single copper trace layer 25 mm long and 2-oz thick. The high-K board gives best case in-use condition, and it consists of two 1-oz buried power planes with a single copper trace layer 25 mm long and 2-oz thick. A 4% to 50% difference in θ_{JA} can be measured between these two test cards

θ_{JC} (**Junction-to-Case Thermal Resistance**) is defined as difference in junction temperature to case divided by the operating power. It is measured by putting the mounted package up against a copper block cold plate to force heat to flow from die, through the mold compound into the copper block.

θ_{JC} is a useful thermal characteristic when a heatsink applied to package. It is *not* a useful characteristic to predict junction temperature because it provides pessimistic numbers if the case temperature is measured in a nonstandard system and junction temperatures are backed out. It can be used with θ_{JB} in 1-dimensional thermal simulation of a package system.

θ_{JB} (**Junction-to-Board Thermal Resistance**) is defined as the difference in the junction temperature and the PCB temperature at the center of the package (closest to the die) when the PCB is clamped in a cold-plate structure. θ_{JB} is only defined for the high-K test card.

θ_{JB} provides an overall thermal resistance between the die and the PCB. It includes a bit of the PCB thermal resistance (especially for BGA's with thermal balls) and can be used for simple 1-dimensional network analysis of package system, see [Figure 15](#).

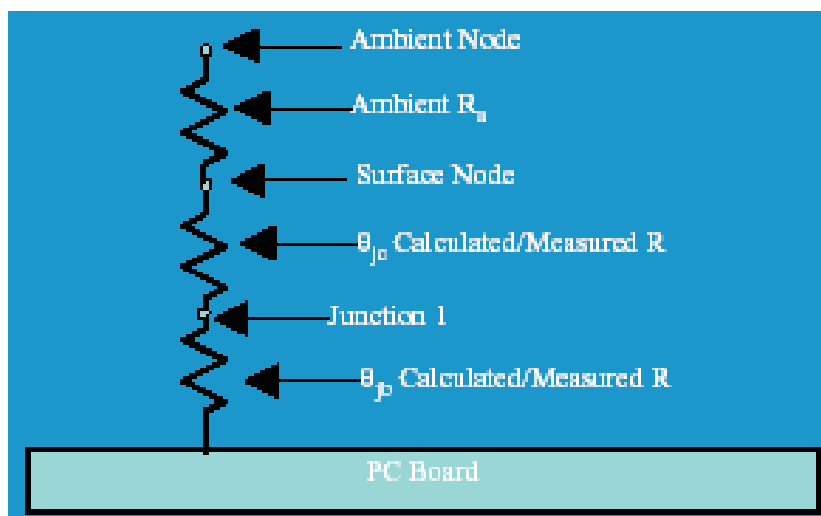


Figure 15. Thermal Resistance

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65HVD179D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP179	Samples
SN65HVD179DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP179	Samples
SN65HVD179DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP179	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

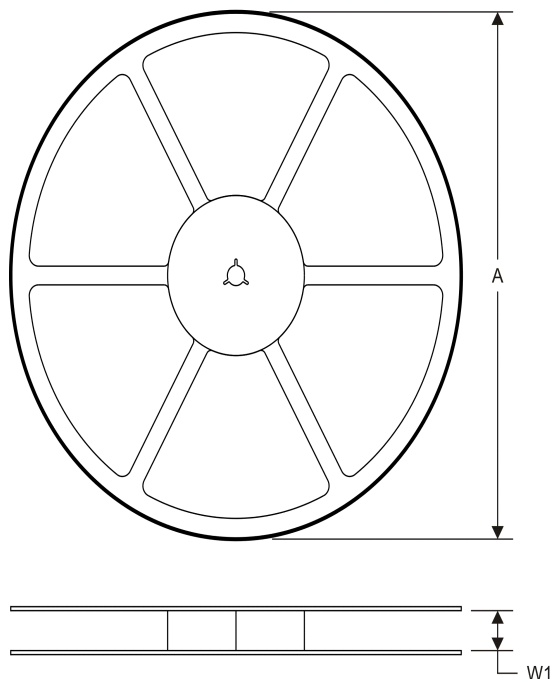
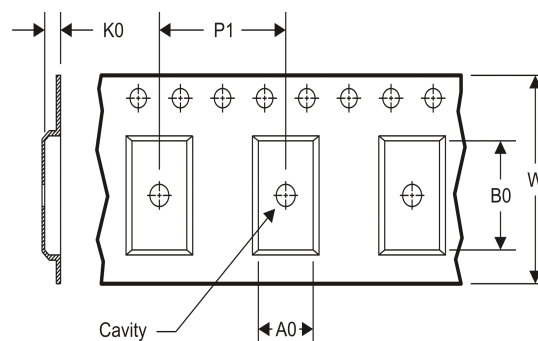


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PACKAGE OPTION ADDENDUM

6-Feb-2020

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


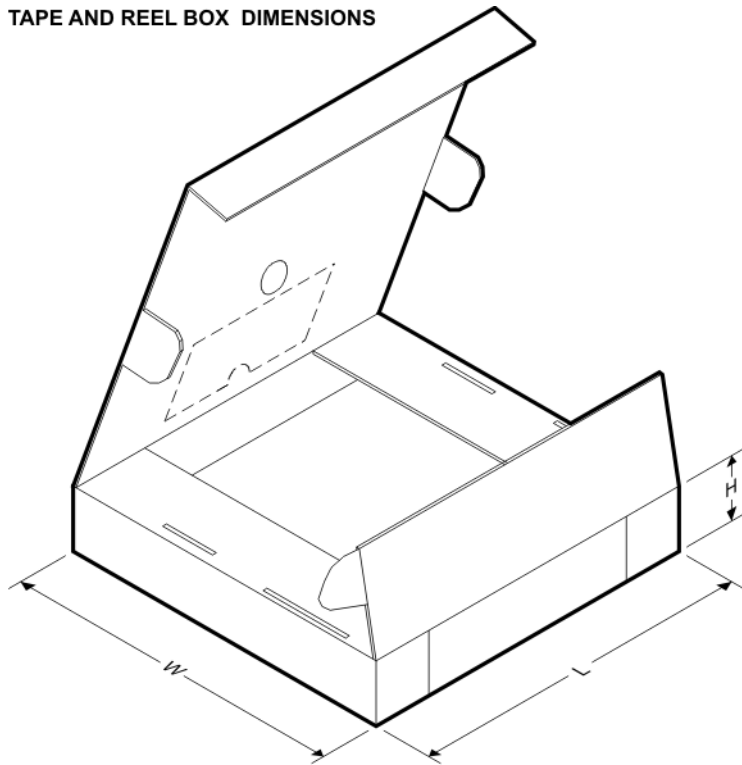
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD179DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD179DR	SOIC	D	8	2500	367.0	367.0	35.0



PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

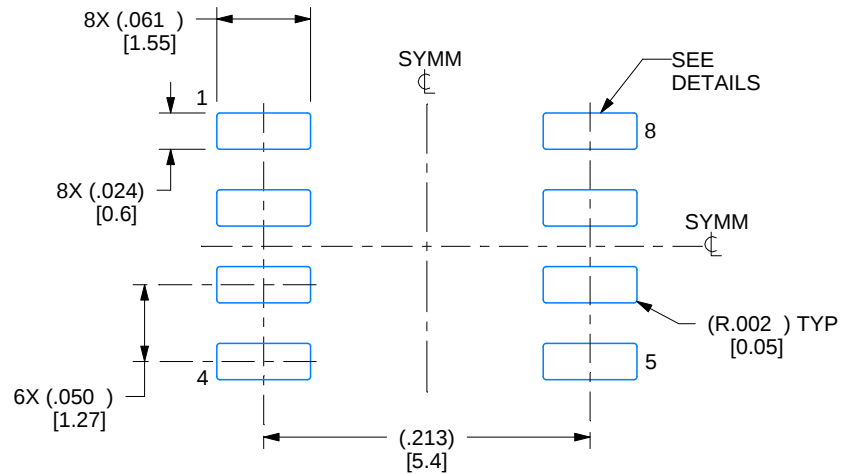


1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

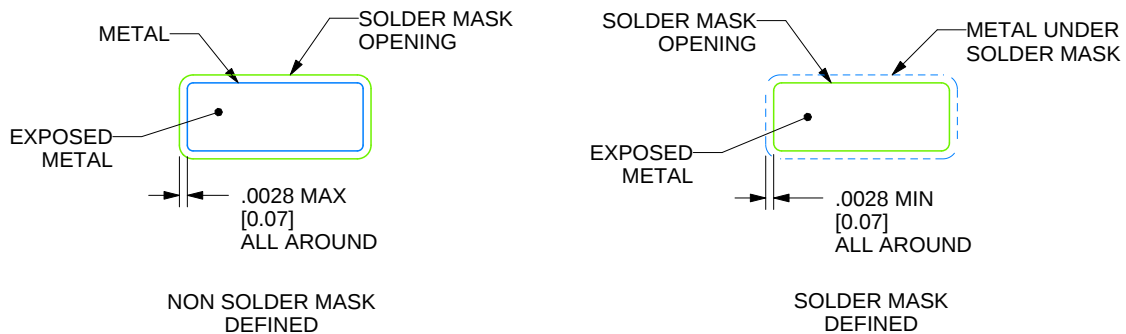
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

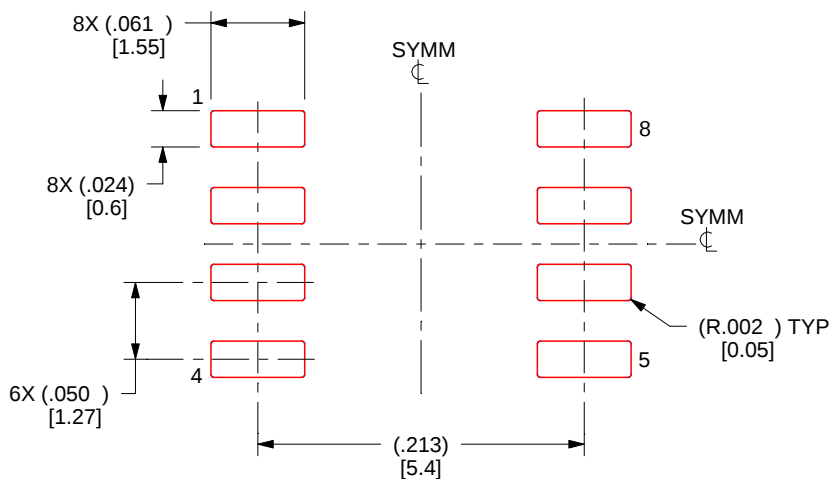
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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