dsPIC33FJ32MC204

dsPIC33FJ32MC204 PIM Information Sheet

The dsPIC33FJ32MC204 PIM is designed to demonstrate the capabilities of the dsPIC33FJ32MC204 family of general purpose devices using the Explorer 16 Development Board and the PICtail™ Plus daughter boards.

The dsPIC33FJ32MC204 is a high-performance 16-bit digital signal controller within a small 44-pin QFN package.

The dsPIC33FJ32MC204 is equipped with Peripheral Pin Select (PPS), which allows many of the digital peripherals to be remapped to use any number of pins on the device.

The PIM takes advantage of PPS by using zero ohm resistors to connect the I/O to the 100-pin Explorer 16 Development Board. Simply removing the zero ohm resistors and using the test points associated with each I/O pin (i.e., Pin1, Pin2, etc.), allows the designer to reroute the pin to any of the available pins on the Explorer 16 Development Board. This capability enables easier and faster design times.

Table 1 shows the mapping between the Explorer 16 functions and the device pins.

TABLE 1: 44-PIN TO 100-PIN PINOUT

Device Pin Number	dsPIC33FJ32MC204	PIM Pin Number	Functional Description
1	SDA1/RP9/CN21/RB9	19	Fault Reset
2	PWM2H1/RP22/CN18/RC6	77	Data 2
3	INT0/RP23/CN23/RB7	78	Data 3
4	TCK/PWM2H1/SCL1/RP24/CN22/RB8	68, 20	Hall Sensor A/QEB_POT
5	TDO/PWM2L1/SDA1/RP25/CN21/RB9	69, 21	Hall Sensor B/QEA
6	VSS	65	
7	VCAP/VDDCORE	85	
8	TDI/PWM1H3/RP10/CN16/RB10	3	PWM1H3
9	TMS/PWM1L3/RP11/CN15/RB11	100	PWM1L3
10	PWM1H2/RP12/CN14/RB12	99	PWM1H2
11	PWM1L2/RP13/CN13/RB13	98	PWM1L2
12	TMS/RA10		
13	TCK/RA7	71	PWM Enable
14	PWM1H1/RP14/CN12/RB14	94	PWM1H1
15	PWM1L1/RP15/CN11/RB15	93	PWM1L1
16	AVSS	31	
17	AVDD	30	
18	$\overline{\text{MCLR}}$	13	
19	AN0/VREF+/CN2/RA0	25	Phase 1 Current Feedback
20	AN1/VREF-/CN3/RA1	24	Phase 2 Current Feedback
21	PGED1/EMUD1/AN2/C2IN-/RP0/CN4/RB0	35	DC Bus
22	PGEC1/EMUC1/AN3/C2IN+/RP1/CN5/RB1	41	Phase 1 Voltage Feedback
23	AN4/RP2/CN6/RB2	42	Phase 2 Voltage Feedback
24	AN5/RP3/CN7/RB3	43	Phase 3 Voltage Feedback
25	AN6/RP16/CN8/RC0		
26	AN7/RP17/CN9/RC1	20	QEB_POT
27	AN8/RP18/CN10/RC2	32	Bus Shunt
28	VDD	16	
29	VSS	15	
30	OSCI/CLKI/CN30/RA2	63	OSC1
31	OSCO/CLKO/CN29/RA3	64	OSC2
32	TDO/RA8	83	Switch 1
33	SOSCI/RP4/CN1/RB4	84	Switch 2
34	SOSCO/T1CK/CN0/RA4	81	Enable
35	TDI/RA9	82	RD/WR
36	RP19/CN28/RC3	44	RS
37	RP20/CN25/RC4	72	Data 0
38	RP21/CN26/RC5	76	Data 1
39	VSS	36	
40	VDD	37	
41	PGED3/EMUD3/ASDA1/RP5/CN27/RB5	27	Debug
42	PGEC3/EMUC3/ASCL1/RP6/CN24/RB6	26	Debug
43	INT0/RP7/CN23/RB7	22, 70	Index/Hall Sensor C
44	SCL1/RP8/CN22/RB8	18	Fault A

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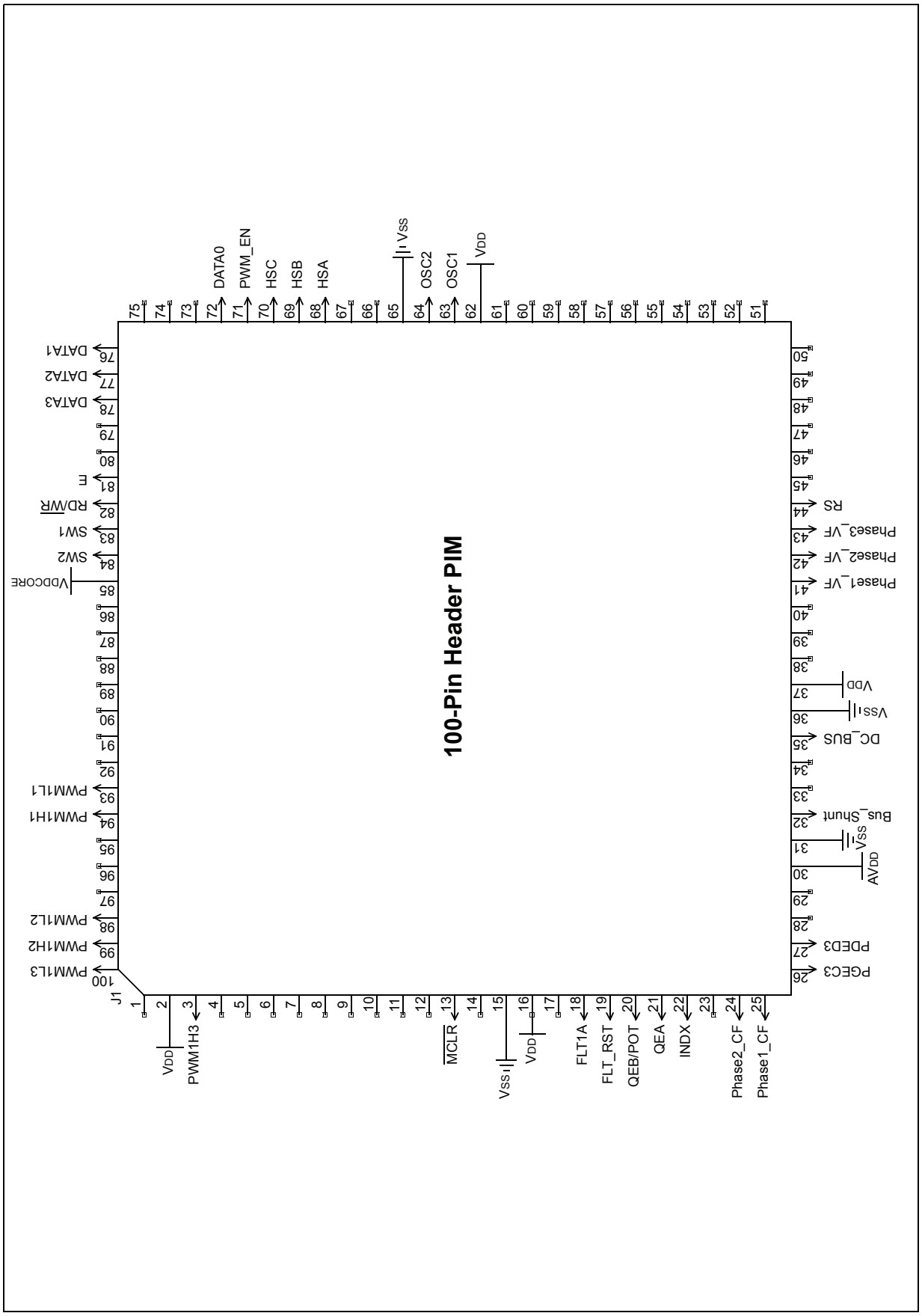


FIGURE 1: 100-PIN HEADER SCHEMATIC

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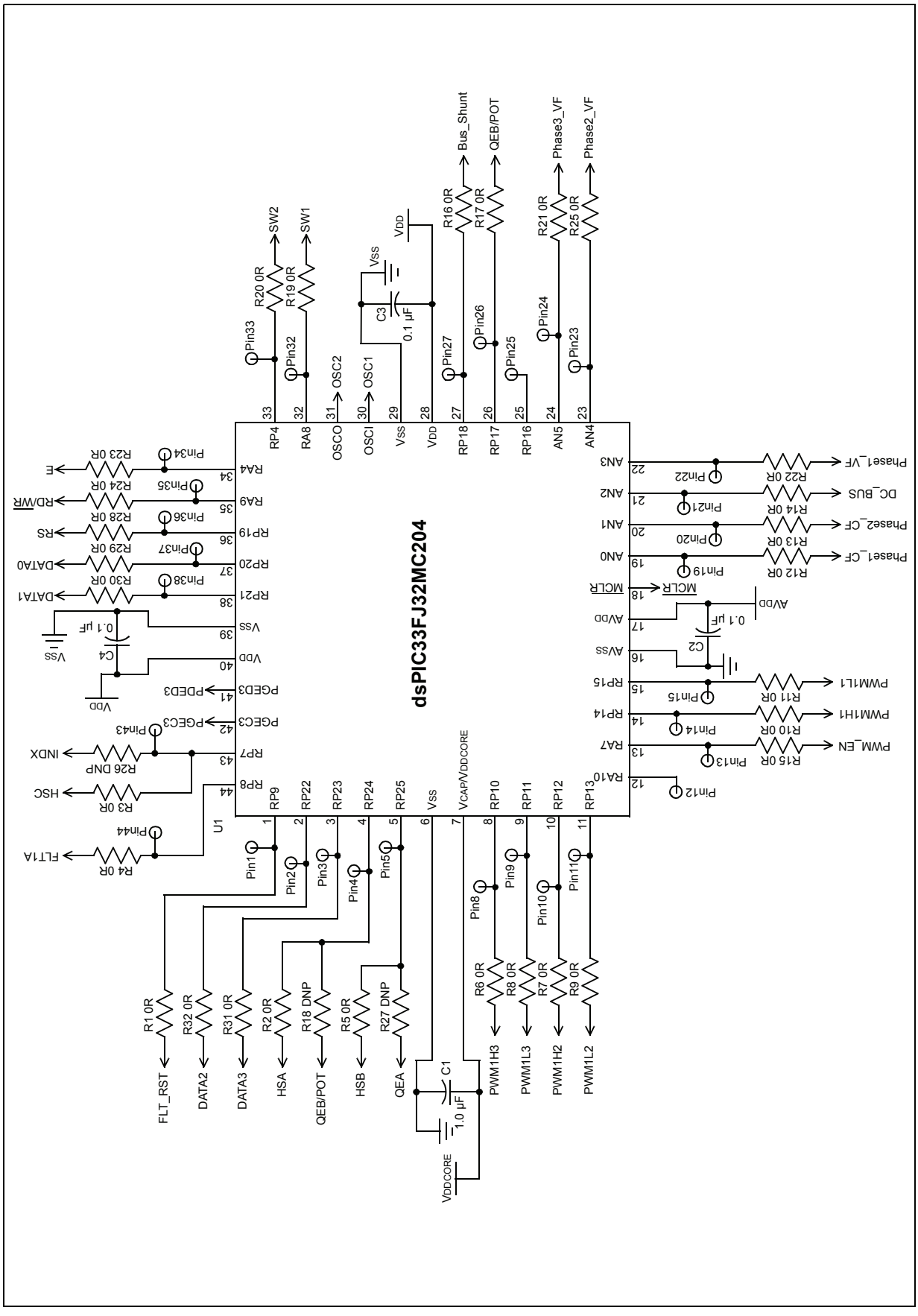


FIGURE 2: 44-PIN DEVICE SCHEMATIC

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