TPD3F303 ESD Protection and EMI Filter for SIM Card Interface

1 Features

- Bidirectional EMI Filtering and Line Termination With Integrated ESD Protection
  - –3-dB Bandwidth 300 MHz
- IEC 61000-4-2 Level 4 ESD Protection
  - ±15-kV Contact Discharge
  - ±15-kV Air Gap Discharge
- DC Breakdown Voltage: 6 V (Minimum)
- Low Leakage Current: 0.1 µA (Maximum)
- Low Noise C-R-C Filter Topology
- Integrated V_{CC} Clamp Eliminates the Need for External ESD Protection
- Space-Saving DPV (0.5-mm Pitch), DQD Packages (0.4-mm Pitch)

2 Applications

- End Equipment
  - Cell Phones
  - Tablets
  - PDAs
  - Hotspots
- Interfaces
  - SIM Cards

3 Description

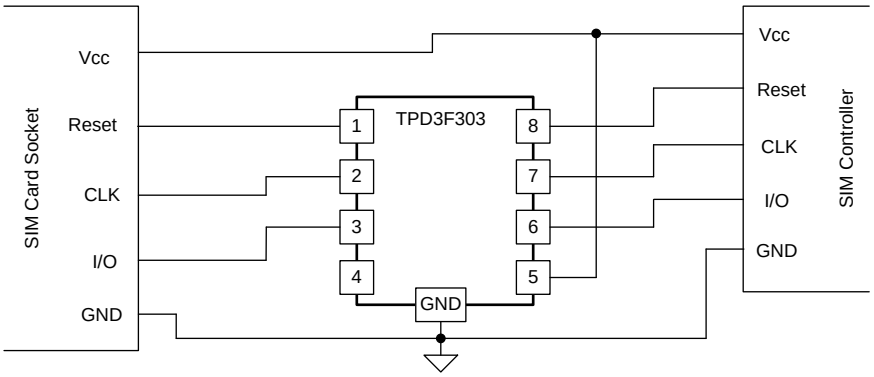
The TPD3F303 device is a highly-integrated device that provides a three-channel Electromagnetic Interference (EMI) filter and a Transient Voltage Suppressor (TVS) based ESD protection diode array. The C-R-C based low-pass filter provides EMI protection for the data, clock, and reset lines of a SIM Card interface. Furthermore, the four-channel TVS Diode array provides IEC 61000-4-2 level 4 ESD protection for the previously mentioned signals (data, clock, reset) and the V_{CC} power line. The TPD3F303 contains a 47-Ω termination resistor for the clock line and 100-Ω termination resistor for both the data and reset lines. The high level of integration offered by the TPD3F303 makes the device well-suited for applications like cell phones, tablets, hotspots, and PDAs.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPD3F303	WSON (8)	1.35 mm × 1.70 mm
	USON (8)	1.60 mm × 2.10 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic



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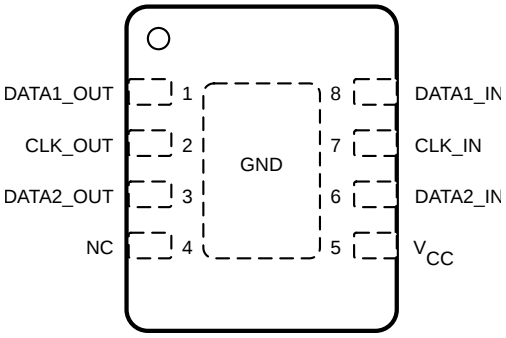
4 Revision History

Changes from Original (January 2011) to Revision A **Page**

- Added *Device Information* table, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1

5 Pin Configuration and Functions

DQD or DPV Package
8-Pin WSON or USON
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
CLK_OUT	2	Output	Clock Input and Output signals.
CLK_IN	7	Input	
DATA1_IN	8	Input	Data and Rest signals Input, Output pins. The DATA1 and DATA2 are symmetric circuits. They can be used interchangeably for either DATA or RESET pins based off board layout scheme.
DATA2_IN	6		
DATA1_OUT	1	Output	
DATA2_OUT	3		
GND	GND	Ground	Ground connection for the EMI filter. It is very important to connect the device GND to the printed circuit board ground plane through Vias directly under the package.
NC	4	No Connect	Not connected to any internal circuit. Leave this pin floating.
V_{CC}	5	Power Clamp	ESD Clamp circuit for the V_{CC} pin.

6 Specifications

6.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
	I/O voltage tolerance	I/O pins		5.5	V
T_A	Operating free-air temperature		–40	85	°C
T_{stg}	Storage temperature		–55	155	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±15000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings – Surge Protection

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 contact discharge	±15000	V
		IEC 61000-4-2 air-gap discharge	±15000	

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IO}	Input pin voltage	0	5.5	V
T_A	Operating free-air temperature	–40	85	°C

6.5 Thermal Information

THERMAL METRIC(1)		TPD3F303		UNIT
		DPV (USON)	DQD (WSON)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	90	92.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	93.4	103.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	41.1	36	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.9	6.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	41	35.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	15.6	16.4	°C/W

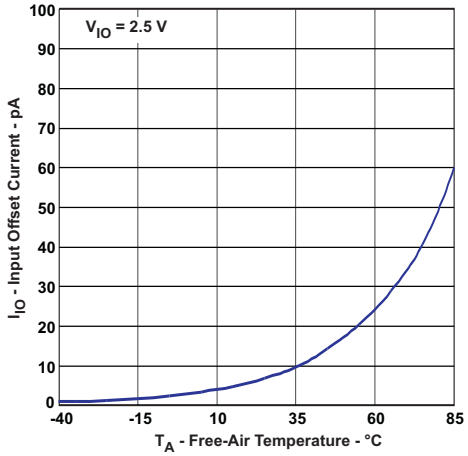
(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{clamp}	Clamp voltage	$I_{I/O}$ = ±2 A	I/O pin to ground			±10	V
I_I	Leakage current	R_{PU} = Open	I/O pin to ground			0.1	µA
R_{CLK}	CLK series resistors			40	47	55	Ω
R_{DAT_RST}	Data/RST series resistors			85	100	115	Ω
C_{Total}	IO Capacitance	$V_{I/O}$ = 0 V	I/O Pins to GND	16	20	24	pF
V_{BR}	Break-down Voltage	$I_{I/O}$ = 1 mA		6			V
F_{-3dB}	–3-dB BW for DATA/RESET line	Z_{SOURCE} = 50 Ω Z_{LOAD} = 50 Ω			294		MHz
F_{-3dB}	–3-dB BW for CLK line	Z_{SOURCE} = 50 Ω Z_{LOAD} = 50 Ω			308		MHz

6.7 Typical Characteristics



V_{IO} = 2.5 V

Figure 1. I_{IO} vs Temperature

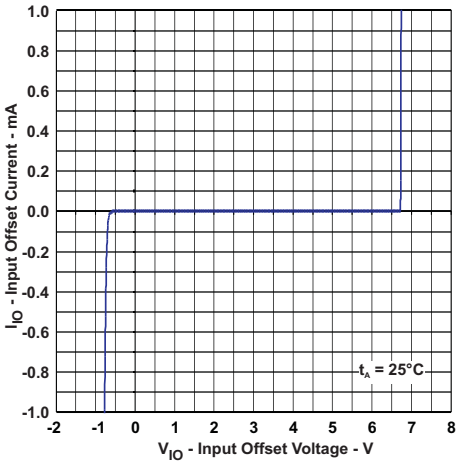


Figure 2. I_{IO} vs V_{IO}

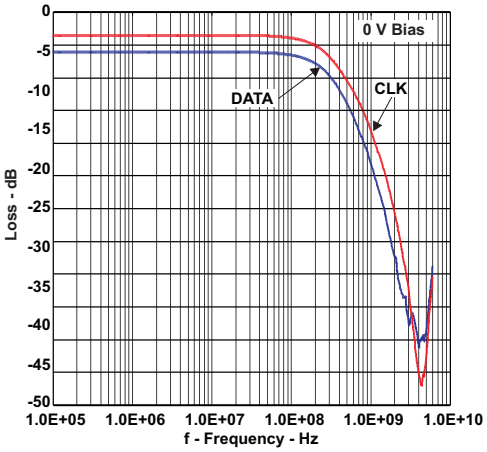


Figure 3. Frequency Response Data (0-V Bias)

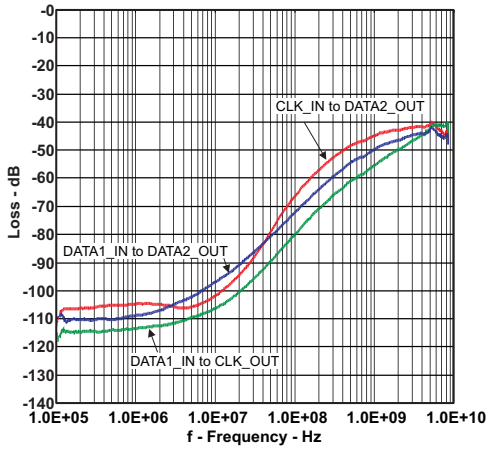
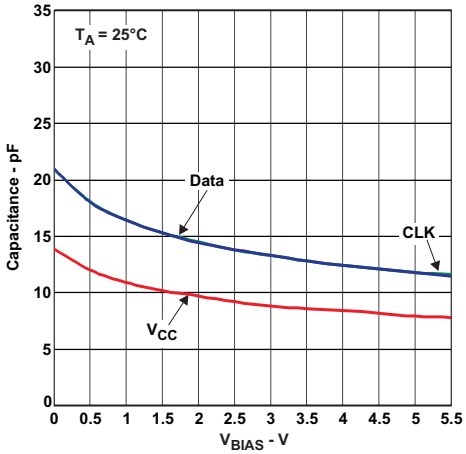


Figure 4. Channel-to-Channel Crosstalk



T_A = 25°C

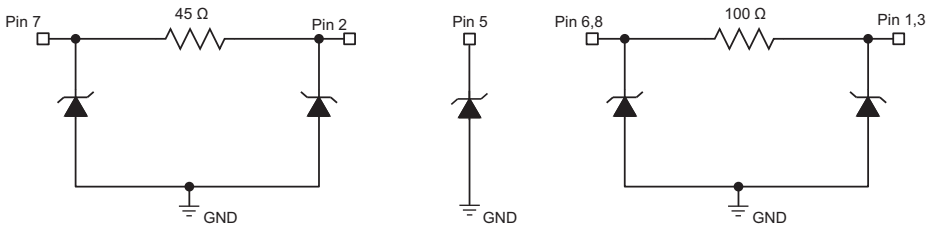
Figure 5. Capacitance vs V_{BIAS}

7 Detailed Description

7.1 Overview

The TPD3F303 is a highly-integrated three-channel EMI filter and unidirectional TVS based protection diode array. This device can be used for a range of applications such as cell phones, tablets, hotspots, and PDAs.

7.2 Functional Block Diagram



Schematic for CLK Line

Schematic for V_{CC}

Schematic for DATA1, DATA2 Lines

7.3 Feature Description

7.3.1 Bidirectional EMI Filtering and Line Termination With Integrated ESD Protection

This device provides bidirectional EMI filtering, integrated line-termination resistors, and integrated ESD protection.

7.3.2 IEC 61000-4-2 ESD Protection

The ESD protection on all pins exceeds the IEC 61000-4-2 level 4 standard. Contact and air-gap ESD is rated at ±15 kV.

7.3.3 DC Breakdown Voltage

The DC breakdown voltage of this device is 6 V minimum.

7.3.4 Low Leakage Current

The I/O pins of this device feature a low leakage current of 0.1-µA maximum.

7.3.5 Low Noise C-R-C Filter Topology

This device has a C-R-C filter topology composed of a series resistor with two capacitors in parallel with the I/O pins. The typical resistor value for the DATA1 and DATA2 pins is 100 Ω and 45 Ω for the CLK pins. The typical capacitance on all lines is 20 pF when biased at 0 V.

7.3.6 Integrated V_{CC} Clamp

This device integrates an ESD clamp for the V_{CC} pin, which eliminates the need for additional components.

7.3.7 Space-Saving Packages

The layout of this device makes it easy to add protection to existing layouts. The packages offer flow-through routing which requires minimal changes to existing layout for addition of these devices. Additionally, the device is offered in two small space-saving packages that take up minimal footprint on the board.

7.4 Device Functional Modes

The TPD3F303 is a passive integrated circuit that triggers when voltages are above V_{BR} or below V_f (–0.7 V). During ESD events, voltages as high as ±15 kV (air or contact) can be directed to ground through the internal diode network. When the voltages on the protected line fall below the trigger levels of TPD3F303 (usually within 10s of nanoseconds) the device reverts to passive.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPD3F303 is a diode type TVS + EMI filter which is used to provide a path to ground for dissipating ESD events on signal lines between a SIM card slot and a system. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC across the termination resistors.

8.2 Typical Application

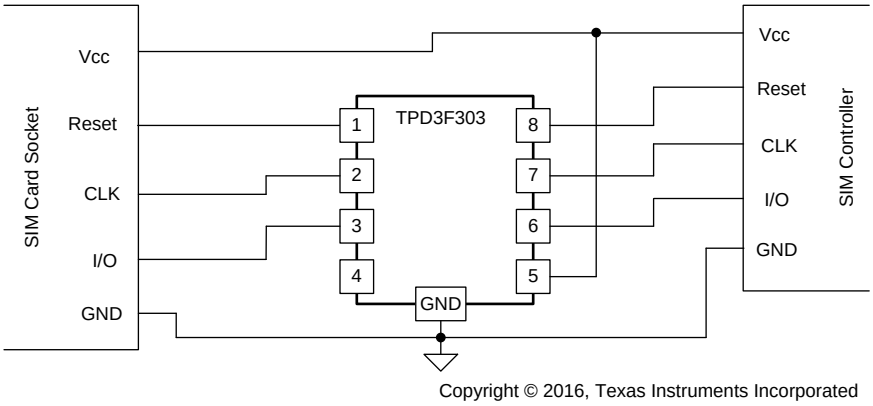


Figure 6. Typical SIM Card Application

8.2.1 Design Requirements

For this design example, one TPD3F303 is used to protect a SIM card interface. Table 1 lists the parameters for Figure 6.

Table 1. Design Parameters

PARAMETER	VALUE
Signal Range on Protected Lines	0 V to 5 V
Required Level of IEC ESD Protection	±15-kV Contact, ±15-kV Air Gap

8.2.2 Detailed Design Procedure

To begin the design process, some parameters must be decided upon; the designer must know the following:

- Voltage range of the signal on all protected lines
- Required ESD protection needed

8.2.2.1 Signal Range

The TPD3F303 supports signal ranges from 0 V to 5.5 V, which supports the SIM card application

8.2.2.2 Required ESD Protection

The TPD3F303 is rated to withstand up to ±15-kV contact and ±15-kV air gap IEC ESD. This meets the IEC ESD design target.

8.2.3 Application Curves

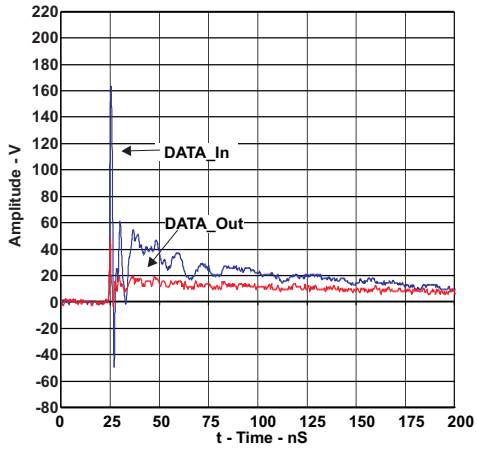


Figure 7. +15-kV IEC Contact, DATA1_In Stressed

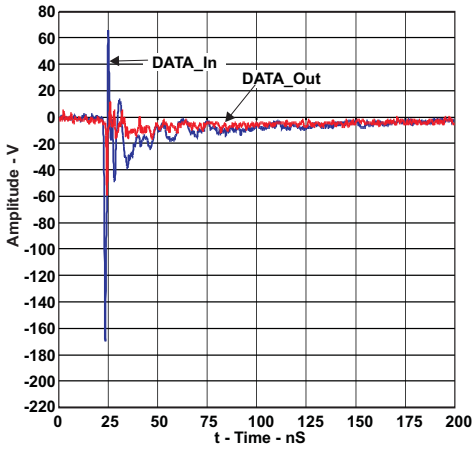


Figure 8. -15-kV IEC Contact, DATA1_In Stressed

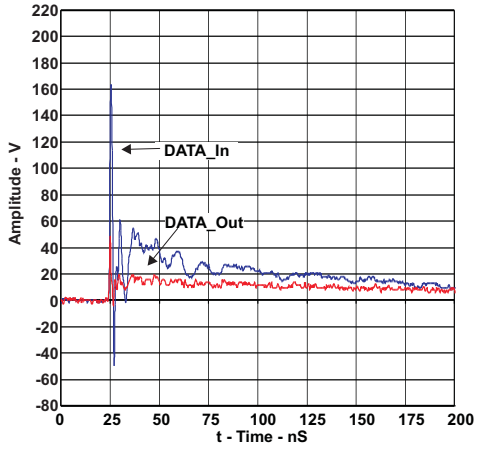


Figure 9. +15-kV IEC Contact, CLK_In Stressed

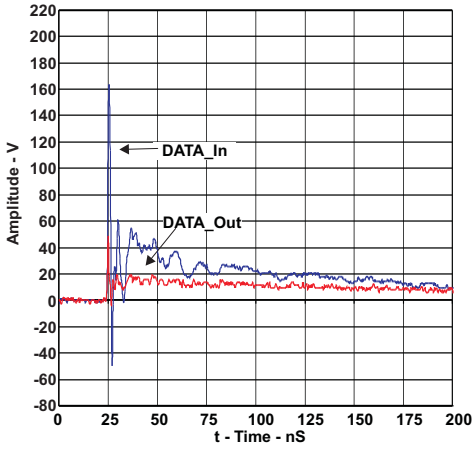


Figure 10. -15-kV IEC Contact, CLK_In Stressed

9 Power Supply Recommendations

This device is a passive ESD device, so there is no need to power it. Take care not to violate the recommended I/O specification (0 V to 5.5 V) to ensure the device functions properly.

10 Layout

10.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

10.2 Layout Example

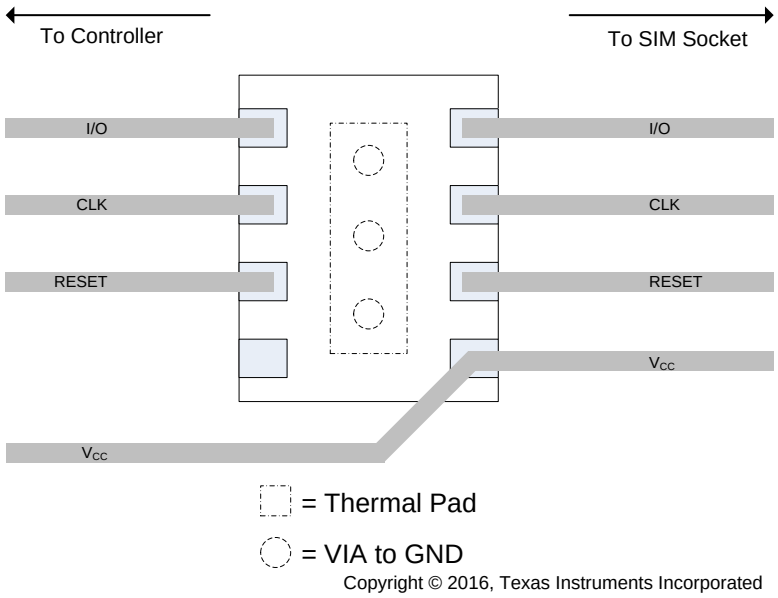


Figure 11. Typical SIM Card Layout

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- *ESD Protection Layout Guide*, SLVA680
- *Reading and Understanding an ESD Protection Datasheet*, SLLA305
- *Design Considerations for System-Level ESD Circuit Protection* , SLYT492

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD3F303DPVR	ACTIVE	USON	DPV	8	3000	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	6SS	Samples
TPD3F303DQDR	ACTIVE	WSON	DQD	8	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	6SS	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

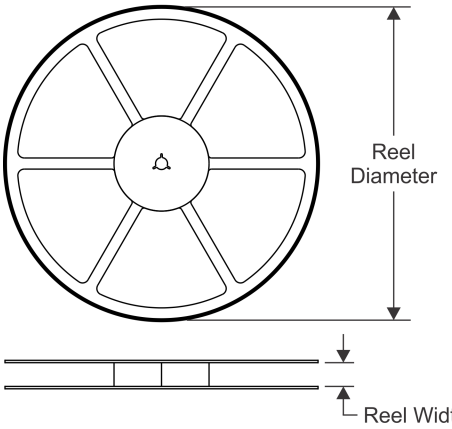
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

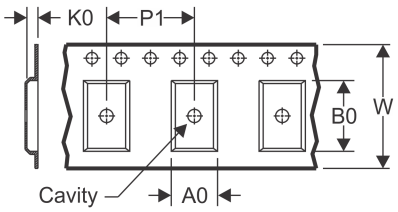
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

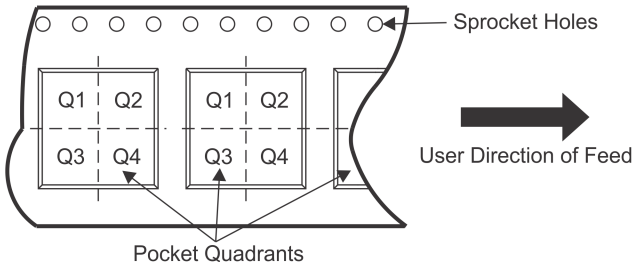


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

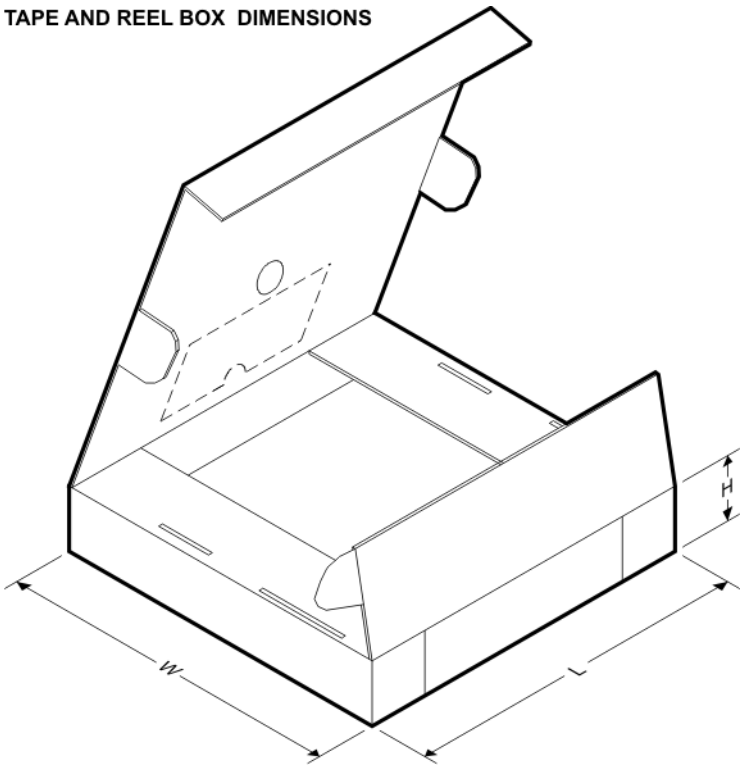
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD3F303DPVR	USON	DPV	8	3000	180.0	8.4	1.84	2.32	0.78	4.0	8.0	Q1
TPD3F303DQDR	WSON	DQD	8	3000	180.0	8.4	1.65	2.0	0.95	4.0	8.0	Q1

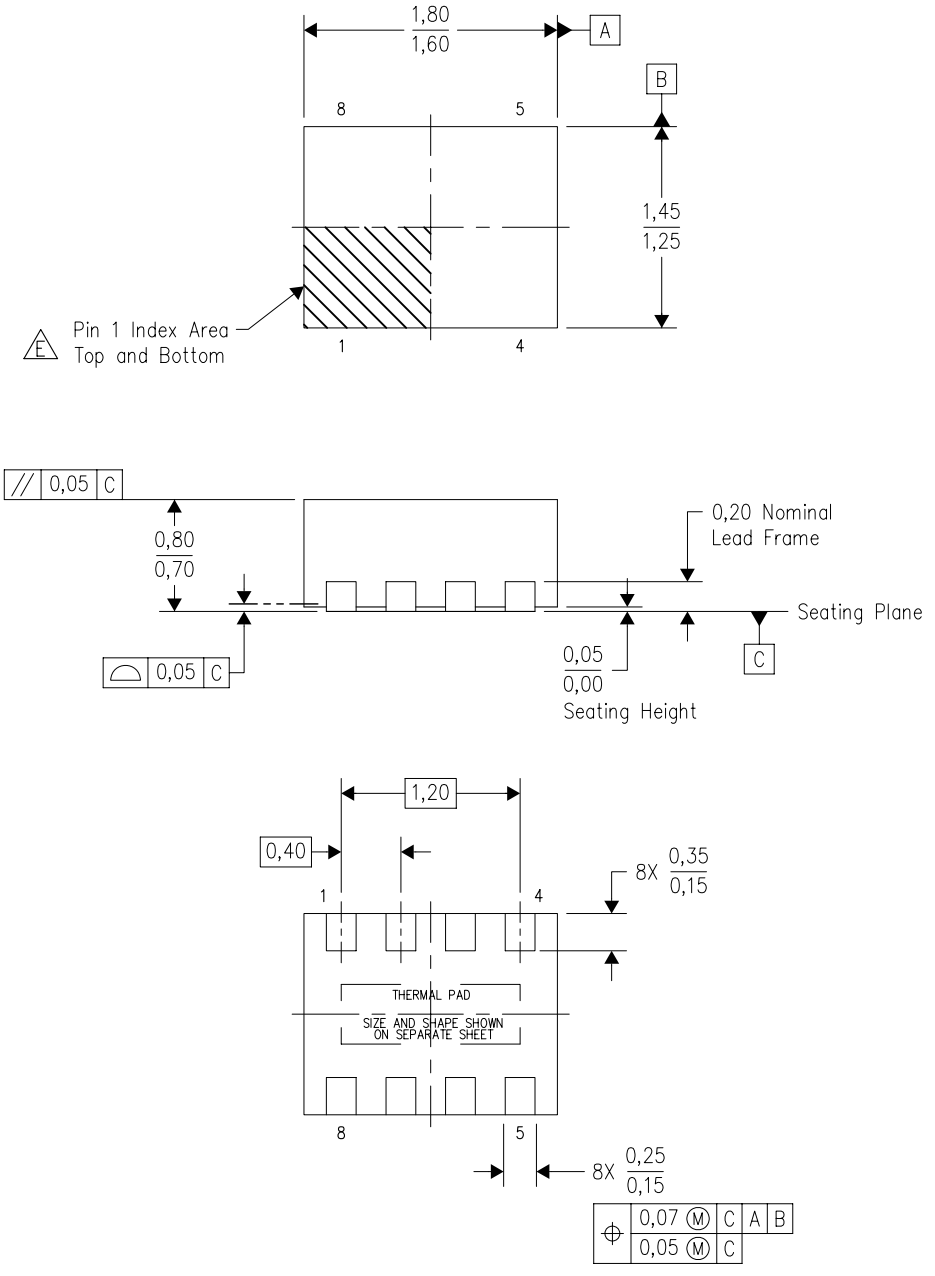
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD3F303DPVR	USON	DPV	8	3000	183.0	183.0	20.0
TPD3F303DQDR	WSON	DQD	8	3000	183.0	183.0	20.0

DQD (R–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



Bottom View

4209732–2/C 12/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.

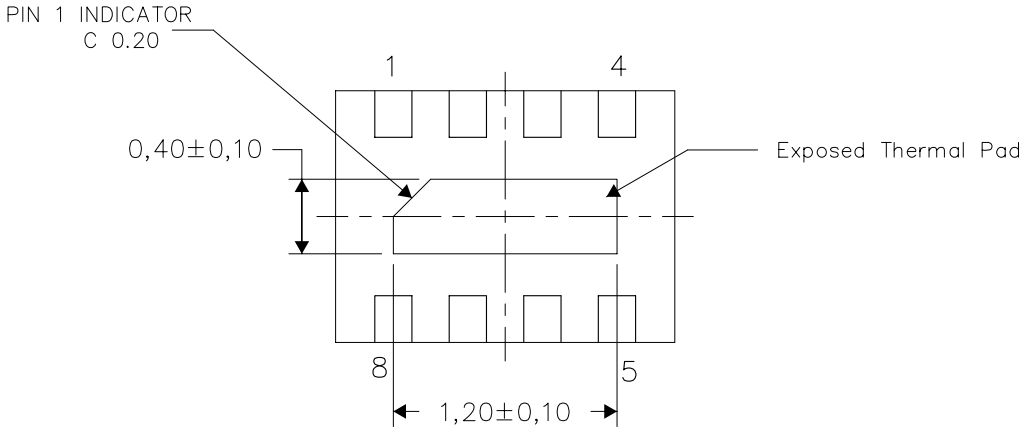
DQD (R–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

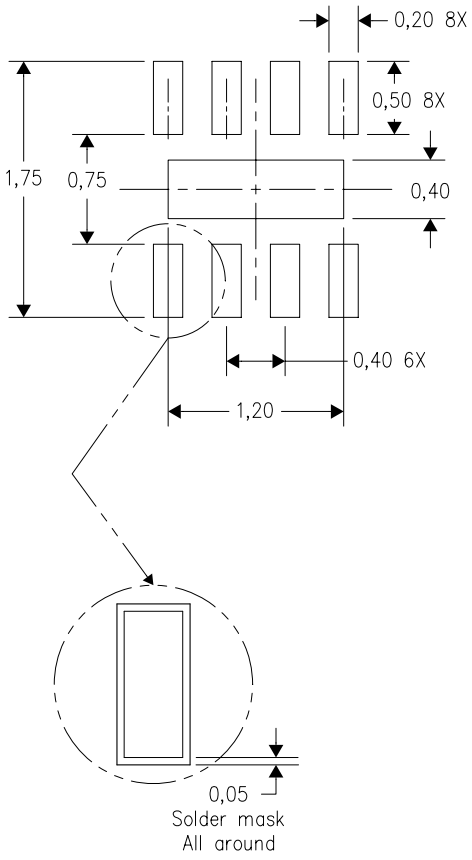
Exposed Thermal Pad Dimensions

4209733–2/C 12/11

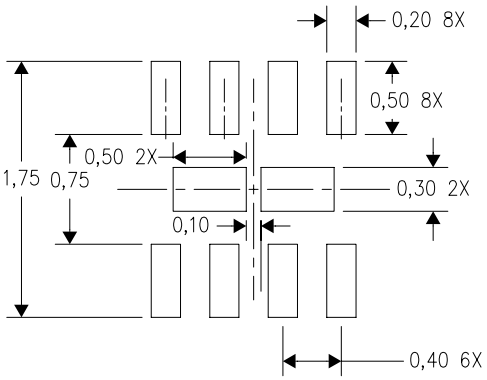
NOTE: All linear dimensions are in millimeters

DQD (R–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD

Land Pattern



Stencil Pattern

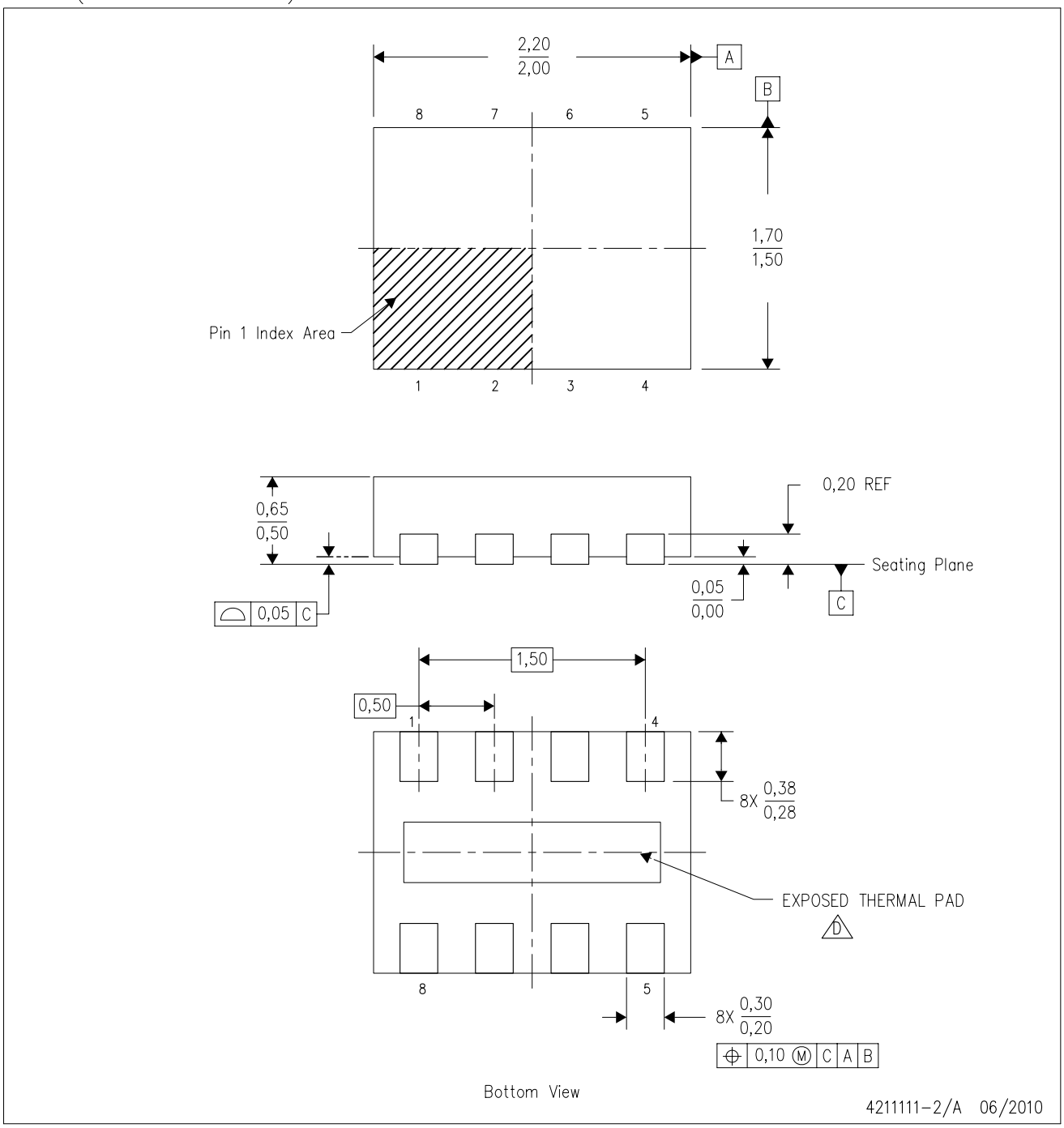


Exposed Pad solder coverage 62%

4211174–2/B 01/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

DPV (R–PUSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.

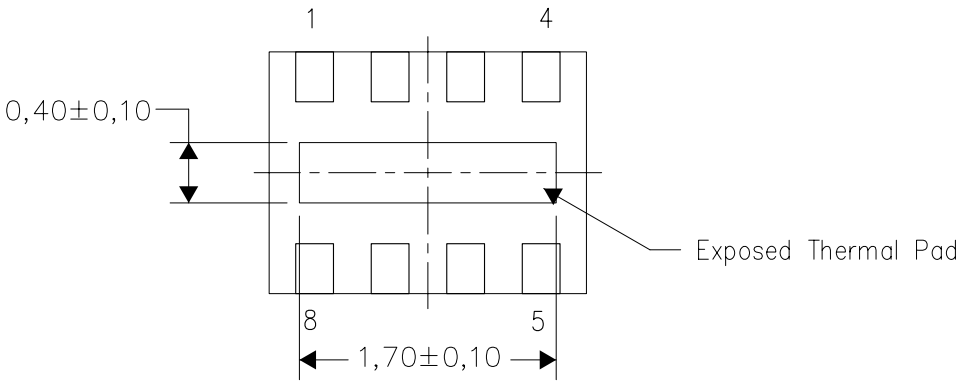
DPV (R–PUSON–N8) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4211680/A 04/11

NOTE: A. All linear dimensions are in millimeters

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