MPQ2167

6V, 4A, Frequency Programmable Buck Converter AEC-Q100 Qualified

DESCRIPTION

The MPQ2167 is a frequency programmable (300kHz to 2.2MHz) synchronous step-down converter. It can achieve up to 4A continuous output current with peak current control for excellent transient response and efficiency performance. The MPQ2167 operates from a 2.7V to 6.0V input range and generates an output voltage as low as 0.606V. It is ideal for a wide range of applications, including automotive infotainment, clusters, telematics, and portable instruments.

The MPQ2167 integrates a 35mΩ high-side switch and a 25mΩ synchronous rectifier for high efficiency without an external Schottky diode. With internal compensation, the MPQ2167 requires a minimum number of readily available standard external components and is available in a QFN-11(2mm x 3mm) package.

The MPQ2167 can be configured for either advanced asynchronous mode (AAM) or forced continuous conduction mode (FCCM) operation at light load. AAM provides high efficiency by reducing switching losses at light load while FCCM has controllable frequency and a lower output ripple.

The MPQ2167 offers standard features, including soft-start, enable control, and a power good indicator. In addition, the MPQ2167 provides over-current protection with valley current detection, which is used to avoid current runaway. Also, it has short-circuit protection, reliable over-voltage protection, and auto recovery thermal protection.

FEATURES

- 2.7V to 6.0V Operating Input Range
- Adjustable Output from 0.606V
- Up to 4A Continuous Output current
- High Efficiency Synchronous Mode Control
- 35mΩ and 25mΩ Internal Power MOSFET
- Programmable Frequency up to 2.2MHz
- 42μA Quiescent Current
- Low Shutdown Mode Current
- 100% Duty Cycle Operation
- Internal Compensation Mode
- Selectable AAM or FCCM Operation Option
- External Soft Start
- Remote EN Control
- Power Good Indicator
- Cycle-by-Cycle Over-Current Protection
- Short-Circuit Protection
- V_{IN} Under-Voltage Lockout
- V_{OUT} Over-Voltage Protection
- Thermal Shutdown
- Available in QFN-11(2mm x 3mm) Package
- Available in AEC-Q100 Grade-1

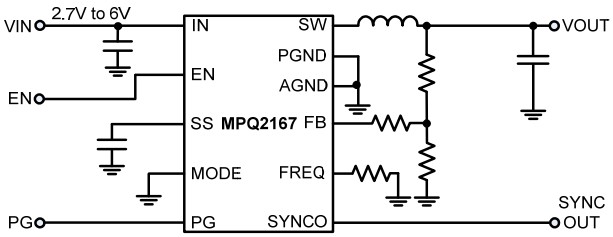
APPLICATIONS

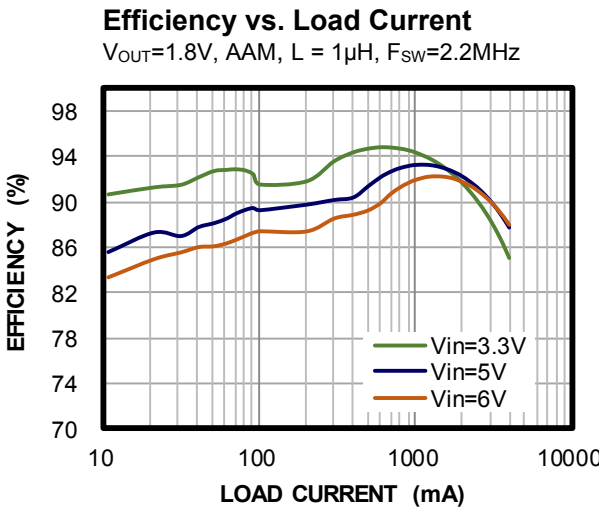
- Automotive Infotainment
- Automotive Clusters
- Automotive Telematics
- Industrial Supplies
- Battery-Powered Devices

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TYPICAL APPLICATION





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ORDERING INFORMATION

Part Number*	Package	Top Marking
MPQ2167GD	QFN-11 (2mm×3mm)	*See Below*
MPQ2167GD-AEC1		

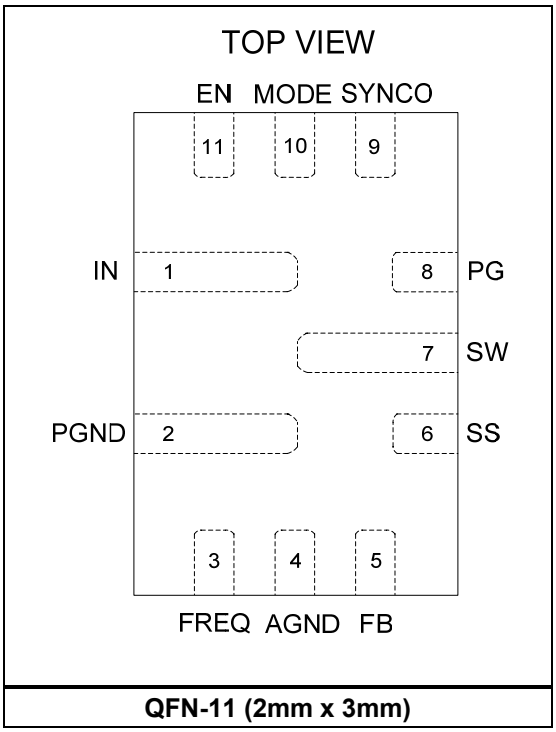
* For Tape & Reel, add suffix –Z (e.g. MPQ2167GD–Z)

TOP MARKING (MPQ2167GD & MPQ2167GD-AEC1)

ATZ
YWW
LLL

ATZ: Product code of MPQ2167GD and MPQ2167GD-AEC1
Y: Year code
WW: Week code
LLL: Lot number

PACKAGE REFERENCE



QFN-11 (2mm x 3mm)

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PIN FUNCTIONS

PIN #	Name	Description
1	IN	**Input supply.** IN supplies all power to the converter. Place a decoupling capacitor to ground as close as possible to the IC to reduce switching spikes.
2	PGND	**Power ground.** Connect to larger copper areas to the negative terminals of the input and output capacitors.
3	FREQ	**Switching frequency programmable input.** Connect a resistor to GND to set the switching frequency.
4	AGND	**Analog ground.** Ground for internal logic and signal circuit.
5	FB	**Feedback point.** Negative input of the error amplifier. Connect to the tap of an external resistor divider between the output and GND to set the regulation voltage. In addition, power good and under-voltage lockout circuits use FB to monitor the output voltage.
6	SS	**Soft-start.** Place a capacitor from SS to GND to set the soft-start time externally. Floating this pin will activate the internal default 1ms soft-start setting.
7	SW	**Switch output.** Internally connect to the high-side and low-side power switches. Outside connect to the output inductor.
8	PG	**Power good indicator.** The PG output is an open drain that connects to V_{IN} by an internal pull-up resistor. PG is pulled up to V_{IN} when the FB voltage is within 15% of the regulation level. If the FB voltage is out of that regulation range, it will drop down.
9	SYNCO	**Synchronization output.** Output a 180° out of phase clock to the other devices.
10	MODE	**Mode selection.** Connect to logic high or input voltage V_{IN} for FCCM. Connect to logic low or ground for AAM. Do not leave MODE floating.
11	EN	**Enable input.** Drive EN high to turn on the device. Leaving EN floating or grounded will disable the device.

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} .....+6.5V
V_{SW} -0.3V(-3V for<10ns) to 6.5V(7.0V for<10ns)
All Other Pins .....-0.3V to +6.5V
Continuous Power Dissipation (T_A = +25°C) (2)
.....1.78W
Junction Temperature..... 150°C
Lead Temperature ..... 260°C
Storage Temperature.....-65°C to +150°C

Recommended Operating Conditions

Continuous Supply Voltage V_{IN} ..... 2.7V to 6.0V
Output Voltage V_{OUT}..... 0.606V to V_{IN}
Load Current Range ..... 0A to 4A
Operating Junction Temp.(T_J)-40°C to +125°C (3)

Thermal Resistance θ_{JA} θ_{JC}

QFN-11(2mmx3mm) .....70.....15 °C/W(4)
QFN-11(2mmx3mm) ..... 42.....13.5 °C/W(5)

Notes:

1) Absolute maximum ratings are rated under room temperature unless otherwise noted. Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the module will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Operating junction temperature above 125°C may be supported; contact MPS for details.
4) Measured on JESD51-7, 4-layer PCB.
5) Measured on standard EVB, 6.35cmx6.35cm, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = V_{EN} =3.6V, T_J =-40°C to +125°C, unless otherwise noted, typical values are at T_J = +25°C.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Input Supply and UVLO						
Supply current (quiescent)	I_Q	Mode=AAM, V_{EN}=2V, No load, R_{FREQ}=1MΩ T_J = +25°C		42	50	µA
		T_J = -40°C to +125°C			120	
Shutdown current	I_{SD}	Mode=AAM, V_{EN}=0V, T_J = +25°C		0	1	µA
		T_J = -40°C to +125°C			20	
V_{IN} under-voltage lockout threshold rising	$INUV_{Vth-R}$		2.3	2.5	2.7	V
V_{IN} under-voltage lockout threshold falling	$INUV_{Vth-F}$		2	2.15	2.3	V
V_{IN} UVLO threshold hysteresis	$INUV_{HYS}$			350		mV
Output and Regulation						
Regulated FB voltage	V_{FB}	T_J = +25°C	0.596	0.606	0.616	V
		T_J = -40°C to +125°C	0.591		0.621	V
FB input current	I_{FB}	V_{FB} = 0.63V		10	100	nA
Output discharge resistor	$R_{DISCHARGE}$		50	100	150	Ω
Switches and Frequency						
High-side switch on-resistance	R_{DSON-P}	V_{IN} = 5V, I_{OUT} =200mA		35	70	mΩ
Low-side switch on-resistance	R_{DSON-N}	V_{IN} = 5V, I_{OUT} =200mA		25	70	mΩ
High-side SW leakage current	$I_{HSW-LKG}$	V_{EN} = 0V; V_{IN} = 6V V_{SW} = 6V, T_J = +25°C		0	1	µA
		T_J = -40°C to +125°C			30	
Low-side SW leakage current	$I_{LSW-LKG}$	V_{EN} = 0V; V_{IN} = 6V V_{SW} = 0V, T_J = +25°C		0	1	µA
		T_J = -40°C to +125°C			10	
Switching frequency	F_{SW}	R_{FREQ} = 526kΩ	380	450	520	kHz
		R_{FREQ} = 85kΩ	1800	2100	2400	
Maximum Duty Cycle	D_{MAX}			100		%
Minimum On Time(6)	T_{ON-MIN}			50		ns
Minimum Off Time(6)	$T_{OFF-MIN}$			95		ns
PG						
PG sink current capacity	$V_{PG-SINK}$	Sink 1mA			300	mV
PG logic high voltage	$V_{PG-HIGH}$	V_{IN} =5V	4.5			V
PG delay time	$T_{PG-DELAY}$	V_{OUT} Rising Edge	40	100	180	µs
		V_{OUT} Falling Edge	5	20	30	µs
PG upper rising threshold	PG_{UP_R}	As Percentage of V_{FB}	108	115	122	%
PG upper hysteresis	PG_{UP_HYS}	As Percentage of V_{FB}		5		%
PG lower rising threshold	PG_{LOW_R}	As Percentage of V_{FB}	80	85	90	%
PG lower hysteresis	PG_{LOW_HYS}	As Percentage of V_{FB}		5		%
EN						
EN input rising threshold	$V_{EN-RISING}$		1.2			V
EN input falling threshold	$V_{EN-FALLING}$				0.4	V
EN input current	I_{EN}	V_{EN}=2V		2	5	µA
		V_{EN}=0V		0	0.5	µA
Mode and Soft Start						
Mode pin rising threshold	$V_{MODE-FCCM}$	Into FCCM	1.2			V
Mode pin falling threshold	$V_{MODE-AAM}$	Into AAM			0.4	V
Mode input leakage current	I_{MODE}	Pulled up to 6V			1	µA

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = V_{EN} =3.6V, T_J =-40°C to +125°C, unless otherwise noted, typical values are at T_J = +25°C.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Soft-start charging current	I_{SS}	V_{SS}=0V	2	4	6	µA
Default soft-start time	$T_{SS-DEFAULT}$			1		ms
Protections						
Peak current limit	$I_{PEAK-LIMIT}$	Sourcing, D=40%	4.8	6.7	8.6	A
Valley current limit	$I_{VALLEY-LIMIT}$			4.7		A
OCP timer (6)	T_{OCP}			100		µs
Zero cross threshold	I_{ZCD}			100		mA
Output over-voltage limit	OV_{Limit}	As Percentage of V_{FB}		115		%
Thermal shutdown(6)	T_{SD}	Temperature Rising		170		°C
Thermal shutdown hysteresis(6)	T_{SD-SYS}			25		°C

Note:

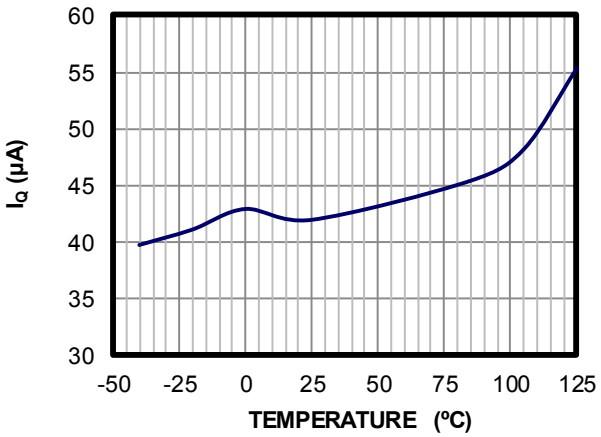
6) Not tested in production and guaranteed by design and characterization.

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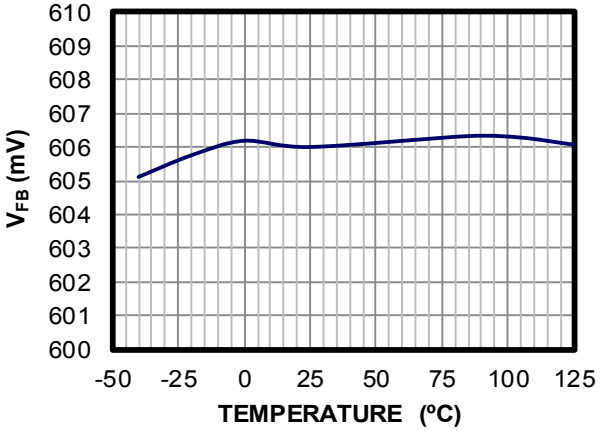
TYPICAL CHARACTERISTICS

V_{IN} = 3.6V, T_J = +25°C, unless otherwise noted.

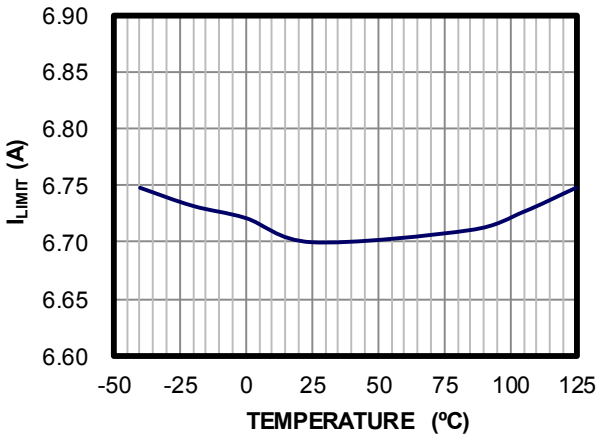
I_Q vs. Temperature



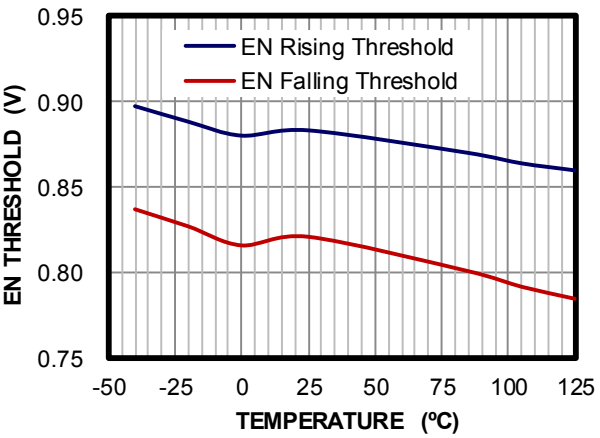
V_{FB} vs. Temperature



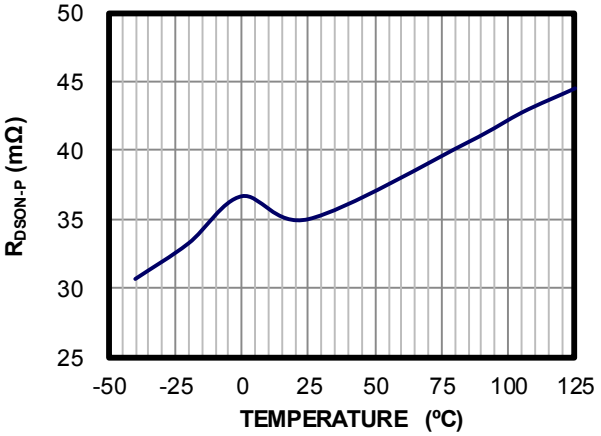
I_{LIMIT} vs. Temperature



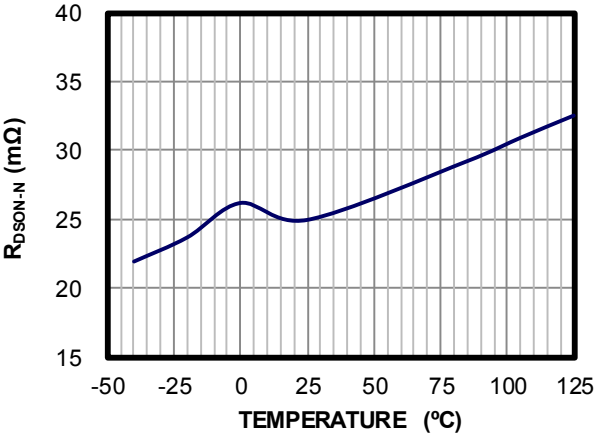
EN Threshold vs. Temperature



R_{DSON-P} vs. Temperature



R_{DSON-N} vs. Temperature

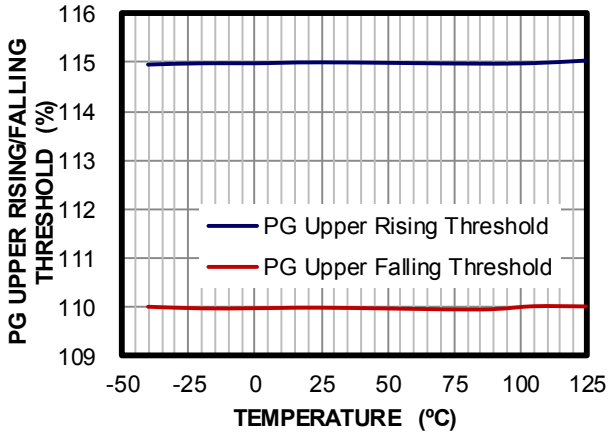


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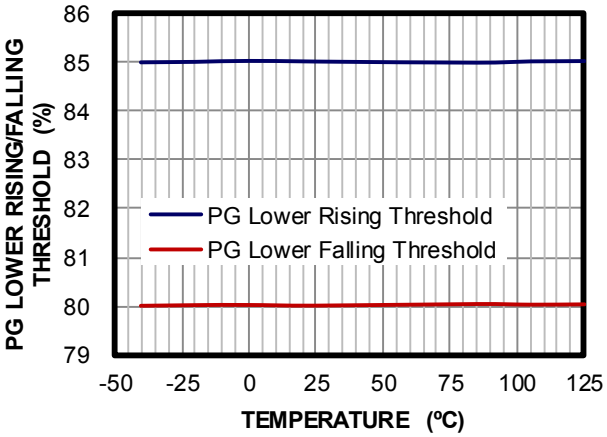
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V_{IN} = 3.6V, T_J = +25°C, unless otherwise noted.

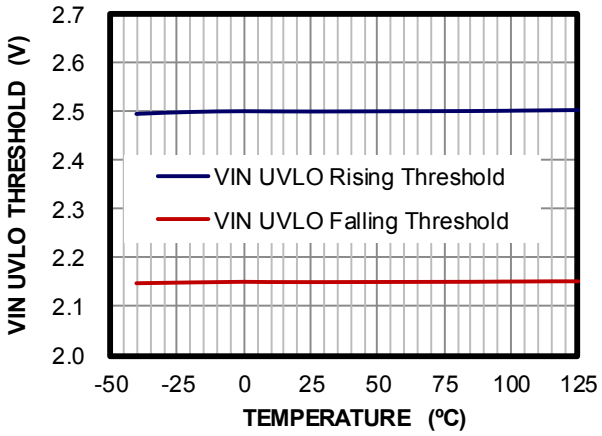
PG Upper Rising/Falling Threshold vs. Temperature



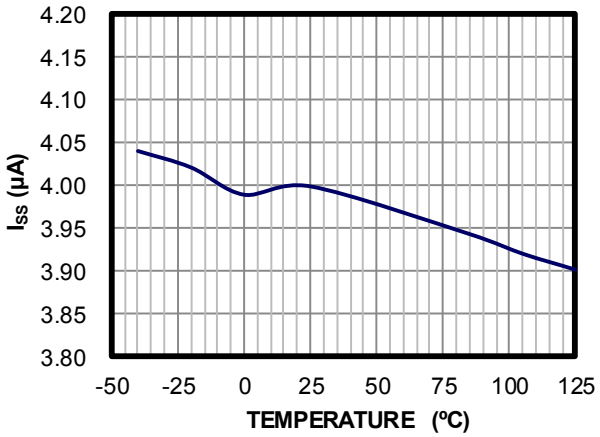
PG Lower Rising/Falling Threshold vs. Temperature



VIN UVLO Threshold vs. Temperature



I_{SS} vs. Temperature

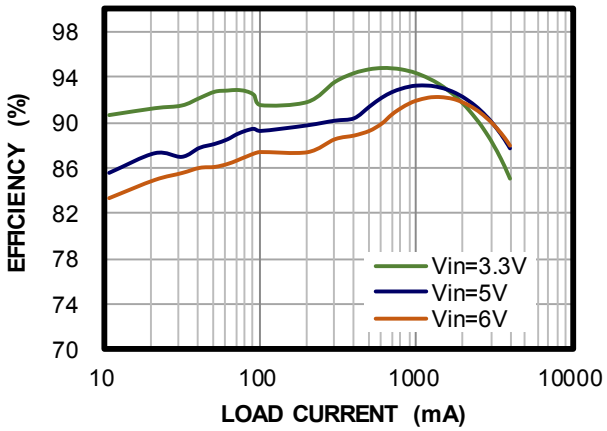


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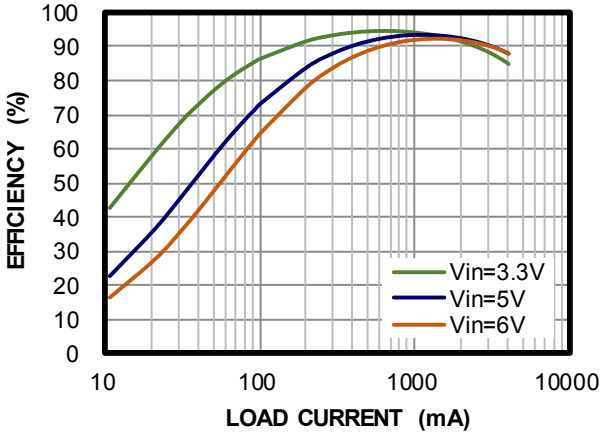
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, V_{OUT} = 1.8V, L = 1µH, C_{OUT}= 44µF, F_{SW}=2.2MHz, T_A = +25°C, unless otherwise noted.

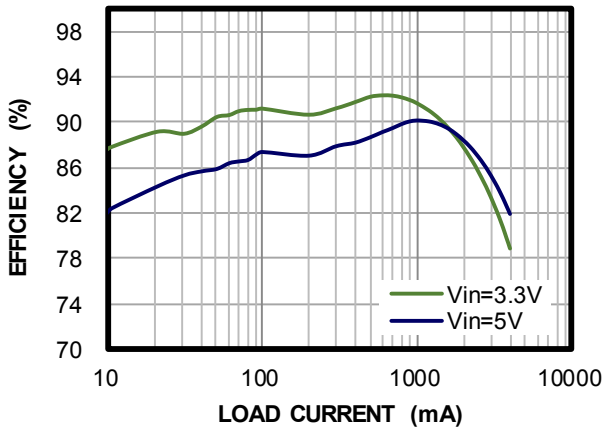
Efficiency vs. Load Current
V_{OUT}=1.8V, AAM



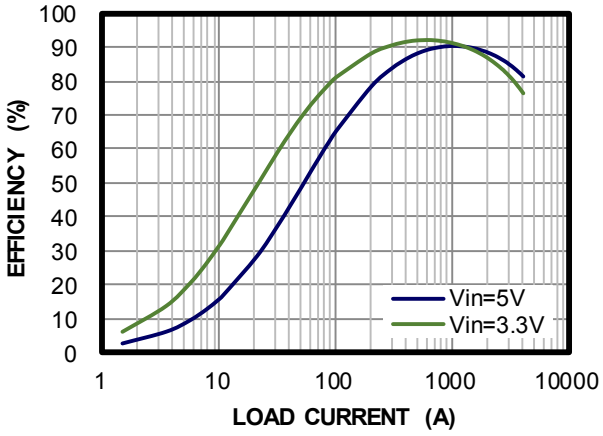
Efficiency vs. Load Current
V_{OUT}=1.8V, CCM



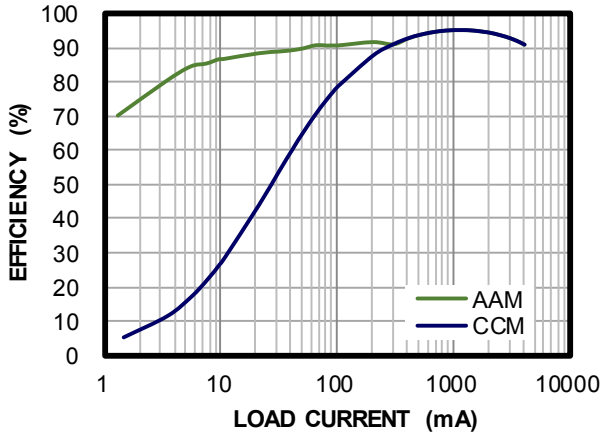
Efficiency vs. Load Current
V_{OUT}=1.2V, AAM



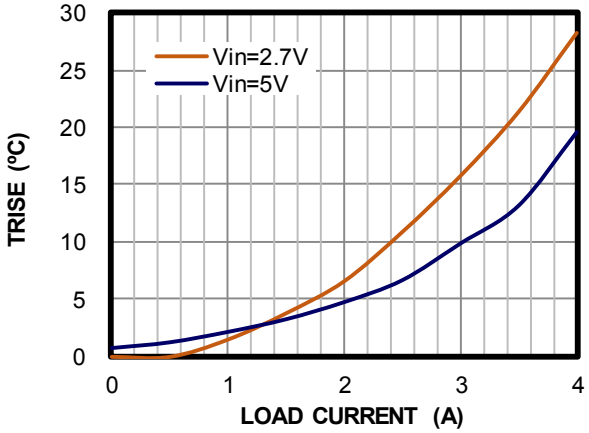
Efficiency vs. Load Current
V_{OUT}=1.2V, CCM



Efficiency vs. Load Current
V_{IN}=5V, V_{OUT}=2.5V



Case Thermal Rise
V_{OUT}=1.8V, AAM



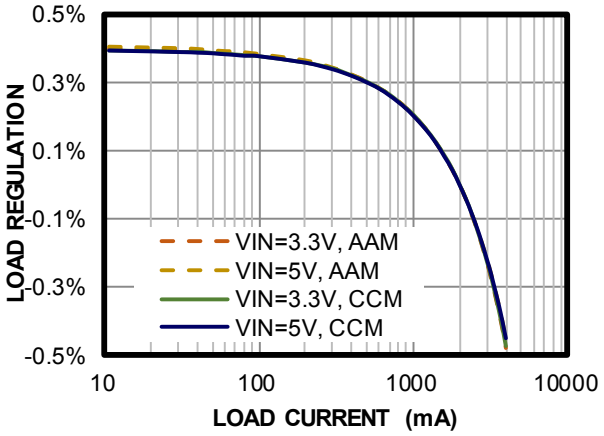
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.8V, L = 1µH, C_{OUT}= 44µF, F_{SW}=2.2MHz, T_A = +25°C, unless otherwise noted.

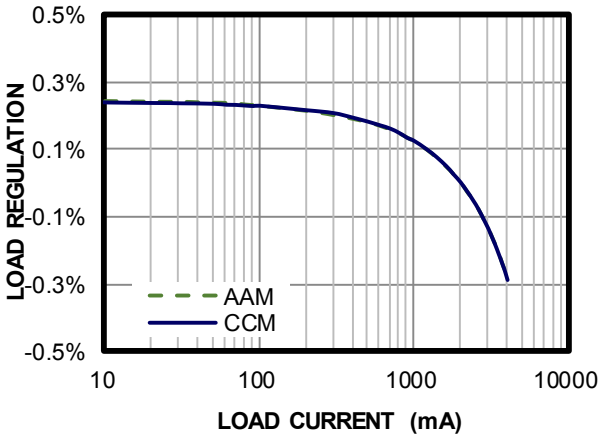
Load Regulation

V_{OUT}=1.8V



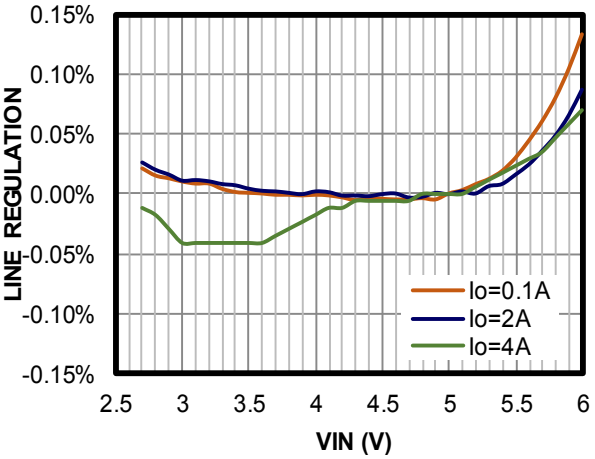
Load Regulation

V_{IN}=5V, V_{OUT}=2.5V

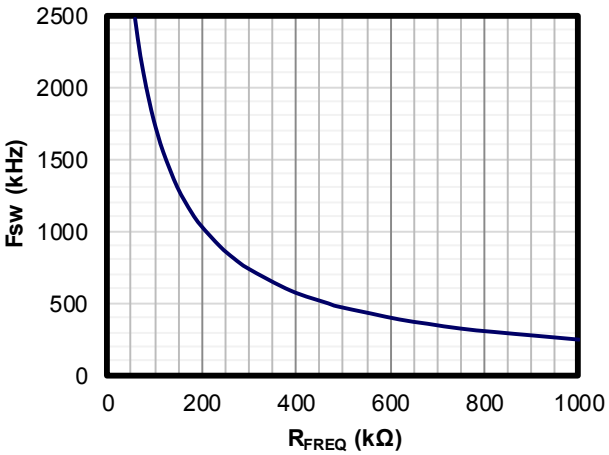


Line Regulation

V_{OUT}=1.8V, AAM



F_{SW} vs. R_{FREQ}

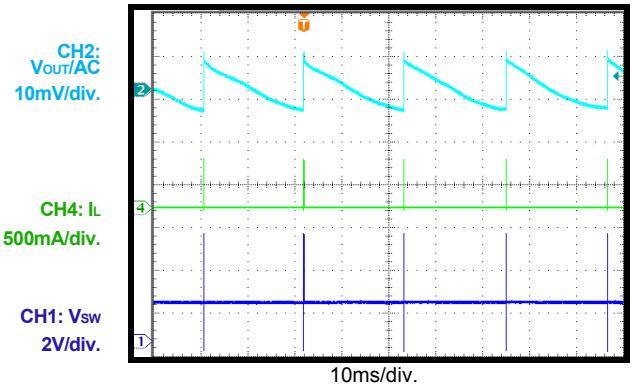


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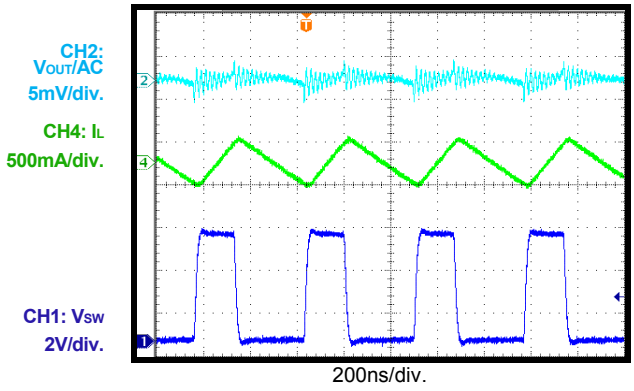
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.8V, L = 1µH, C_{OUT}= 44µF, F_{SW}=2.2MHz, T_A = +25°C, unless otherwise noted.

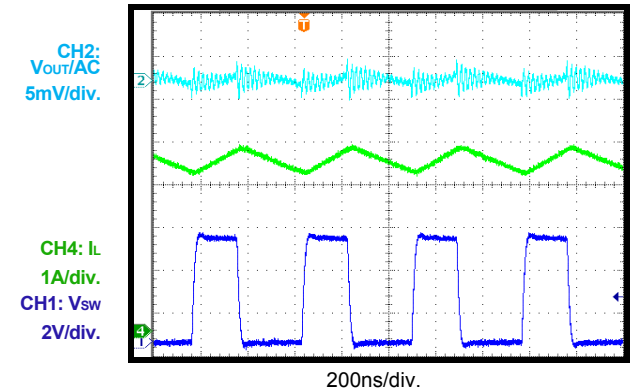
Steady State
I_{OUT}=0A, AAM



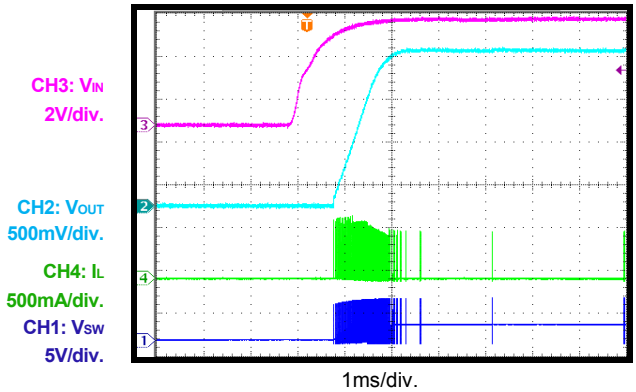
Steady State
I_{OUT}=0A, CCM



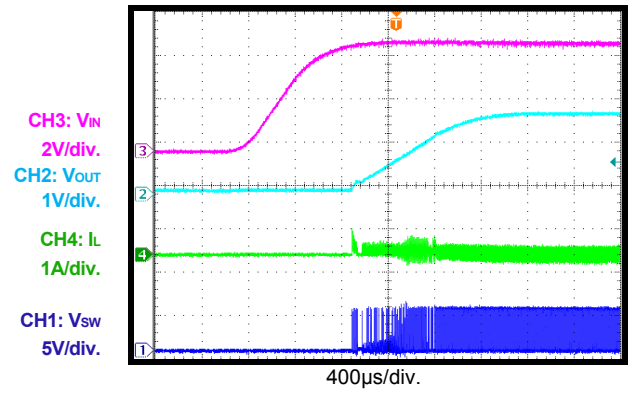
Steady State
I_{OUT}=4A



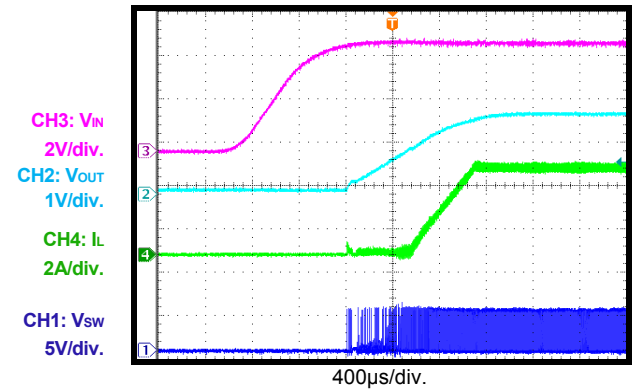
Start-Up through VIN
I_{OUT}=0A, AAM



Start-Up through VIN
I_{OUT}=0A, CCM



Start-Up through VIN
I_{OUT}=4A

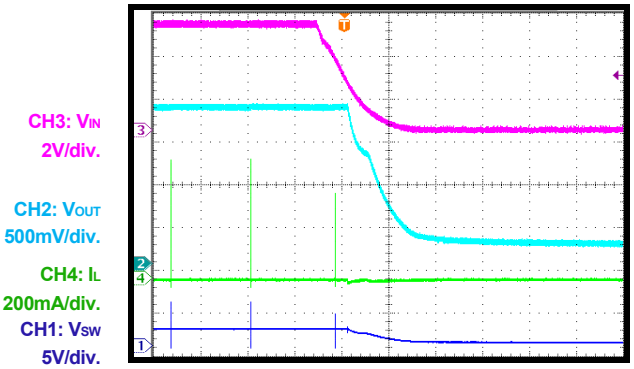


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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

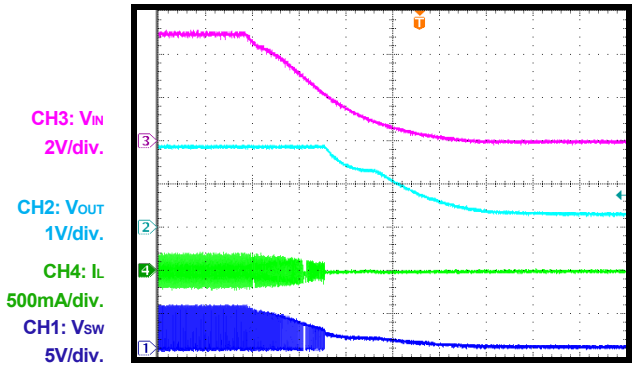
V_{IN} = 5V, V_{OUT} = 1.8V, L = 1µH, C_{OUT}= 44µF, F_{SW}=2.2MHz, T_A = +25°C, unless otherwise noted.

Shutdown through VIN
I_{OUT}=0A, AAM



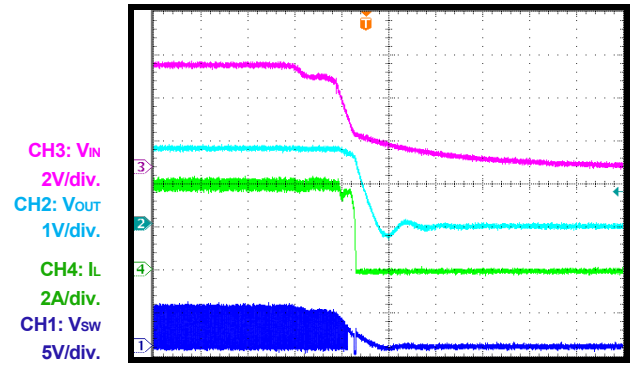
10ms/div.

Shutdown through VIN
I_{OUT}=0A, CCM



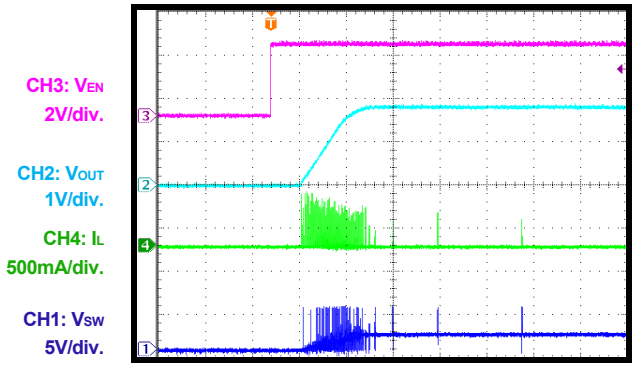
4ms/div.

Shutdown through VIN
I_{OUT}=4A



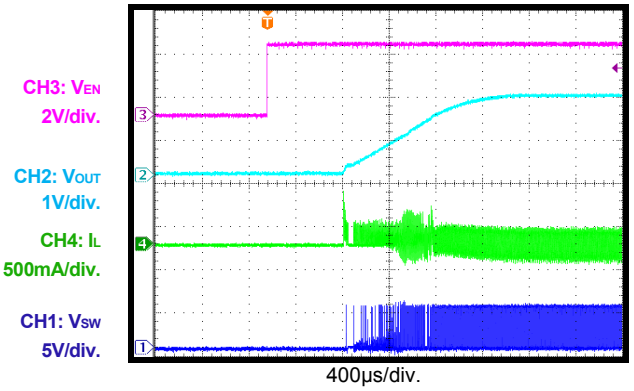
40µs/div.

Start-Up through EN
I_{OUT}=0A, AAM



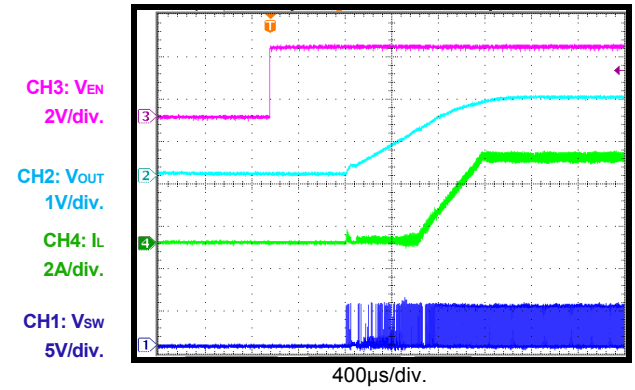
1ms/div.

Start-Up through EN
I_{OUT}=0A, CCM



400µs/div.

Start-Up through EN
I_{OUT}=4A



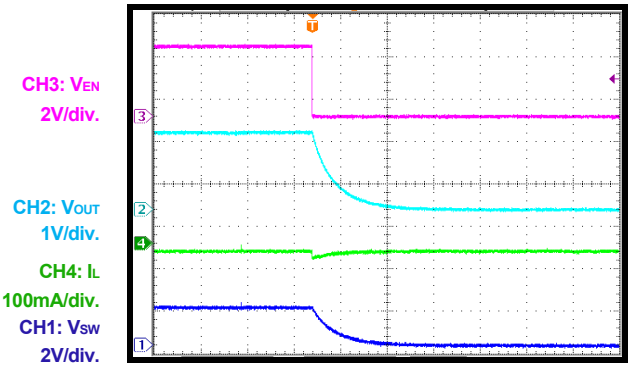
400µs/div.

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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

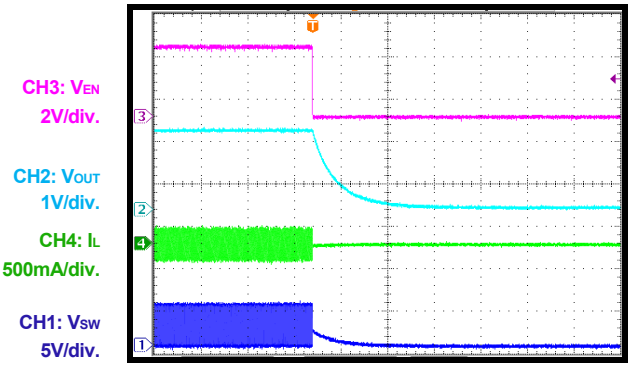
V_{IN} = 5V, V_{OUT} = 1.8V, L = 1µH, C_{OUT}= 44µF, F_{SW}=2.2MHz, T_A = +25°C, unless otherwise noted.

Shutdown through EN
I_{OUT}=0A, AAM



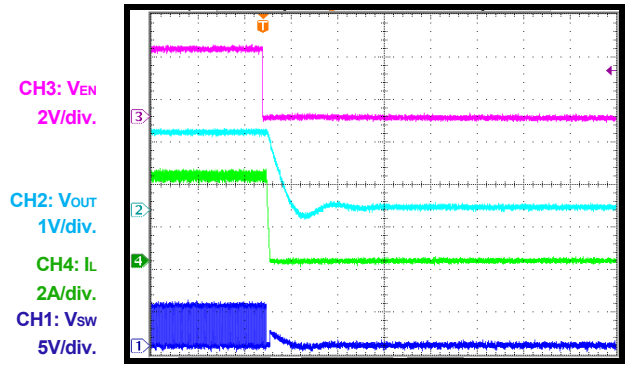
10ms/div.

Shutdown through EN
I_{OUT}=0A, CCM



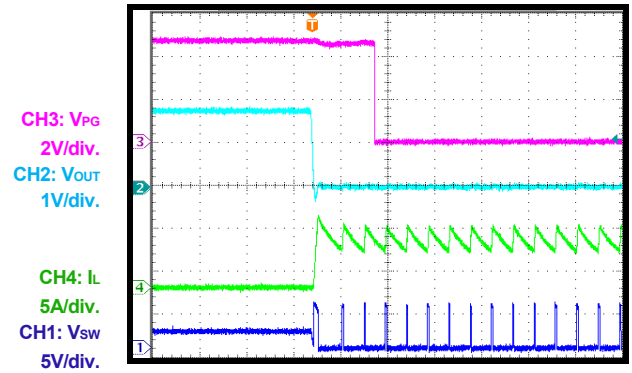
10ms/div.

Shutdown through EN
I_{OUT}=4A



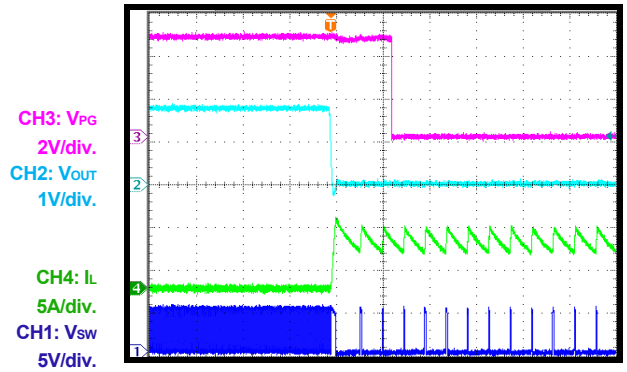
40µs/div.

SCP Entry
I_{OUT}=0A, AAM



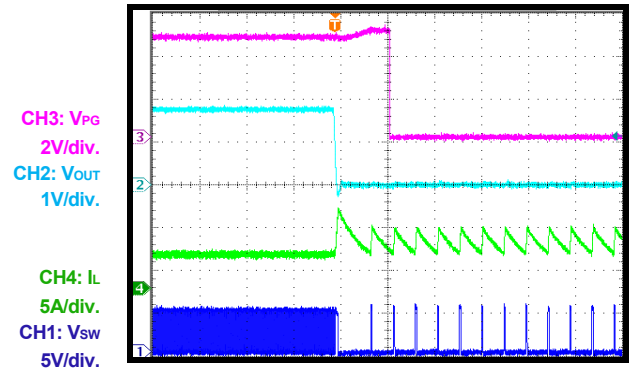
20µs/div.

SCP Entry
I_{OUT}=0A, CCM



20µs/div.

SCP Entry
I_{OUT}=4A



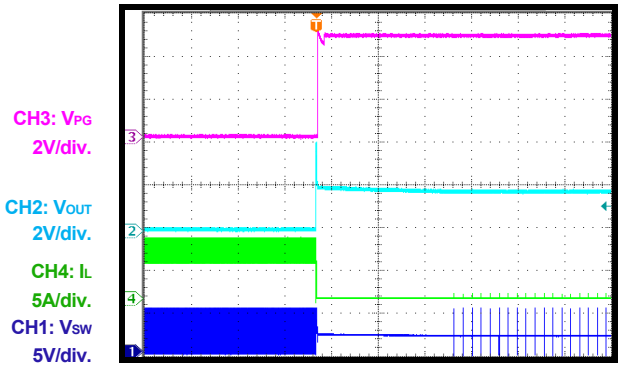
20µs/div.

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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

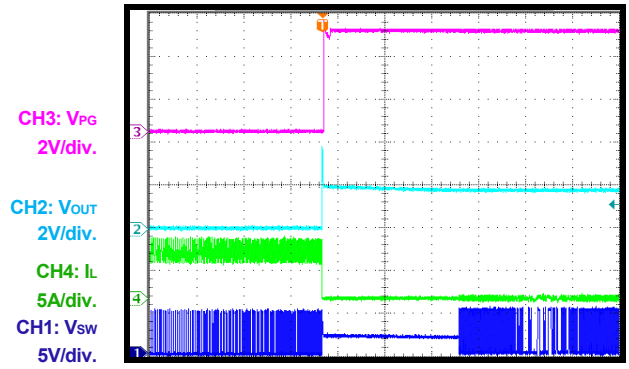
V_{IN} = 5V, V_{OUT} = 1.8V, L = 1µH, C_{OUT}= 44µF, F_{SW}=2.2MHz, T_A = +25°C, unless otherwise noted.

SCP Recovery
I_{OUT}=0A, AAM



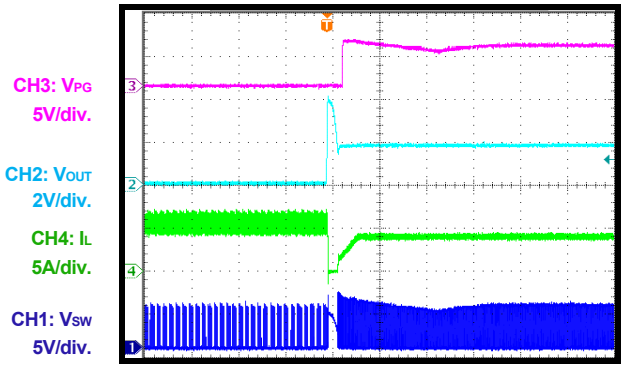
100ms/div.

SCP Recovery
I_{OUT}=0A, CCM



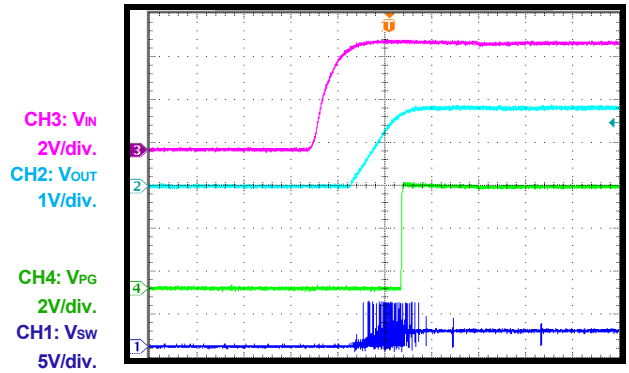
100ms/div.

SCP Recovery
I_{OUT}=4A



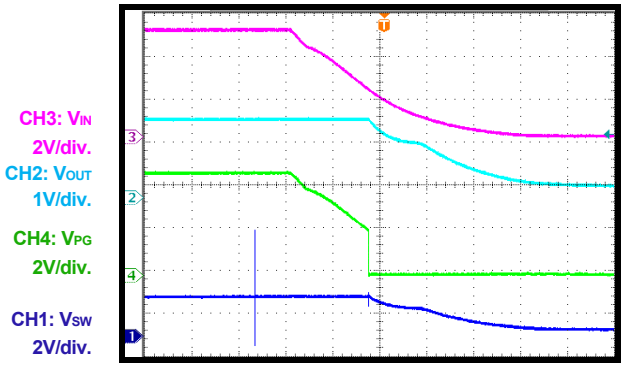
1ms/div.

PG in Start-Up through VIN
I_{OUT}=0A, AAM



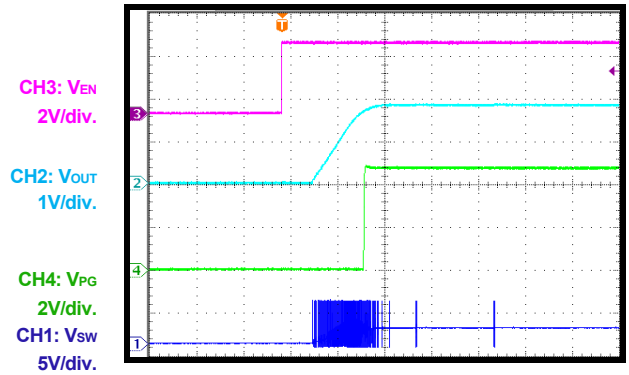
1ms/div.

PG in Shutdown through VIN
I_{OUT}=0A, AAM



4ms/div.

PG in Start-Up through EN
I_{OUT}=0A, AAM



1ms/div.

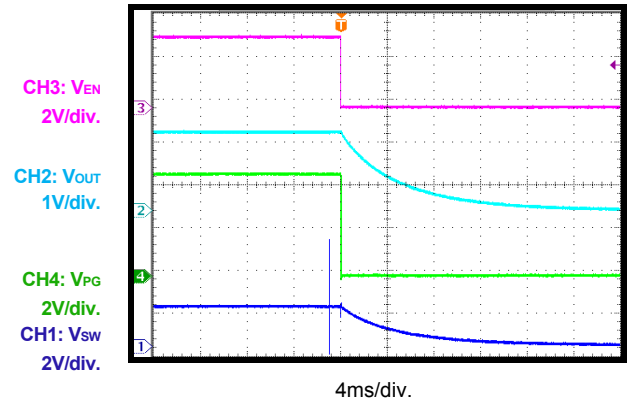
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

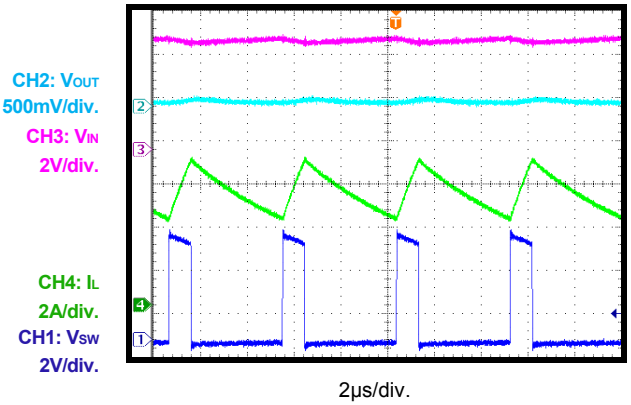
V_{IN} = 5V, V_{OUT} = 1.8V, L = 1µH, C_{OUT}= 44µF, F_{SW}=2.2MHz, T_A = +25°C, unless otherwise noted.

PG in Shutdown through EN

I_{OUT}=0A, AAM

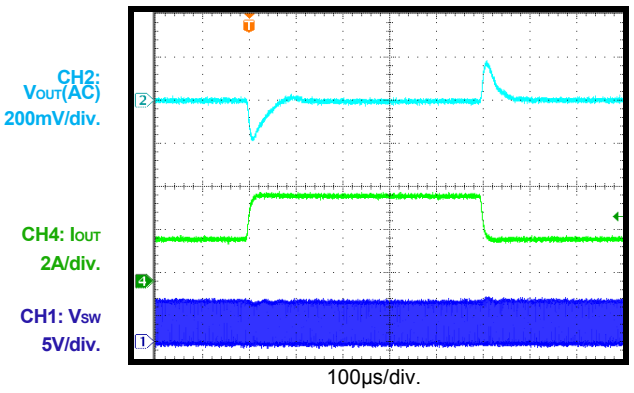


SCP Steady State



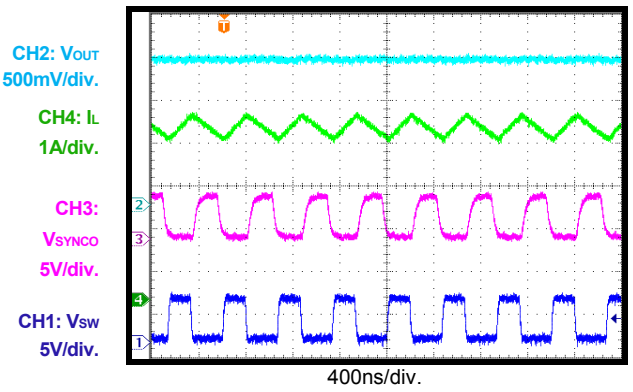
Load Transient

I_{OUT}=2A<->4A, 1.6A/µs



SYNCO

I_{OUT}=4A



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BLOCK DIAGRAM

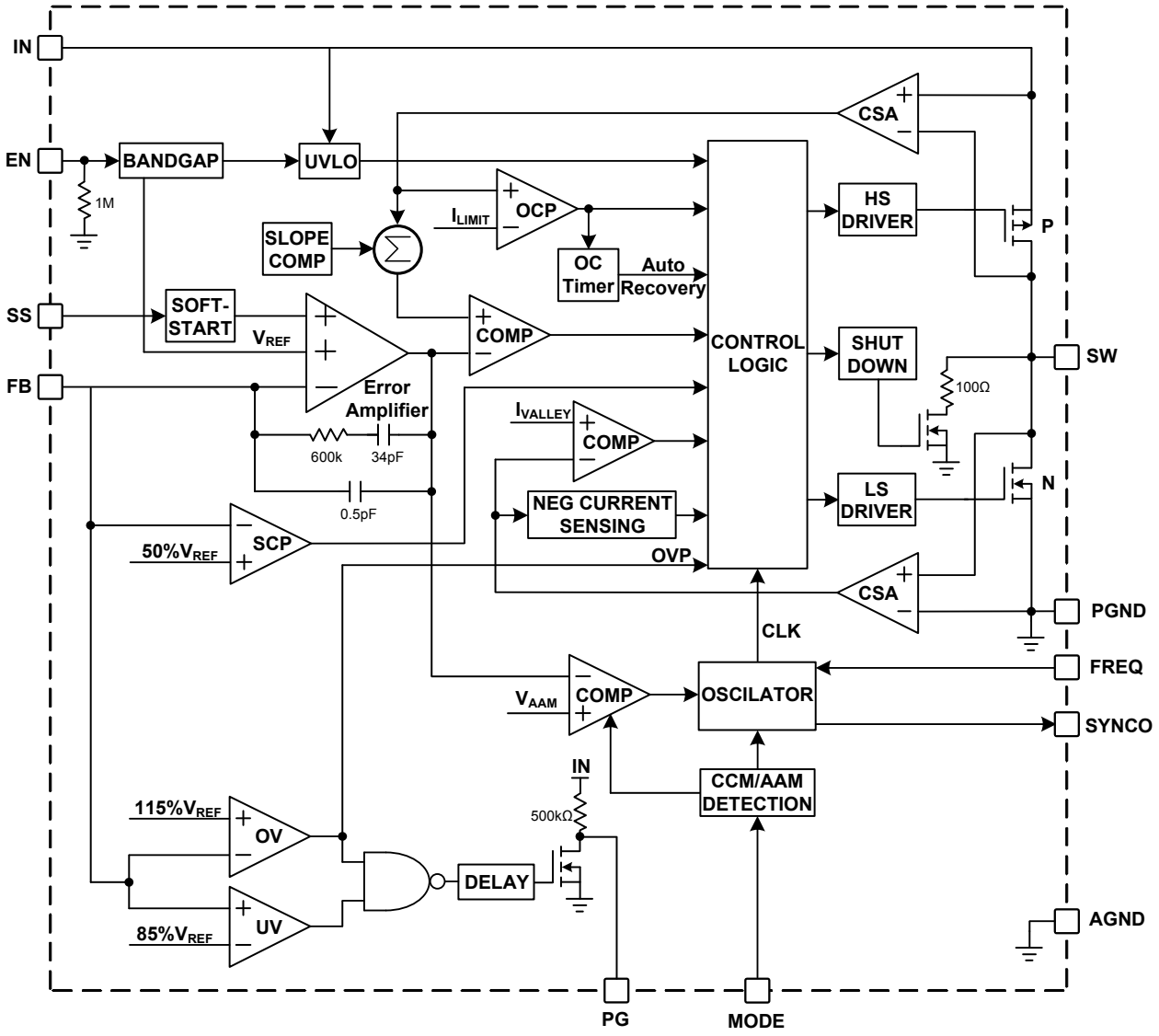


Figure 1: Functional Block Diagram

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OPERATION

The MPQ2167 is a fully integrated, synchronous rectified, step-down, non-isolated switch-mode converter. It uses peak-current-mode control with internal compensation for faster transient response and cycle-by-cycle current limit.

A block diagram of the device is shown in Figure 1. It is available with a 2.7V to 6.0V input supply range and can achieve up to 4A continuous output current with excellent load and line regulation over an ambient temperature range of -40°C to +125°C. The output voltage can be regulated as low as 0.606V.

The MPQ2167 is optimized for low voltage portable applications where efficiency and small size are critical. It can operate up to 2.2MHz switching frequency, which enables the use of a smaller inductor while also providing excellent efficiency. It also allows for high power conversion efficiency under a light load condition with AAM.

FCCM

Pulling MODE high (>1.2V) forces the converter into FCCM. In FCCM, the MPQ2167 operates in a fixed frequency peak-current-control mode to regulate the output voltage, regardless of the output current. An internal clock initiates a FCCM cycle. At the rise edge of the clock, the high-side switch (HS-FET) turns on, and the inductor current rises linearly to provide energy to the load. The HS-FET remains on until its current hits the COMP voltage, which is the output of the internal error amplifier. The output voltage of the error amplifier depends on the difference of the output feedback voltage and the internal high precision reference; it will determine how much energy should be transferred to the load. The higher the load current, the higher the COMP voltage.

When the HS-FET is off, the low-side switch (LS-FET) will be turned on immediately and remains on until the next clock starts. During this time, the inductor current will flow through the LS-FET. In order to avoid shoot-through, a dead time is inserted to avoid the HS-FET and LS-FET turning on at the same time. For each turn on/off period in a switching cycle, the HS-FET will remain on/off with a minimum on/off time limit.

AAM

Pulling MODE low (<0.4V) forces the converter into light load advanced asynchronous mode (AAM). There is an internally fixed AAM threshold voltage (V_{AAM}). Under a light load condition, the value of V_{COMP} is low. If V_{COMP} becomes higher than V_{AAM}, the MPQ2167 first enters discontinuous conduction operation with a fixed frequency, as long as the inductor current approaches zero. If the load decreases further, or there is no load that makes V_{COMP} lower than V_{AAM}, the internal clock will be blocked, making the MPQ2167 skip some pulses. During this time, V_{FB} is lower than V_{REF}, so V_{COMP} will ramp up until it exceeds V_{AAM}. Then the internal clock will be reset, and the crossover time is taken as a benchmark for the next clock. This control scheme helps achieve high efficiency by scaling down the frequency to reduce the switching and gate driver losses.

As the output current increases from a light load condition, V_{COMP} becomes larger, and the switching frequency increases.

If the output current exceeds the critical level, when V_{COMP} is higher than V_{AAM}, the MPQ2167 resumes fixed-frequency control (same as FCCM). See Figure 2.

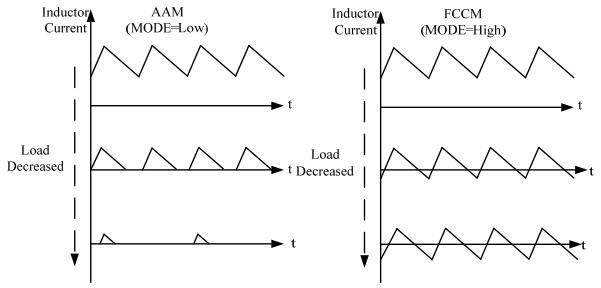


Figure 2: AAM and FCCM

Enable

The MPQ2167 can be enabled or disabled via a remote EN signal that is referenced to ground. The remote EN control operates with positive logic that is compatible with popular logic devices. Positive logic implies that when the input voltage exceeds the under-voltage lockout (UVLO) threshold (typically 2.5V), the converter is enabled by pulling EN above 1.2V. Leaving the EN pin floating or grounded will disable the MPQ2167. There is an internal 1MΩ resistor from EN to ground.

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Oscillator

The oscillating frequency of the MPQ2167 can be programmed by an external frequency resistor. The frequency resistor should be located between FREQ and GND as close to the device as possible.

Select the R_{FREQ} value following the F_{SW} vs. R_{FREQ} curve in the Typical Performance Characteristics (TPC) section.

The MPQ2167 has a SYNCO pin, which can output a 180° phase shift clock. This signal can be used to synchronize other devices to keep the same operation frequency but opposite phase, which can reduce the total input current ripple.

Soft-Start and Output Discharge

The MPQ2167 has soft start (SS), which ramps up the output voltage in a controlled slew rate when EN goes high, avoiding overshoot at start-up.

When the soft-start period starts, an internal current source charges the external soft-start capacitor. When the SS voltage (V_{SS}) falls below the internal reference (V_{REF}), the V_{SS} overrides V_{REF} as the error amplifier reference. When V_{SS} exceeds V_{REF}, V_{REF} acts as the reference. After soft start finishes, the MPQ2167 enters steady state. It can be used for tracking and sequencing.

The SS time set by the external SS capacitor can be calculated with equation (1):

$$t_{SS}(ms) = \frac{C_{SS}(nF) \times V_{REF}(V)}{I_{SS}(\mu A)} \quad (1)$$

Where C_{SS} is the external SS capacitor, V_{REF} is the internal reference voltage (0.606V), and I_{SS} is the internal 4μA SS charge current.

When SS is floating, the SS time is 1ms following the internal setting.

When disabled or in an input shutdown, the MPQ2167 discharges the output voltage to GND through an internal 100Ω resistor that is in parallel to the LS-FET.

Pre-Bias Start-Up

At start-up, if V_{FB}>V_{SS} (which means the output has pre-bias voltage), neither the high-side nor low-side MOSFET is turned on until V_{SS} is higher than V_{FB}.

100% Duty Cycle

The MPQ2167 can operate with 100% duty cycle, which can help extend the battery life. When the input voltage is too low to maintain the regulation of the output, the device will completely turn on the HS-FET to achieve maximum output voltage.

Power Good Indicator

The MPQ2167 has power good (PG) indication. PG is the open drain of the MOSFET. In the presence of an input voltage, the MOSFET turns on so that PG is pulled to GND before a soft start is ready. When the output voltage is within a ± 15% window of the rated voltage set by FB, PG will be pulled up to V_{IN} by an internal resistor after a delay. If V_{FB} moves outside the ±15% range with a hysteresis, the device pulls PG low to indicate a failure output status.

Over-Current Protection (OCP)

The MPQ2167 has a 6.7A cycle-by-cycle peak current limit control. The inductor current is monitored during a HS-FET on state. Once the inductor current hits the current limit, the HS-FET will be turned off immediately. Then the LS-FET will be turned on to discharge the energy, and the inductor current will decrease. The HS-FET will not be on again until the inductor is lower than a certain current threshold, which is called valley current limit. It is very useful to prevent the inductor current from running away and possibly damaging the components.

When the valley current limit is triggered, the OCP timer will start immediately. The OCP timer is set at 100μs. Hitting the valley current limit during each cycle during this 100μs time frame will trigger SCP.

Short-Circuit Protection (SCP)

When a short circuit occurs, the MPQ2167 will immediately hit its current limit. Meanwhile, the output voltage drops until V_{FB} is below 50%×V_{REF} (0.606V). Then the device will consider this an output dead short and will trigger SCP immediately. In SCP, the inductor current is monitored during the HS-FET on state. Once the inductor current hits the current limit, the HS-FET will be turned off immediately. Then the LS-FET will be turned on to discharge the energy and the inductor current will decrease. The HS-FET will

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not be on again until the inductor is lower than a certain current threshold, which is called valley current limit. The device will repeat this operation until the short circuit disappears, and the output returns to the regulation level. This protection mode is very useful to prevent the inductor current from running away and possibly damaging the components.

Over-Voltage Protection (OVP)

The MPQ2167 monitors the output voltage through FB to detect output over-voltage conditions. A V_{FB} that exceeds 115% × V_{REF} (0.606V) triggers OVP, and the LS-FET turns on to discharge V_{OUT} until the inductor current drops to zero while the HS-FET remains off. Then the LS-FET will be shut off, and the output will be discharged through the internal 100Ω resistor in parallel to the LS-FET. The control will not begin to switch until the output is within regulation.

Under Voltage Lock Out Protection (UVLO)

The MPQ2167 has input under voltage lock out protection (UVLO) to ensure reliable output power. Assuming EN is active, the MPQ2167 is powered on when the input voltage is higher than the UVLO rising threshold. It is powered off when the input voltage drops below the UVLO falling threshold. This function prevents the device from operating at an insufficient voltage. It is a non-latch protection.

Thermal Shutdown

The MPQ2167 has thermal protection by monitoring the IC temperature internally. This function prevents the chip from operating at an exceedingly high temperature. If the junction temperature exceeds the threshold value (typically 170°C), it shuts down the whole chip. This is a non-latch protection. There is a 25°C hysteresis. Once the junction temperature drops to about 145°C, the device resumes operation by initiating a soft start.

Start-Up and Shutdown

If both V_{IN} and V_{EN} exceed their appropriate thresholds, the chip starts up. The reference block starts first, generating stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

While the internal supply rail is up, an internal timer holds the power MOSFET OFF for about 50μs to blank the start-up glitches. When the soft-start block is enabled, it first holds its SS output low to ensure the rest of the circuitries are ready, and then it slowly ramps up.

Three events can shut down the chip: EN low, V_{IN} UVLO, and thermal shutdown. In the shutdown procedure, the signaling path is blocked first to avoid any fault triggering. The COMP voltage and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command, but its charging path is disabled.

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APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider connected to FB sets the output voltage (see Figure 3). The feedback resistor R1 must account for both stability and dynamic response, so it cannot be too large or too small. R1 is estimated to be 100kΩ. R2 is then given using equation (2):

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.606} - 1} \quad (2)$$

The T-type feedback network is highly recommended (see Figure 3).

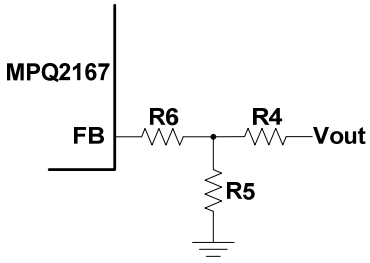


Figure 3: Feedback Network

R6+R4 is used to set the loop bandwidth. Basically, a higher R6+R4 brings lower bandwidth. To ensure loop stability, it is strongly recommended to limit the bandwidth at around $0.1f_{SW}$.

Table 1 lists the recommended feedback divider resistor values for common output voltages. Check the loop analysis before using in application. Change the resistance of R_T for loop stability if necessary.

Table 1: Resistor Values for Typical V_{OUT}

V_{OUT} (V)	R6 (kΩ)	R4 (kΩ)	R5 (kΩ)
1.2	100	100(1%)	100(1%)
1.5	100	100(1%)	66.5(1%)
1.8	100	100(1%)	49.9(1%)
2.5	100	100(1%)	31.6(1%)
3.3	100	100(1%)	22.1(1%)

Selecting the Inductor

The inductor is required to supply constant current to the output load while being driven by the switching input voltage. For a default 2.2MHz application, a 0.47μH to 1.5μH inductor is recommended. For highest efficiency, chose an inductor with a DC resistance less than 15mΩ. When setting the frequency, the inductance may need to be increased with the frequency decreasing. A large inductance will result in less ripple current and a lower output ripple voltage. However, this also results in a larger inductor, which will be physically larger and have a higher series resistance and/or lower saturation current. A good rule for determining the inductor value is to allow the inductor ripple current to be approximately 30% of the maximum load current. Ensure that the peak inductor current is below the device peak current limit. The inductance value can be calculated with equation (3):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (3)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

Choose an inductor that will not saturate under the maximum inductor peak current. The peak inductor current can be calculated with equation (4):

$$I_{LP} = I_{OUT} + \frac{V_{OUT}}{2f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (4)$$

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous, and therefore requires a capacitor to supply the AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR values and small temperature coefficients. Other types, including Y5V and Z5U must not be used as these lose too much capacitance with frequency, temperature, and bias voltage. Be sure to place the input capacitors as close to IN as possible. For most applications, a 22μF capacitor is sufficient. For higher output voltage, use 47μF to improve system stability. To get a small solution size, it is better to choose a proper package size capacitor with a rating voltage compliant to the input spec.

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Since the input capacitor absorbs the input switching current, it requires an adequate ripple current rating, which should be greater than the converter's maximum input ripple current. The input ripple current can be estimated with equation (5):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (5)$$

The worst case condition occurs at V_{IN} = 2V_{OUT}, where:

$$I_{CIN} = \frac{I_{OUT}}{2}$$

For simplification, choose an input capacitor whose RMS current rating is greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, use a small high-quality ceramic capacitor (0.1µF) placed as close to the IC as possible. The input capacitance value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system design, choose an input capacitor that meets the specification.

The input voltage ripple caused by capacitance can be estimated with equation (6):

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (6)$$

The worst-case condition occurs at V_{IN} = 2V_{OUT}, where:

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{f_{SW} \times C_{IN}}$$

Selecting the Output Capacitor

The output capacitor maintains the output DC voltage. Ceramic capacitors with low ESR are recommended for keeping the output voltage ripple low and their smaller size. Electrolytic and polymer capacitors may also be used. The output voltage ripple can be estimated with equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \cdot (1 - \frac{V_{OUT}}{V_{IN}}) \cdot (R_{ESR} + \frac{1}{8 f_{SW} \times C_{OUT}}) \quad (7)$$

R_{ESR} is the equivalent series resistance of the output capacitor.

For ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated with equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times {f_{SW}}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (8)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (9)$$

Another consideration of the output capacitance is the allowable overshoot in V_{OUT} if the load is suddenly removed. In this case, energy stored in the inductor will be transferred to C_{OUT} causing its voltage to rise. In order to achieve a desired overshoot relative to the regulated voltage, the output capacitance can be estimated with equation (10):

$$C_{OUT} = \frac{{I_{OUT}}^2 \times L}{{V_{OUT}}^2 \times ((V_{OUTMAX} / V_{OUT})^2 - 1)} \quad (10)$$

Where V_{OUTMAX}/V_{OUT} is the allowable maximum overshoot. After calculating the capacitance required for both the ripple and overshoot, choose the larger of the calculated values.

The characteristics of the output capacitor also affect the stability of the regulation system. The MPQ2167 can be optimized for a wide range of capacitance and ESR values.

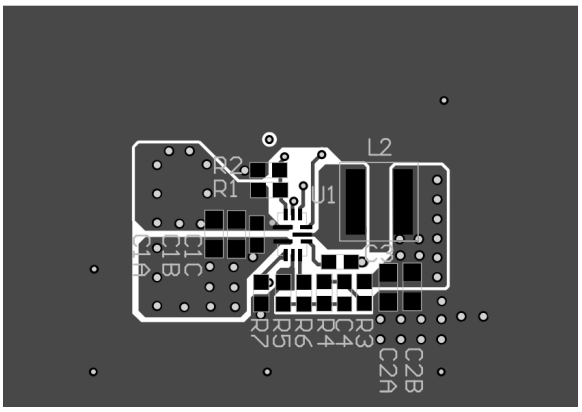
Layout Recommendation

Efficient PCB layout is critical for stable operation. Refer to Figure 4 and follow the guidelines below for optimal design layout:

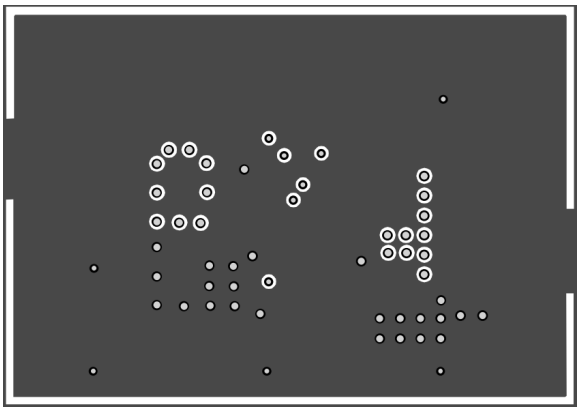
1. Place high-current paths (GND, IN, and SW) very close to the device with short, direct, and wide traces.
2. Place input capacitors as close to IN as possible to minimize high frequency noise.
3. Place the feedback resistor divider as close as possible to FB. And keep the FB trace away from switching node.

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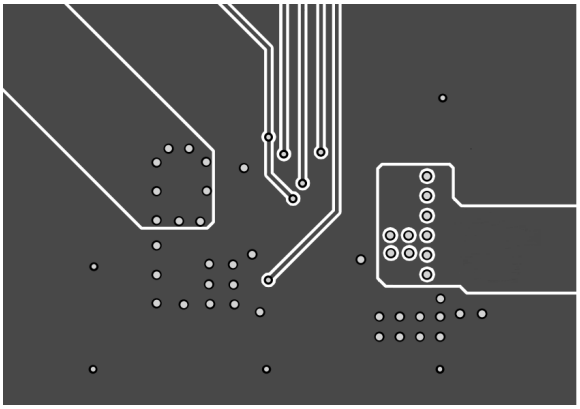
4. Connect the bottom IN and SW pads to a large copper area to achieve better thermal performance.
5. Use large copper areas for power planes (IN, SW, OUT, and GND) to minimize conduction loss and thermal stress.
6. A four-layer layout is strongly recommended to achieve better thermal performance. Use multiple vias to connect the power planes to the internal layers.



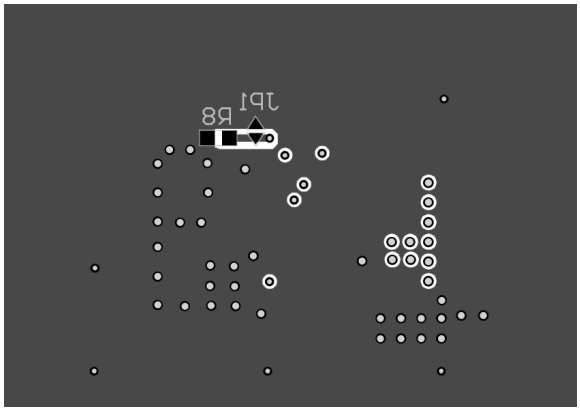
Top and Top Silk Layer



Inner Layer 1



Inner Layer 2



Bottom and Bottom Silk Layer

Figure 4: Recommended PCB Layout [7]

Note:

7) The recommended PCB layout is based on Figure 5.

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TYPICAL APPLICATION

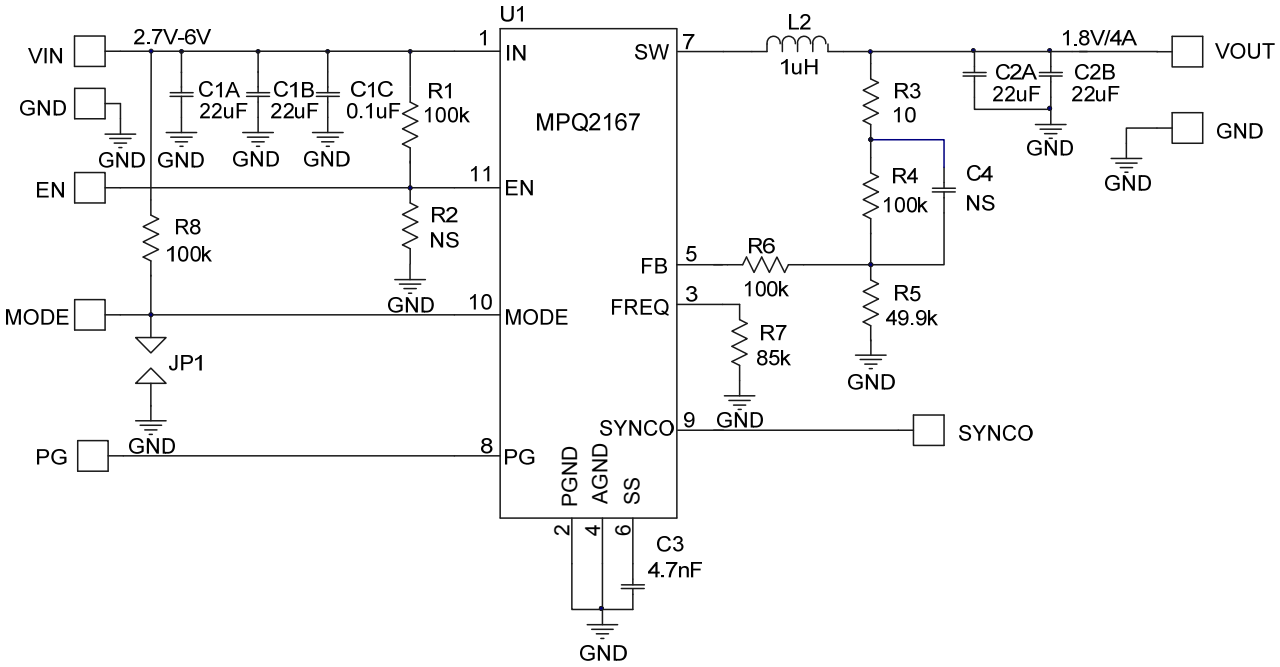


Figure 5: V_{OUT}=1.8V, I_{OUT}=4A Application Circuit

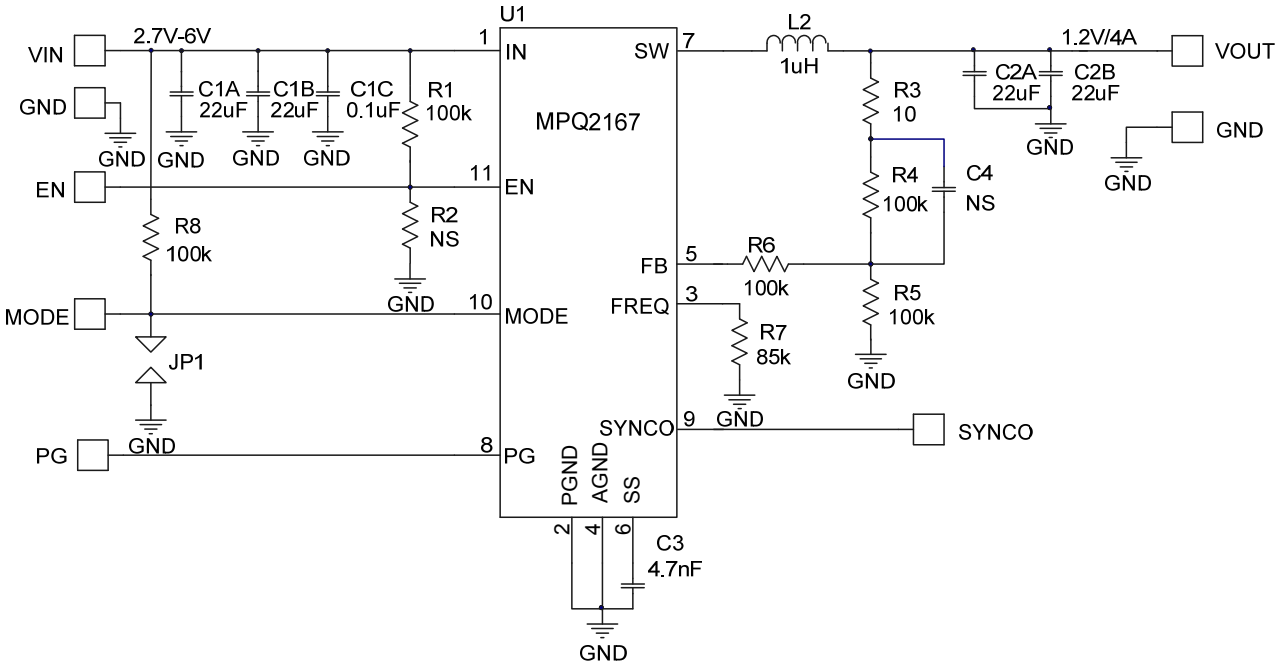
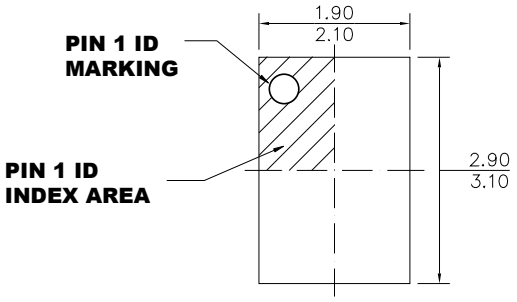


Figure 6: V_{OUT}=1.2V, I_{OUT}=4A Application Circuit

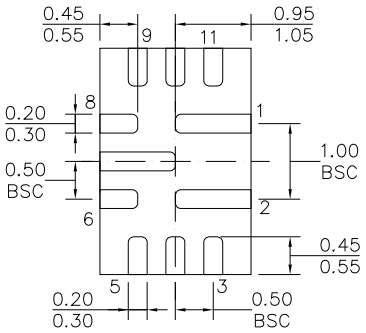
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PACKAGE INFORMATION

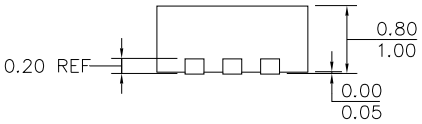
QFN-11 (2mmx3mm)



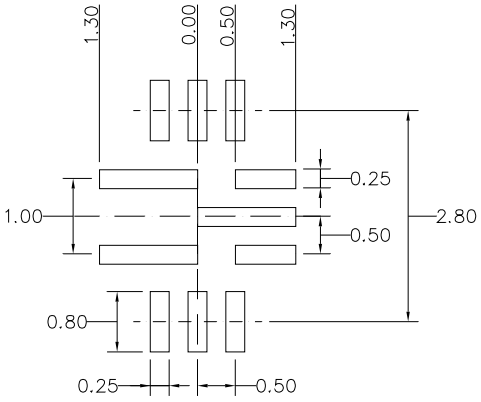
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) LAND PATTERNS OF PIN1,2 AND 7 HAVE THE SAME SHAPE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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