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April 2016

FPF34891 / FPF34892
SIDO Over-Voltage Protection Load Switch

Features

- Single Input Dual Output (SIDO) Switch
  - V_{BUS} to V_{OUT} Path
  - V_{BUS} to BAT Path
- Surge Protection under IEC 61000-4-5
  - V_{BUS}: ±100 V
- Input Voltage Range
  - V_{BUS}: 2.7 V ~ 13.5 V
- Max. Continuous Current Capability
  - V_{OUT} Path: 3.5 A
  - BAT Path: 6 A
- Ultra Low On-Resistance
  - V_{OUT} Path: Typ. 28 mΩ
  - BAT Path: Typ. 33 mΩ
- Selectable OVLO for V_{OUT} Path
- Programmable OVLO for V_{BAT}
- Over-Voltage Protection (OVP)
  - V_{OUT} Path: 13.9 V ± 400 mV (FPF34891)
  - V_{OUT} Path: 10.4 V ± 300 mV (FPF34892)
  - V_{OUT} Path: 5.8 V ± 200 mV (OVSEL = GND)
  - BAT Path: 5.8 V ± 200 mV
- Active LOW Control for V_{BUS} to V_{OUT} Path
- Active HIGH Control for V_{BUS} to BAT Path
- CMOS Output PowerGOOD for VBUS to BAT Path
- RCB for VBUS to BAT Path
- Over-Temperature Protection (OTP)

Description

The FPF3489x features a Single Input Dual Output (SIDO) power switch, which offers surge protection and Over-Voltage Protection (OVP), to protect downstream components and enhancing overall system robustness.

Channel one (V_{BUS} to V_{OUT}) is an active-low, 28 V/3.5 A rated, power MOSFET switch with an internal clamp supporting ±100 V surge protection, fixed OVP at 5.8V when OVSEL is tied to GND or 13.9V (FPF34891) / 10.4V (FPF34892) when OVSEL is floating.

Channel two (V_{BUS} to BAT) is an active-high, 5 V/6 A rated, power MOSFET, fixed OVP at VBUS is 5.8 V (±200 mV) and Reverse Current Blocking (RCB) during its OFF State. OVLO at BAT can be programmed by external resistors. The Over-Voltage status will be latched and FLAG will signal the fault by pulling low. To re-start this channel from OVLO, EN2 need to be toggled from LOW to HIGH.

The FPF3489x is available in a 28-bump, 1.67 mm x 2.96 mm Wafer-Level Chip-Scale Package (WL-CSP) with 0.4 mm pitch.

Applications

- Mobile Handsets and Tablets
- Wearable Devices

Ordering Information

Part Number	Operating Temperature Range	Top Mark	Package	Packing Method
FPF34891UCX	-40°C to +85°C	VF	28-Ball, 0.4 mm Pitch WLCSP	Tape & Reel
FPF34892UCX		VG		

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Application Diagram

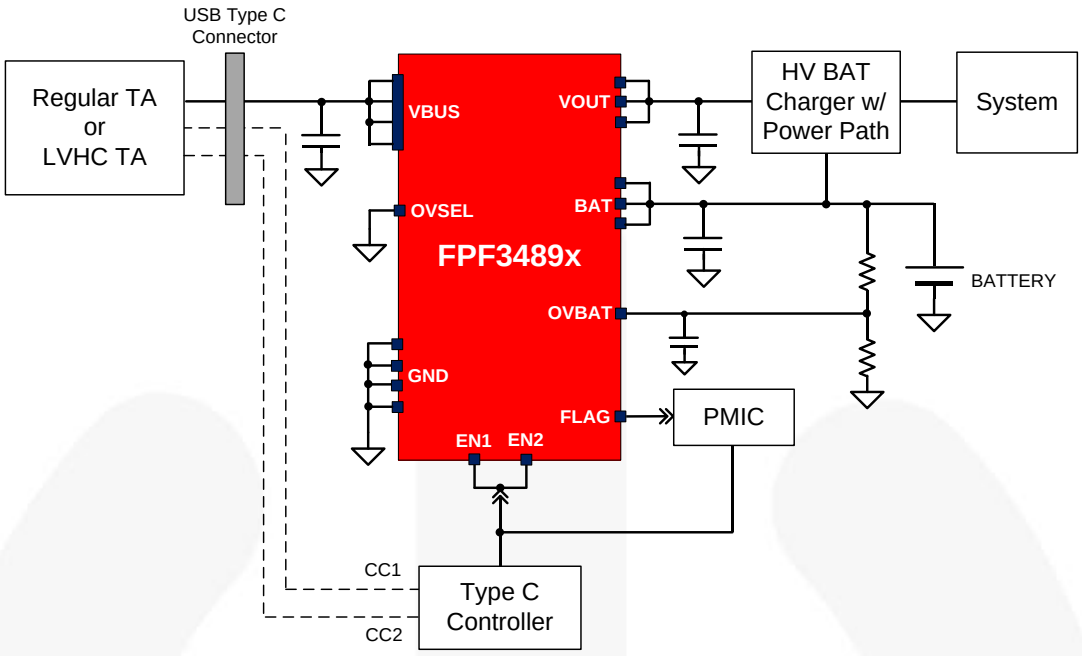


Figure 1. Typical Application

Block Diagram

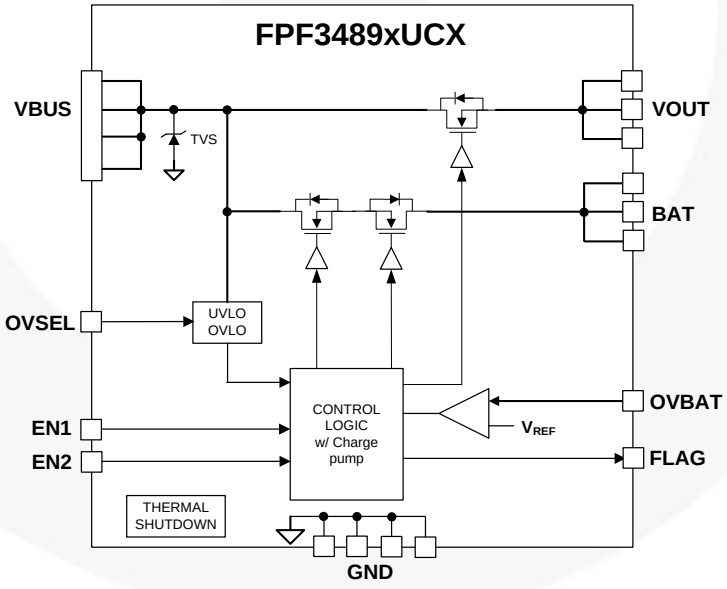


Figure 2. Functional Block Diagram

Pin Configuration

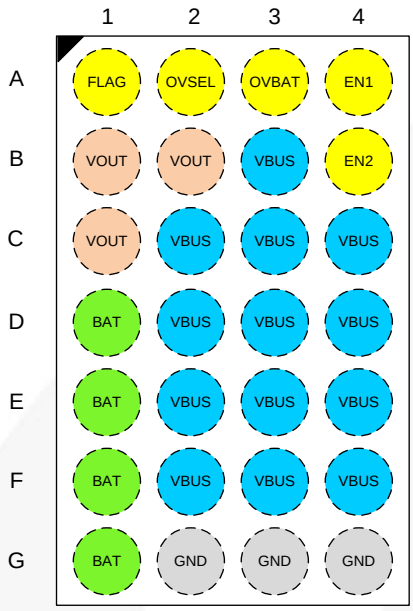


Figure 3. Pin Configuration (Top View)

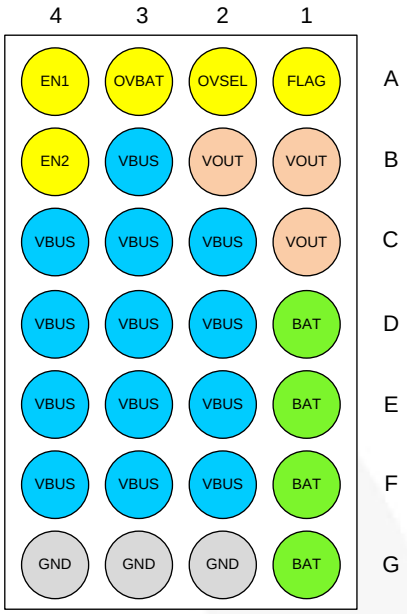


Figure 4. Pin Configuration (Bottom View)

Pin Definitions

Name	Bump	Type	Description
VBUS	B3, C2, C3, C4, D2, D3, D4, E2, E3, E4, F2, F3, F4	Input/Supply	Power Switch Input and Device Supply
VOUT	B1, B2, C1	Output	Power Switch Output to Load
BAT	D1, E1, F1, G1	Output	Power Switch Output to Battery
OVBAT	A3	Input	Over-Voltage Lockout on BAT Adjustment Pin
EN2	B4	Input	Active HIGH. Channel 2, VBUS to BAT path only. Internal pull-down resistor of 1 MΩ is included.
EN1	A4	Input	Active LOW. Channel 1, VBUS to VOUT path only. Internal pull-down resistor of 1 MΩ is included.
OVSEL	A2	Input	OVSEL Floating, OVP 13.9 V (FPF34891) or 10.4 V (FPF34892); OVSEL = GND, OVP 5.8V.
FLAG	A1	Output	Active HIGH PowerGOOD output for VBUS to BAT path. CMOS output requiring no external bias. HIGH: VBUS to BAT path is ON and in normal state. LOW: VBUS to BAT path is OFF due to EN2=LOW, UVLO, OVLO, thermal shutdown or device shutdown
GND	G2, G3, G4	GND	Ground

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Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameters		Min.	Max.	Unit
VBUS	VBUS to GND & VBUS to VOUT = GND or Float		-2[1]	28	V
VOUT	VOUT to GND		-0.3	V_{BUS}+0.3	V
BAT	BAT to GND		-0.3	6.0	V
OVBAT	OVBAT to GND			6	V
$V_{EN(n)_OVSEL_FLAG}$	EN(n), OVSEL or FLAG to GND			6	V
$I_{IN_VBUS_VOUT}$	Continuous VBUS to VOUT Current			3.5	A
	Peak VBUS to VOUT Current (5 ms)			7	A
$I_{IN_VBUS_BAT}$	Continuous VBUS to BAT Current			6	A
	Peak VBUS to BAT Current (5 ms)			12	A
t_{PD}	Total Power Dissipation at T_A=25°C			2.27	W
T_{STG}	Storage Junction Temperature		-65	+150	°C
T_J	Operating Junction Temperature			+150	°C
T_L	Lead Temperature (Soldering, 10 Seconds)			+260	°C
Θ_{JA}	Thermal Resistance, Junction-to-Ambient (1in.^{2} pad of 2 oz. copper)			55[2]	°C/W
ESD	Electrostatic Discharge Capability	Human Body Model, ANSI/ESDA/JEDEC JS-001	2		kV
		Charged Device Model, JESD22-C101	1		
	IEC61000-4-2 System Level	Air Discharge	15		
		Contact Discharge	8		
Surge	IEC 61000-4-5	V_{BUS}	±100		V

Notes:

1. Pulsed, 50 ms maximum non-repetitive.
2. Measured using 2S2P JEDEC std. PCB.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
V_{BUS}	Supply Voltage	2.7	13.5	V
C_{IN} / C_{OUT}	Input and Output Capacitance	0.1		µF
C_{BAT}	BAT Capacitance	47		µF
T_A	Operating Temperature	-40	+85	°C

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Electrical Characteristics

Unless otherwise noted, VBUS = 2.7 to 13.5 V, T_A = -40 to 85°C; Typical values are at VBUS = 5 V, I_{IN} ≤ 2 A, C_{IN}= 0.1µF and T_A = 25°C.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Basic Operation						
I_Q	Input Quiescent Current	VBUS = 5 V, EN1= EN2=LOW		145	215	µA
I_{IN_Q}	OVLO Supply Current	VBUS = 15 V, VOUT = 0 V, EN1=EN2=LOW		190	290	µA
		VBUS = 5.5 V, BAT = 0 V, EN1=EN2=HIGH		150	210	µA
V_{BUS_CLAMP}	Input Clamping Voltage	I_{IN}=10 mA		35		V
V_{BUS_UVLO}	Under-Voltage Trip Level	VBUS Rising, T_A= -40 to 85°C	2.35	2.5	2.65	V
		VBUS Falling, T_A= -40 to 85°C	2.20	2.35	2.50	V
T_{SDN}	Thermal Shutdown(3)			150		°C
T_{SDN_HYS}	Thermal Shutdown Hysteresis(3)			20		°C
VBUS to VOUT Switch (Channel 1)						
V_{CH1_OVP}	Over-Voltage Trip Level (OVSEL Floating)	VBUS Rising (FPF34891)	13.5	13.9	14.3	V
		VBUS Falling (FPF34891)		13.6		
		VBUS Rising (FPF34892)	10.0	10.4	10.8	
		VBUS Falling (FPF34892)		10.1		
	Over-Voltage Trip Level (OVSEL = GND)	VBUS Rising	5.6	5.8	6.0	
		VBUS Falling		5.65		
R_{ON_VOUT}	On-Resistance	VBUS = 5 V, I_{OUT} = 1 A, T_A = 25°C		28	39	mΩ
		VBUS = 12 V, I_{OUT} = 1 A, T_A = 25°C		28	39	mΩ
t_{DEB_VOUT}	Debounce Time	Time from V_{BUS_UVLO} < VBUS < V_{BUS_OVLO} to VOUT = 0.1 × VBUS		15		ms
t_{ON_VOUT}	Switch Turn-On Time	R_L = 100 Ω, C_L = 10 µF, VOUT from 0.1 × VBUS to 0.9 × VBUS		2		ms
t_{OFF_VOUT}	Switch Turn-Off Time(3)	R_L = 100 Ω, No C_L, VBUS > V_{OUT_OVLO} to V_{OUT} = 0.9 × VBUS			150	ns
VBUS to BAT Switch (Channel 2)						
V_{CH2_OVP}	Over-Voltage Trip Level for VBUS monitor	VBUS Rising, T_A = -40 to 85°C	5.6	5.8	6.0	V
		VBUS Falling, T_A = -40 to 85°C		5.65		V
V_{OVLO_TH}	BAT OVP set Threshold	OVBAT = 0V to V_{OVLO}, T_A = 0 to 85°C	1.145	1.155	1.165	V
		OVBAT = 0V to V_{OVLO}, T_A = -40 to 85°C	1.140	1.155	1.165	
R_{ON_BAT}	On-Resistance	VBUS = 3 V, I_{OUT} = 1 A, T_A = 25°C		33	40	mΩ
I_{RCB}	Reverse Current	VBUS = 0 V, BAT = 4.4 V			1	µA
t_{DEB_BAT}	Debounce Time	Time from V_{BUS_UVLO} < VBUS < V_{BUS_OVLO} to BAT = 0.1 × VBUS		15		ms
t_{BAT_START}	Soft-Start Time	Time from VBUS = V_{BUS_UVLO} to 0.1 × FLAG		30		ms
t_{ON_BAT}	Switch Turn-On Time	R_L = 100 Ω, C_L = 10 µF, VOUT from 0.1 × VBUS to 0.9 × VBUS		2.5		ms

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Electrical Characteristics

Unless otherwise noted, VBUS = 2.7 to 13.5 V, T_A = -40 to 85°C; Typical values are at VBUS = 5 V, I_{IN} ≤ 2 A, C_{IN}= 0.1µF and T_A = 25°C.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{OFF_BAT}	Switch Turn-Off Time[3]	R_L = 100 Ω, No C_L, VBUS > V_{BAT_OVBAT} to BAT = 0.9 × VBUS			150	ns
Digital Signals						
V_{OH}	FLAG Output HIGH Voltage	VBUS = 5 V, EN2 = LOW	1.6	1.8	2.0	V
V_{OL}	FLAG Output LOW Voltage	VBUS = 5 V, EN2 = HIGH			0.5	V
$R_{PD_EN(n)}$	Internal Pull-Down Resistor at EN1 and EN2			1		MΩ
R_{PU_OVSEL}	Internal Pull-Up Resistor at OVSEL			1		MΩ
$VIH_{_EN(n)_OVSEL}$	Logic Enable HIGH Voltage	VBUS Operating Range	1.2			V
$VIL_{_EN(n)_OVSEL}$	Logic Enable LOW Voltage	VBUS Operating Range			0.5	V
$I_{OVSEL_EN(n)_LEAK}$	OVSEL and EN(n) Leakage Current	VBUS = 5 V, VOUT, BAT = Floating		5	7	µA

Note:

3. Guaranteed by characterization and design.

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Timing Diagrams

VBUS to VOUT Path



Figure 5. Timing for VBUS to VOUT Power Up/Down and Normal Operation

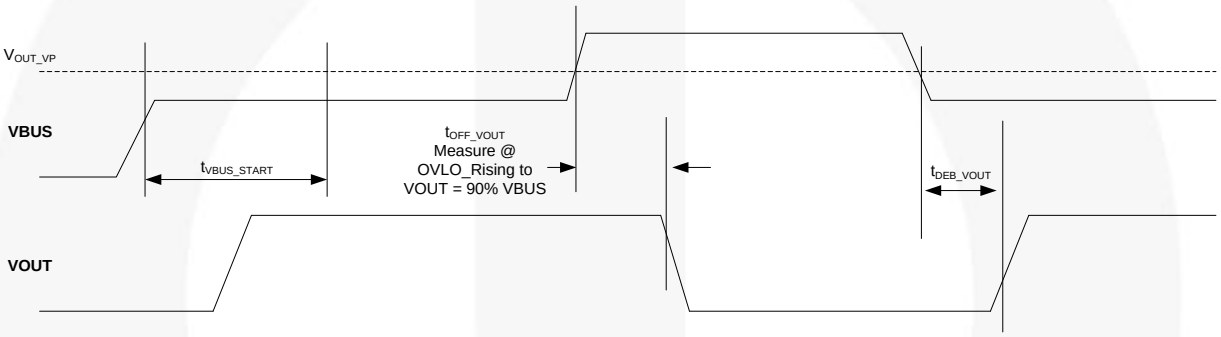


Figure 6. Timing for VBUS to VOUT OVLO Operation (EN1=LOW)

VBUS to BAT Path

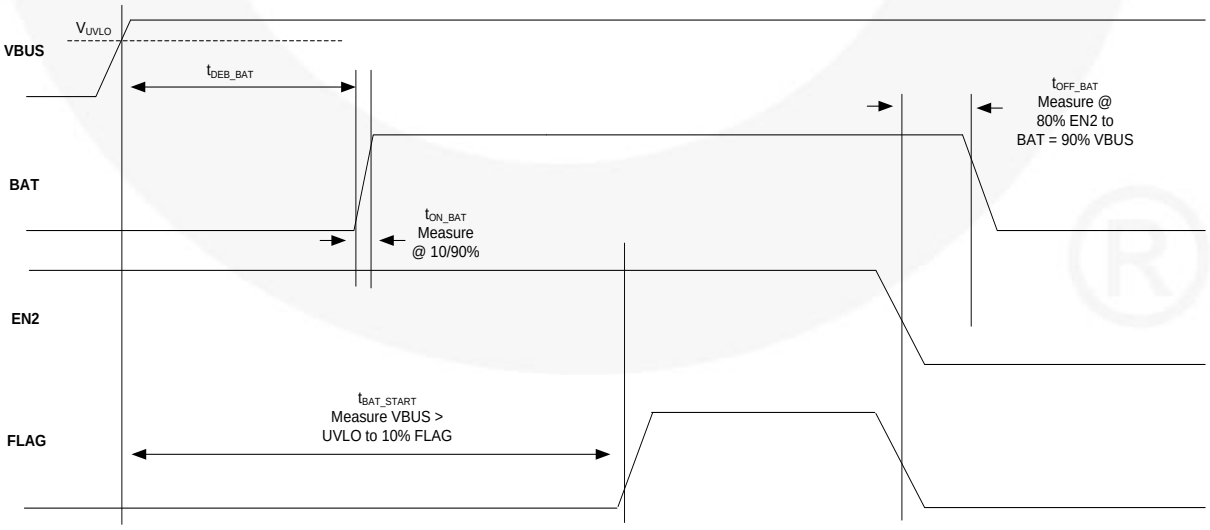


Figure 7. Timing for VBUS to BAT Power Up/Down and Normal Operation

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Timing Diagrams (Continued)

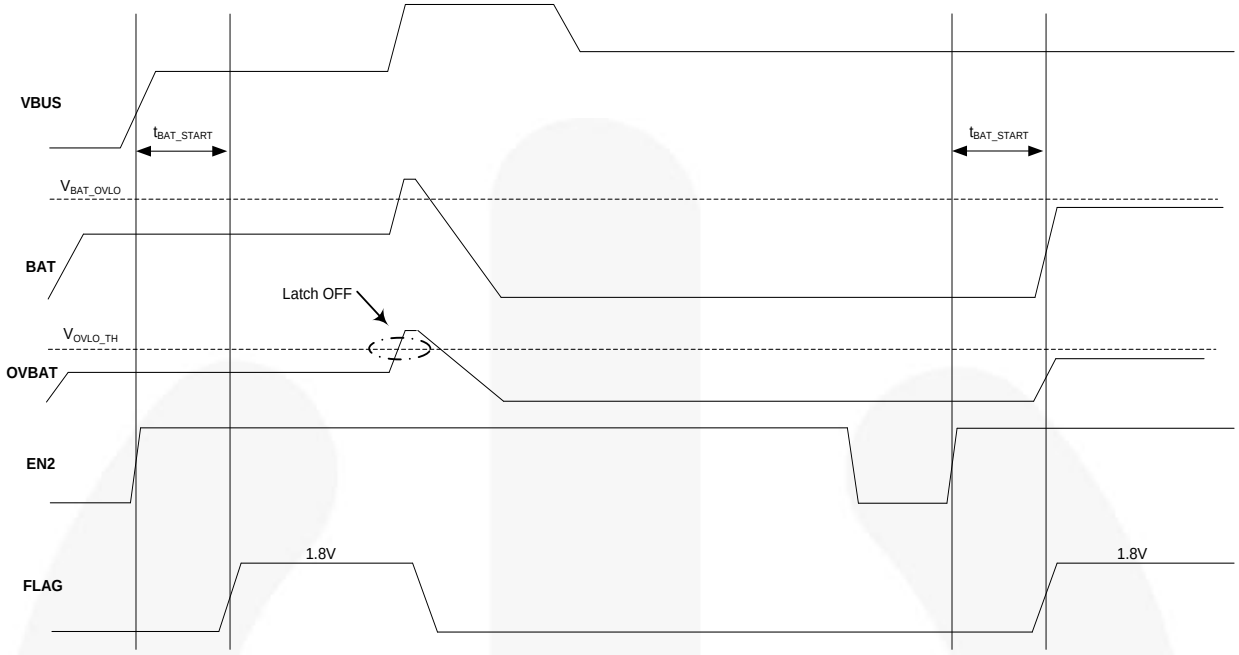


Figure 8. Timing for VBUS to BAT OVLO Operation (EN2=HIGH)

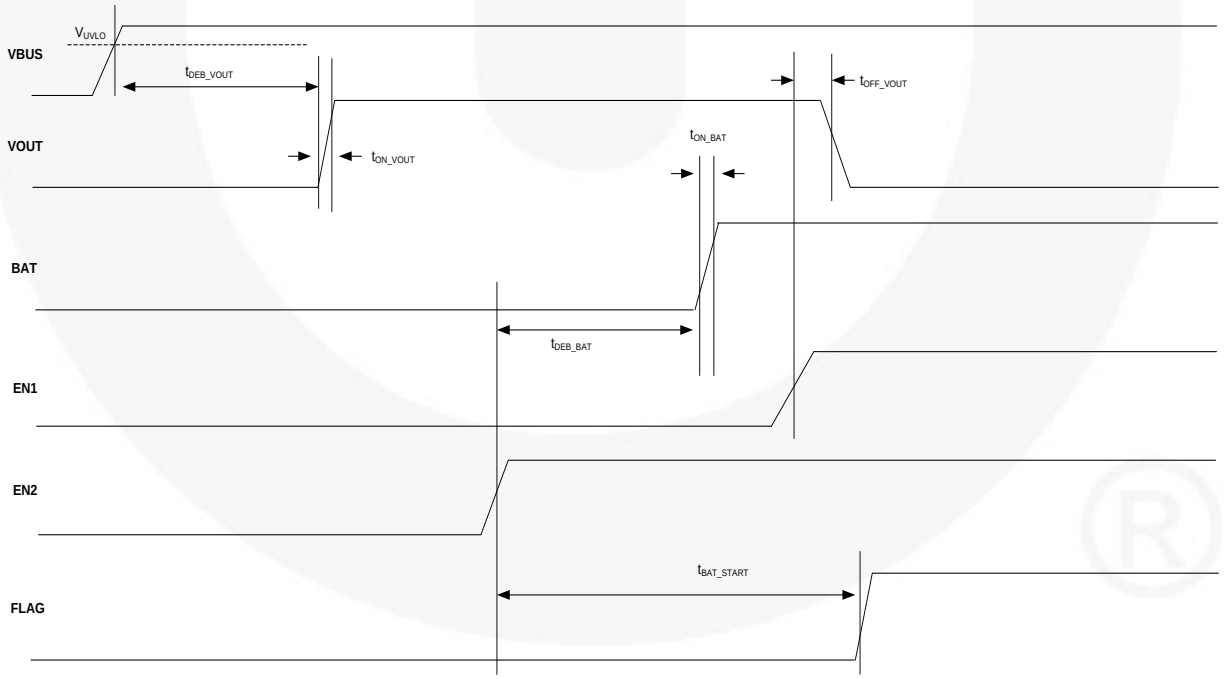


Figure 9. Timing for Overall ON/OFF Operation

Operation and Application Description

Input Capacitor

To limit the voltage drop on the input supply caused by transient inrush current when the switches turns, a capacitor must be placed in between the VBUS and GND pins. A high-value capacitor on C_{IN} can be used to reduce the voltage drop in high-current applications.

Under-Voltage Lockout (UVLO)

The under-voltage lockout turns the switches off if the input voltage drops below the lockout threshold. With the enable pins, EN1 & EN2, active, the input voltage rising above the UVLO threshold releases the lockout and enables the switches.

Thermal Shutdown

The thermal shutdown protects the die from internally or externally generated excessive temperature. During an over-temperature condition, the switch is turned off. The switch automatically turns on again if the temperature of the die drops below the threshold temperature.

FLAG Reporting

To indicate the status of channel 2, push-pull output FLAG signal high (typical 1.8V) when channel 2 is turned on. FLAG will output low when channel 2 is turned off.

Over-Voltage Lockout

To protect the system, FPF3489x provide multi level over voltage protection.

For channel 1 (VBUS to VOUT), 3 different levels can be chosen. When OVSEL is tied to GND, OVP will be triggered once VBUS voltage is higher than typical 5.8V. With OVSEL floating, OVP will be triggered when VBUS voltage is higher than typical 13.9V (FPF34891) or 10.4V (FPF34892). FLAG voltage will output low until the over voltage condition disappears.

For channel 2 (VBUS to BAT), both VBUS and BAT voltage will be monitored. Once VBUS voltage is higher than typical 5.8V, channel 2 will be turned off and output low at FLAG pin until VBUS drop below 5.65V (typical). Once BAT voltage is higher than pre-set value (set by external resistors), channel 2 will be turned off and output low at FLAG pin. This status will be latched even after BAT voltage drop to lower than OVP value. To re-active the switch, EN2 need to be toggled.

The OVLO level on BAT can be pre-set by connecting external resistor ladder to the OVBAT pin. Equation (1) can produce the desired trip voltage and resistor values.

$$V_{BAT_OVLO} = V_{OVLO_TH} \times [1 + R1/R2] \quad (1)$$

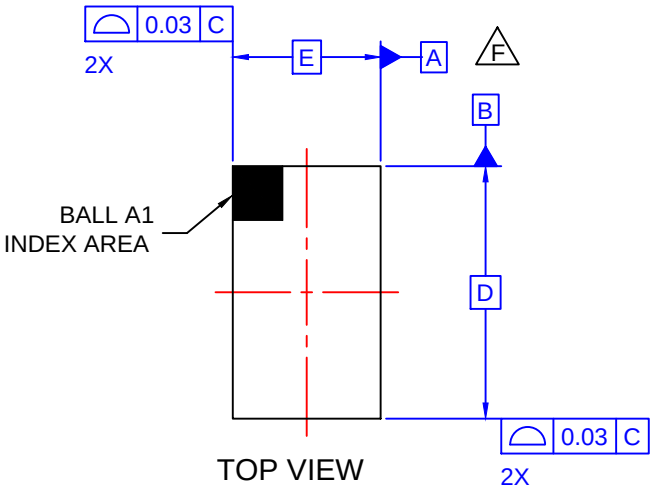
Recommended minimum R1 = 1 MΩ to reduce leakage and screen unexpected glitch.

The following information applies to the WL-CSP package dimensions on the next page:

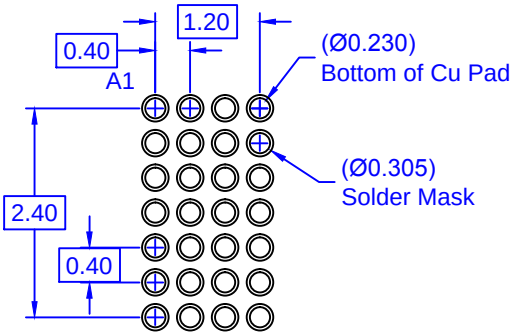
Product-Specific Dimensions

D	E	X	Y
2960 µm ±30 µm	1670 µm ±30 µm	235 µm ±18 µm	280 µm ±18 µm

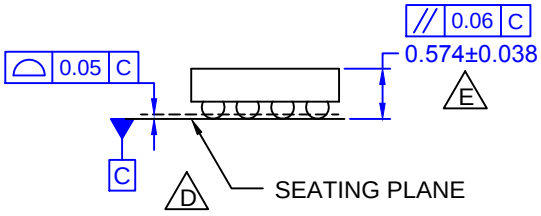
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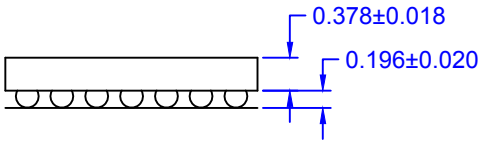


TOP VIEW

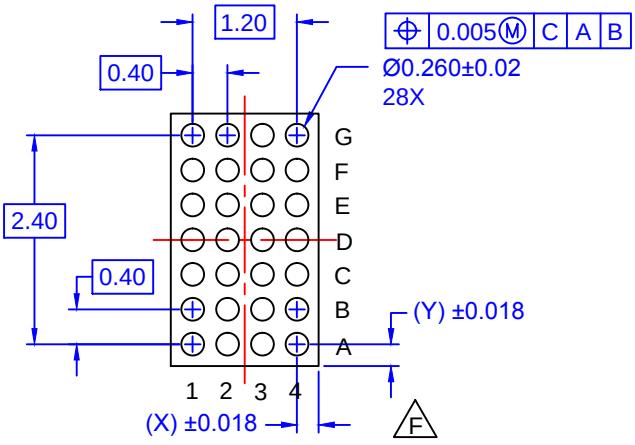


RECOMMENDED LAND PATTERN
(NSMD PAD TYPE)





SIDE VIEWS



BOTTOM VIEW

NOTES

A. NO JEDEC REGISTRATION APPLIES.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCE PER ASMEY14.5M, 2009.
D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.
E. PACKAGE NOMINAL HEIGHT IS 574 ± 38 MICRONS (536-612 MICRONS).
F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.
G. DRAWING FILENAME: MKT-UC028AB REV1.

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