# 2 MHz, Synchronous Boost DC-to-DC Converters

Data Sheet

# ADP1606/ADP1607

## FEATURES

- Up to 96% efficiency
- 0.8 V to $V_{OUT}$ input voltage range
- Low 0.9 V input start-up voltage
- 1.8 V fixed output voltage (ADP1606)
- 1.8 V to 3.3 V adjustable output voltage range (ADP1607)
- 23 µA quiescent current
- Fixed pulse-width modulation (PWM) and light load pulse frequency modulation (PFM) mode options
- Synchronous rectification
- True shutdown output isolation
- Internal soft start, compensation, and current limit
- 2 mm × 2 mm, 6-lead LFCSP
- Compact solution size

## APPLICATIONS

- 1-cell and 2-cell alkaline and NiMH/NiCd powered devices
- Portable audio players, instruments, and medical devices
- Solar cell applications
- Miniature hard disk power supplies
- Power LED status indicators

## TYPICAL APPLICATION CIRCUITS

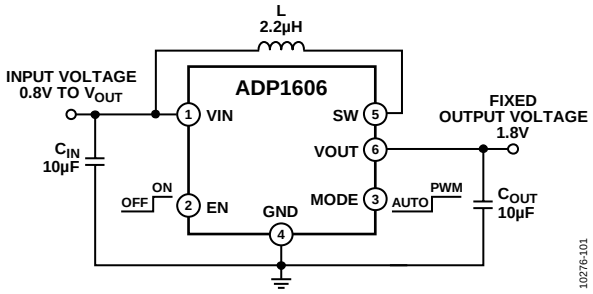



*Figure 1. ADP1606*

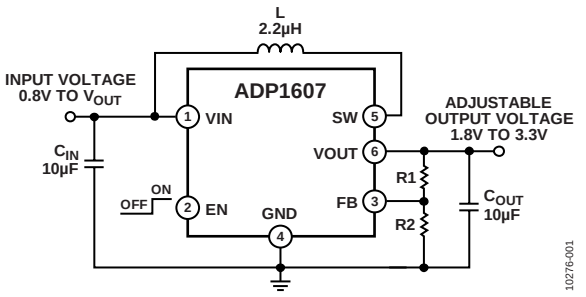



*Figure 2. ADP1607*

## GENERAL DESCRIPTION

The ADP1606/ADP1607 are high efficiency, synchronous, fixed frequency, step-up dc-to-dc switching converters with a 1.8 V fixed output voltage option and a 1.8 V to 3.3 V adjustable output voltage option for use in portable applications.

The 2 MHz operating frequency enables the use of small footprint, low profile external components. Additionally, the synchronous rectification, internal compensation, internal fixed current limit, and current mode architecture allow excellent transient response and a minimal external part count.

Other key features include fixed PWM and light load PFM mode options, true output isolation, thermal shutdown (TSD), and logic controlled enable. Available in a lead-free, thin, 6-lead LFCSP package, the ADP1606/ADP1607 are ideal for providing efficient power conversion in portable devices.

Rev. D

Document Feedback

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## REVISION HISTORY

**7/14—Rev. C to Rev. D**

Added ADP1606 ... Universal
Change to Features Section and General Description Section ... 1
Added Figure 1; Renumbered Sequentially ... 1
Changes to Table 1 ... 3
Changes to Table 2 and Thermal Resistance Section ... 4
Added Figure 3 and Table 5; Renumbered Sequentially ... 5
Changes to Table 4 ... 5
Changes to Figure 11 ... 7
Added Figure 26 and Figure 27 ... 9
Changes to Figure 28, Overview Section, Modes of Operation Section, and PWM Mode Section ... 10
Added Table 6 ... 10
Changes to Auto Mode Section, PFM Mode Section, and Mode Transition Section ... 11
Changes to Setting the Output Voltage Section and Inductor Selection Section ... 12
Changes to Layout Guidelines Section ... 14
Added Figure 30 ... 14
Changes to Ordering Guide ... 15

**12/13—Rev. B to Rev. C**

Changes to Figure 21 ... 9

**7/13—Rev. A to Rev. B**

Changes to Captions for Figure 22 and Figure 23 ... 9
Changed Synchronous Rectification Section ... 11

**12/12—Rev. 0 to Rev. A**

Changes to Features Section ... 1
Changed $T_J$ to $T_A$ in Specifications Section ... 3
Changed Figure 6, Figure 7, and Figure 8 Captions ... 6
Changes to Table 5 ... 12
Changes to Choosing the Output Capacitor Section ... 13

**10/12—Revision 0: Initial Version**

# SPECIFICATIONS

$V_{IN}$ = $V_{EN}$ = 1.2 V, $V_{OUT}$ = 3.3 V at $T_A$ = −40°C to +85°C for minimum/maximum specifications, and $T_A$ = 25°C for typical specifications, unless otherwise noted. All limits at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC). Specifications are subject to change without notice.

**Table 1.**

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| SUPPLY | | | | | | |
| Minimum Start-Up Voltage[1] | | $R_{MIN}$ = 22 Ω | 0.9 | | | V |
| Operating Input Voltage Range[2] | $V_{IN}$ | | 0.8 | | $V_{OUT}$ | V |
| Shutdown Current | $I_{QSD}$ | $V_{EN}$ = GND, $V_{OUT}$ = GND, $T_A$ = −40°C to +45°C[3] | | 0.06 | 0.67 | µA |
| Quiescent Current | | Nonswitching, auto operating mode only | | | | |
| Measured on VOUT | | $T_A$ = −40°C to +45°C, ADP1607 | | 23 | 29 | µA |
| | | $T_A$ = −40°C to +85°C, ADP1607 | | 23 | 40 | µA |
| | | $T_A$ = −40°C to +45°C, ADP1606, $V_{OUT}$ = 1.8 V | | 25 | 35 | µA |
| | | $T_A$ = −40°C to +85°C, ADP1606, $V_{OUT}$ = 1.8 V | | 25 | 55 | µA |
| Measured on VIN | | $T_A$ = −40°C to +45°C | | 6 | 11 | µA |
| | | $T_A$ = −40°C to +85°C | | 6 | 14.6 | µA |
| Soft Start Time | | | | 1.3 | | ms |
| SWITCH | | | | | | |
| Current Limit | $I_{CL}$ | ADP1607, $V_{OUT}$ = 3.3 V | 0.8 | 1 | 1.3 | A |
| | | ADP1606, $V_{OUT}$ = 1.8 V | 0.8 | 1 | 1.3 | A |
| NMOS On Resistance | $R_{DSON_N}$ | $I_{SW}$ = 500 mA | | 120 | 165 | mΩ |
| PMOS On Resistance | $R_{DSON_P}$ | $I_{SW}$ = 500 mA | | 160 | 225 | mΩ |
| SW Leakage Current[3] | | $V_{SW}$ = 1.2 V, $V_{OUT}$ = 0 V, $T_A$ = −40°C to +45°C[3] | | 0.18 | 2 | µA |
| OSCILLATOR | | | | | | |
| Switching Frequency | $f_{SW}$ | | 1.8 | 2 | 2.2 | MHz |
| Maximum Duty Cycle | $D_{MAX}$ | | 85 | 90 | | % |
| OUTPUT | | | | | | |
| $V_{OUT}$ Range | $V_{OUT}$ | ADP1607 | 1.8 | | 3.3 | V |
| $V_{OUT}$ Accuracy | $V_{OUT}$ | ADP1606, $V_{OUT}$ = 1.8 V | 1.764 | 1.8 | 1.836 | V |
| FB Pin Voltage | $V_{FB}$ | PWM mode, ADP1607 | 1.2338 | 1.259 | 1.2842 | V |
| FB Pin Current | $I_{FB}$ | $V_{FB}$ = 1.26 V, ADP1607 | | 0.1 | 0.25 | µA |
| EN/MODE LOGIC | | | | | | |
| Input Voltage Threshold Low | $V_{IL}$ | | | | 0.25 | V |
| Input Voltage Threshold High | $V_{IH}$ | | 0.8 | | | V |
| EN Leakage Current | | $V_{EN}$ = GND or VIN, $V_{OUT}$ = 0 V | | 0.001 | 0.25 | µA |
| MODE Leakage Current | | $V_{MODE}$ = GND or VIN, $V_{OUT}$ = 0 V, ADP1606 | | 0.001 | 0.25 | µA |
| THERMAL SHUTDOWN (TSD)[4] | | | | | | |
| Thermal Shutdown Threshold | | | | 150 | | °C |
| Thermal Shutdown Hysteresis | | | | 15 | | °C |

[1] Guaranteed by design, but not production tested. VIN can never exceed VOUT once the ADP1606/ADP1607 is enabled.
[2] Minimum value is characterized by design. Maximum value is characterized on the bench.
[3] This parameter is the semiconductor leakage current. The semiconductor leakage current doubles with every 10°C increase in temperature. The maximum limit follows the same trend over temperature.
[4] TSD protection is only active in PWM mode.

# ABSOLUTE MAXIMUM RATINGS

**Table 2.**

| Parameter | Rating |
|---|---|
| VIN, VOUT to GND | −0.3 V to +3.6 V |
| FB to GND | −0.3 V to +1.4 V |
| EN, SW, MODE to GND (When VIN ≥ VOUT) | −0.3 V to VIN + 0.3 V |
| EN, SW, MODE to GND (When VIN < VOUT) | −0.3 V to VOUT + 0.3 V |
| EPAD to GND | −0.3 V to + 0.3 V |
| Operating Ambient Temperature Range | −40°C to +85°C |
| Maximum Junction Temperature | 90°C |
| Storage Temperature Range | −65°C to +150°C |

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Absolute maximum ratings apply individually only, not in combination.

## THERMAL OPERATING RANGES

The ADP1606/ADP1607 can be damaged when the junction temperature limits are exceeded. The maximum operating junction temperature ($T_{J(MAX)}$) takes precedence over the maximum operating ambient temperature ($T_{A(MAX)}$). Monitoring ambient temperature does not guarantee that the junction temperature ($T_J$) is within the specified temperature limits.

In applications with high power dissipation and poor printed circuit board (PCB) thermal resistance, the maximum ambient temperature may need to be derated. In applications with moderate power dissipation and low PCB thermal resistance, the maximum ambient temperature can exceed the maximum limit as long as the junction temperature is within specification limits.

The junction temperature ($T_J$) of the device is dependent on the ambient temperature ($T_A$), the power dissipation of the device ($P_D$), and the junction-to-ambient thermal resistance of the package ($\theta_{JA}$). Maximum junction temperature ($T_J$) is calculated from the ambient temperature ($T_A$) and power dissipation ($P_D$) using the following formula:

$$T_J = T_A + (P_D \times \theta_{JA})$$

## THERMAL RESISTANCE

Junction-to-ambient thermal resistance ($\theta_{JA}$) of the package is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages. The junction-to-ambient thermal resistance is highly dependent on the application and board layout. In applications where high maximum power dissipation exists, attention to thermal board design is required. The value of $\theta_{JA}$ may vary, depending on PCB material, layout, and environmental conditions.

$\theta_{JA}$ and $\theta_{JC}$ (junction to case) are determined according to JESD51-9 on a 4-layer PCB with natural convection cooling and the exposed pad soldered to the board with thermal vias.

**Table 3.**

| Package Type | $\theta_{JA}$ | $\theta_{JC}$ | Unit |
|---|---|---|---|
| 6-Lead LFCSP | 66.06 | 4.3 | °C/W |

For additional information on thermal resistance, refer to the *Thermal Characteristics of IC Assembly*.

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

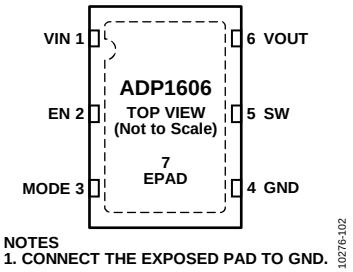



*Figure 3. ADP1606 Pin Configuration*

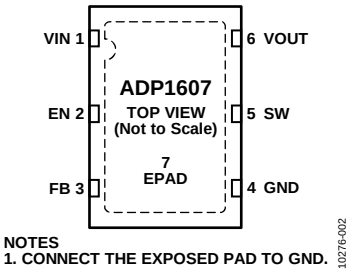



*Figure 4. ADP1607 Pin Configuration*

**Table 4. ADP1606 Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | VIN | Analog and Power Supply Pin. |
| 2 | EN | Shutdown Control Pin. Drive EN high to turn on the synchronous boost; drive EN low to turn it off. |
| 3 | MODE | Mode Select Pin. This pin toggles between auto mode (automatic transitioning between PFM and PWM mode) and fixed PWM mode. Set MODE low to allow the device to operate in auto mode. Pull MODE high to force the device to operate in PWM mode. The voltage applied to MODE cannot be higher than the voltage applied to VIN. Do not leave this pin floating. |
| 4 | GND | Analog and Power Ground Pin. |
| 5 | SW | Drain Connection for NMOS and PMOS Power Switches. |
| 6 | VOUT | Output Voltage and Source Connection of PMOS Power Switch. |
| 7 | EPAD | Exposed Pad. Connect to GND. |

**Table 5. ADP1607 Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | VIN | Analog and Power Supply Pin. |
| 2 | EN | Shutdown Control Pin. Drive EN high to turn on the synchronous boost; drive EN low to turn it off. |
| 3 | FB | Output Voltage Feedback Pin. |
| 4 | GND | Analog and Power Ground Pin. |
| 5 | SW | Drain Connection for NMOS and PMOS Power Switches. |
| 6 | VOUT | Output Voltage and Source Connection of PMOS Power Switch. |
| 7 | EPAD | Exposed Pad. Connect to GND. |

# TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN}$ = 1.2 V, $V_{OUT}$ = 3.3 V, L = 2.2 µH ($DCR_{MAX}$ = 66 mΩ, VLF302512MT-2R2M), $C_{IN}$ = 10 µF, $C_{OUT}$ = 10 µF (10 V, 20%, LMK107BJ106MALTD), $V_{EN}$ = $V_{IN}$, and $T_A$ = 25°C, unless otherwise noted.

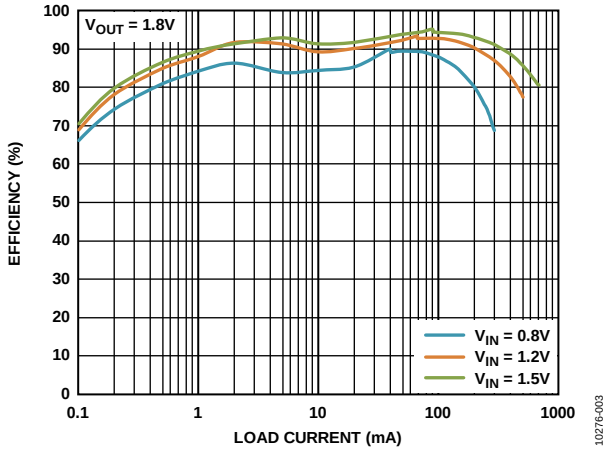



Figure 5. ADP1607 Auto Mode Efficiency vs. Load Current, $V_{OUT}$ = 1.8 V

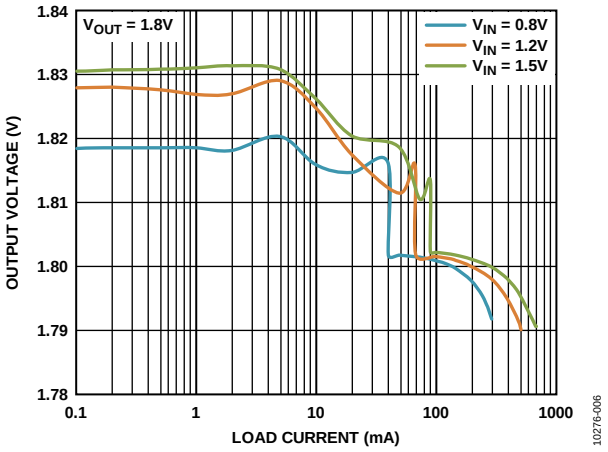



Figure 8. ADP1607 Auto Mode Output Voltage Load Regulation, $V_{OUT}$ = 1.8 V

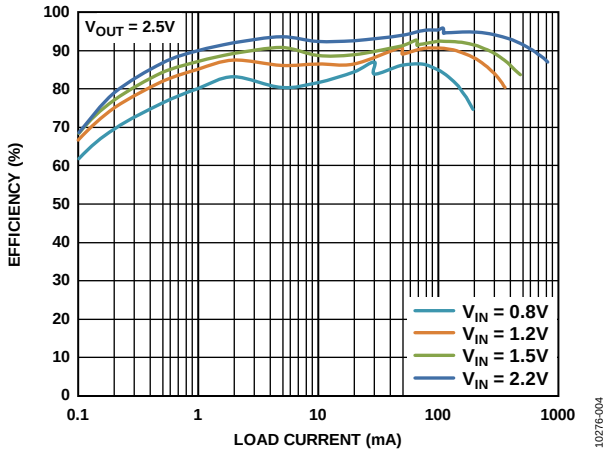



Figure 6. ADP1607 Auto Mode Efficiency vs. Load Current, $V_{OUT}$ = 2.5 V

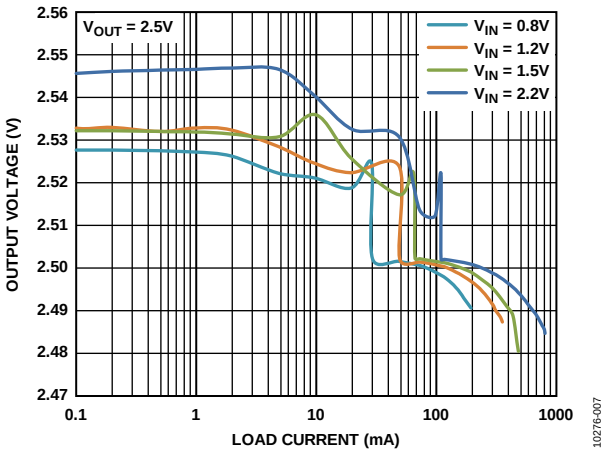



Figure 9. ADP1607 Auto Mode Output Voltage Load Regulation, $V_{OUT}$ = 2.5 V

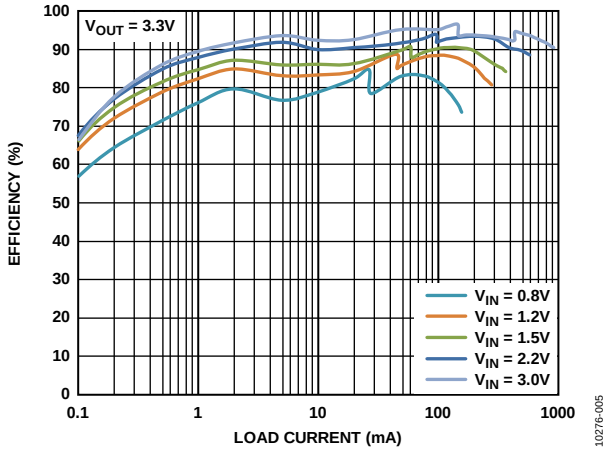



Figure 7. ADP1607 Auto Mode Efficiency vs. Load Current, $V_{OUT}$ = 3.3 V

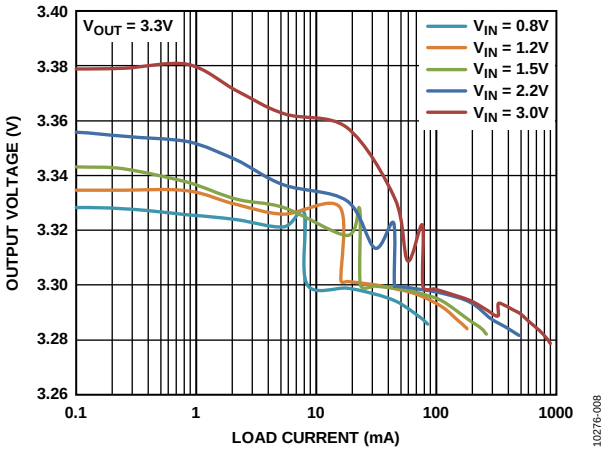



Figure 10. ADP1607 Auto Mode Output Voltage Load Regulation, $V_{OUT}$ = 3.3 V

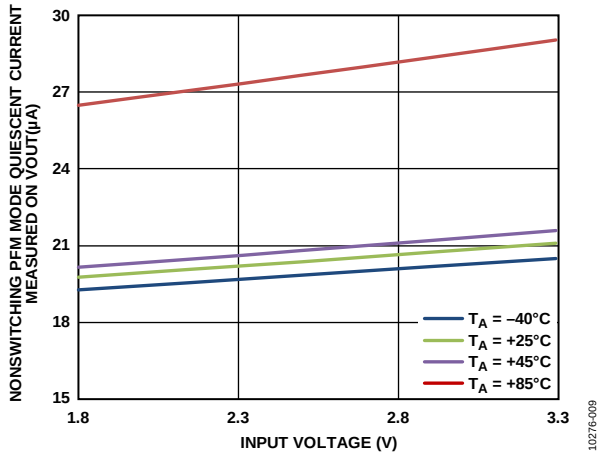



Figure 11. ADP1607 Nonswitching PFM Mode Quiescent Current Measured on VOUT vs. Input Voltage

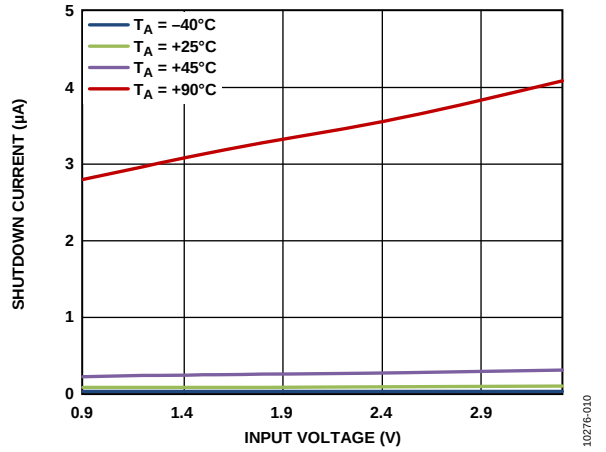



Figure 12. Shutdown Current vs. Input Voltage

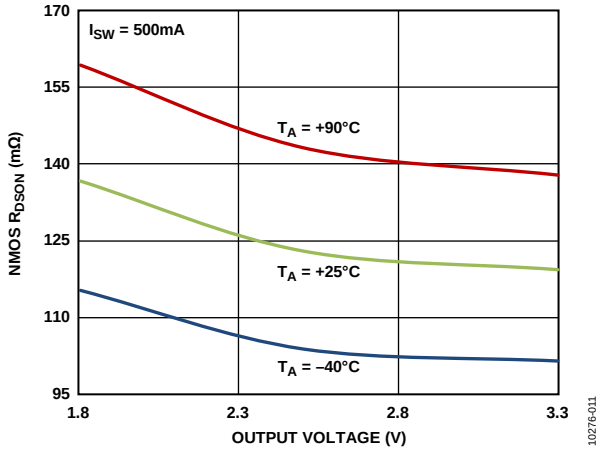



Figure 13. NMOS Drain-to-Source On Resistance

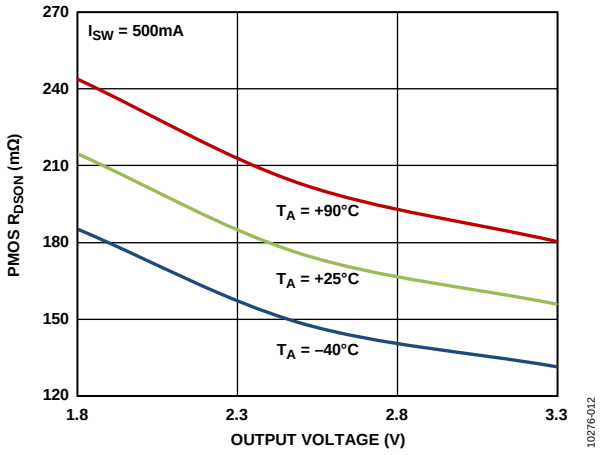



Figure 14. PMOS Drain-to-Source On Resistance

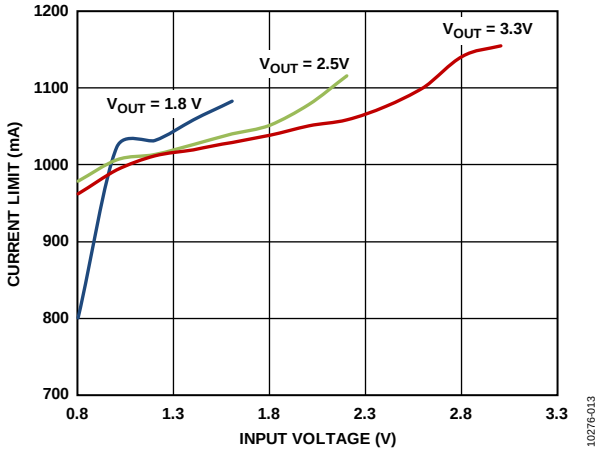



Figure 15. Switch Current Limit vs. Input Voltage

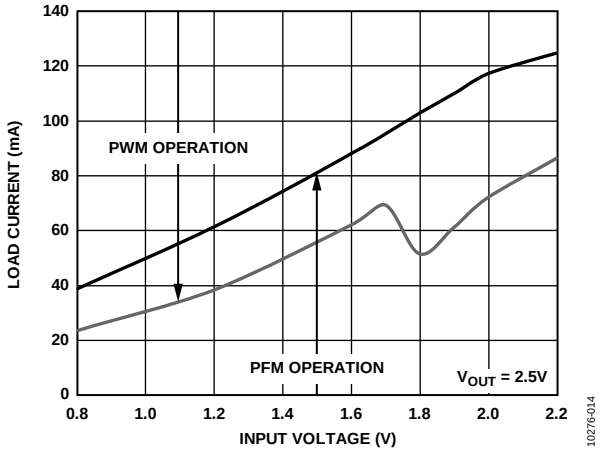



Figure 16. Auto Mode Transition Thresholds

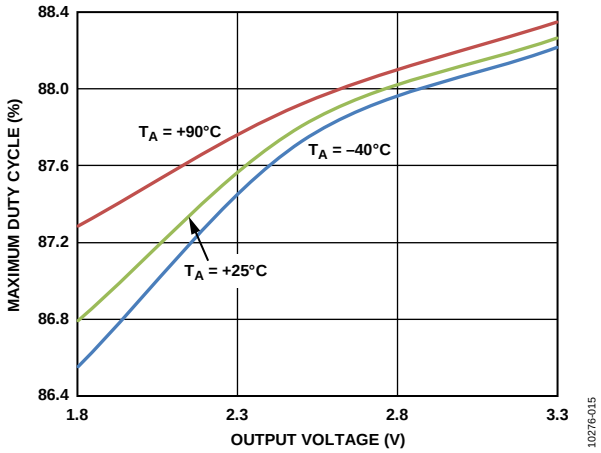



Figure 17. Maximum Duty Cycle vs. Output Voltage

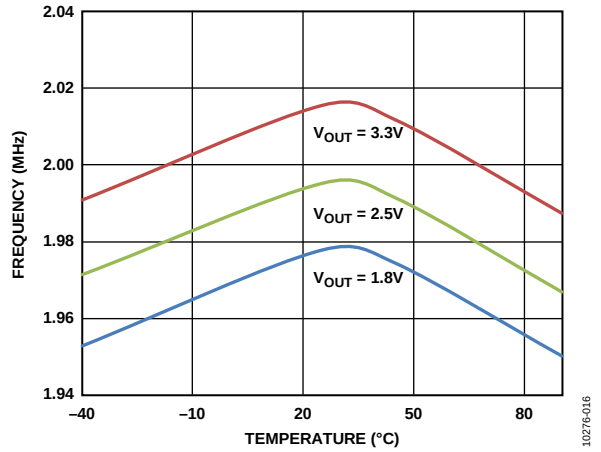



Figure 18. Frequency vs. Temperature

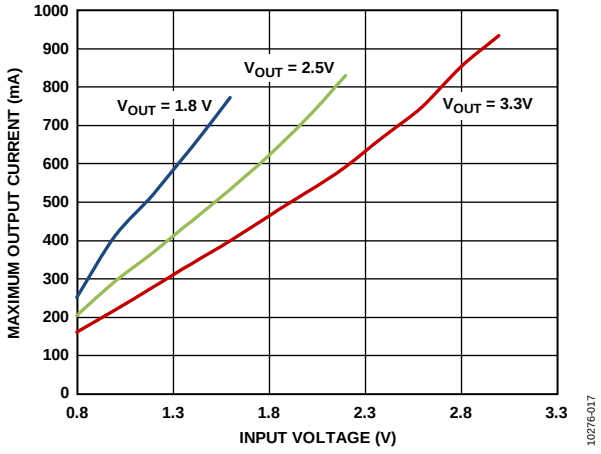



Figure 19. Maximum Output Current vs. Input Voltage

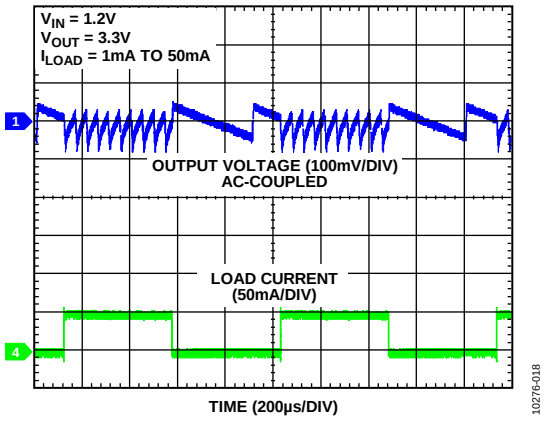



Figure 20. PFM Mode Load Transient Response (Auto Mode Part)

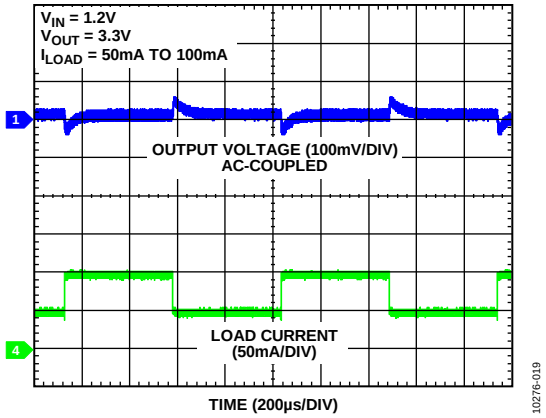



Figure 21. PWM Mode Load Transient Response (Fixed PWM Mode Part)

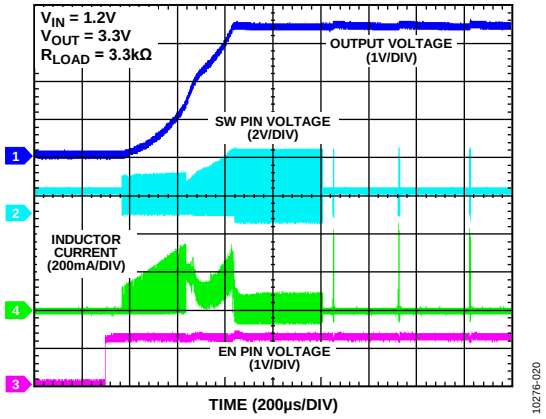



Figure 22. Startup, $R_{LOAD}$ = 3.3 kΩ

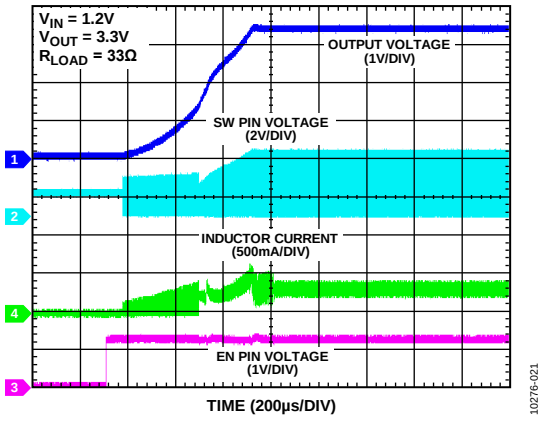



Figure 23. Startup, $R_{LOAD}$ = 33 Ω

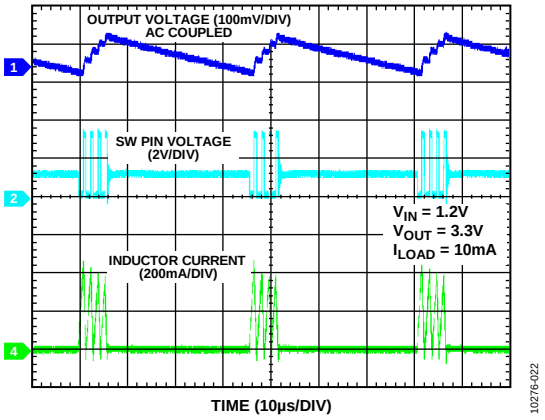



Figure 24. Typical PFM Mode Operation, $I_{LOAD}$ = 10 mA

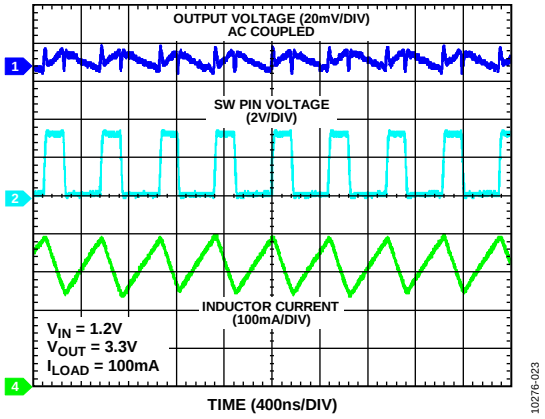



Figure 25. Typical PWM Mode Operation, $I_{LOAD}$ = 100 mA

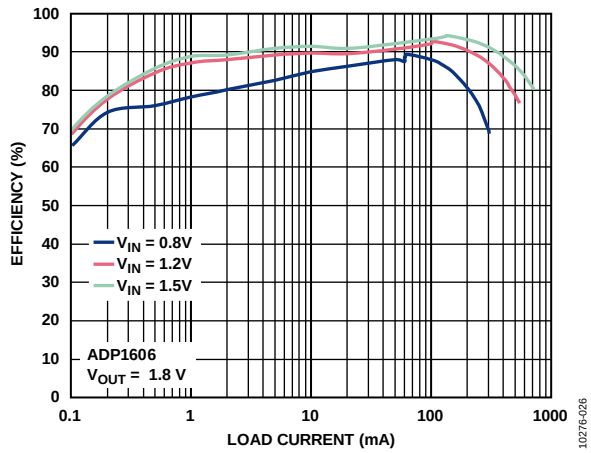



Figure 26. ADP1606 Auto Mode Efficiency vs. Load Current, $V_{OUT}$ = 1.8 V

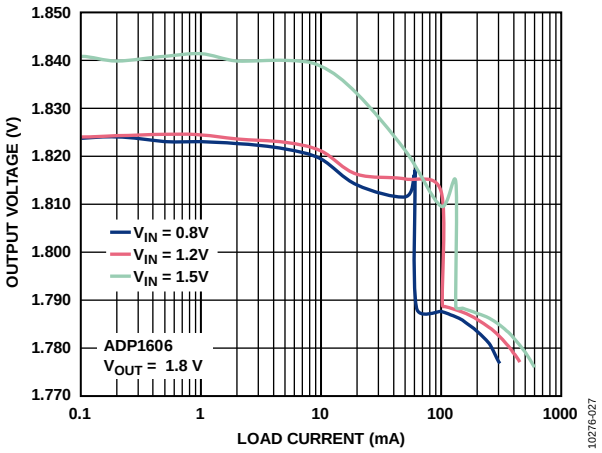



Figure 27. ADP1606 Auto Mode Output Voltage Load Regulation, $V_{OUT}$ = 1.8 V

# THEORY OF OPERATION

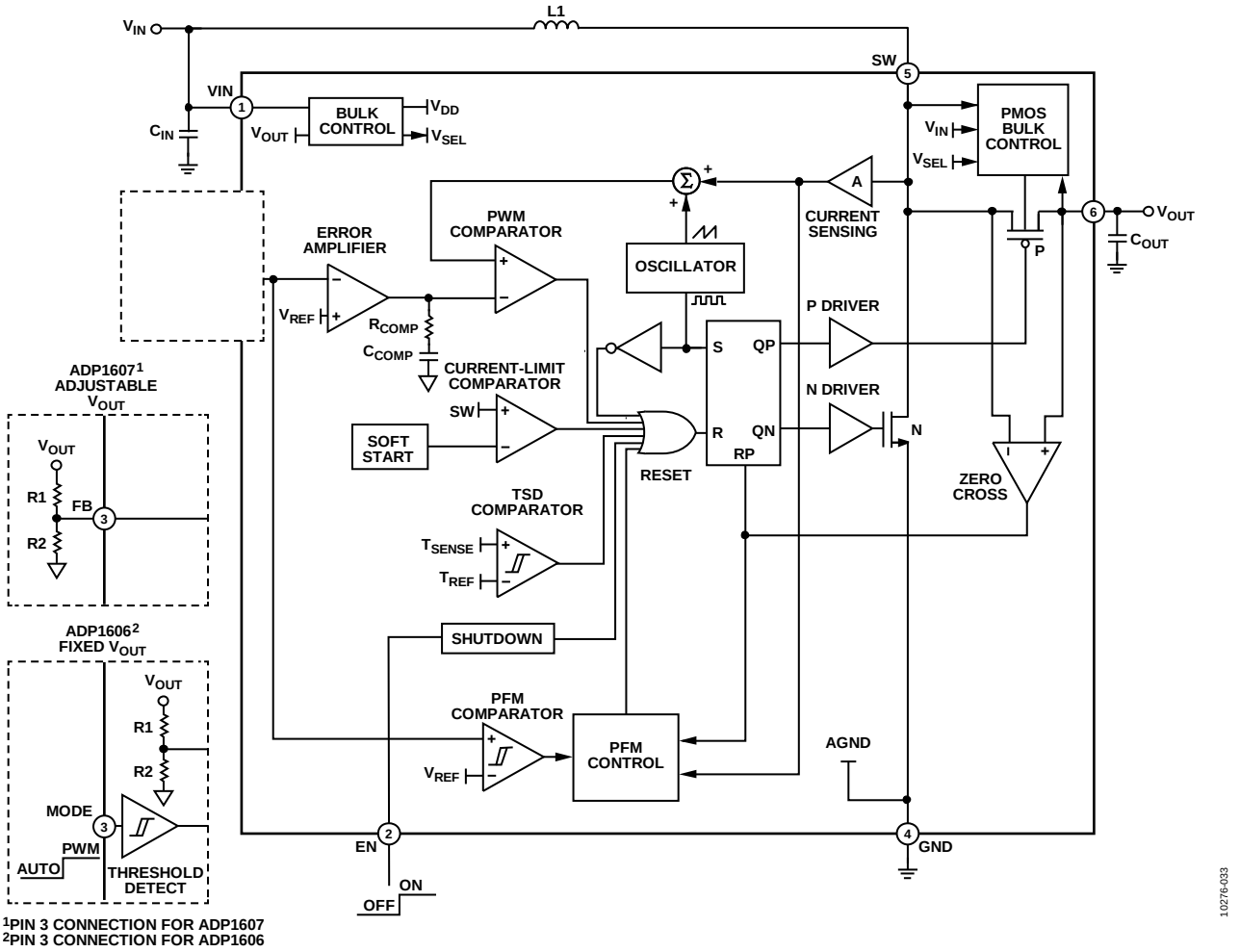



*Figure 28. Block Diagram*

## OVERVIEW

The ADP1606/ADP1607 are current mode, synchronous, step-up dc-to-dc switching converters available in a 1.8 V fixed output voltage option and a 1.8 V and 3.3 V adjustable output voltage option. Other features include logic controlled enable, fixed PWM and light load PFM mode options, true output isolation, internal soft start, internal fixed current limit, internal compensation, and TSD protection.

## ENABLE/SHUTDOWN

The EN input turns the ADP1606/ADP1607 on or off. Connect EN to GND or logic low to shut down the device and reduce the current consumption to 0.06 µA (typical). Connect EN to VIN or logic high to enable the device. Do not exceed $V_{IN}$. Do not leave this pin floating.

## MODES OF OPERATION

The ADP1606/ADP1607 are available in a fixed PWM mode option for noise sensitive applications or in an auto PFM-to-PWM transitioning mode option to optimize power at light loads. The ADP1606 has a MODE pin for application controlled selection of fixed PWM mode or automatic switching from PFM to PWM.

**Table 6. ADP1606/ADP1607 Options**

| Model No. | Output Voltage | Operating Modes |
|---|---|---|
| ADP1606ACPZN1.8-R7 | 1.8 V | MODE pin |
| ADP1607ACPZN001-R7 | Adjustable | Fixed PWM |
| ADP1607ACPZN-R7 | Adjustable | Fixed auto |

### *PWM Mode*

The PWM version of the ADP1607 and the PWM mode of the ADP1606 use a current mode PWM control scheme to force the device to maintain a fixed 2 MHz fixed frequency while regulating the output voltage over all load conditions. The auto mode version of the ADP1607 and the auto mode of the ADP1606 operate in PWM for higher load currents. In PWM, the output voltage is monitored at the FB pin through the external resistive voltage divider. The voltage at FB is compared to the internal 1.259 V reference by the internal error amplifier.

This current-mode PWM regulation system allows fast transient response and tight output voltage regulation. PWM mode operation results in lower efficiencies than PFM mode at light loads.

### Auto Mode

Auto mode is a power saving feature that forces the auto mode version of the ADP1607 and the auto mode of the ADP1606 to switch between PFM and PWM in response to output load changes. In auto mode, the ADP1606/ADP1607 operate in PFM mode for light load currents and switch to PWM mode for medium and heavy load currents.

### PFM Mode

When the auto mode version of the ADP1607 and the auto mode of the ADP1606 are operating under light load conditions, the effective switching frequency and supply current are decreased and varied using PFM to regulate the output voltage. This results in improved efficiencies and lower quiescent currents. In PFM mode, the converter only switches when necessary to keep the output voltage between the PFM comparator high output voltage threshold and the lower sleep mode exit voltage threshold. Switching stops when the upper PFM limit is reached and resumes when the lower sleep mode exit threshold is reached.

When $V_{OUT}$ exceeds the upper PFM threshold, switching stops and the device enters sleep mode. In sleep mode, the ADP1606/ADP1607 are mostly shut down, significantly reducing the quiescent current. The output voltage is discharged by the load until the output voltage reaches the lower sleep mode exit threshold. After crossing the lower sleep mode exit threshold, switching resumes and the process repeats.

### Mode Transition

The auto mode version of the ADP1607 and the auto mode of the ADP1606 switch automatically between PFM and PWM modes to maintain optimal efficiency. Switching to PFM allows the converter to save power by supplying the lighter load current with fewer switching cycles. The mode transition point depends on the operating conditions. See Figure 16 for typical transition levels for $V_{OUT}$ = 2.5 V. Hysteresis exists in the transition point to prevent instability and decreased efficiencies that may result if the converter oscillates between PFM and PWM for a fixed input voltage and load current.

The output voltage in PWM can be greater than or less than the PFM voltage of that device.

## INTERNAL CONTROL FEATURES

### Input to Output Isolation

While in shutdown, the ADP1606/ADP1607 manage the voltage of the bulk of the PMOS to force it off and internally isolate the path from the input to output. This isolation allows the output to drop to ground, reducing the current consumption of the application in shutdown.

### Soft Start

The ADP1606/ADP1607 soft start sequence is designed for optimal control of the device. When EN goes high, or when the device recovers from a TSD, the start-up sequence begins. The output voltage increases through a sequence of stages to ensure that the internal circuitry is powered up in the correct order as the output voltage rises to its final value.

### Current Limit

The ADP1606/ADP1607 are designed with a fixed 1 A typical current limit that does not vary with duty cycle.

### Synchronous Rectification

In addition to the N-channel MOSFET switch, the ADP1606/ADP1607 have a P-channel MOSFET switch to build the synchronous rectifier. The synchronous rectifier improves efficiency, especially for heavy load currents, and reduces cost and board space by eliminating the need for an external Schottky diode.

### Compensation

The PWM control loop of the ADP1606/ADP1607 is internally compensated to deliver maximum performance with no additional external components. The ADP1606/ADP1607 are designed to work with 2.2 µH chip inductors and 10 µF ceramic capacitors. Other values may reduce performance and/or stability.

### TSD Protection

The ADP1606/ADP1607 include TSD protection when the device is in PWM mode only. If the die temperature exceeds 150°C (typical), the TSD protection activates and turns off the power devices. They remain off until the die temperature falls below 135°C (typical), at which point the converter restarts.

# APPLICATIONS INFORMATION

## SETTING THE OUTPUT VOLTAGE

The ADP1606 is available with a 1.8 V fixed output voltage. The output voltage is set by an internal resistive feedback divider, and no external resistors are necessary.

The ADP1607 has an adjustable output voltage and can be configured for output voltages between 1.8 V and 3.3 V. The output voltage is set by a resistor voltage divider, R1, from the output voltage ($V_{OUT}$) to the 1.259 V feedback input at FB and R2 from FB to GND (see Figure 28). Resistances between 100 kΩ and 1 MΩ are recommended.

For larger R1 and R2 values, the voltage drop due to the FB pin current ($I_{FB}$) on R1 becomes proportionally significant and must be factored in.

To account for the effect of $I_{FB}$ for all values of R1 and R2, use the following equation to determine R1 and R2 for the desired $V_{OUT}$:

$$V_{OUT} = \left(1 + \frac{R1}{R2}\right)V_{FB} + I_{FB}(R1) \quad (1)$$

where:
$V_{FB}$ = 1.259 V, typical.
$I_{FB}$ = 0.1 µA, typical.

## INDUCTOR SELECTION

The ADP1606/ADP1607 are designed with a 2 MHz operating frequency, enabling the use of small chip inductors ideal for use in applications with limited solution size constraints. The ADP1606/ADP1607 are designed for optimal performance with 2.2 µH inductors, which have favorable saturation currents and lower series resistances for their given physical size.

To ensure stable and efficient performance with the ADP1606/ADP1607, take care to select a compatible inductor with a sufficient current rating, saturation current, and low dc resistance (DCR.)

The maximum rated rms current of the inductor must be greater than the maximum input current to the regulator. Likewise, the saturation current of the chosen inductor must be able to support the peak inductor current (the maximum input current plus half the inductor ripple current) of the application.

The inductor ripple current ($\Delta I_L$) in steady state continuous mode can be calculated with Equation 2.

$$\Delta I_L = \frac{V_{IN} \times D}{L \times f_{SW}} \quad (2)$$

where:
$D$ is the duty cycle of the application.
$L$ is the inductor value.
$f_{SW}$ is the switching frequency of the ADP1606/ADP1607.

The duty cycle (D) can be determined with Equation 3.

$$D = \frac{V_{OUT} - V_{IN}}{V_{OUT}} \quad (3)$$

Inductors with a low DCR minimize power loss and improve efficiency. DCR values below 100 mΩ are recommended.

**Table 7. Suggested Inductors**

| Manufacturer | Part Number | Inductance (µH) | DCR (mΩ) Typ | Current Rating (A) | Saturation Current (A) | Size (L × W × H) (mm) | Package |
|---|---|---|---|---|---|---|---|
| TDK | MLP2016S2R2M | 2.2 ± 20% | 110 | 1.20 | | 2.00 × 1.60 × 1.00 | 0806 |
| | MLP2520S2R2S | 2.2 ± 20% | 110 | 1.20 | 1.20 | 2.50 × 2.00 × 1.00 | 1008 |
| | VLF252012MT-2R2M | 2.2 ± 20% | 57 | 1.67 | 1.04 | 2.50 × 2.00 × 1.00 | 1008 |
| | VLF302510MT-2R2M | 2.2 ± 20% | 70 | 1.23 | 1.37 | 3.00 × 2.50 × 1.00 | |
| | VLF302515MT-2R2M | 2.2 ± 20% | 42 | 2.71 | 1.57 | 3.00 × 2.50 × 1.40 | |
| Murata | LQM2HPN2R2MG0 | 2.2 ± 20% | 80 | 1.30 | | 2.50 × 2.00 × 0.90 | 1008 |
| | LQH32PN2R2NNC | 2.2 ± 30% | 64 | 1.85 | | 3.20 × 2.50 × 1.55 | 1210 |
| Wurth | 74479787222 | 2.2 ± 20% | 80 | 1.50 | 0.70 | 2.50 × 2.00 × 1.00 | 1008 |
| | 7440430022 | 2.2 ± 30% | 23 | 2.50 | 2.35 | 4.80 × 48.0 × 2.80 | |
| Taiyo Yuden | BRC2012T2R2MD | 2.2 ± 20% | 110 | 1.00 | 1.10 | 2.00 × 1.25 × 1.40 | 0805 |
| Toko | MDT2520-CR2R2M | 2.2 ± 20% | 90 | 1.35 | | 2.50 × 2.00 × 1.00 | 1008 |
| | DEM2810C (1224AS-H-2R2M) | 2.2 ± 20% | 85 | 1.10 | 1.40 | 3.20 × 3.00 × 1.00 | |
| | DEM2815C (1226AS-H-2R2M) | 2.2 ± 20% | 43 | 1.40 | 2.20 | 3.20 × 3.00 × 1.50 | |
| Coilcraft | XFL3012-222 | 2.2 ± 20% | 81 | 1.9 | 1.6 | 3.00 × 3.00 × 1.20 | 1212 |
| | XFL4020-222 | 2.2 ± 10% | 21 | 8.0 | 3.1 | 4.00 × 4.00 × 2.10 | 1515 |

## CHOOSING THE INPUT CAPACITOR

The ADP1606/ADP1607 require a 10 µF or greater input bypass capacitor ($C_{IN}$) between VIN and GND to supply transient currents while maintaining a constant input voltage. The value of the input capacitor can be increased without any limit for smaller input voltage ripple and improved input voltage filtering. The capacitor must have a 4 V or higher voltage rating to support the maximum input operating voltage. It is recommended that $C_{IN}$ be placed as close to the ADP1606/ADP1607 as possible.

Different types of capacitors can be considered, but for battery-powered applications, the best choice is the multilayer ceramic capacitor, due to its small size, low equivalent series resistance (ESR), and low equivalent series inductance (ESL). X5R or X7R dielectrics are recommended. Do not use Y5V capacitors due to their variation in capacitance over temperature. Alternatively, use a high value, medium ESR capacitor in parallel with a 0.1 µF low ESR capacitor.

## CHOOSING THE OUTPUT CAPACITOR

The ADP1606/ADP1607 require a 10 µF output capacitor ($C_{OUT}$) to maintain the output voltage and supply current to the load. The output capacitor supplies the current to the load when the N-channel switch is on. Similar to $C_{IN}$, a 4 V or greater, low ESR, X5R or X7R ceramic capacitor is recommended for $C_{OUT}$. When choosing the output capacitor, it is also important to account for the loss of capacitance due to output voltage dc bias. The loss of capacitance due to output voltage dc bias may necessitate the use of a capacitor with a higher rated voltage to achieve the desired capacitance value. See Figure 29 for an example of how the capacitance of a 10 µF ceramic capacitor changes with the dc bias voltage.

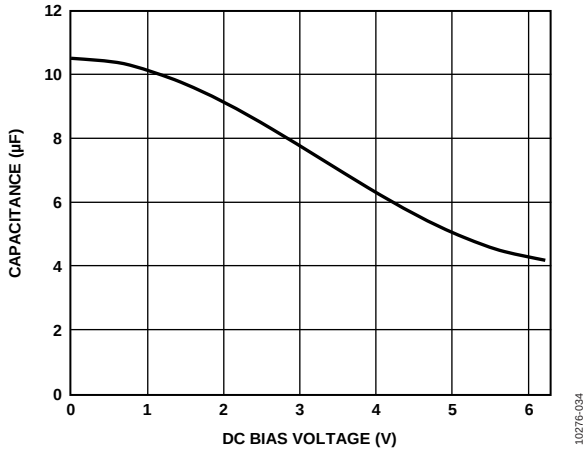



*Figure 29. Typical Ceramic Capacitor Performance*

The value and characteristics of the output capacitor greatly affect the output voltage ripple, transient performance, and stability of the regulator. The output voltage ripple ($\Delta V_{OUT}$) in continuous operation is calculated as follows:

$$\Delta V_{OUT} = \frac{Q_C}{C_{OUT}} = \frac{I_{OUT} \times t_{ON}}{C_{OUT}} \quad (4)$$

where:
$Q_C$ is the charge removed from the capacitor.
$I_{OUT}$ is the output load current.
$t_{ON}$ is the on time of the N-channel switch.
$C_{OUT}$ is the effective output capacitance.

$$t_{ON} = \frac{D}{f_{SW}} \quad (5)$$

and,

$$D = \frac{V_{OUT} - V_{IN}}{V_{OUT}} \quad (6)$$

As shown in the duty cycle and output ripple voltage equations, the output voltage ripple increases with the load current.

# LAYOUT GUIDELINES

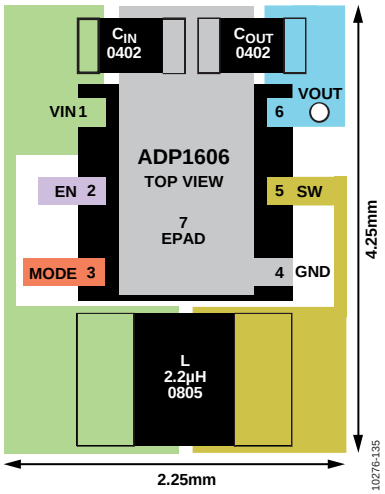



*Figure 30. ADP1606 Recommended Layout Showing the Smallest Footprint*

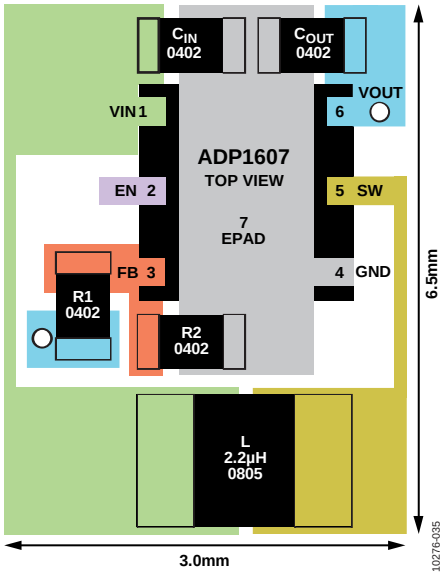



*Figure 31. ADP1607 Recommended Layout Showing the Smallest Footprint*

For high efficiency, good regulation, and stability, a well designed PCB layout is required.

Use the following guidelines when designing a PCB. See Figure 28 for a block diagram, and Figure 3 and Figure 4 for pin configurations.

- Keep the low ESR input capacitor, $C_{IN}$, close to VIN and GND. This minimizes noise injected into the device from board parasitic inductance.
- Keep the high current path from $C_{IN}$ through the L inductor to SW as short as possible.
- For ADP1607, place the feedback resistors, R1 and R2, as close to FB as possible to prevent noise pickup. Connect the ground of the feedback network directly to an AGND plane that makes a Kelvin connection to the GND pin. See Figure 31 for more information.
- Avoid routing high impedance traces from feedback resistors near any node connected to SW or near the inductor to prevent radiated noise injection.
- Keep the low ESR output capacitor, $C_{OUT}$, close to VOUT and GND. This minimizes noise injected into the device from board parasitic inductance.
- Connect Pin 7 (EPAD) and GND to a large copper plane for proper heat dissipation.

# OUTLINE DIMENSIONS

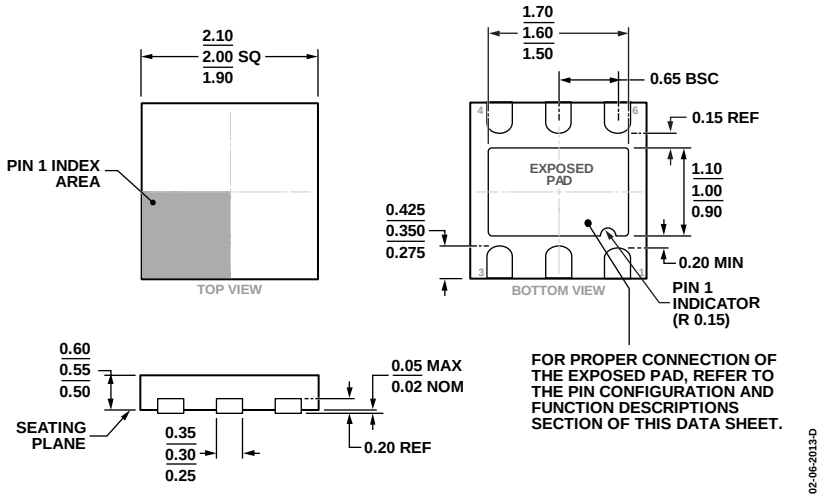



*Figure 32. 6-Lead Lead Frame Chip Scale Package [LFCSP_UD]*
*2.00 mm × 2.00 mm Body, Ultra Thin, Dual Lead*
*(CP-6-3)*
*Dimensions Shown in Millimeters*

## ORDERING GUIDE

| Model[1] | Output Voltage | Operating Modes | Temperature Range | Package Description | Package Option | Branding |
|---|---|---|---|---|---|---|
| ADP1606ACPZN1.8-R7 | 1.8 V | MODE Pin | −40°C to +85°C | 6-Lead LFCSP_UD | CP-6-3 | LM8 |
| ADP1606-1.8-EVALZ | 1.8 V | MODE Pin | −40°C to +85°C | Evaluation Board, $V_{OUT}$ = 1.8 V | | |
| ADP1607ACPZN-R7 | Adjustable | Auto | −40°C to +85°C | 6-Lead LFCSP_UD | CP-6-3 | LJ5 |
| ADP1607ACPZN001-R7 | Adjustable | PWM | −40°C to +85°C | 6-Lead LFCSP_UD | CP-6-3 | LJ1 |
| ADP1607-EVALZ | | Auto | | Evaluation Board, Automatic PFM/PWM Switching Modes | | |
| ADP1607-001-EVALZ | | PWM | | Evaluation Board, PWM Mode Only | | |

[1] Z = RoHS Compliant Part.

## NOTES

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