

ADS5231/32/37 EVM

User's Guide

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ADS5231/32/37 EVM

This preliminary user's guide gives a general overview of the ADS5231/32/37 evaluation module (EVM), and provides a general description of the features and functions to be considered while using this module.

1 Overview

1.1 Purpose

The ADS5231/32/37 EVM provides a platform for evaluating the ADS5231/32/37 dual, 12-bit, analog-to-digital converter (ADC) under various signal, reference, and supply conditions. This document should be used in combination with the EVM schematic diagram supplied.

1.2 EVM Basic Functions

Analog inputs to the ADC are provided via external SMA connectors. The single-ended input the user provides is converted into a differential signal at the input of the device for both channels. Both analog input channels of the ADS5231/32/37 EVM have two independent paths. One input path uses a differential amplifier, while the other path is transformer-coupled.

The EVM provides an external SMA connector for input of the ADC clock. The single-ended input that the user provides is transformer-coupled to provide a differential signal at both clock inputs of the device. The EVM also allows the user to send a single-ended or true-differential clock if desired.

Digital outputs from the EVM are via two 40-pin connectors. The digital outputs from the ADC are buffered before going to the connectors. The digital output connectors can be mated to TI's TSW1100 for digital capture.

Power connections to the EVM are via banana jack sockets. Separate sockets are provided for the ADC analog and output driver supplies, external buffers supply, and differential amplifiers supply.

1.3 Power Requirements

The EVM can be powered directly with only a single 3.3-V supply if using the module with transformer-coupled input and internal reference mode. ± 5 V is required if using the differential amplifier input. A provision has been made to allow the EVM to be powered with independent analog and digital supplies to provide higher performance.

Voltage Limits

Exceeding the maximum input voltages can damage EVM components. Undervoltage may cause improper operation of some or all of the EVM components.

1.4 ADS5231/32/37 EVM Operational Procedure

The ADS5231/32/37 EVM provides a flexible means of evaluating the ADS5231/32/37 in a number of modes of operation. A basic setup procedure that can be used as a board confidence check is as follows:

1. Verify all jumper settings against the schematic jumper list in [Table 1](#):
2. Connect supplies to the EVM as follows:
 - 3.3-V ADC output buffer supply to J17 and return to J18.
 - 3.3-V ADC analog supply to J11 and return to J10.
3. Switch power supplies on
4. Use a function generator with 50-Ω output to input a 45-MHz, 1.5-V offset, 3-V square-wave signal into J3. The frequency of the clock must be within the specification for the device speed grade. **Caution: the ADS5231/32/37 does not work with a sinusoidal clock source.**
5. Use frequency generators with a 50-Ω output to provide a 10.1-MHz, 0-V offset, –1-dBFS amplitude, sine-wave signal into J15 and J16. This provides a transformer-coupled differential input signal to both channels of the ADC. A full-scale input tone into channel A or channel B can be calculated by using the following formula:

$$- \text{dBFS} = 20 \log \left(\frac{\text{captured max code} - \text{captured min code}}{2^N} \right), N \text{ is the number of bits}$$

6. The digital patterns on output connectors J8 and J21 should now represent a sine wave and can be monitored using a logic analyzer or TSW1100.

Table 1. Three-Pin Jumper List

Jumper	Function	Location: Pins 1- 2	Location: Pins 2-3	Default
W1	Reference select	Internal reference	External reference	1-2
W2	Channel B output enable	Output disabled	Output enabled	2-3
W3	Power down select	Power-down mode	Operate mode	2-3
W4	Channel A output enable	Output disabled	Output enabled	2-3
SJP1	Common-mode voltage-path provider	Common-mode voltage to CHA differential amplifier	Provide common-mode voltage to transformer T1	2-3
W9	Invert most significant bit	2s complement	Offset binary	2-3
SJP3	Common-mode voltage path	Provide common-mode voltage to CHB differential amplifier	Provide common-mode voltage to transformer T2	2-3

2 Circuit Description

2.1 Schematic Diagram

The schematic diagram for the EVM is attached to the end of this document.

2.2 Circuit Function

The following paragraphs describe the function of individual circuits. See the *ADS5232 Dual, 12-Bit, 65MSPS, +3.3V Analog-to-Digital Converter* data sheet ([SBAS294](#)), the *ADS5231 Dual, 12-Bit, 40MSPS, +3.3V Analog-to-Digital Converter* data sheet ([SBAS295](#)), or the *ADS5237 Dual, 10-Bit, 65MSPS, +3.3V Analog-to-Digital Converter* data sheet ([SBAS420](#)) for device operating characteristics.

2.2.1 Analog Inputs

The EVM can be configured to provide the ADC with either transformer-coupled or differential amplifier inputs from a single-ended source. The inputs are provided via SMA connectors J15 and J16 for transformer-coupled input, and J1, J2, J7, and J9 for differential amplifier input. To set up for one of these options, the EVM must be configured as follows:

1. For a 1:1 transformer-coupled input to the ADC, a single-ended source is connected to J15 for channel A and J16 for channel B. R5, R6, R8, and R9 must not be installed. This is the default configuration for the EVM.
2. For single-ended inputs into the differential amplifiers, sources are connected to J2 for channel A and J9 for channel B. R5, R6, R8, and R9 must be installed, and R74, R75, R78, and R79 removed.
3. For a differential input into the amplifiers, the positive source of channel A is connected to J2 and the negative source to J1. The positive source of channel B is connected to J9 and the negative source to J7. R5, R6, R8, and R9 must be installed, and R74, R75, R78, and R79 removed. R19 and R22 must be replaced with 383- Ω resistors, and R12 and R14 must be replaced with 54.9- Ω resistors for proper termination.

2.2.2 Clock Input

To provide a clock to the ADS5231/32/37, apply a 3.3-V, 1.65-V offset, square-wave input to J3. This input is terminated with a 50- Ω resistor to ground. **Caution: the ADS5231/32/37 does not work with a sinusoidal clock source.**

2.2.3 Control Inputs

The EVM has five discrete inputs to control the operation of the device.

2.2.3.1 Output Enable

With jumper W4 installed between pins 2 and 3, channel A of the ADC is enabled. This channel is disabled with the jumper installed between pins 1 and 2. With jumper W2 installed between pins 2 and 3, channel B is enabled. Channel B is disabled with the jumper installed between pins 1 and 2.

2.2.3.2 MSB Control

With jumper W9 installed between pins 2 and 3, the outputs of the ADC are straight binary. The outputs are 2s complement with jumper W9 installed between pins 1 and 2.

2.2.3.3 Power Down

With jumper W3 installed between pins 1 and 2, the ADC is in power-down mode.

2.2.3.4 External Reference

With jumper W1 installed between pins 1 and 2, the ADC is in internal reference mode. The device is in external reference mode with jumper W1 installed between pins 2 and 3. When using the external reference mode, install R3 and R4. Use the potentiometers R17 and R18 to adjust the corresponding top reference and bottom reference. For convenience, two test points, TP6 and TP7, allow monitoring the voltage while using the external reference mode.

2.2.4 Power

Power is supplied to the EVM via banana jack sockets. Separate connections are provided for a 3.3-V analog supply (J11 and J10), 3.3-V driver supply, external buffer supply (J17 and J18), and ± 5 -V amplifier supply (J14, J13, and J12).

2.2.5 Outputs

The data outputs from the ADC are buffered using two Texas Instruments SN74AVC16244s. Output data headers J8 and J21 are standard 40-pin headers on a 100-mil grid, and allow easy connection to a logic analyzer or TSW1100. The connector pinout is listed in [Table 2](#). Furthermore, five test points are provided. They are listed in [Table 3](#).

Table 2. Output Connectors J8 and J21

PIN NO.	DESCRIPTION		PIN NO.	DESCRIPTION	
	ADS5231/ADS5232	ADS5237		ADS5231/ADS5232	ADS5237
1	CLK OUT	CLK OUT	2	GND	GND
3	NC	NC	4	GND	GND
5	NC	NC	6	GND	GND
7	NC	NC	8	GND	GND
9	D11 (MSB)	D9 (MSB)	10	GND	GND
11	D10	D8	12	GND	GND
13	D9	D7	14	GND	GND
15	D8	D6	16	GND	GND
17	D7	D5	18	GND	GND
19	D6	D4	20	GND	GND
21	D5	D3	22	GND	GND
23	D4	D2	24	GND	GND
25	D3	D1	26	GND	GND
27	D2	D0 (LSB)	28	GND	GND
29	D1	NC	30	GND	GND
31	D0 (LSB)	NC	32	GND	GND
33	NC	NC	34	GND	GND
35	NC	NC	36	GND	GND
37	NC	NC	38	GND	GND
39	NC	NC	40	GND	GND

Table 3. Test Point Descriptions

Test Point	Function
TP1	GND
TP3	GND
TP4	GND
TP6	Bottom reference voltage when forcing external voltage (typical = 1 V)
TP7	Bottom reference voltage when forcing external voltage (typical = 2 V)

3 EVM Use With the TSW1100

The ADS5231/32/37 EVM allows for connection to the TSW1100, allowing easy capture and analysis of the ADC digital output data. See the *TSW1100 Data Capture Board Quick Start Guide* ([SLAU155](#)) and *TSW1100 User's Guide* ([SLAU164](#)) for more information.

3.1 Connecting to the TSW1100

Gently insert the ADS5231/32/37 EVM output connectors J8 and J21 into the TSW1100 input connectors J2 and J1, respectively.

3.2 Provide Power to the ADS5231/32/37 EVM

Follow the steps in [Section 1.4](#) and power on the ADS5231/32/37 EVM.

3.3 Providing Power to the TSW1100

Use either a wall-mount transformer that has an output rating of 12 VDC and 500 mA or a lab power supply that can supply 12 VDC. Connect the output to J8 and the return to J9. Texas Instruments recommends setting a current limit of 500 mA. Power on the TSW1100.

3.4 Connecting to the USB

With the PC turned on, connect the USB cable from the PC to the TSW1100 USB connector, J10. At this point, the PC should recognize the TSW1100. To verify, go to the Hardware Device Manager, select USB Device, and ensure the TSW1100 is listed as a USB device. At this point, LED D13 lights on the TSW1100, signaling that the device has been configured properly and is communicating with the PC. This should be the only lighted LED. If at this point more than D13 is lighted, depress the reset switch, SW2, on the TSW1100.

3.5 Launching the TSW1100 Software

With the TSW1100 recognized by the hardware device manager, the software package can be run. To run the program, click on Start → Program Files → Texas Instruments → TI ADC Capture Card.

3.6 Using the TSW1100 Software

Using the TI chip selector, select the ADS5231/32/37. The software then configures itself for operation with the ADS5231/32/37 EVM. Fill in the appropriate fields describing the hardware setup conditions. When finished, acquire data by clicking on the red circular Acquire Data button.

4 Physical Description

This chapter describes the physical characteristics of the PCB, providing the layout of each board layer.

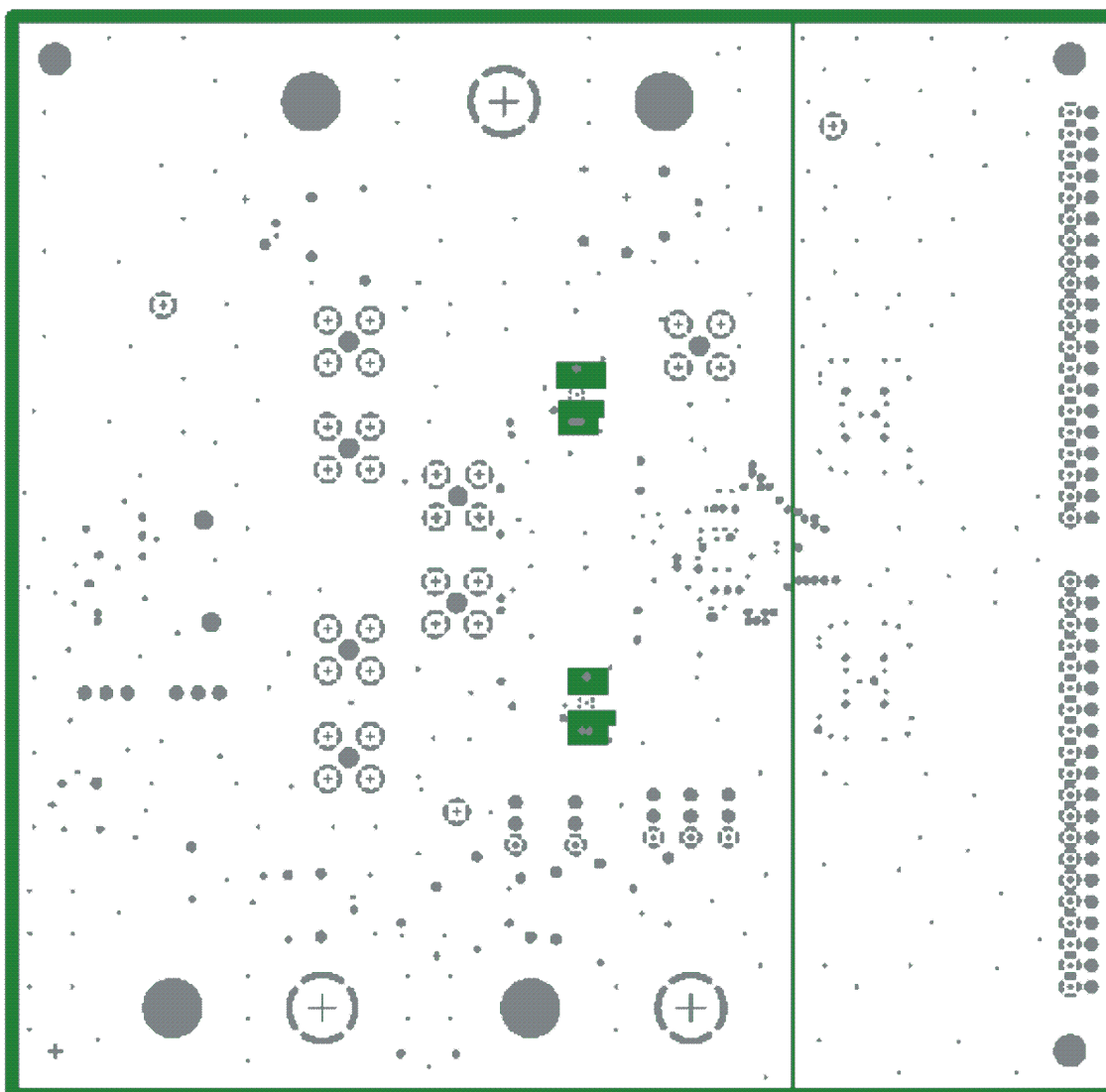


Figure 2. Layer 2, Ground Plane

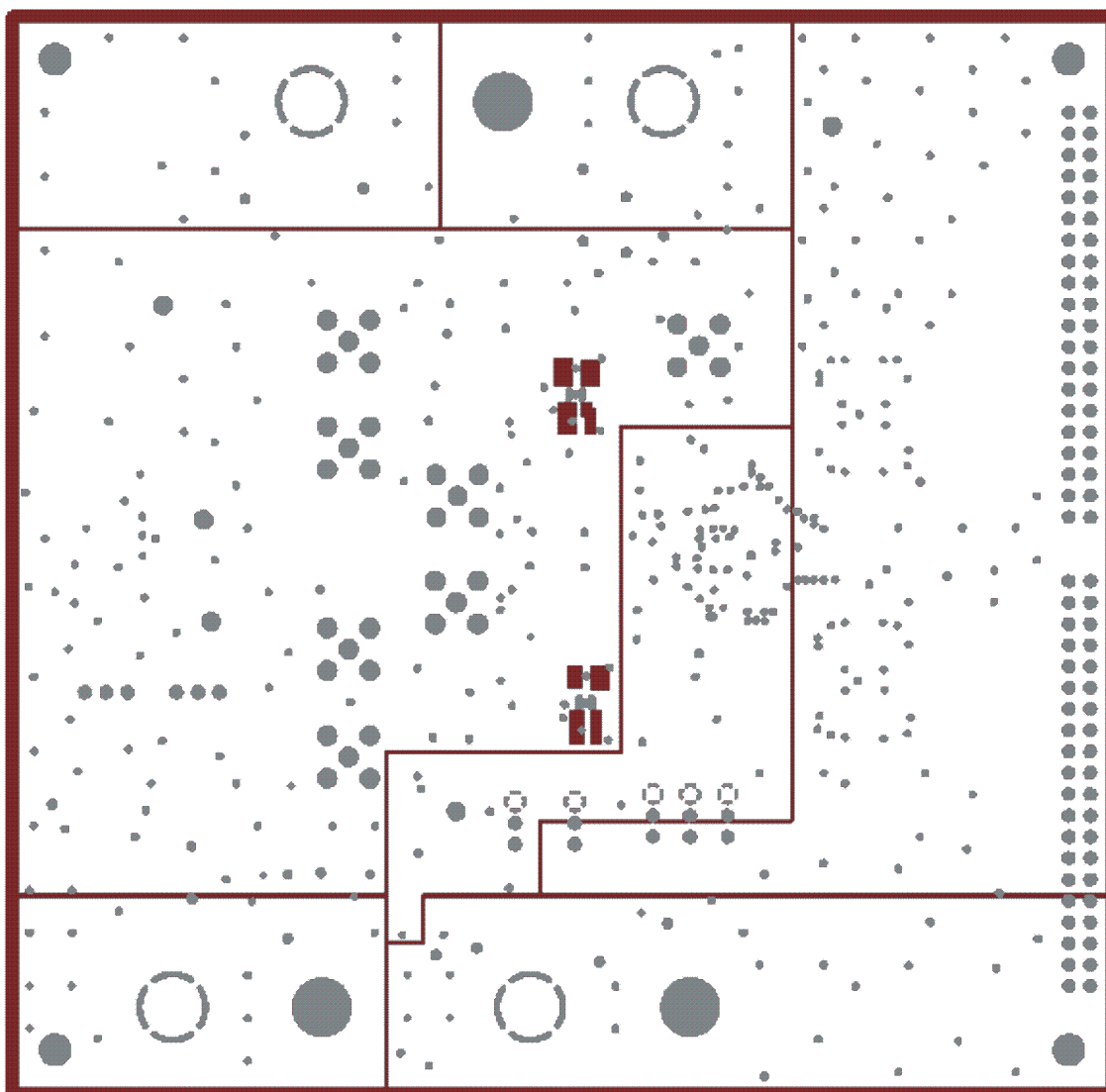


Figure 3. Layer 3, Power Plane #1

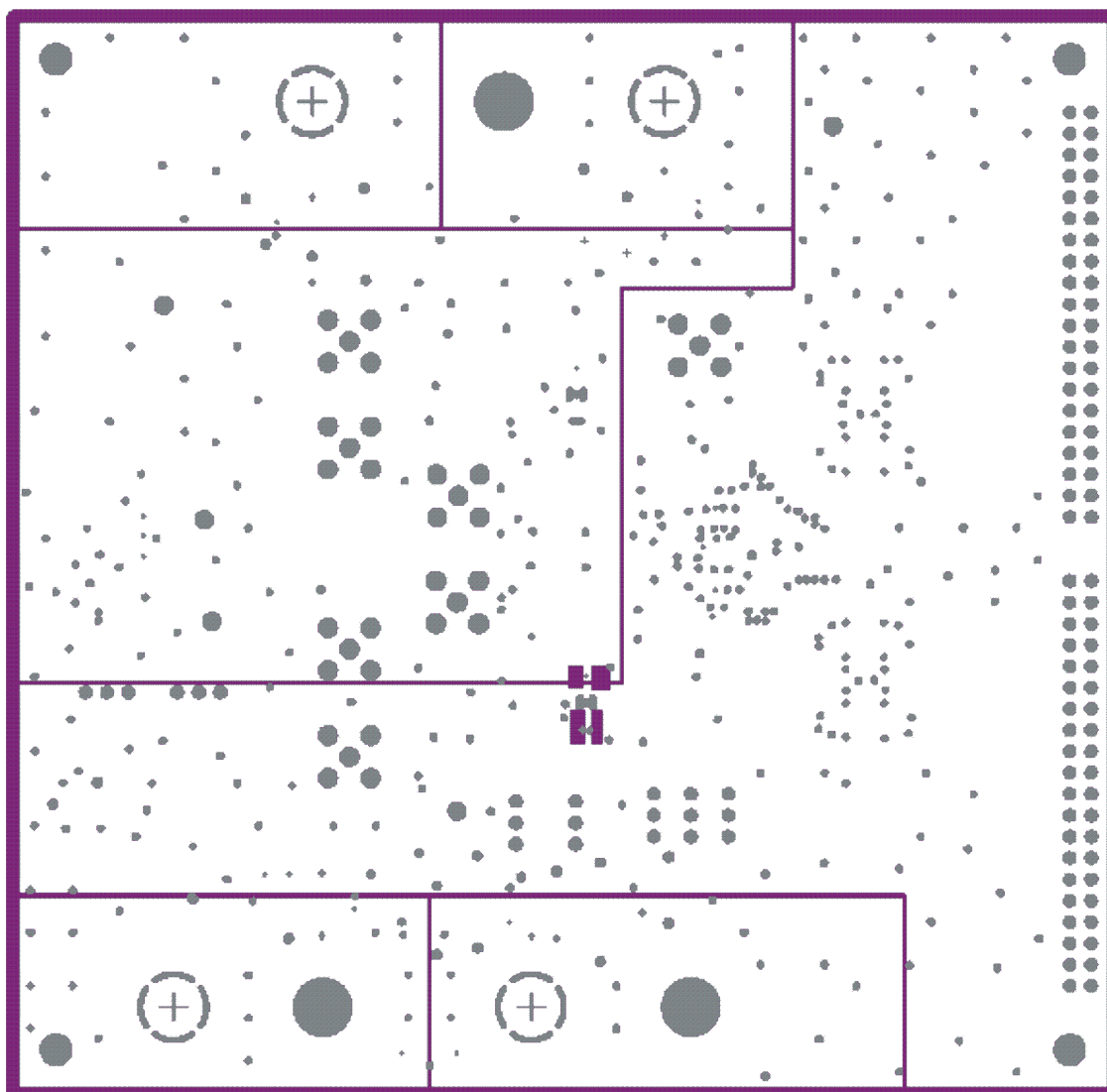


Figure 4. Layer 4, Power Plane #2

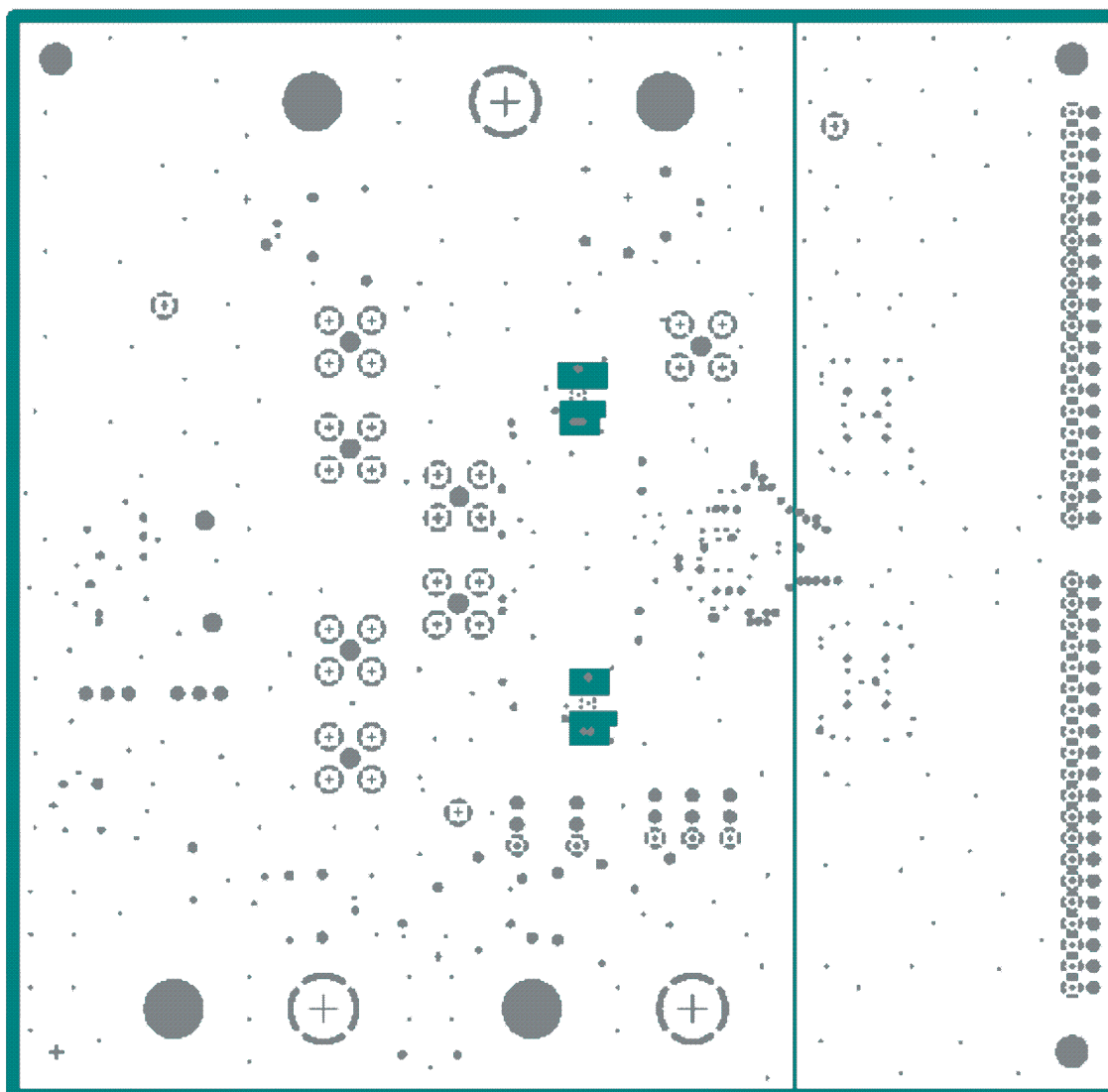


Figure 5. Layer 5, Ground Plane

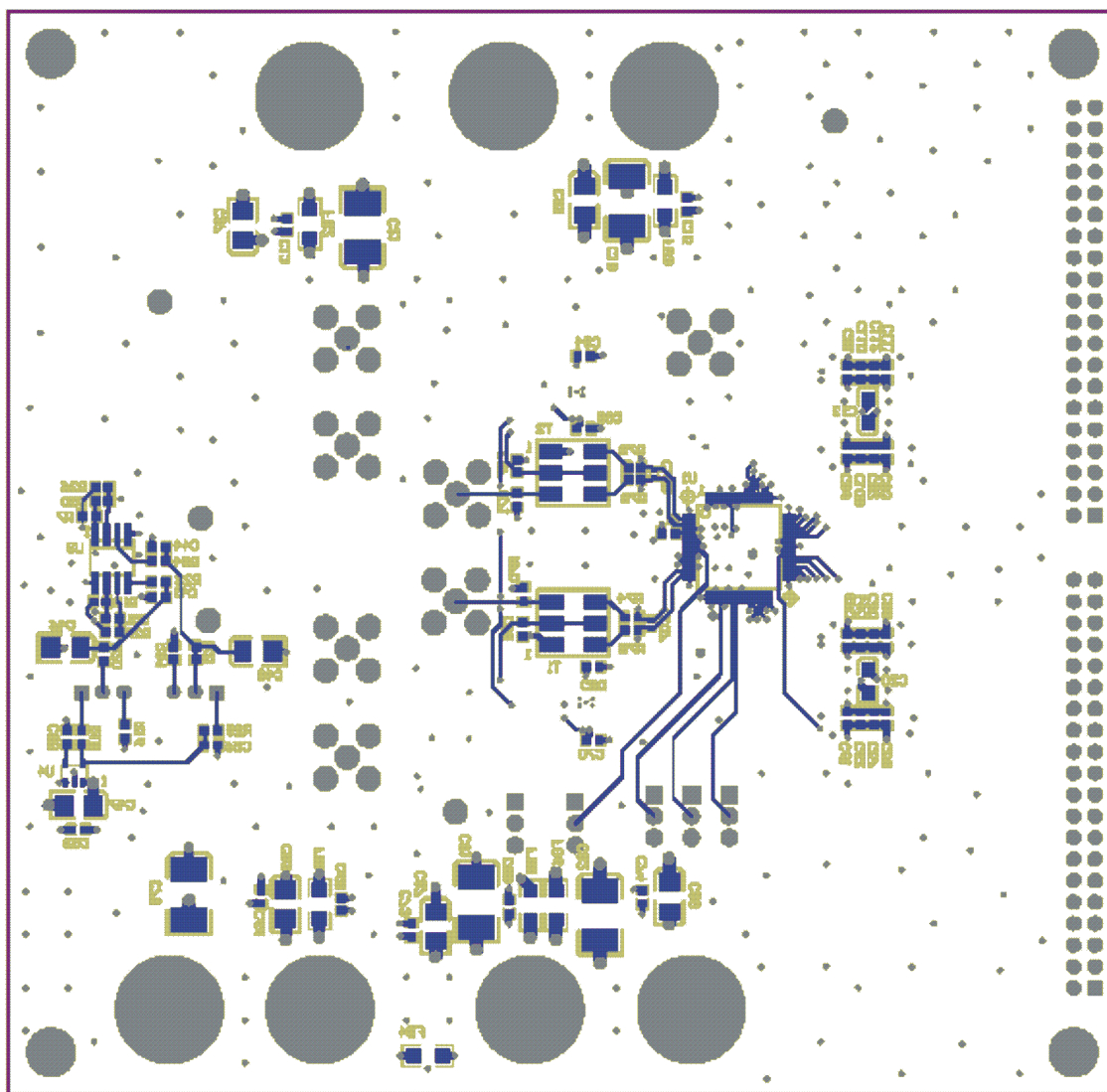


Figure 6. Layer 6, Bottom Layer

5 Parts List and Schematics

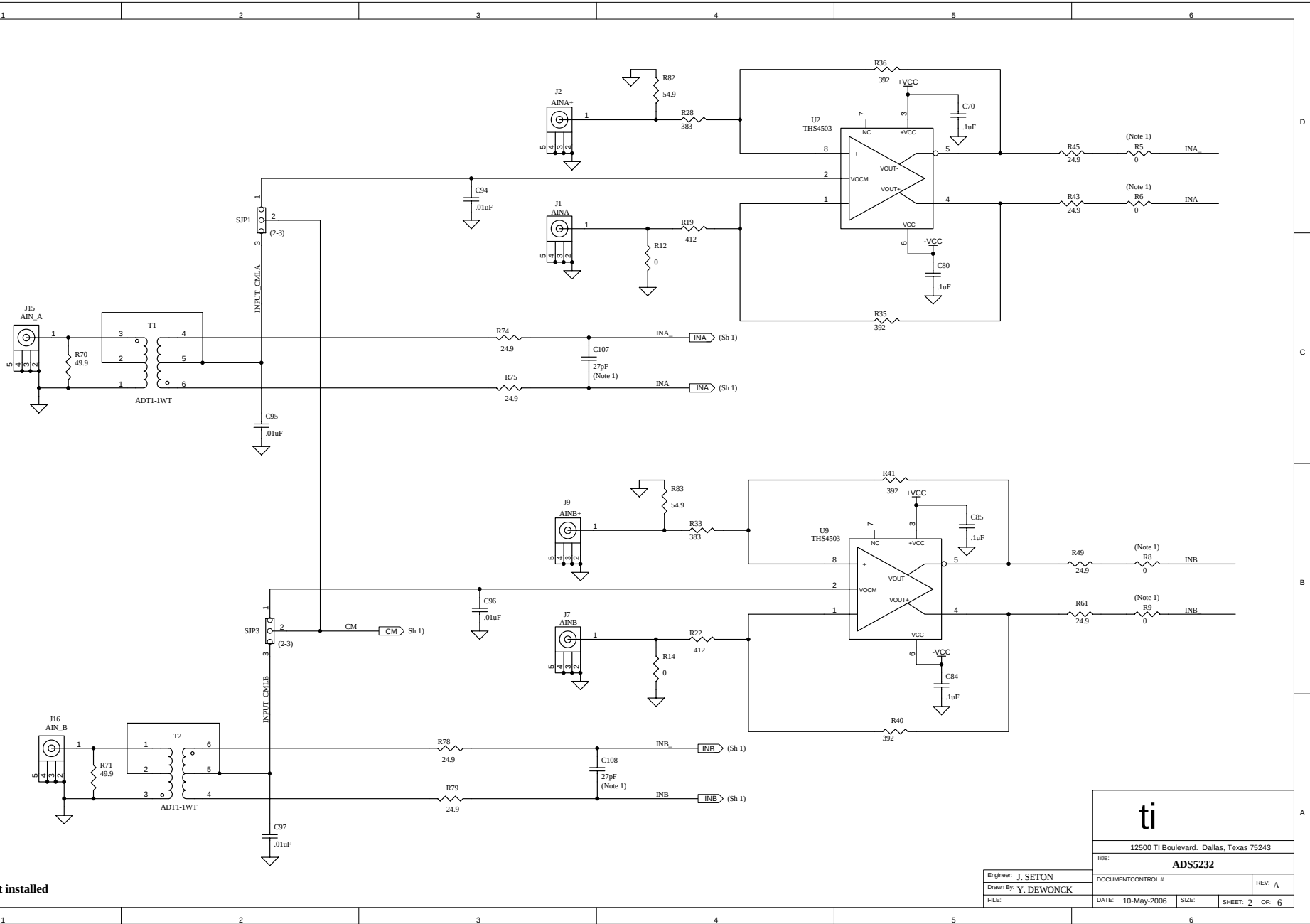
Table 4 lists the parts used in constructing the EVM. The EVM schematics are appended at the end of this section.

Table 4. ADS5231/32/37 EVM Parts List

Value	QTY	Part Number	Vendor	Ref Des	Not Installed
CAPACITORS					
47- μ F, tantalum, 20%, 10-V capacitor	5	ECS-T1AD476R	Panasonic	C19 C21 C75 C81 C82	
10- μ F, 10-V, 20% capacitor	8	ECS-T1AX106R	Panasonic	C23 C27 C46 C47 C48 C83 C87 C88	
10- μ F, 10-V, 10% capacitor	4	T491A106K010AS	KEMET	C12 C20 C22 C26	
0.47-pF, 100-V, 10% capacitor	10	ECJ-1VB2A471K	Panasonic	C33 C34 C57 C59 C61 C63 C109 C110 C111 C112	
0.047- μ F, 16-V, 10% capacitor	2	ECJ-1VB1H473K	Panasonic	C50 C51	
0.01- μ F, 50-V, 10% capacitor	5	ECJ-1VB1C103K	Panasonic	C55 C94 C95 C96 C97	
0.1- μ F, 16-V, 10% capacitor	25	ECJ-1VB1C104K	Panasonic	C8 C10 C13 C15 C41 C42 C43 C44 C58 C60 C62 C64 C65 C66 C70 C73 C74 C80 C84 C85 C86 C89 C90 C91 C92 C93	C7
1- μ F, 6.3-V, 10% capacitor	1	ECJ-1VB0J105K	Panasonic	C53	
2.2- μ F, 6.3-V, 10% capacitor	1	ECJ-1VF0J225Z	Panasonic	C56	
0.1- μ F, 16-V, 10% capacitor	7	ECJ-0EF1C104Z	Panasonic	C2–C6 C9 C28	
27-pF, 50-V, 5% capacitor	0	ECU-E1H270JCQ	Panasonic	C107 C108	
RESISTORS					
0- Ω resistor, 1/16-W, 1%	2	ERJ-6ENF0R00V	Panasonic	R12 R14	
54.9- Ω resistor, 1/16-W, 1%	2	ERJ-6ENF54R9V	Panasonic	R82 R83	
383- Ω resistor, 1/16-W, 1%	2	ERJ-6ENF3830V	Panasonic	R28 R33	
392- Ω resistor, 1/16-W, 1%	4	ERJ-6ENF3920V	Panasonic	R35 R36 R40 R41	
412 Ω resistor, 1/16 W, 1%	2	ERJ-6ENF4120V	Panasonic	R19 R22	
0- Ω resistor, 1/16-W, 1%	3	ERJ-3GEY0R00V	Panasonic	C1 R42 R102	R3 R4 R5 R6 R8 R9
100- Ω resistor, 1/16-W, 1%	6	ERJ-3EKF1000V	Panasonic	R23 R24 R74 R75 R78 R79	
24.9- Ω resistor, 1/16-W, 1%	4	ERJ-3EKF24R9V	Panasonic	R43 R45 R49 R61	
49.9- Ω resistor, 1/16-W, 1%	5	ERJ-3EKF49R9V	Panasonic	R2 R7 R13 R70 R71	
2-k Ω resistor, 1/16-W, 1%	4	ERJ-3EKF2001V	Panasonic	R15 R26 R27 R29	
56.2-k Ω resistor, 1/16-W, 1%	1	ERJ-3EKF5622V	Panasonic	R1	
4.99-k Ω resistor, 1/16-W, 1%	2	ERJ-3EKF4991V	Panasonic	R16 R34	
10-k Ω resistor, 1/16-W, 1%	2	ERJ-3EKF1002V	Panasonic	R20 R21	
1-k Ω variable resistor	2	CT94W102	CERMET	R17 R18	
0- Ω R-pack, EXB-38V series	6	EXB-38V000JV	Panasonic	RP1–RP6	
CONNECTORS, JUMPER, HEADERS, FERRITE BEADS, TRANSFORMERS, IC's					
Ferrite bead	8	EXC-ML32A680U		FB1 FB2 FB3 FB5-FB9	FB4
Transformer	2	ADT4-1WT	Mini-Circuits	T1 T2	
SMA connectors	7	2262-0000-09	Newark	J1 J2 J3 J7 J9 J15 J16	
Black test point	3	5011K-ND	Keystone	TP1 TP3 TP4	
Red test point	2	5010K-ND	Keystone	TP6 TP7	
3POS_header	5	TSW-150-07-L-S	Samtec	W1 W2 W3 W4 W9	
40-pin IDC connector	2	TSW-120-07-L-D	Samtec	J8 J21	
Red banana jacks	4	ST-351A	Allied	J11 J13 J14 J17	
Black banana jacks	3	ST351B	Allied	J10 J12 J18	

Table 4. ADS5231/32/37 EVM Parts List (continued)

Value	QTY	Part Number	Vendor	Ref Des	Not Installed
ADS5231, ADS5232, or ADS5237	1	ADS5231, ADS5232, or ADS5237	TI	U1	
THS4503	2	THS4503ID	TI	U2 U9	
OPA2227UA	1	OPA2227UA	TI	U3	
TPS79225	1	TPS79225	TI	U4	
SN74AVC16244	2	SN74AVC16244DGG	TI	U7 U10	
Screw, machine, PH 4-40 × 3/8	4	PMS 440 0038 PH	Building Fasteners		
Standoff, hex .5/4-40THR, nylon	4	1902C	Keystone Electronic		



Note 1. Part not installed

ti

12500 TI Boulevard, Dallas, Texas 75243

Title: AD55232

DOCUMENT CONTROL #

REV: A

Engineer: J. SETON

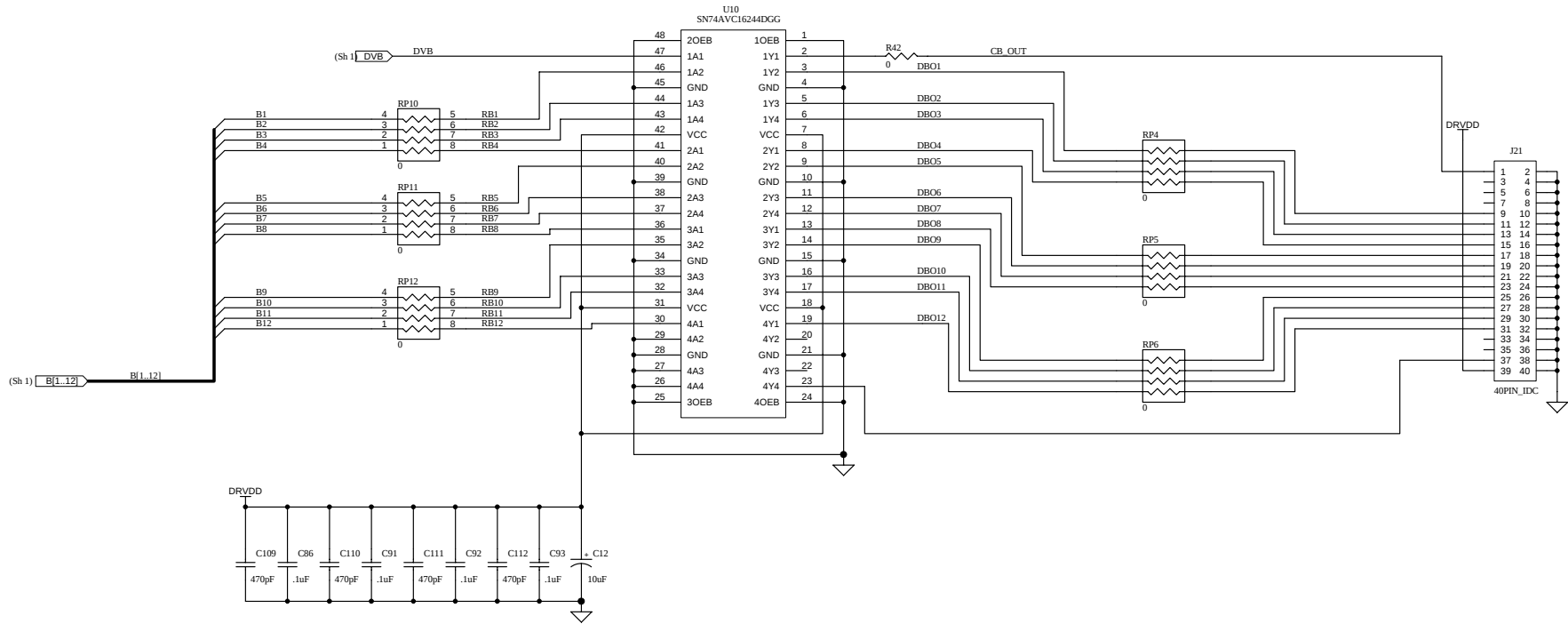
Drawn By: Y. DEWONCK

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DATE: 10-May-2006

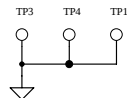
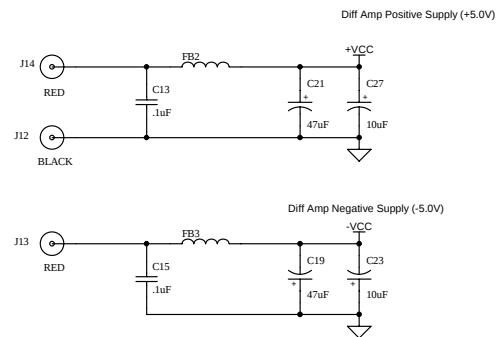
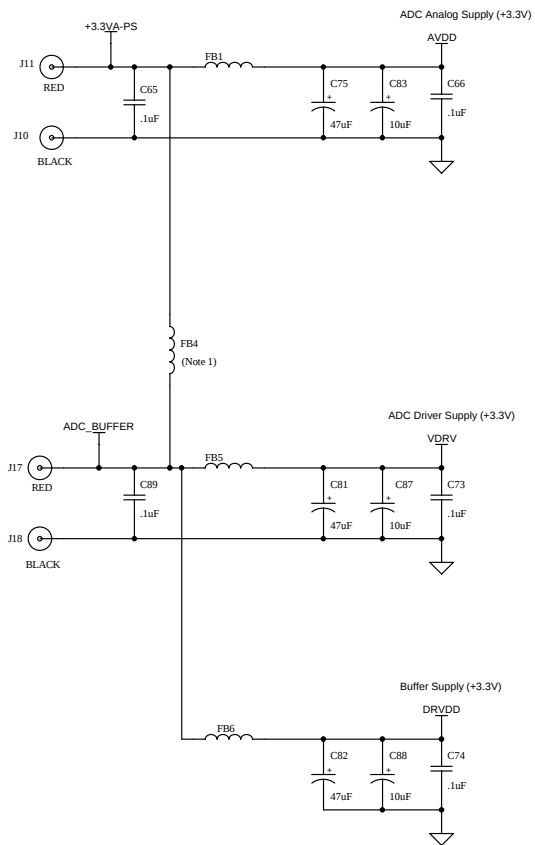
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Note 1. Part not installed

ti 12500 TI Boulevard, Dallas, Texas 75243			
Title: ADS5232		REV: A	
Engineer: J. SETON		DOCUMENT CONTROL #	
Drawn By: Y. DEWONCK		DATE: 10-May-2006	
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Note 1. Part not installed

ti

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Title: ADS5232

Engineer: J. SETON

Drawn By: Y. DEWONCK

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the AVDD voltage range of -0.3 V to 3.8 V and the DVDD voltage range of -0.3 V to 3.8 V .

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 25°C . The EVM is designed to operate properly with certain components above 50°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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