

AFIC901N 136-174 MHz REFERENCE CIRCUIT OVERVIEW

ORDERABLE PART NUMBER: AFIC901N-135MHZ



PUBLIC



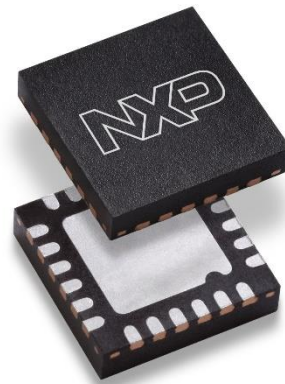
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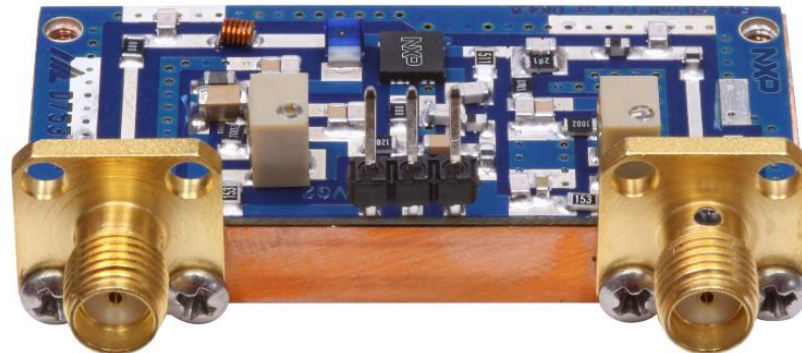
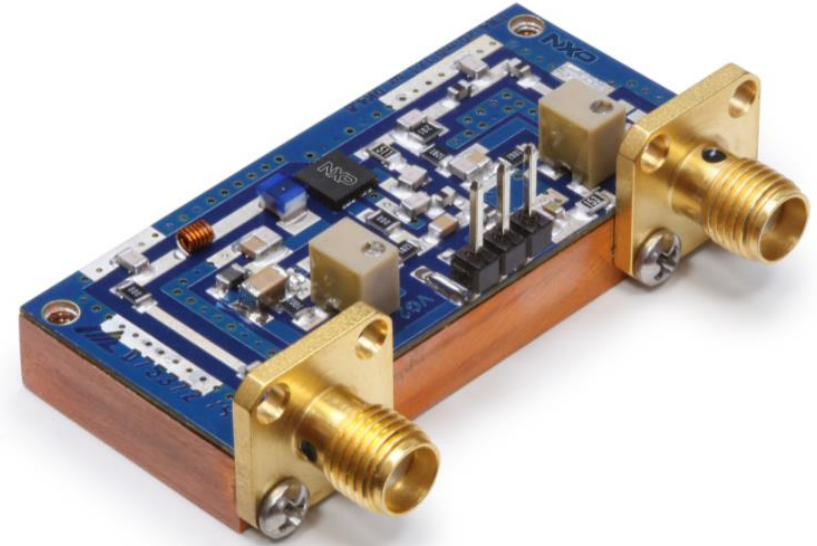
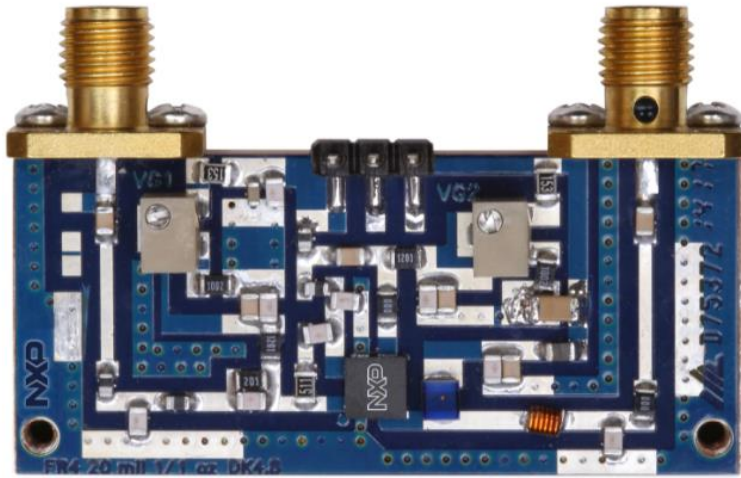
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Introduction

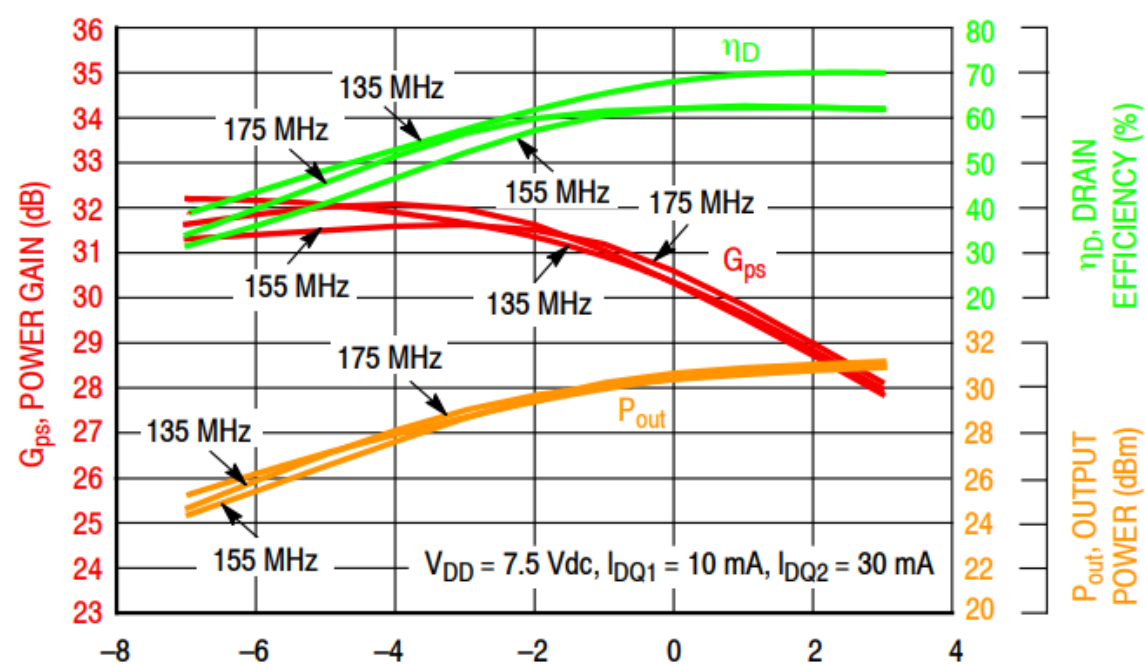
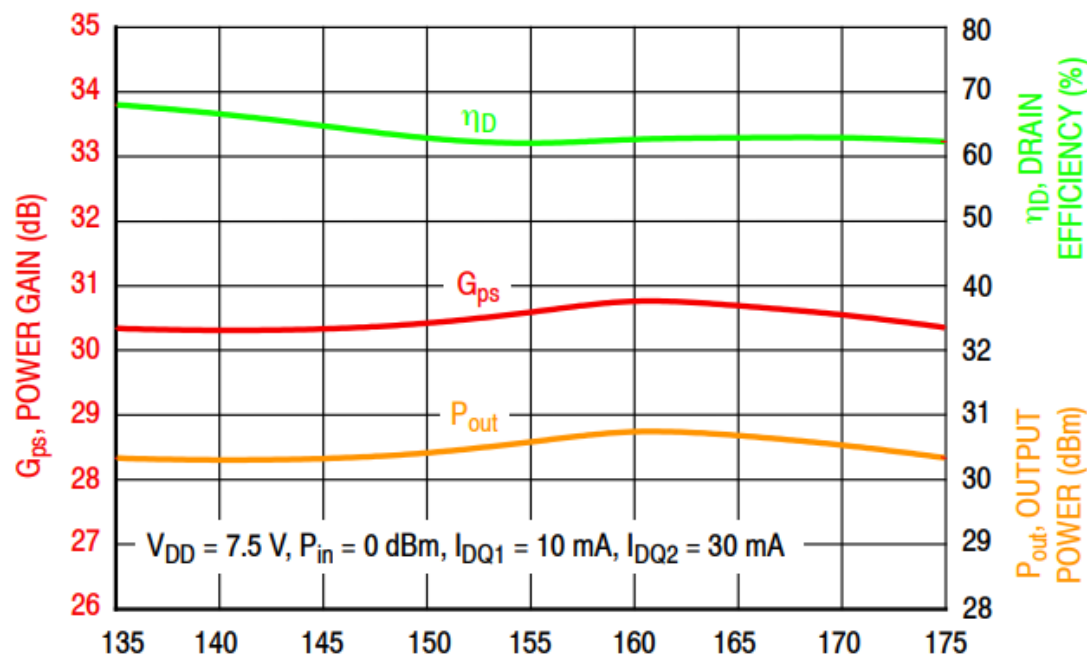
- The NXP AFIC901N is a 1.8-1000 MHz, 1 W CW RF power LDMOS transistor housed in a QFN package. It has no input, no output and no inter-stage matching, allowing off-chip matching for flexible use across frequencies.
 - Further details about the device, including its data sheet, are available [here](#).
- The following pages describe the 136-174 MHz reference circuit (evaluation board). Its typical applications are VHF land mobile radio and use as a generic driver.
- The reference circuit can be ordered through NXP's distribution partners and etailers using part number AFIC901N-135MHZ.



Circuit Overview – 2.11 cm × 4.72 cm (0.83" × 1.86")



Typical CW Performance



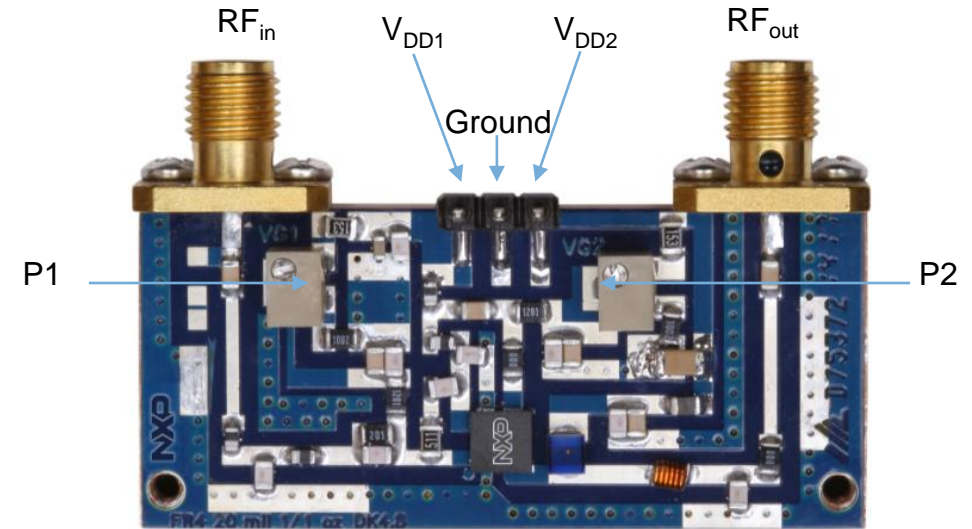
Typical Performance: $V_{DD1} = V_{DD2} = 7.5\text{ Vdc}$, $I_{DQ1} = 10\text{ mA}$, $I_{DQ2} = 30\text{ mA}$, $P_{out} = 1\text{ W}$ (30 dBm), CW

Frequency (MHz)	P_{in} (dBm)	G_{ps} (dB)	η_D (%)	P_{out} (dBm)
135	-0.8	30.8	65.9	30.0
155	-1.3	31.3	59.6	30.0
175	-1.1	31.1	61.4	30.0

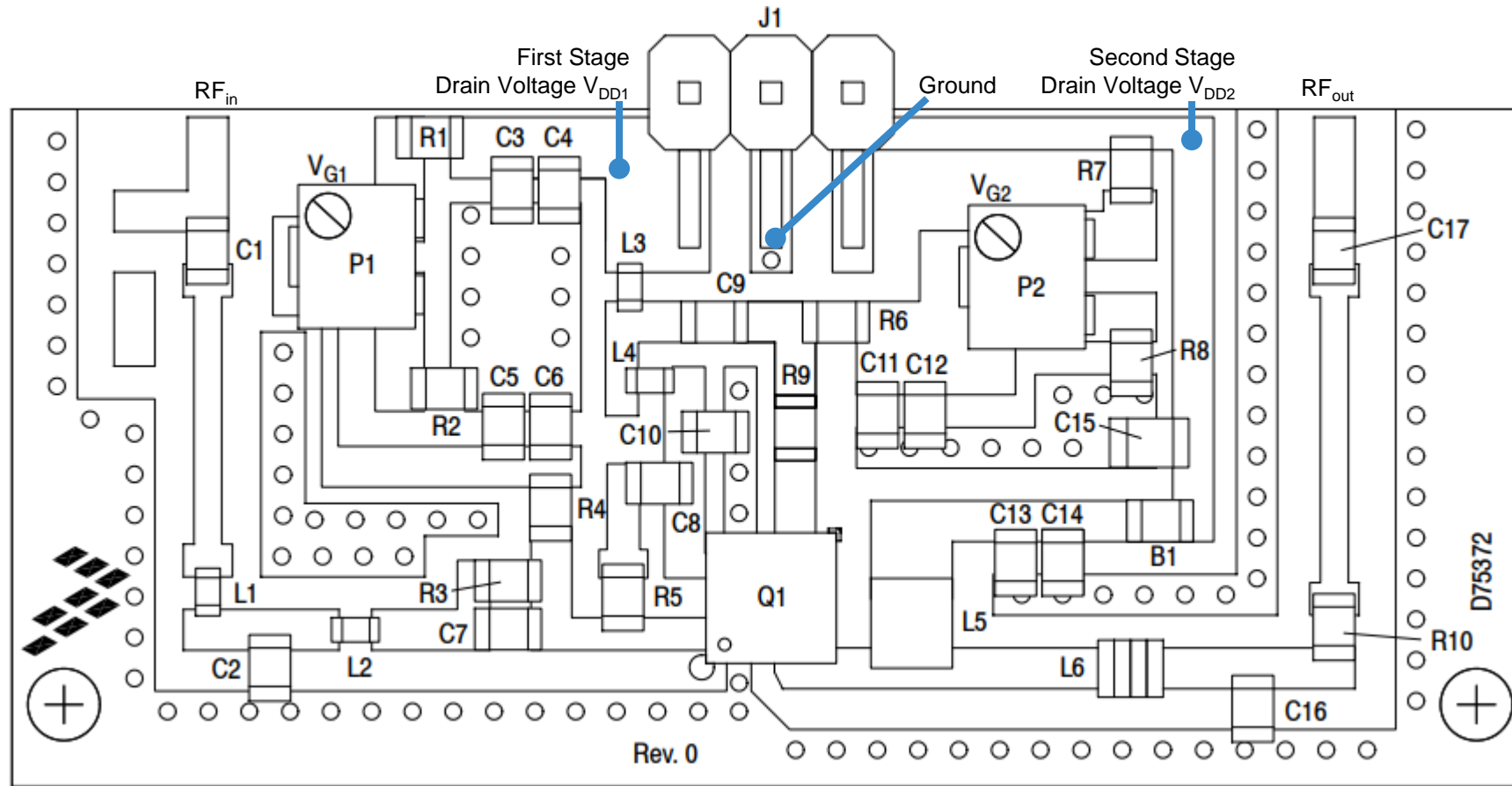


Quick Start

1. Connect the ground.
2. Terminate the RF output with a 50 ohm load capable of handling more than 1 W power.
3. Connect the RF input to a 50 ohm source with the RF off.
4. Connect the first stage drain voltage (V_{DD1}) and raise it slowly to 7.5 V while ensuring that the drain current remains below or equal to the typical drain quiescent current of $I_{DQ1} = 10$ mA.
5. If needed, adjust the P1 potentiometer to modify the first stage gate voltage to control the first stage drain quiescent current I_{DQ1} .
6. Disconnect the first stage drain voltage V_{DD1} . Connect the second stage drain voltage (V_{DD2}) and raise it slowly to 7.5 V while ensuring that the drain current remains below or equal to the typical quiescent current of $I_{DQ2} = 30$ mA.
7. If needed, adjust the P2 potentiometer to modify the second stage gate voltage to control the second stage drain current I_{DQ2} .
8. Keep V_{DD2} connected to 7.5 V and connect again first stage V_{DD1} to 7.5 V. The total drain current should typically be 40 mA.
9. Raise the RF input slowly to 0 dBm (1 mW).
10. Check the RF output power (typically 1 W), the drain current (around 0.3 A for this power level) and the temperature of the board. Ensure the baseplate is not overheating.



Component Placement Reference

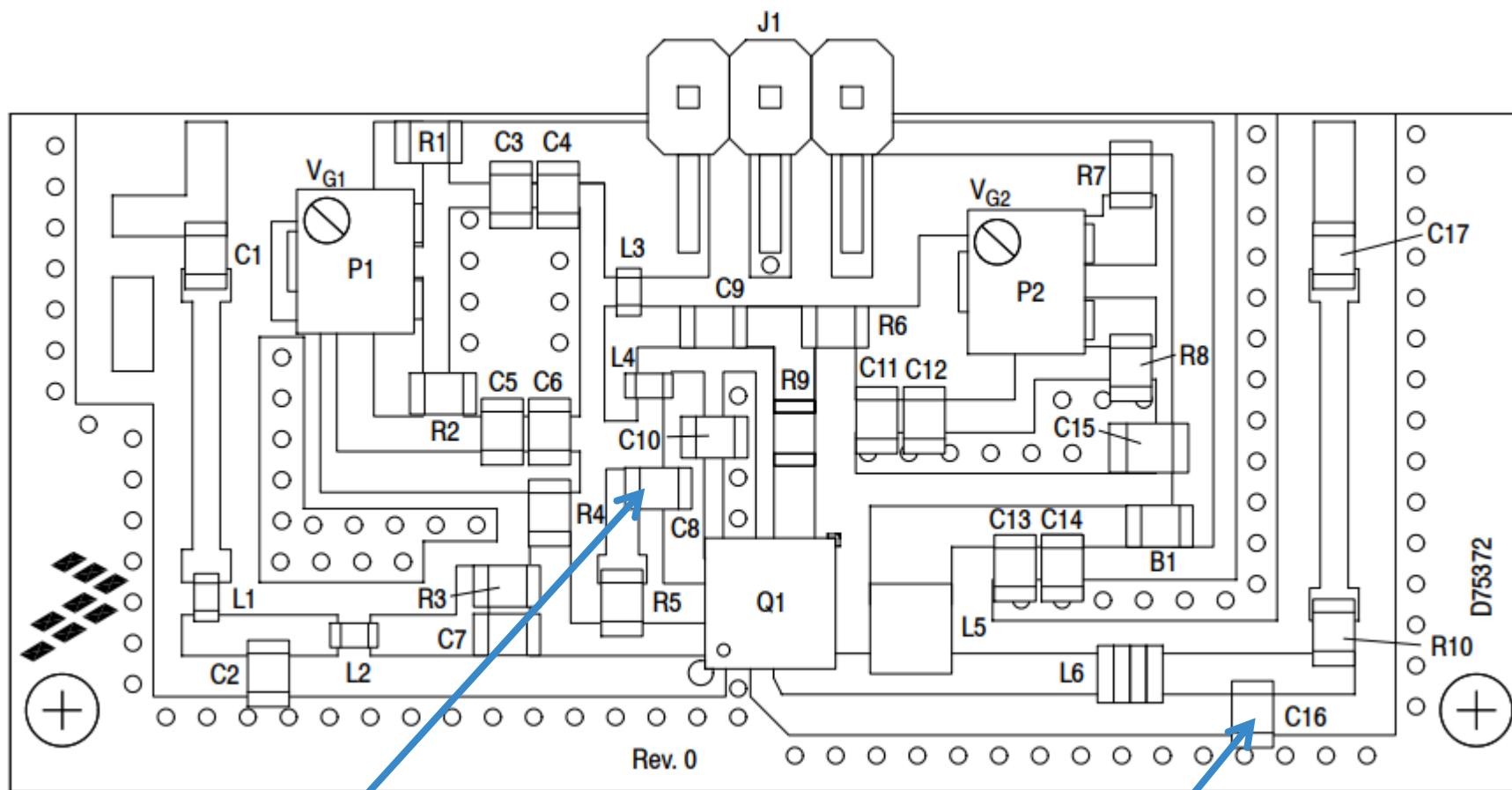


Note: PCBs may have either NXP or Freescale markings. Existing Freescale boards will not migrate to NXP markings unless a board is revised.

Bill of Materials

Part	Description	Part Number	Manufacturer
B1	RF Bead	2508051107Y0	Fair-Rite
C1, C5, C9, C12, C14, C17	1000 pF Chip Capacitors	C2012X7R2E102M085AA	TDK
C2, C16	15 pF Chip Capacitors	GQM2195C2E150FB12D	Murata
C3	1 μ F Chip Capacitor	GRM21BR71H105KA12L	Murata
C4, C6, C7, C8, C11, C13	100 pF Chip Capacitors	GQM2195C2E101GB12D	Murata
C10	6.2 pF Chip Capacitor	GQM2195C2E6R2BB12D	Murata
C15	10 μ F Chip Capacitor	GRM31CR61H106KA12L	Murata
J1	Right-Angle Breakaway Headers (3 Pins)	22-28-8360	Molex
L1, L4	56 nH Inductors	LL1608-FSL56NJ	TOKO
L2	180 nH Inductor	LL1608-FSLR18J	TOKO
L3	120 nH Inductor	LL1608-FSLR12J	TOKO
L5	180 nH Inductor	1008CS-181XJLB	Coilcraft
L6	15.7 nH Inductor	0806SQ15N	Coilcraft
P1, P2	5.0 k Ω Multi-turn Cermet Trimmer Potentiometer	3224W-1-502E	Bourns
Q1	RF Power LDMOS Amplifier	AFIC901NT1	Freescale
R1, R7	15 k Ω , 1/10 W Chip Resistors	RR1220P-153-B-T5	Susumu
R2, R8	10 k Ω , 1/8 W Chip Resistors	CRCW080510K0FKEA	Vishay
R3	200 Ω , 1/8 W Chip Resistor	CRCW0805200RJNEA	Vishay
R4, R6	1.2 k Ω , 1/8 W Chip Resistors	CRCW08051K20FKEA	Vishay
R5	510 Ω , 1/10 W Chip Resistor	RR1220P-511-B-T5	Susumu
R9, R10	0 Ω , 2.5 A Chip Resistors	CWCR08050000Z0EA	Vishay
PCB	FR4 (S-1000), 0.020", $\epsilon_r = 4.8$	D75372	MTL

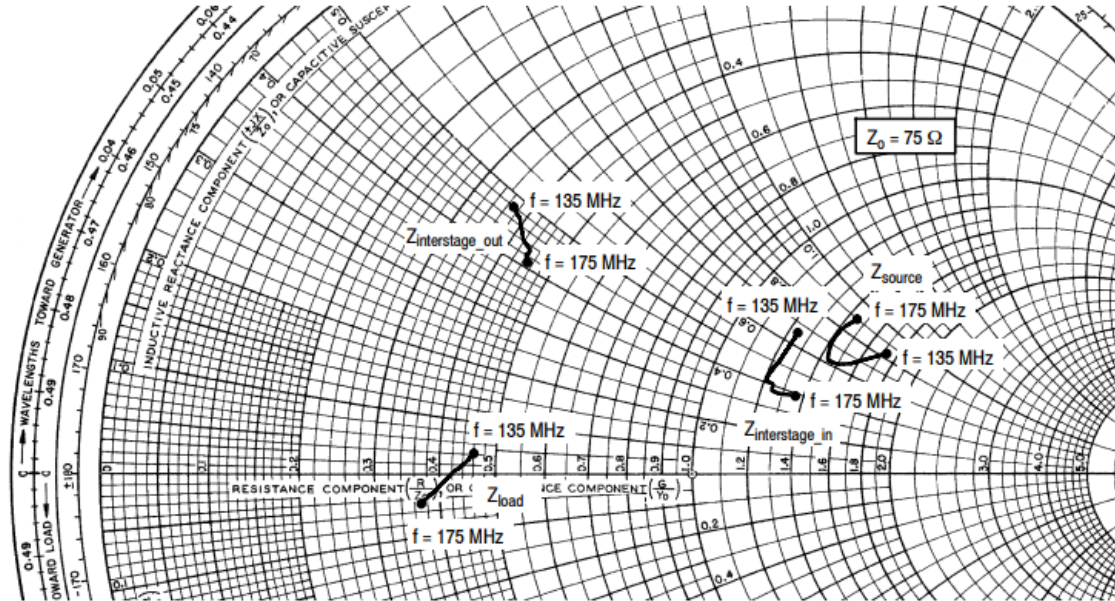
Tuning Tips



Change C10 to a larger value to increase gain and efficiency at 136 MHz

Change C16 to a smaller value to increase power and efficiency at 174 MHz

Impedances



f MHz	$Z_{source1}$ Ω	Z_{load1} Ω	$Z_{source2}$ Ω	Z_{load2} Ω
135	$129.8 + j62.2$	$93.0 + j49.5$	$27.8 + j35.9$	$34.3 + j2.85$
140	$123.1 + j54.4$	$92.5 + j42.5$	$29.4 + j35.1$	$33.4 + j1.92$
145	$117.3 + j49.7$	$91.6 + j37.2$	$30.7 + j34.1$	$32.5 + j1.00$
150	$112.5 + j47.8$	$91.0 + j33.3$	$31.8 + j33.1$	$31.7 + j0.08$
155	$109.1 + j47.7$	$90.9 + j30.7$	$32.7 + j32.2$	$30.9 - j0.83$
160	$107.1 + j49.6$	$91.9 + j29.2$	$33.2 + j31.4$	$30.0 - j1.66$
165	$106.3 + j53.5$	$93.9 + j28.6$	$33.6 + j31.0$	$29.1 - j2.41$
170	$106.8 + j59.2$	$97.4 + j28.7$	$33.9 + j30.9$	$28.2 - j3.03$
175	$108.3 + j67.5$	$102.6 + j29.4$	$34.1 + j31.1$	$27.4 - j3.49$

Z_{source} = Test circuit impedance as measured from gate to gate.

Z_{load} = Test circuit impedance as measured from drain to drain.

Revision History

- The following table summarizes revisions to the content of the AFIC901N 136-174 MHz Reference Circuit zip file.

Revision	Date	Description
0	September 2019	• Initial Release



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