

# A Large Current Source with High Accuracy and Fast Settling

By **Nick Jiang**

Share on   

Voltage controlled current sources (VCCSs) are widely used in many areas, like medical machine and industrial automation. The dc precision, ac performance, and drive capability of a VCCS are highly important in these applications. This article analyzes the enhanced Howland current source (EHCS) circuit's limitations and shows how to improve it with a composite amplifier topology to implement a  $\pm 500$  mA current source with high precision and fast settling.

## Enhanced Howland Current Source

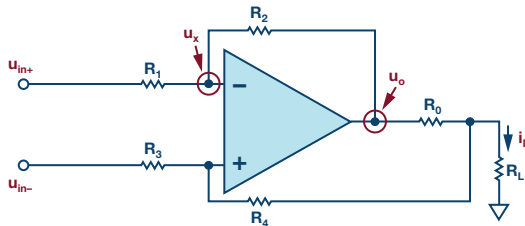


Figure 1. Howland current source circuit.

Figure 1 shows the traditional Howland current source (HCS) circuit, while Equation 1 shows how the output current can be calculated. The output current will be constant if R2 is large enough.

$$i_L R_0 \left[ 1 + \frac{R_1}{R_2} + R_L \left( \frac{1}{R_2} + \frac{1 - \frac{R_1}{R_2} \times \frac{R_4}{R_3}}{R_0} \right) \right] = u_{in+} \left( \frac{R_0}{R_2} + \frac{R_4}{R_3} + 1 \right) - u_{in-} \left( \frac{R_4}{R_3} + \frac{R_1}{R_2} \times \frac{R_4}{R_3} \right) \quad (1)$$

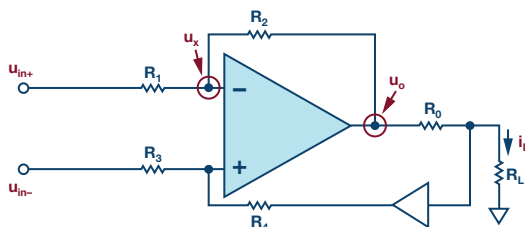


Figure 2. Enhanced Howland current source circuit.

While a large R2 will reduce the speed and precision of the circuit, inserting a buffer into the feedback route to form an enhanced Howland current source will eliminate this, as shown in Figure 2. All the current flows through R0 is through into RL. The output current is calculated with Equation 2.

$$i_L R_0 \left[ 1 + \frac{R_1}{R_2} + R_L \left( 1 - \frac{R_1}{R_2} \times \frac{R_4}{R_3} \right) \right] = u_{in+} \left( \frac{R_4}{R_3} + 1 \right) - u_{in-} \left( \frac{R_4}{R_3} + \frac{R_1}{R_2} \times \frac{R_4}{R_3} \right) \quad (2)$$

If  $R_1/R_2 = R_3/R_4 = k$ , the equation is changed to Equation 3. The output current is independent of the load and only controlled by the input voltage. It's an ideal VCCS.

$$i_L = \frac{u_{in+} - u_{in-}}{k R_0} \quad (3)$$

## Performance Analysis

Equation 3 is based on the ideal system. Figure 3 shows the dc error analysis model of the EHCS.  $V_{OS}$  and  $I_{B+}/I_{B-}$  are the input offset voltage and bias current of the main amplifier.  $V_{OSbuf}$  and  $I_{Bbuf}$  are the input offset voltage and bias current of the buffer. The total output error can be calculated by Equation 4.

$$I_O \left[ R_0 + R_L \left( 1 - \frac{R_1 + R_2}{R_1} \times \frac{R_3}{R_3 + R_4} \right) \right] = \left( \frac{R_2}{R_1} + 1 \right) \times V_{OS} + \left( \frac{R_2}{R_1} + 1 \right) \times \frac{R_3 R_4}{R_3 + R_4} \times I_{B+} - \left( \frac{R_2}{R_1} + 1 \right) \times \frac{R_1 R_2}{R_1 + R_2} \times I_{B-} + \left( \frac{R_2}{R_1} + 1 \right) \times \frac{R_3}{R_3 + R_4} \times V_{OSbuf} - I_{Bbuf} R_0 \quad (4)$$

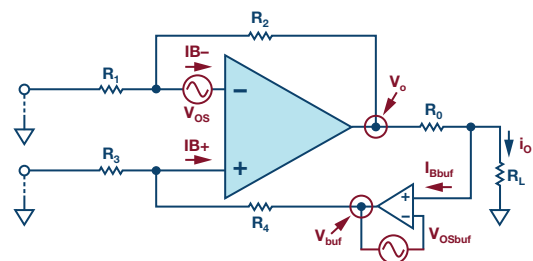


Figure 3. Offset voltage calculation.

Ignore the mismatch from the gain resistors, and consider  $R_1/R_2 = R_3/R_4 = k$ ,  $R_1/R_2 = R_3/R_4$ . The output offset current depends on the amplifiers' offset and bias current, as shown in Equation 5.

$$I_O = \left(\frac{1}{k} + 1\right) \times \frac{1}{R_0} \times V_{os} + \left(\frac{1}{k} + 1\right) \times \frac{1}{R_0} \times \frac{R_1 R_2}{R_1 + R_2} \times I_{os} + \frac{1}{R_0} \times V_{OSbuf} - I_{Bbuf}$$

(5)

Taking the mismatch of  $R_1/R_2$  and  $R_3/R_4$  into consideration,  $R_L$  will influence the output offset current. The worst relative error is shown in Equation 6. The error depends on  $R_L/R_0$  and  $k$ . A smaller load resistor and higher  $k$  will decrease the offset error.

$$Max\ Relative\ Error\ of\ I_O = \frac{R_L}{R_0} \times \frac{2\Delta_k}{k(k+1)}$$

(6)

We can also calculate the temperature drift of the circuit, which comes from amplifiers and resistors. Amplifiers' offset voltage and bias current change with the work temperature. For most CMOS input amplifiers, the bias current doubles for every increase of 10°C. The drift of resistors changes a lot with different types. For example, carbon composition units' TC is approximately 1500 ppm/°C, while metal film and bulk metal resistors' TC can be 1 ppm/°C.

Table 1. Precision Amplifiers Parameters

Devices	V <sub>os</sub> Max (μV)	IB Max (pA)	GPB (MHz)	Slew Rate (V/μs)	Isc (mA)
ADA4522	5	150	3	1.3	22
ADA4077	25	1500	4	1	22
LTC2057HV	4	120	2	1.2	26
LT1012	25	100	1	0.2	13

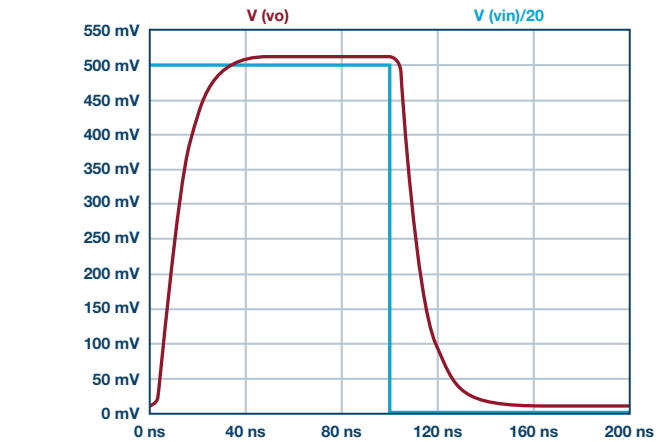


Figure 5. Settling time and frequency response of an EHCS based on ADA4870

Choosing a precision amplifier is good for the dc accuracy of the output current. However, there are many limitations in the precision amplifier selection. The drive capability and ac performance are not good enough. Table 1 lists some common precision amplifiers. We want to build a ±500 mA current source with 1 μs settling time. For a current source we would need high drive capability. For a current source with additional high settling time we need good ac performance. In general, precision amplifiers do not provide that specification combination as the slew rate and bandwidth are not good enough. This requires choosing from a few other amplifiers.

### EHCS Implementation

ADA4870 is a high speed, high voltage, and high drive capacity amplifier. It can supply 10 V to 40 V with 1.2 A output current limitation. Its bandwidth is over 52 MHz for a large signal and the slew rate is up to 2500 V/μs. All these specifications make it the right fit for fast settling and a large current source. Figure 4 shows an EHCS circuit based on the ADA4870 that generates a ±500 mA output current source by 10 V input.

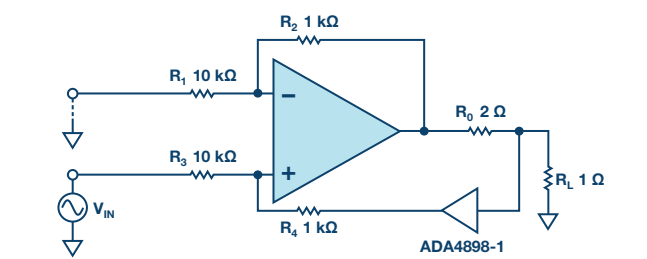
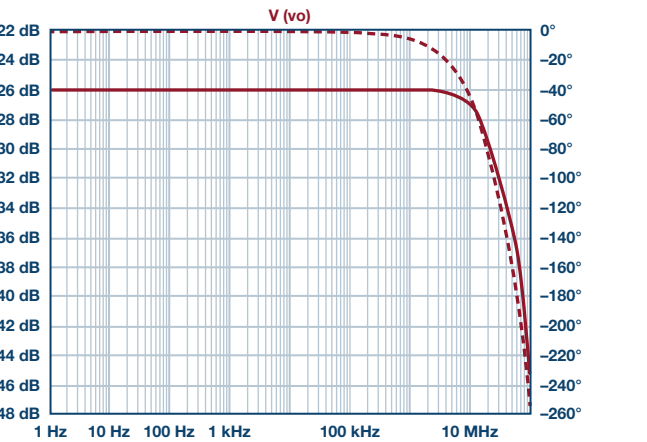


Figure 4. EHCS circuit based on ADA4870.

In ac specifications, we are more care about settling time, slew rate, bandwidth, and noise. The settling time is about 60 ns and bandwidth is about 18 MHz as shown in Figure 5. The output current slew rate can be calculated by measuring the slope of the rising and falling stage. The positive and negative slew rate are +25 A/μs and −25 A/μs. The noise performance is shown in the output noise density curve. It's about 24 nV/√Hz at 1 kHz.



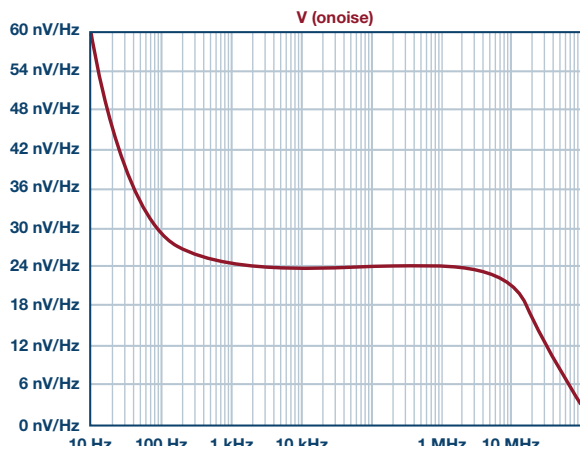


Figure 6. Output noise density curve of EHCS based on ADA4870.

Due to large input offset voltage and bias current, the dc precision is not good in this circuit. Table 2 shows different dc error sources and contribution. The main dc error comes from the  $V_{OS}$  and  $I_B$  of ADA4870. The typical output current offset is about 11.06 mA, which is about 2.21% range error referring to 500 mA full range.

Table 2. The DC Error of EHCS Based on ADA4870

Error Source	Parameters (Typ)	Error Output (mA)	Percentage
$I_B$	$-12 \mu A$	6.00	54.2%
$I_{B+}$	$+9 \mu A$	4.50	40.7%
$V_{OS}$	1 mV	0.55	5.0%
$I_{Bbuf}$	$-0.1 \mu A$	0.00	0.0%
$V_{OSbuf}$	0.02 mV	0.01	0.1%
Total		11.06	100%

### Composite Amplifier Topology

High drive amplifiers like ADA4870's dc parameters limit output current accuracy, and high precision amplifiers don't have enough speed. Here we can combine all these qualities into one circuit with composite amplifier topology. Figure 7 shows the composite amplifier enhanced Howland current source (CAEHCS) that is formed by ADA4870 and ADA4898-2.

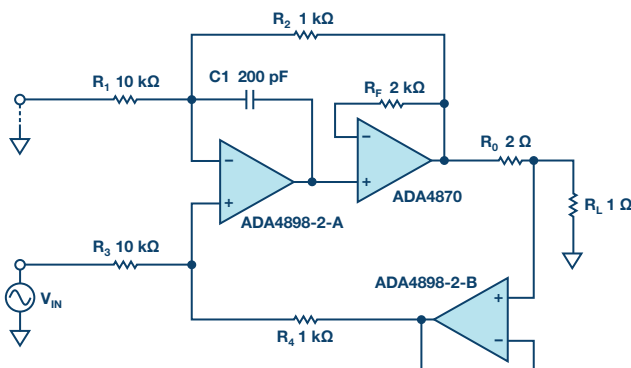


Figure 7. EHCS circuit with composite amplifier.

ADA4898-2 is chosen to form the composite amplifier for its excellent ac and dc performance. Its  $-3$  dB bandwidth is 63 MHz. The settling time to 0.1% with a 5 V output step is 90 ns and the slew rate is up to 55 V/ $\mu$ s. It has ultralow noise, too. The voltage noise density is 0.9 nV/ $\sqrt{\text{Hz}}$  and current noise density is 2.4 pA/ $\sqrt{\text{Hz}}$ . As for dc specifications, it performs well, too. The typical input offset voltage is 20  $\mu$ V with 1  $\mu$ V/ $^{\circ}\text{C}$  temperature drift. The bias current is 0.1  $\mu$ A. Table 3 shows the dc error of the CAEHCS. The output current offset is decreased to 0.121 mA, which means the range error is lower than 0.03%.

Table 3. The DC Error of CAEHCS Based on ADA4898

Error Source	Parameters (Typ)	Error Output (mA)	Percentage
$I_{B-}$	$-0.1 \mu A$	0.050	41.3%
$I_{B+}$	$+0.1 \mu A$	0.0050	41.3%
$V_{OS}$	20 mV	0.011	9.1%
$I_{Bbuf}$	$-0.1 \mu A$	0.000	0.1%
$V_{OSbuf}$	20 $\mu$ V	0.01	8.2%
Total		0.121	100%

The ac performance of the CAEHCS is shown in Table 4. The settling time and bandwidth are lower than EHCS due to the loop delay of the composite amplifier. CAEHCS output noise is much lower than EHCS output noise due to low current noise of ADA4898-2. As specified in the data sheet, the ADA4870's invert input current noise density is 47 pA/ $\sqrt{\text{Hz}}$ . With several k $\Omega$  resistors, it will generate much higher noise than the voltage noise (2.1 nV/ $\sqrt{\text{Hz}}$ ). While the input current noise density of the CAEHCS is 2.4 pA/ $\sqrt{\text{Hz}}$ . It will generate much lower output noise.

Table 4. The AC Specification of the CAEHCS

Parameter	CAEHCS	EHCS
Settling time (ns)	200	60
Slew rate (A/ $\mu$ s)	7.7	25
Bandwidth (MHz)	6	18
Output Noise Density at 1 kHz (nV/ $\sqrt{\text{Hz}}$ )	4	24

Above all, CAEHCS has greatly improved the dc accuracy of the VCCS with comparable drive capacity and ac performance. Besides, there are many selections of the composite amplifiers for different requirements. Table 5 shows the performance of different amplifiers in the CAEHCS circuit. LT6275 is the best in ac performance. Its settling time can be within 100 ns, and the slew rate is up to 15 A/ $\mu$ s. Zero-drift amplifiers like ADA4522-2 are suitable for high precision applications that have about 0.002 mA output current offset error.

Table 5. Selection of Main Amplifier in CAEHCS

Main Amplifier	EHCS	CAEHCS
ADA4898	Good	Good
LT6275	Good	Excellent
ADA4522	Excellent	Not good

### Test Results

The performance of the EHCS and CAEHCS based on ADA4898 are shown in Table 6 and Figure 8.

Table 6. Comparison of EHCS vs. CAEHCS

Main Amplifier		EHCS	CAEHCS
DC Parameters	Output current offset (mA)	10.9	0.2
	Settling time (ns)	100	100
AC Parameters	Slew rate (A/μs)	22.2	12.6
	Bandwidth (MHz)	18	8

Table 7. Test Results of the Different Main Amplifier in CAEHCS

Main Amplifier	I <sub>os</sub> (mA)	Settling time (ns)	Slew Rate (A/μs)	Bandwidth (MHz)
ADA4898	0.2	100	12.6	10
LT6275	0.8	60	16.6	11
ADA4522	0.04	1000	0.4	1.2

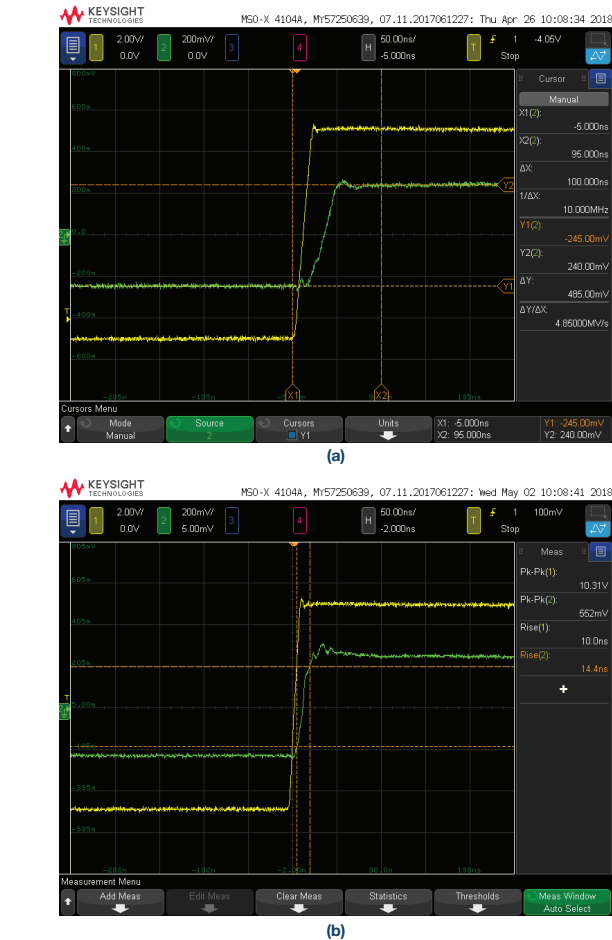


Figure 9. The settling time of the LT6275 (CH1-Input, CH2-Output).

Thermal Consideration

The output current of the VCCS can be several hundred milliamperes. The whole power dissipation can be several watts. If output efficiency is bad, the temperature of the part will rise rapidly. The thermal resistance ( $\theta_{JA}$ ) of ADA4870 without a head sink can be 15.95°C/W. The temperature rising can be calculated by using Equation 7.

$$T_{\text{rise}} = \theta_{JA} \times P \tag{7}$$

The value of  $R_0$  will influence the power dissipation of ADA4870. Table 8 shows the temperature rise with different  $R_0$  selected at a  $\pm 20\text{ V}$  supply. The temperature rising will decrease greatly when larger  $R_0$  is used. Therefore, larger  $R_0$  is recommended to decrease the temperature rise.

Table 8. ADA4870’s Power Dissipation and Temperature Rise vs.  $R_0$  ( $I_o = 500\text{ mA}$ )

RL/Q	Power Dissipation (W)			Temperature Rise (°C)
	$R_0 = 2\ \Omega$	$R_0 = 10\ \Omega$	$R_0 = 2\ \Omega$	$R_0 = 10\ \Omega$
1	10.55	8.55	168.3	136.4
5	9.55	7.55	152.3	120.4
10	8.30	6.30	132.4	100.5

Conclusion

The CAEHCS circuit that combines a high drive amplifier and a high precision amplifier can provide excellent ac and dc performance with large output capacity in VCCS applications. ADA4870 combined with ADA4898, LT6275, and ADA4522 are recommended for use in this circuit.

Figure 8. The settling time of the ADA4898-2 (CH1-Input, CH2-Output).

The CAEHCS circuit has much better dc specifications than an EHCS circuit. Its output current offset is 0.2 mA, while the EHCS circuit’s output current offset is 10.9 mA. The CAEHCS circuit has good ac specifications, too. The settling time both are about 100 ns. The bandwidth of the EHCS circuit is 18 MHz, and the CAEHCS circuit is 8 MHz.

The performance of the CAEHCS based on the ADA4522-2 and LT6275 is shown in Table 7. The output offset error of ADA4522-2 version is lower to 0.04 mA. The settling time of LT6275 version is about 60 ns and the output current slew rate is up to 16.6 A/μs, which is shown in Figure 9.

Nick Jiang is a product applications engineer in the Analog Devices Linear and Precision Technology Group, and he is based in Beijing. He graduated from Xi’an Jiaotong University, with a bachelor’s and master’s degree in electrical engineering.



Nick Jiang