19-4951; Rev 1; 11/09

EVALUATION KIT AVAILABLE

MAXIM

Step-Up, Step-Down Regulator, Gate-On Charge Pump, and Boost-Buck Regulator for TV TFT LCD Display

MAX17122

General Description

The MAX17122 multiple-output power-supply IC generates all the supply rails for thin-film transistor (TFT) liquid-crystal display (LCD) TV panels. It can operate from 8V to 16.5V input voltages and is optimized for LCD TV panel applications running directly from 12V regulated supplies. It includes a 22V internal-switch step-down regulator for digital logic, a 22V internal switch step-up regulator to power the TFT source drivers, and a temperature-compensated 36V internal-switch boost-buck regulator that produces a negative output that can vary according to the temperature sensed by an external NTC thermistor. All three of these regulators feature high-efficiency and fixed-frequency operation. High-frequency operation allows the use of small inductors and capacitors, resulting in a compact solution.

The MAX17122 includes a positive charge-pump linear regulator controller that uses an external pnp bipolar junction transistor (BJT) to typically form a regulated charge-pump doubler to supply the LCD positive gate-driver supply voltage. A negative gate-driver supply is derived linearly between the boost-buck regulator's output and ground, using an external npn BJT connected to ground and a small bypass capacitor.

Other features include an external-capacitor-timed, open-drain, power-good output that monitors the step-down regulator's feedback and a simple untimed output that monitors the positive charge-pump linear regulator's feedback. A high-voltage stress function is available for the step-up regulator output. The GATE output directly drives an external p-channel MOSFET to provide True Shutdown™ of the step-up output.

The MAX17122 is available in a 6mm x 6mm, 40-pin thin QFN lead-free package and operates over the -40°C to +85°C temperature range.

Applications

LCD TV Panels

Features

- **8V to 16.5V Operating Range**
- **750kHz Switching Frequency**
- **22V Internal-Switch High-Performance Step-Up Regulator**
  - **Fast Load-Transient Response**
  - **Current-Mode PWM Operation**
  - **100mΩ, 3.9A nMOS Switch**
  - **Capacitor-Adjustable Soft-Start**
  - **High-Voltage Stress Function**
  - **Drives External pMOS Shutdown Switch**
- **22V Internal-Switch Step-Down Regulator**
  - **Preset 1% Accurate 3.3V Output Voltage or Adjustable Output (Dual Mode™)**
  - **Current-Mode PWM Operation**
  - **200mΩ, 2.5A nMOS Switch**
  - **Capacitor-Adjustable Power-Good Output**
- **36V Internal-Switch Boost-Buck Regulator**
  - **Temperature-Compensated Output**
  - **Programmable Fixed Levels with Temperature-Controlled Transition**
  - **Current-Mode PWM Operation**
  - **200mΩ, 1.8A pMOS Switch**
- **Positive Charge-Pump Linear Regulator Controller**
  - **Adjustable 1% Accurate Output Voltage**
  - **Uses External pnp Transistor**
  - **Regulates Switching-Node-Driven Charge-Pump Doubler**
  - **Power-Good Output**
- **Negative Linear Regulator Controller**
  - **Adjustable 1.5% Accurate Output Voltage**
  - **Uses External npn Transistor**
- **Soft-Start for All Outputs**
- **Adjustable Power-Up Sequence**
- **Timed-Output Fault Protection with Restart for All Outputs**
- **Latched Thermal-Shutdown Protection**
- **40-Pin, 6mm x 6mm Thin QFN Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX17122ETL+	-40°C to +85°C	40 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

True Shutdown and Dual Mode are trademarks of Maxim Integrated Products, Inc.

Pin Configuration appears at end of data sheet.

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

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ABSOLUTE MAXIMUM RATINGS

IN, IN2, IN3, EN1, EN2, LX1, GATE, DRVP, RHVS to AGND ..... -0.3V to +22V
GATE to IN ..... -6.5V to +0.3V
GND1 to AGND ..... ±0.3V
DLY1, DLY2, DEL, VL, RESET, GPGD, HVS to AGND ..... -0.3V to +6V
FBP, FBN, FB1, FB2, FB3, COMP1, COMP3, OUTB SET, NTC, SS to AGND ..... -0.3V to (V_{VL} + 0.3V)
DRVN to VL ..... -36V to +0.3V
LX2 to GND1 ..... -0.3V to (V_{IN2} + 0.3V)
LX3 to IN3 ..... -36V to +0.3V
BST2 to VL ..... -0.3V to +22V
BST2 to LX2 ..... -0.3V to +6V
RMS LX1, GND1, IN2, IN3, LX3 Current (each pin) 1.6A
RMS LX2 (total for both pins) 2.4A
RMS VL, DRVN, DRVP Current 50mA
Continuous Power Dissipation (T_A = +70°C)
40-Pin Thin QFN (derate 35.7mW/°C above +70°C) 2857.1mW
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature ..... +160°C
Storage Temperature Range ..... -65°C to +165°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V_{IN} = V_{IN2} = V_{IN3} = 12V, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL						
IN, IN2, IN3 Input-Voltage Range			8		16.5	V
IN + IN2 + IN3 Quiescent Current	Only LX2 and LX3 switching (V_{FB1} = V_{FBP} = 1.5V, V_{FB2} = 1.1V, V_{FB3} = 1.8V, V_{FBN} = 1.5V); V_{EN1} = V_{EN2} = 5V			10	15	mA
	LX2 and LX3 not switching (V_{FB1} = V_{FB2} = V_{FBP} = 1.5V, V_{FBN} = 1.5V, V_{FB3} = 0); V_{EN1} = V_{EN2} = 5V			2	4	
IN + IN2 + IN3 Shutdown Current	EN1 = EN2 = AGND (shutdown)			0.55	1	mA
SMPS Operating Frequency			638	750	862	kHz
Phase Difference Between Regulators	Step-down and boost-buck			180		Degrees
	Step-down and step-up			180		
IN Undervoltage-Lockout Threshold	V_{IN} rising, 2.5% hysteresis		6	7	8	V
VL REGULATOR						
VL Output Voltage	I_{VL} = 10mA, V_{FB1} = V_{FB2} = V_{FBP} = 1.1V, V_{FBN} = 0.75V, V_{FB3} = 1.8V (all regulators switching)		4.9	5.0	5.1	V
VL Undervoltage-Lockout Threshold	VL rising, 2.5% hysteresis		3.6	4.0	4.4	V
STEP-DOWN REGULATOR						
OUTB Voltage in Fixed Mode	FB2 = AGND, no load (Note 1)	T_A = +25°C	3.267	3.300	3.333	V
		0°C < T_A < +85°C	3.25		3.35	
FB2 Voltage in Adjustable Mode	V_{OUTB} = 3.3V, no load (Note 1)	T_A = +25°C	1.2375	1.250	1.2625	V
		0°C < T_A < +85°C	1.23		1.27	
FB2 Adjustable-Mode Threshold Voltage	Dual-mode comparator		0.10	0.15	0.20	V

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = V_{IN2} = V_{IN3} = 12V, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage Adjust Range	Step-down output		1.5		3.6	V
FB2 Fault-Trip Level	Falling edge		0.96	1.0	1.04	V
FB2 Input-Bias Current	V_{FB2} = 1.5V		50	125	200	nA
DC Load Regulation	0.4A < I_{LOAD} < 2A			0.5		%
DC Line Regulation	No load, 10.8V < V_{IN2} < 13.2V			0.1		%/V
LX2-to-IN2 nMOS Switch On-Resistance				200	400	mΩ
LX2-to-GND1 nMOS Switch On-Resistance			6	10	24	Ω
BST2-to-VL pMOS Switch On-Resistance			6	12	24	Ω
Low-Frequency Operation OUTB Threshold	LX2 only			0.8		V
Low-Frequency Operation Switching Frequency				188		kHz
LX2 Positive Current Limit			2.5	3.0	3.5	A
Soft-Start Ramp Time	Zero to full limit			3		ms
Maximum Duty Factor			68	75	82	%
BOOST-BUCK REGULATOR						
FB3 Regulation Voltage	No load, V_{NTC} = 2V	T_A = +25°C	1.63	1.65	1.67	V
		0°C < T_A < +85°C	1.62	1.65	1.68	
FB3 Input-Bias Current	V_{FB3} = 0.5V		-50	-125	-210	nA
FB3 Pulldown Resistance	EN1 = AGND		300		1200	Ω
FB3 Fault-Trip Level	Rising edge		1.9	2.0	2.1	V
DC Load Regulation	0A < I_{LOAD} < 400mA			0.3		%
DC Line Regulation	No load, 10.8V < V_{IN2} < 13.2V			0.1		%/V
LX3-to-IN3 pMOS Switch On-Resistance				200	400	mΩ
LX3 Positive Current Limit	Duty cycle = 60%		1.8	2.1	2.4	A
Soft-Start Ramp Time	Zero to full limit			3		ms
Maximum Duty Factor			85	89	94	%
NTC, SET Current	0°C < T_A < +25°C		98	100	102	µA
	+25°C < T_A < +85°C			100		
NTC, SET Effective Voltage Range	0°C < T_A < +25°C		0.1		1.65	V
	+25°C < T_A < +85°C		0.3		1.65	

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ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, $V_{IN} = V_{IN2} = V_{IN3} = 12V$, **$T_A$ = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
STEP-UP REGULATOR						
Output-Voltage Range			V_{IN}		20	V
Oscillator Maximum Duty Cycle			70	76	83	%
FB1 Regulation Voltage	V_{FB1} = COMP, C_{COMP} = 1nF	T_A = +25°C	1.2375	1.250	1.2625	V
		0°C < T_A < +85°C	1.23		1.27	
FB1 Output Undervoltage Fault Trip Level	Falling edge		0.96	1.0	1.04	V
FB1 Output Short Trip Level	Falling edge		0.35	0.375	0.4	V
FB1 Load Regulation	0 < I_{LOAD} < full, transient only			-1		%
FB1 Line Regulation	10.8V < V_{IN} < 13.2V			0.08	0.15	%/V
FB1 Input-Bias Current	V_{FB1} = 2V		10	125	200	nA
FB1 Transconductance	ΔI = ±2.5µA at COMP, FB1 = COMP		150	320	560	µS
FB1 Voltage Gain	FB1 to COMP			3500		V/V
LX1 Bias Current	V_{FB1} = 1.5V, V_{LX1} = 20V			10	40	µA
LX1 Current Limit	V_{FB1} = 1.1V, duty cycle = 25%		3.9	4.5	5.1	A
Current-Sense Transresistance			0.16	0.23	0.3	V/A
LX1 On-Resistance				100	200	mΩ
SS Full Output Level				1.25		V
SS Charge Current			6	9	12	µA
POSITIVE CHARGE-PUMP LINEAR REGULATOR (DRVP)						
FBP Regulation Voltage	I_{DRVP} = 1.35mA	T_A = +25°C	1.2375	1.250	1.2625	V
		0°C < T_A < +85°C	1.23		1.27	
FBP Input-Bias Current	V_{FBP} = 1.25V		-50		+50	nA
FBP Effective Load-Regulation Error (Transconductance)	V_{DRVP} = 15V, I_{DRVP} = 0.6mA to 6mA			15	30	mV
DRVP Sink Current	V_{DRVP} = 15V, V_{FBP} = 1.1V		10		30	mA
DRVP Off-Leakage Current	V_{DRVP} = 15V, V_{FBP} = 1.5V			0.1	10	µA
FBP Fault-Trip Level	Falling edge		0.96	1.0	1.04	V
Positive Regulator Soft-Start Period	7-bit voltage ramp with filtering to prevent high peak currents			3		ms
NEGATIVE LINEAR-REGULATOR CONTROLLER (DRVN)						
FBN Regulation Voltage	I_{DRVN} = 1.35mA	T_A = +25°C	0.985	1	1.015	V
		0°C < T_A < +85°C	0.98	1	1.02	
FBN Input-Bias Current			-50		+50	nA
FBN Pulldown Resistance	EN1 = AGND		250		1000	Ω
FBN Fault-Trip Level	Falling edge		0.45	0.5	0.55	V
FBN Effective Load-Regulation Error (Transconductance)	V_{DRVN} = -7.5V, I_{DRVN} = 0.6mA to 6mA			23	46	mV
DRVN Source Current	V_{DRVN} = -7.5V, V_{FBN} = 0.85V		10			mA
DRVN Off-Leakage Current	V_{DRVN} = -7.5V, V_{FBN} = 1.15V				40	µA

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = V_{IN2} = V_{IN3} = 12V, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
POWER-GOOD BLOCKS					
FB2 Power-Good Threshold	FB2 rising	0.975	1.00	1.025	V
FB2 Threshold Hysteresis			12		mV
RESET Output Low Voltage	I_{RESET} = 1mA			0.4	V
RESET Leakage Current	V_{RESET} = 3V			1	µA
FBP Power-Good Threshold	FBP rising	1.1	1.15	1.2	V
FBP Threshold Hysteresis			125		mV
GPGD Output Low Voltage	I_{GPGD} = 1mA			0.4	V
GPGD Leakage Current	V_{GPGD} = 3V			1	µA
GATE FUNCTION					
GATE Pulldown Current	GATE charging current		0.15		mA
	Gate done current		0.62		
GATE Drive Voltage	V_{IN2} - V_{GATE}, GATE enabled	5.0	5.35	5.65	V
GATE Pullup Resistance	GATE off, to IN2		25		Ω
HVS BLOCK					
HVS Input Low Voltage				0.6	V
HVS Input High Voltage		1.85			V
HVS Input Pulldown Resistance			1		MΩ
RHVS Output Resistance	I_{RHVS} = 4mA		25		Ω
SEQUENCE CONTROL					
EN1, EN2, DLY1, DLY2, DEL Charge Current	Measured at 1V	6	8.5	11	µA
EN1, EN2, DLY1, DLY2, DEL Turn-On Threshold			1.25	1.30	V
EN1, EN2 Discharge Switch On-Resistance	VL < UVLO or fault tripped		50		Ω
DLY1, DLY2, DLP Discharge Switch On-Resistance	EN1 = low or fault tripped		10		Ω
FAULT DETECTION					
Duration to Trigger Fault			50		ms
Duration to Restart After Fault			160		ms
Thermal-Shutdown Threshold	Typical hysteresis = 15°C		+160		°C

Step-Up, Step-Down Regulator, Gate-On Charge Pump, and Boost-Buck Regulator for TV TFT LCD Display

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, $V_{IN} = V_{IN2} = V_{IN3} = 12V$, **$T_A$ = -40°C to +85°C**.) (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL						
IN, IN2, IN3 Input-Voltage Range			8		16.5	V
IN + IN2 + IN3 Quiescent Current	Only LX2 and LX3 switching ($V_{FB1} = V_{FBP} = 1.5V$, $V_{FB2} = 1.1V$, $V_{FB3} = 1.8V$, $V_{FBN} = 1.5V$); $V_{EN1} = V_{EN2} = 5V$				15	mA
IN + IN2 + IN3 Quiescent Current	LX2 and LX3 not switching ($V_{FB1} = V_{FB2} = V_{FBP} = 1.5V$, $V_{FBN} = 1.5V$, $V_{FB3} = 0$); $V_{EN1} = V_{EN2} = 5V$				4	mA
IN + IN2 + IN3 Shutdown Current	EN1 = EN2 = AGND (shutdown)				1	mA
SMPS Operating Frequency			638		862	kHz
IN Undervoltage-Lockout Threshold	V_{IN} rising, 2.5% hysteresis		6		8	V
VL REGULATOR						
VL Output Voltage	$I_{VL} = 10mA$, $V_{FB1} = V_{FB2} = V_{FBP} = 1.1V$, $V_{FBN} = 0.75V$, $V_{FB3} = 1.8V$ (all regulators switching)		4.9		5.1	V
VL Undervoltage-Lockout Threshold	VL rising, 2.5% hysteresis		3.6		4.4	V
STEP-DOWN REGULATOR						
OUTB Voltage in Fixed Mode	FB2 = AGND, no load (Note 1)	-40°C < T_A < +85°C	3.25		3.35	V
FB2 Voltage in Adjustable Mode	$V_{OUTB} = 3.3V$, no load (Note 1)	-40°C < T_A < +85°C	1.23		1.27	V
FB2 Adjustable-Mode Threshold Voltage	Dual-mode comparator		0.10		0.20	V
Output Voltage Adjust Range	Step-down output		1.5		3.6	V
FB2 Fault-Trip Level	Falling edge		0.96		1.04	V
FB2 Input-Bias Current	$V_{FB2} = 1.5V$		50		200	nA
LX2-to-IN2 nMOS Switch On-Resistance					400	mΩ
LX2-to-GND1 nMOS Switch On-Resistance				6	24	Ω
BST2-to-VL pMOS Switch On-Resistance				6	24	Ω
LX2 Positive Current Limit			2.5		3.5	A
Maximum Duty Factor			68		82	%
BUCK-BOOST REGULATOR						
FB3 Regulation Voltage	No load, $V_{NTC} = 2V$	-40°C < T_A < +85°C	1.62		1.68	V
FB3 Input-Bias Current	$V_{FB3} = 0.5V$		-50		-210	nA
FB3 Pulldown Resistance	EN1 = AGND		300		1200	Ω
FB3 Fault-Trip Level	Rising edge		1.9		2.1	V
LX3-to-IN3 pMOS Switch On-Resistance					400	mΩ

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = V_{IN2} = V_{IN3} = 12V, **T_A = -40°C to +85°C**.) (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
LX3 Positive Current Limit	Duty cycle = 60%		1.8		2.4	A
Maximum Duty Factor			85		94	%
NTC, SET Current	-40°C < T_A < +25°C		97		104	µA
NTC, SET Effective Voltage Range	0°C < T_A < +25°C		0.1		1.65	V
	+25°C < T_A < +85°C		0.3		1.65	
STEP-UP REGULATOR						
Output-Voltage Range			V_{IN}		20	V
Oscillator Maximum Duty Cycle			70		83	%
FB1 Regulation Voltage	FB1 = COMP, C_{COMP} = 1nF	-40°C < T_A < +85°C	1.23		1.27	V
FB1 Output Undervoltage Fault-Trip Level	Falling edge		0.96		1.04	V
FB1 Output Short-Trip Level	Falling edge		0.35		0.4	V
FB1 Line Regulation	10.8V < V_{IN} < 13.2V				0.15	%/V
FB1 Input-Bias Current	V_{FB1} = 2V		10		200	nA
FB1 Transconductance	ΔI = ±2.5µA at COMP, FB1 = COMP		150		560	µS
LX1 Bias Current	V_{FB1} = 1.5V, V_{LX1} = 20V				40	µA
LX1 Current Limit	V_{FB1} = 1.1V, duty cycle = 25%		3.9		5.1	A
Current-Sense Transresistance			0.16		0.3	V/A
LX1 On-Resistance					200	mΩ
SS Charge Current			6		12	µA
POSITIVE CHARGE-PUMP LINEAR REGULATOR (DRVP)						
FBP Regulation Voltage	I_{DRVP} = 1.35mA	-40°C < T_A < +85°C	1.23		1.27	V
FBP Input-Bias Current	V_{FBP} = 1.25V		-50		+50	nA
FBP Effective Load-Regulation Error (Transconductance)	V_{DRVP} = 15V, I_{DRVP} = 0.6mA to 6mA				30	mV
DRVP Sink Current	V_{DRVP} = 15V, V_{FBP} = 1.1V		10		30	mA
DRVP Off-Leakage Current	V_{DRVP} = 15V, V_{FBP} = 1.5V				10	µA
FBP Fault-Trip Level	Falling edge		0.96		1.04	V
NEGATIVE LINEAR-REGULATOR CONTROLLER (DRVN)						
FBN Regulation Voltage	I_{DRVN} = 1.35mA	-40°C < T_A < +85°C	0.98		1.02	V
FBN Input-Bias Current			-50		+50	nA
FBN Pulldown Resistance	EN1 = AGND		250		1000	Ω
FBN Fault-Trip Level	Falling edge		0.45		0.55	V
FBN Effective Load-Regulation Error (Transconductance)	V_{DRVN} = -7.5V, I_{DRVN} = 0.6mA to 6mA				46	mV
DRVN Source Current	V_{DRVN} = -7.5V, V_{FBN} = 0.85V		10			mA
DRVN Off-Leakage Current	V_{DRVN} = -7.5V, V_{FBN} = 1.15V				40	µA

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = V_{IN2} = V_{IN3} = 12V, **T_A = -40°C to +85°C**.) (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
POWER-GOOD BLOCKS					
FB2 Power-Good Threshold	FB2 rising	0.975		1.025	V
RESET Output Low Voltage	I_{RESET} = 1mA			0.4	V
RESET Leakage Current	V_{RESET} = 3V			1	µA
FBP Power-Good Threshold	FBP rising	1.1		1.2	V
GPGD Output Low Voltage	I_{GPGD} = 1mA			0.4	V
GPGD Leakage Current	V_{GPGD} = 3V			1	µA
GATE FUNCTION					
GATE-Drive Voltage	V_{IN2} - V_{GATE}, GATE enabled	5.0		5.65	V
HVS BLOCK					
HVS Input Low Voltage				0.6	V
HVS Input High Voltage		1.85			V
SEQUENCE CONTROL					
EN1, EN2, DLY1, DLY2, DEL Charge Current	Measured at 1V	6		11	µA
EN1, EN2, DLY1, DLY2, DEL Turn-On Threshold				1.30	V

Note 1: When the inductor is in continuous conduction (EN2 = VL or heavy load), the output voltage has a DC regulation level lower than the error-comparator threshold by 50% of the output-voltage ripple. In discontinuous conduction (light load), the step-down regulator's output voltage has a DC regulation level higher than the error-comparator threshold by up to 50% of the output-voltage ripple.

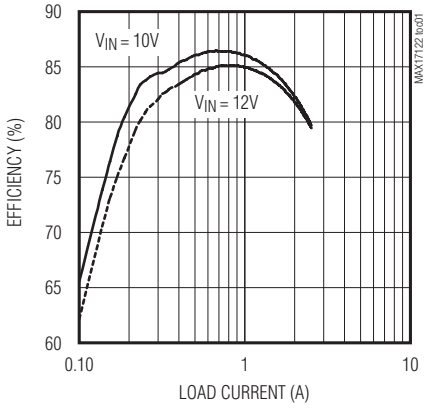
Note 2: Specifications to -40°C are guaranteed by design, not production tested.

Step-Up, Step-Down Regulator, Gate-On Charge Pump, and Boost-Buck Regulator for TV TFT LCD Display

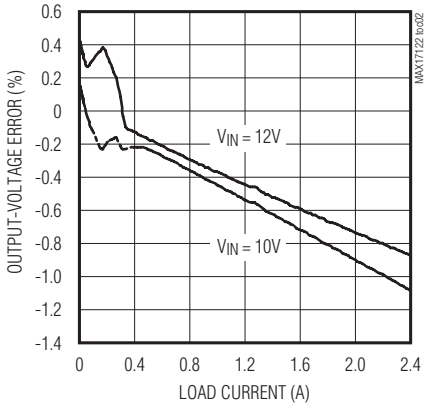
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

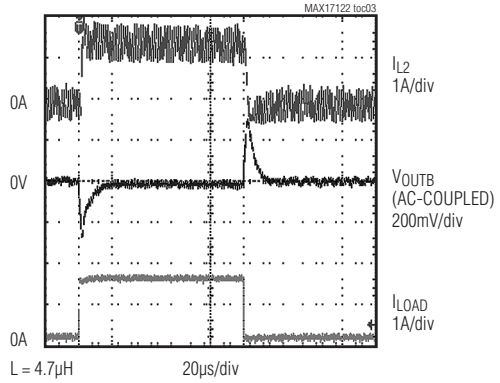
STEP-DOWN REGULATOR EFFICIENCY vs. LOAD CURRENT



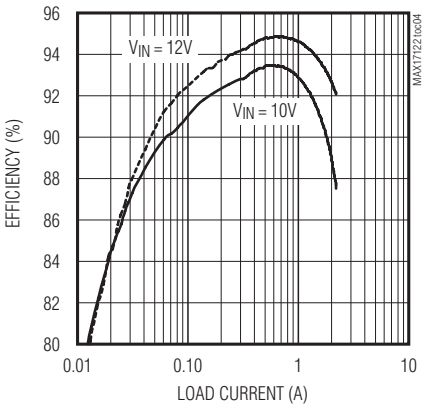
STEP-DOWN REGULATOR NORMALIZED OUTPUT VOLTAGE vs. LOAD CURRENT



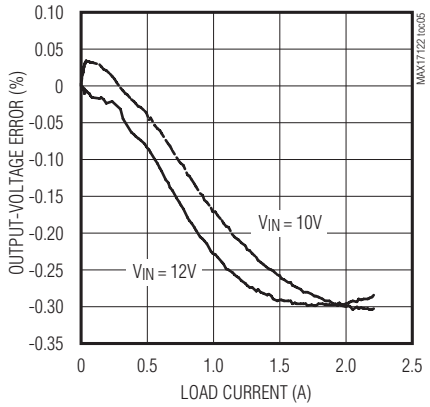
STEP-DOWN REGULATOR LOAD-TRANSIENT RESPONSE (0.2A TO 1.7A)



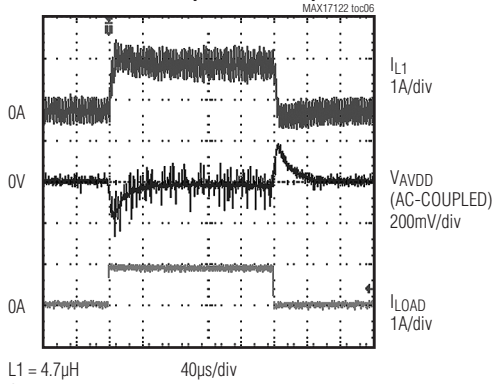
STEP-UP REGULATOR EFFICIENCY vs. LOAD CURRENT



STEP-UP REGULATOR NORMALIZED OUTPUT VOLTAGE vs. LOAD CURRENT



STEP-UP REGULATOR LOAD-TRANSIENT RESPONSE (0.2A TO 1.2A)

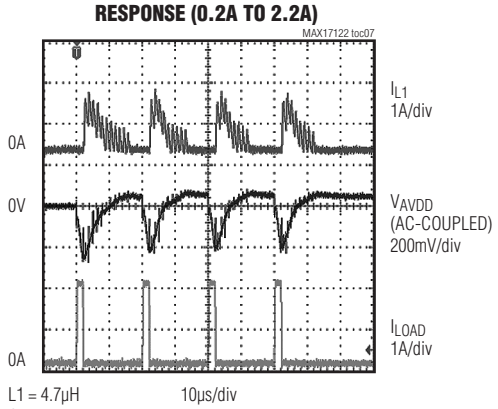


Step-Up, Step-Down Regulator, Gate-On Charge Pump, and Boost-Buck Regulator for TV TFT LCD Display

Typical Operating Characteristics (continued)

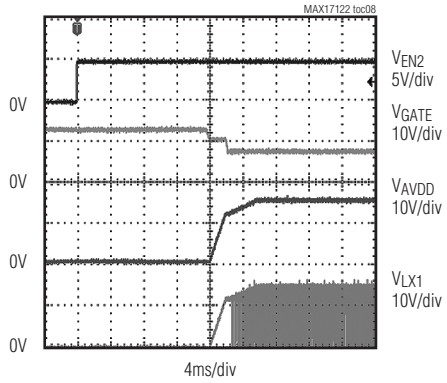
(T_A = +25°C, unless otherwise noted.)

STEP-UP REGULATOR PULSED LOAD-TRANSIENT RESPONSE (0.2A TO 2.2A)

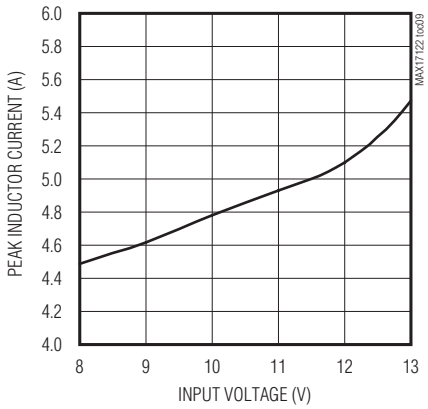


L1 = 4.7µH
C_{COMP1} = 330pF
R_{COMP1} = 39.2kΩ
C_{COMP1P} = 10pF

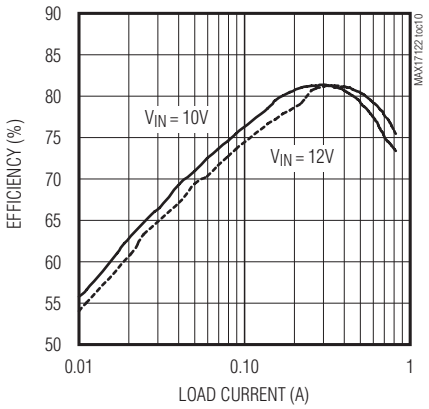
STEP-UP REGULATOR STARTUP SEQUENCE



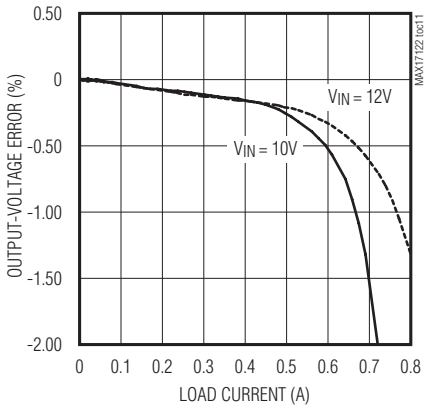
STEP-UP REGULATOR PEAK INDUCTOR CURRENT AT CURRENT LIMIT vs. INPUT VOLTAGE



BOOST-BUCK REGULATOR EFFICIENCY vs. LOAD CURRENT



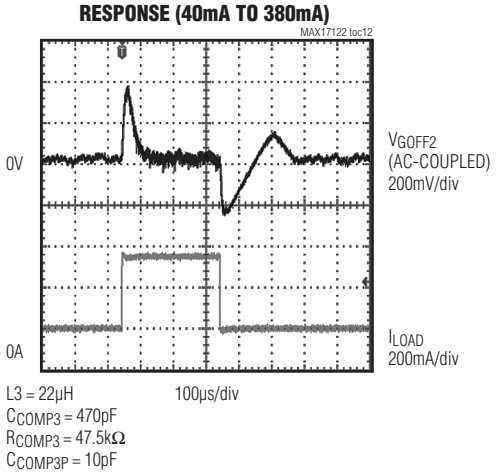
BOOST-BUCK REGULATOR NORMALIZED OUTPUT VOLTAGE vs. LOAD CURRENT



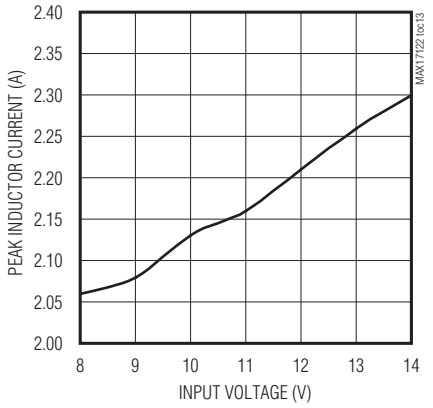
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

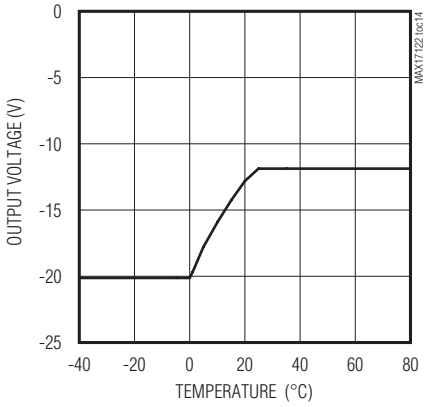
BOOST-BUCK REGULATOR LOAD-TRANSIENT RESPONSE (40mA TO 380mA)



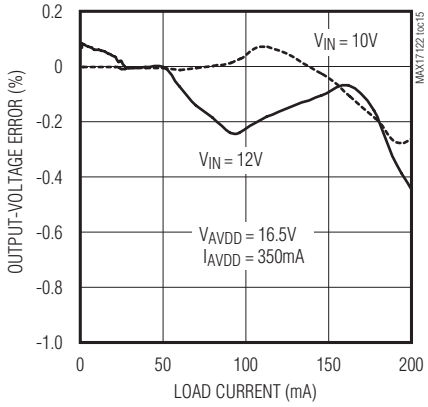
BOOST-BUCK REGULATOR PEAK INDUCTOR CURRENT AT CURRENT LIMIT vs. INPUT VOLTAGE



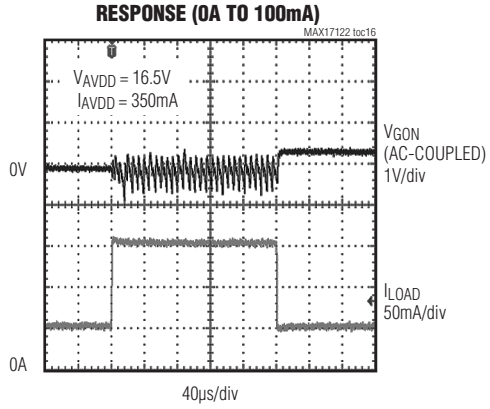
BOOST-BUCK REGULATOR OUTPUT TEMPERATURE COMPENSATION



POSITIVE CHARGE-PUMP REGULATOR NORMALIZED LOAD REGULATION



POSITIVE CHARGE-PUMP REGULATOR LOAD-TRANSIENT RESPONSE (0A TO 100mA)

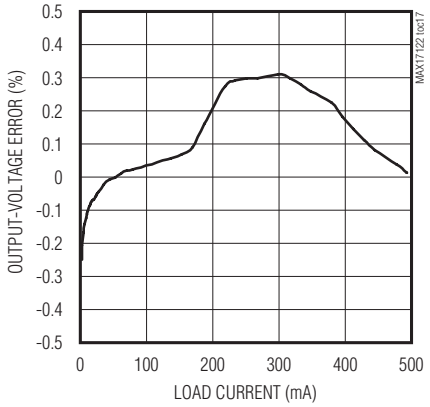


Step-Up, Step-Down Regulator, Gate-On Charge Pump, and Boost-Buck Regulator for TV TFT LCD Display

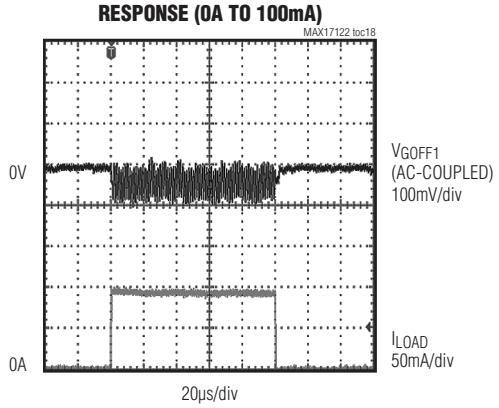
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

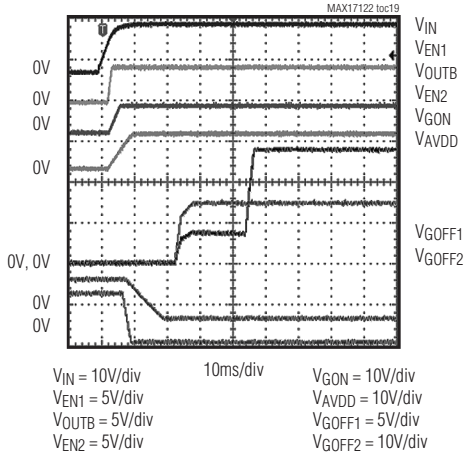
NEGATIVE LINEAR REGULATOR NORMALIZED LOAD REGULATION



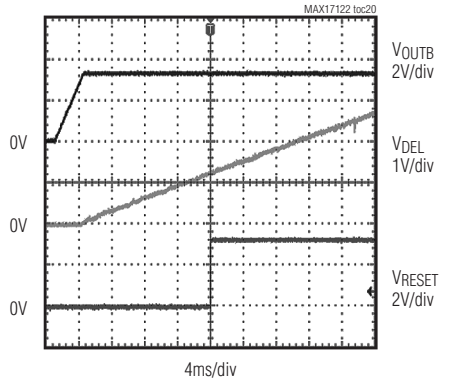
NEGATIVE LINEAR REGULATOR LOAD-TRANSIENT RESPONSE (0A TO 100mA)



POWER-UP SEQUENCE OF ALL SUPPLY OUTPUTS



RESET FUNCTION



Pin Description

PIN	NAME	FUNCTION
1	GATE	External p-Channel MOSFET Control Output. When the step-up regulator is enabled, GATE pulls down to control the step-up output during its soft-start. Once GATE is fully on, the step-up regulator begins switching to regulate the final portion of its soft-start.
2	IN	Input of the Internal 5V Linear Regulator and the Startup Circuitry. Bypass IN to AGND with 0.22µF close to the IC.
3, 4	IN2	Step-Down Regulator Power Input. Drain of the internal n-channel MOSFET connected between IN2 and LX2.
5, 24	AGND	Analog Ground
6, 7	LX2	Step-Down Regulator Switching Node. LX2 is the source of the internal n-channel MOSFET connected between IN2 and LX2. Connect the inductor and Schottky catch diode to LX2 and minimize the trace area for low EMI.
8	BST2	Step-Down Regulator Bootstrap Capacitor Connection for High-Side Gate Driver. Connect a 0.1µF ceramic capacitor from BST2 to LX2.
9	OUTB	Step-Down Regulator Output-Voltage Sense Input. Connect OUTB to the step-down regulator output.
10	FB2	Step-Down Regulator Feedback Input. Connect FB2 to AGND to select the step-down converter's 3.3V fixed mode. For adjustable mode, connect FB2 to the center of a resistive voltage-divider between the step-down regulator output and AGND to set the step-down regulator output voltage. Place the resistive voltage-divider within 5mm of FB2.
11	GPGD	GON Power-Good Signal Open-Drain Output. GPGD is connected to AGND whenever V_{FBP} is less than the V_{FBP} power-good threshold. GPGD is high impedance whenever V_{FBP} is greater than the threshold.
12	DLY1	Step-Up Regulator Delay Input. Connect a capacitor from DLY1 and AGND to set the delay time between EN2's rise and the step-up regulator's soft-start. An 8µA current source charges C_{DLY1}. DLY1 is internally pulled to AGND whenever either EN1 or EN2 is low or VL is below its UVLO threshold.
13	EN1	Step-Down Enable Input. An 8µA current source charges the capacitor at EN1. When EN1 is high, the step-down regulator begins operating.
14	EN2	Step-Up and Positive Charge-Pump Linear Regulator Enable Input. Negative linear regulator and boost-buck regulator enable input. An 8µA current source charges the capacitor at EN2. When EN2 is high, DLY1 and DLY2 begin charging. DLY1 starts GATE, which turns on the external p-channel MOSFET and the step-up regulator. DLY2 starts the positive charge-pump linear regulator. EN2 is inactive until after the step-down regulator soft-start is finished.
15	HVS	High-Voltage Stress Mode Control Input. When HVS is high, the RHVS open-drain output connects to AGND. RHVS is high impedance when HVS is low.
16	FBN	Negative Linear-Regulator Controller Feedback Input. Connect FBN to the center of a resistive voltage-divider between the negative output and a 3.3V reference to set the negative charge-pump regulator output voltage. Place the resistive voltage-divider within 5mm of FBN.

Step-Up, Step-Down Regulator, Gate-On Charge Pump, and Boost-Buck Regulator for TV TFT LCD Display

Pin Description (continued)

PIN	NAME	FUNCTION
17	SS	Step-Up Regulator Soft-Start Input. Connect a capacitor at SS to control the step-up regulator soft-start ramp time. The capacitor charge current is 10µA and the SS voltage ramps from 0 to 1.25V for a zero-to-full-scale regulated output.
18	DRVN	GOFF1 Negative Linear-Regulator Controller Base-Drive Output. Open drain of an internal p-channel MOSFET. Connect DRVN to the base of the external npn output transistor as shown in the typical operating circuit (Figure 1). The buffer can source current from ground to GOFF2 to maintain a regulated voltage on GOFF1 as measured at FBN.
19	DLY2	Positive Charge-Pump Linear-Regulator Delay Input. Connect a capacitor from DLY2 to AGND to set the delay time between the step-up regulator and the startup of the positive charge pump. An 8µA current source charges C_{DLY2}. DLY2 is internally pulled to AGND until the step-down soft-start is finished or when either EN1 or EN2 is low or VL is below its UVLO threshold.
20	FBP	Positive Charge-Pump Linear-Regulator Feedback Input. Connect FBP to the center of a resistive voltage-divider between the positive charge-pump output and AGND to set the positive charge-pump output voltage. Place the resistive voltage-divider within 5mm of FBP.
21	DRVP	Positive Charge-Pump Linear-Regulator Controller Base-Drive Output. Open drain of an internal n-channel MOSFET. Connect DRVP to the base of the external pnp transistor as shown in the typical operating circuit (Figure 1). The buffer can source current from AVDD to the charge-pump diodes to maintain a regulated voltage on GON as measured at FBP.
22	RESET	Open-Drain Power-Good Output. Monitors the step-down output voltage. RESET is connected to AGND whenever the internal feedback voltage is less than its power-good threshold and DEL is less than 1.25V. RESET is high impedance whenever the internal feedback voltage is greater than the threshold and DEL is greater than 1.25V.
23	DEL	Power-Good Reset Timing Pin. Connect a capacitor from DEL to AGND to set the step-down output-rising RESET delay. An 8µA current source charges C_{DEL}.
25	SET	GOFF2 Cold-Temperature Reference-Voltage Input. Connect a resistor from SET to AGND to set the cold-temperature GOFF2 reference level. The SET output current is 100µA (typ). Leave SET unconnected or connect to 3.3V if GOFF2 temperature compensation is not used.
26	NTC	Thermistor Network Connection Input. Connect a network including a thermistor from NTC to AGND to control the temperature behavior of the GOFF2 output voltage. If thermal compensation is not used, NTC may be left unconnected or connected to AGND.
27	FB3	GOFF2 Regulator Feedback Input. FB3 regulates at 1.65V nominal and can vary from 0.1V to 1.65V with temperature according to the voltages on SET and NTC. Connect FB3 to the center of a resistive voltage-divider between the regulator output and a 3.3V reference to set the GOFF2 regulator output voltage.
28	COMP3	Compensation Pin for the Boost-Buck Error Amplifier. Connect a series resistor and capacitor from COMP3 to AGND. Typical values are 5kΩ and 4.7nF.
29, 36	N.C.	No Connection. Not internally connected.
30	LX3	GOFF2 Boost-Buck Regulator Switching Node. LX3 is the source of the internal n-channel MOSFET connected between IN3 and LX3. Connect the inductor and Schottky catch diode to LX3 and minimize the trace area for low EMI.

Pin Description (continued)

PIN	NAME	FUNCTION
31	IN3	Boost-Buck Regulator Power Input. Drain of the internal p-channel MOSFET connected between IN3 and LX3.
32	RHVS	High-Voltage Stress Mode Output. When HVS is high, the RHVS open-drain output connects to AGND. RHVS is high impedance when HVS is low.
33	FB1	Boost Regulator Feedback Input. Connect FB1 to the center of a resistive voltage-divider between the step-up regulator output and AGND to set the step-up regulator output voltage. Place the resistive voltage-divider within 5mm of FB1.
34	COMP1	Compensation Pin for the Step-Up Error Amplifier. Connect a series resistor and capacitor from COMP1 to AGND. Typical values are 40kΩ and 330pF.
35	VL	5V Internal Linear-Regulator Output. Bypass VL to AGND with 1µF minimum. Provides power for the internal MOSFET driving circuits, the PWM controllers, charge-pump regulators, logic and references, and other analog circuitry. Provides 25mA load current when all switching regulators are enabled. VL is active whenever IN is above its UVLO threshold.
37, 38	LX1	Step-Up Regulator Switching Node. LX1 is the drain of the internal n-channel MOSFET connected between LX1 and PGND. Connect the inductor and Schottky catch diode to both LX1 pins and minimize the trace area for low EMI.
39, 40	GND1	Step-Up Regulator Power Ground. Source of the internal power n-channel MOSFET.
—	EP	Exposed Pad. Connect EP to the ground plane to maximize thermal dissipation.

Step-Up, Step-Down Regulator, Gate-On Charge Pump, and Boost-Buck Regulator for TV TFT LCD Display

Typical Operating Circuit

The typical operating circuit (Figure 1) of the MAX17122 is a complete power-supply system for TFT LCD TV panels. The circuit generates a +3.3V logic supply, a +15V source driver supply, a +28V positive gate-driver supply, and a negative gate-driver supply that is derived linearly between -7.5V and -12V. Table 1 lists some selected components and Table 2 lists the contact information of component suppliers.

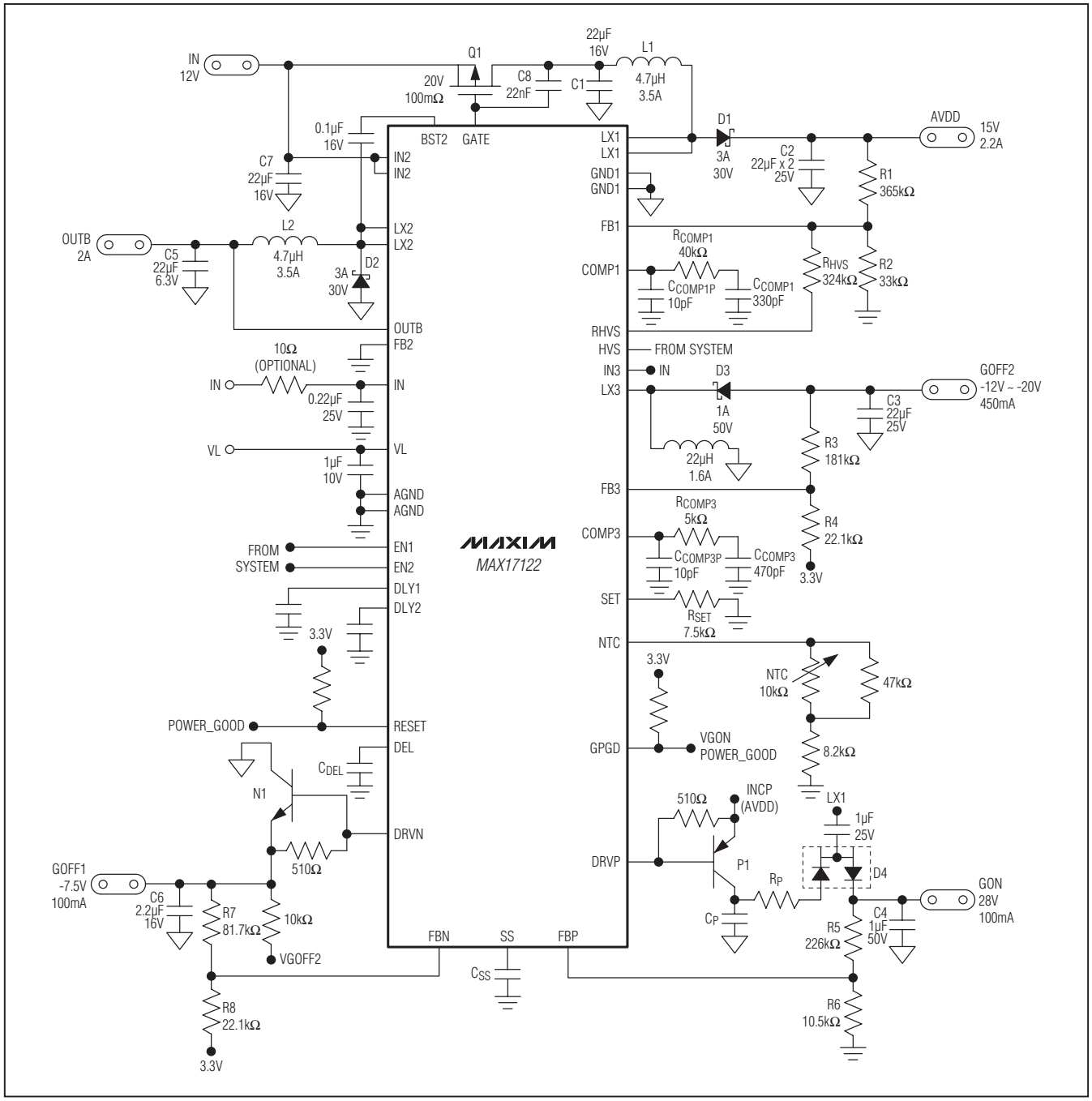


Figure 1. Typical Operating Circuit

Step-Up, Step-Down Regulator, Gate-On Charge Pump, and Boost-Buck Regulator for TV TFT LCD Display

Table 1. Component List

DESIGNATION	DESCRIPTION
C1, C7	22µF ±20%, 16V X5R ceramic capacitors (1206) Murata GRM31CR61C226M Taiyo Yuden EMK316BJ226M
C2, C3	22µF ±20%, 25V X5R ceramic capacitors (1210) Murata GRM32ER61E226K Murata GRM32ER61E226M
C4	1µF ±10%, 50V X7R ceramic capacitor (1206) Murata GRM31MR71H105KA TDK C3216X7R1H105K
C5	22µF ±20%, 6.3V X5R ceramic capacitor (0805) Murata GRM21BR60J226M TDK C2012X5R0J226K
C6	2.2µF ±10%, 16V X5R ceramic capacitor (0603) Murata GRM188R61C225K TDK C1608Y5V1C225ZT
D1, D2	Schottky diodes 30V, 3A (M Flat) Toshiba CMS02
D3	Schottky diode 50V, 1A (SMA) Fairchild SS15 Diodes Inc. B150
D4	Small-signal diode (SOT23) Fairchild BAT54S Diodes Inc. BAT54S
L1, L2	Inductors, 4.7µH, 3.5A TOKO FDV0620-4R7M Sumida CDRH6D26HPNP-4R7P NEC MPLC0730L4R7
L3	Inductor, 22µH, 1.6A Sumida CDRH8D28NP-220N
N1	High-gain, 25V npn transistor (DPAK) Fairchild KSH200 ON Semi MJD200
P1	High gain, -25V pnp transistor (DPAK) Fairchild KSH210 ON Semi MJD210
Q1	-30V, 0.056Ω p-channel MOSFET (6-pin SC70 PowerPAK) Vishay SiA421DJ

Table 2. Component Suppliers

SUPPLIER	PHONE	FAX	WEBSITE
Diodes Incorporated	805-446-4800	805-446-4850	www.diodes.com
Fairchild Semiconductor	408-822-2000	408-822-2102	www.fairchildsemi.com
Murata Electronics North America, Inc.	770-436-1300	770-436-3030	www.murata-northamerica.com
ON Semiconductor	888-743-7826	—	www.onsemi.com
Sumida Corp.	847-545-6700	847-545-6720	www.sumida.com
TDK Corp.	847-803-6100	847-390-4405	www.component.tdk.com
Toshiba America Electronic Components, Inc.	949-455-2000	949-859-3963	www.toshiba.com/taec

Detailed Description

The MAX17122 is a multiple-output power supply designed primarily for TFT LCD TV panels. It contains a step-down switching regulator to generate the supply for system logic, a step-up switching regulator to generate the supply for source-driver ICs, a linear-controlled positive charge-pump regulator to generate the supply for TFT positive gate drivers, a boost-buck regulator, and a negative linear regulator to generate the supply for TFT negative gate drivers.

Each switching regulator features adjustable output voltage, digital soft-start, and timer-delayed fault protection. They all use fixed-frequency (750kHz) current-mode control architectures. The step-up regulator switches in-phase with a boost-buck regulator while 180° out-of-phase with a step-down regulator to minimize the input ripple and noise coupling.

The boost-buck regulator also features a temperature-compensated output so it can vary according to the temperature sensed by an external NTC thermistor. The step-down regulator also features an adjustable-delay, open-drain, power-good output. A simple untimed output monitors the positive charge-pump linear regulator's feedback.

Step-Up, Step-Down Regulator, Gate-On Charge Pump, and Boost-Buck Regulator for TV TFT LCD Display

In addition, the MAX17122 features an internal 5V linear regulator, well-defined power-up and power-down sequences, and fault and thermal-overload protection. Figure 2 shows the MAX17122's functional diagram.

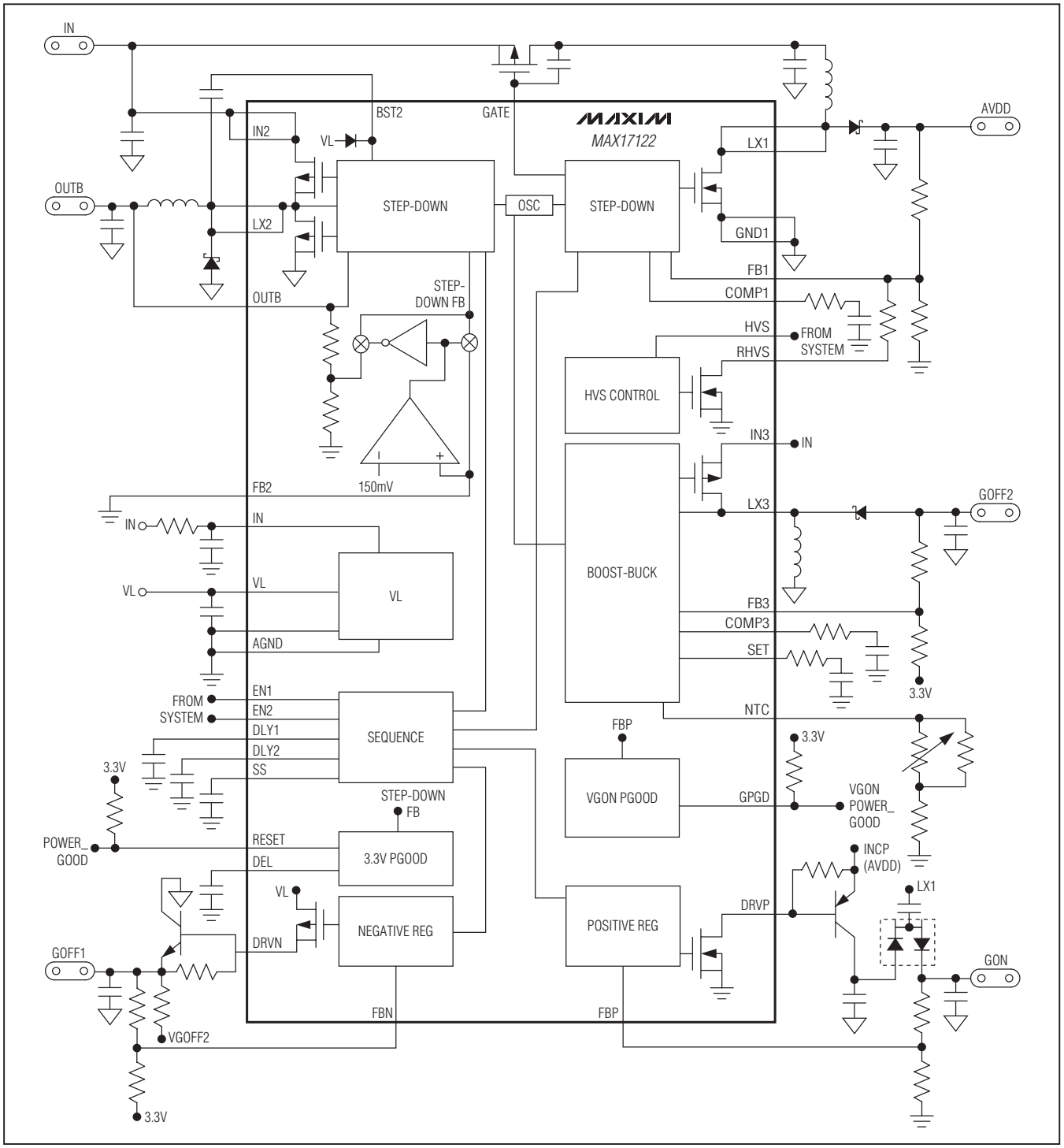


Figure 2. Functional Diagram

Step-Up, Step-Down Regulator, Gate-On Charge Pump, and Boost-Buck Regulator for TV TFT LCD Display

Step-Down Regulator

The step-down regulator consists of an internal n-channel MOSFET with gate driver, a lossless current-sense network, a current-limit comparator, and a PWM controller block. The external power stage consists of a Schottky diode rectifier, an inductor, and output capacitors. The output voltage is regulated by changing the duty cycle of the high-side MOSFET. A bootstrap circuit that uses a 0.1µF flying capacitor between LX2 and BST provides the supply voltage for the high-side gate driver. Although the MAX17122 also includes a 10Ω (typical) low-side MOSFET, this switch is used to charge the bootstrap capacitor during startup and maintains fixed-frequency operation at light load and cannot be used as a synchronous rectifier. An external Schottky diode (D2 in Figure 1) is always required.

PWM Controller Block

The heart of the PWM controller block is a multi-input, open-loop comparator that sums three signals: the output voltage signal with respect to the reference voltage, the current-sense signal, and the slope compensation signal. The PWM controller is a direct-summing type, lacking a traditional error amplifier and the phase shift associated with it. This direct-summing configuration approaches ideal cycle-by-cycle control over the output voltage.

The step-down controller always operates in fixed-frequency PWM mode. Each pulse from the oscillator sets the main PWM latch that turns on the high-side switch until the PWM comparator changes state. As the high-side switch turns off, the low-side switch turns on. The low-side switch stays on until the beginning of the next clock cycle.

Current Limiting and Lossless Current Sensing

The current-limit circuit turns off the high-side MOSFET switch whenever the voltage across the high-side MOSFET exceeds an internal threshold. The actual current limit is typically 3A.

For current-mode control, an internal lossless sense network derives a current-sense signal from the inductor DCR. The time constant of the current-sense network is not required to match the time constant of the inductor and has been chosen to provide sufficient current-ramp signal for stable operation. The current-sense signal is AC-coupled into the PWM comparator, eliminating most DC output-voltage variation with load current.

Dual-Mode Feedback

The MAX17122's step-down regulator supports both fixed output and adjustable output. Connect FB2 to AGND to enable the 3.3V fixed output voltage. Connect a resistive voltage-divider between OUTB and AGND with the center tap connected to FB2 to adjust the output voltage. Choose RB (resistance from FB2 to AGND) to be between 5kΩ and 50kΩ, and solve for RA (resistance from OUTB to FB2) using the following equation:

$$RA = RB \times \left(\frac{V_{OUTB}}{V_{FB2}} - 1 \right)$$

where V_{FB2} = 1.25V and V_{OUTB} may vary from 1.5V to 5V.

Soft-Start

The step-down regulator includes a 7-bit soft-start DAC that steps its internal reference voltage from 0 to 1.25V in 128 steps. The soft-start period is 3ms (typ) and FB2 fault detection is disabled during this period. The soft-start feature effectively limits the inrush current during startup (see the Step-Down Regulator Soft-Start Waveforms in the *Typical Operating Characteristics*).

Step-Down Regulator Power Good (RESET)

The RESET power-good block is an open-drain-type design with a capacitor-adjustable, active-low, output timing. The block monitors the step-down regulator feedback node (FB2 in variable mode, or OUTB after divider in fixed mode) with a 1.0V threshold. The threshold has a 12mV (typ) hysteresis. RESET goes low when the monitored voltage is below the threshold. When the feedback node voltage rises above the 1.0V threshold, DEL starts to charge the capacitor connected there. RESET stays low until V_{DEL} exceeds 1.25V.

Step-Up Regulator

The step-up regulator employs a current-mode, fixed-frequency PWM architecture to maximize loop bandwidth and provide fast-transient response to pulsed loads typical of TFT LCD panel source drivers. The integrated MOSFET and the built-in digital soft-start function reduce the number of external components required while controlling inrush currents. The output voltage can be set from V_{IN} to 20V with an external resistive voltage-divider. (**Note:** If the HVS function is used, AVDD cannot be set to this maximum value under normal operating conditions.) The regulator controls the output voltage and the power delivered to the output by modulating duty cycle D_{SU} of the internal power MOSFET in each switching cycle. The duty cycle of the MOSFET is approximated by:

$$D_{SU} \approx \frac{V_{AVDD} + V_{D1} - V_{IN}}{V_{AVDD} + V_{D1} - V_{LX1}}$$

Step-Up, Step-Down Regulator, Gate-On Charge Pump, and Boost-Buck Regulator for TV TFT LCD Display

where V_{AVDD} is the output voltage of the step-up regulator, V_{D1} is the voltage drop across diode D1, and V_{LX1} is the voltage drop across the internal MOSFET. Figure 3 shows the step-up regulator block diagram.

PWM Controller Block

An error amplifier compares the signal at FB1 to 1.25V and changes the COMP1 output. The voltage at COMP1 sets the peak inductor current. As the load varies, the error amplifier sources or sinks current to the COMP1 output accordingly to produce the inductor peak current necessary to service the load. To maintain stability at high duty cycles, a slope-compensation signal is summed with the current-sense signal.

On the rising edge of the internal clock, the controller sets a flip-flop, turning on the n-channel MOSFET and applying the input voltage across the inductor. The current through the inductor ramps up linearly, storing energy in its magnetic field. Once the sum of the current-feedback signal and the slope-compensation exceed the COMP1 voltage, the controller resets the flip-flop and turns off the MOSFET. Since the inductor current is continuous, a transverse potential develops across the inductor that turns on diode D1. The voltage across the inductor then becomes the difference between the output voltage and the input voltage. This discharge condition forces the current through the inductor to ramp back down, transferring the energy stored in the magnetic field to the output capacitor and the load. The MOSFET remains off for the rest of the clock cycle.

Step-Up Regulator External pMOS Pass Switch

As shown in Figure 1, a series external p-channel MOSFET (Q1) can be installed between the power supply and inductor L1. This feature is used to sequence power to AVDD after the MAX17122 has proceeded through normal startup to limit input surge current during the output capacitor initial charge, and to provide true shutdown when the step-up regulator is disabled. When EN2 is low, GATE is internally pulled up to IN2 through a 25Ω resistor. Once EN2 is high and the step-down regulator soft-start is finished, DLY1 begins charging. Once DLY1 is above 1.25V, the GATE starts pulling down with a 160µA (typ) internal current source. The step-up regulator is enabled and initiates a soft-start routine. When the gate-source voltage of this external pMOS exceeds approximately 3V, a boost current of 1mA is added to quickly complete the charge of GATE capacitance. The external p-channel MOSFET (Q1) turns on and connects IN2 to step-up regulator power inductor L1 when GATE falls below the turn-on threshold of the MOSFET. When V_{GATE} reaches V_{IN2} - 5.5V(GATE_OK), LX1 is allowed to toggle.

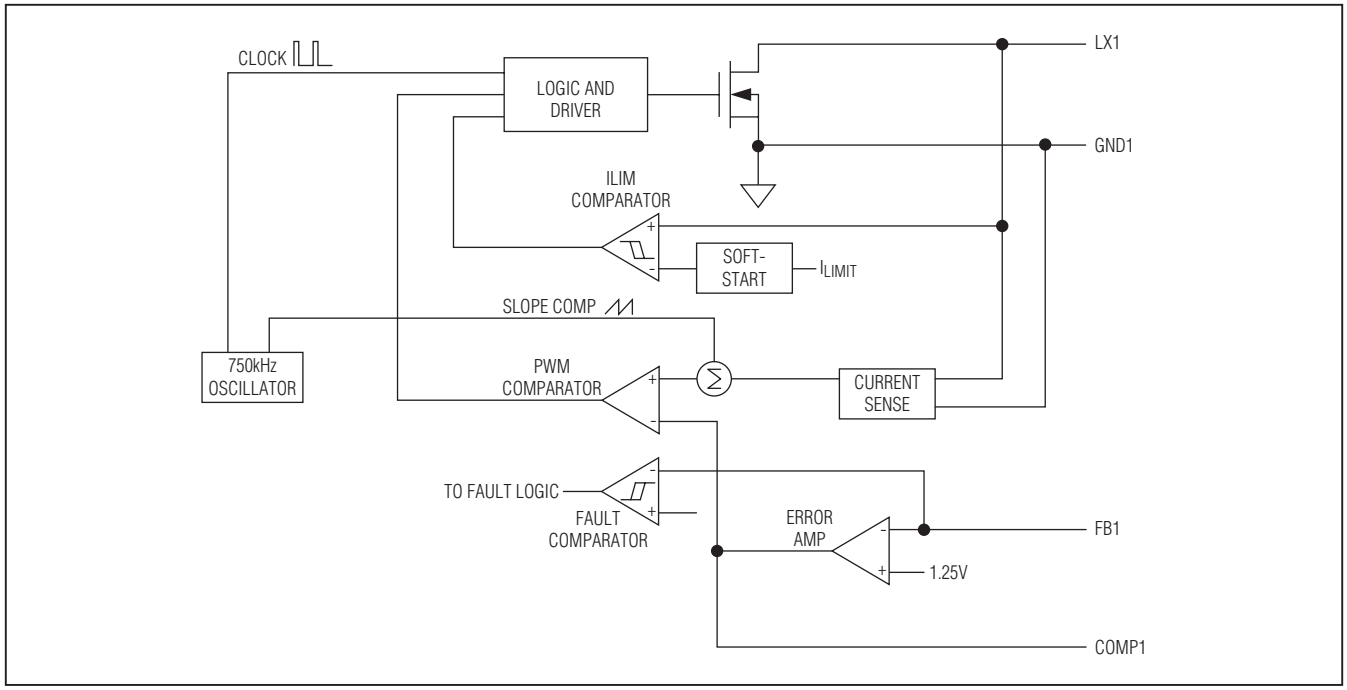


Figure 3. Step-Up Regulator Block Diagram

Since this is an open-loop control, gate-drain capacitor, C8 is always required to reduce the inrush current during startup; 22nF is suitable for this purpose.

When not using this feature, leave GATE high impedance, and connect IN2 to the step-up regulator power inductor (L1) directly.

Soft-Start

The step-up regulator achieves soft-start by linearly ramping up its internal current limit. Connect a soft-start capacitor (C_{SS}) of at least 1nF between SS and AGND. The SS pin voltage initially follows the FB1 pin voltage. Once the GATE pin voltage reaches the GATE_OK threshold (typically V_{IN} - 5.5V), C_{SS} is charged by a 10µA constant current. The soft-start terminates when the SS pin voltage reaches 1.25V. Calculate C_{SS} with the following equation:

$$C_{SS} = t_{SS} \times \frac{10\mu A}{1.25V}$$

where t_{SS} is the desired soft-start duration. The soft-start feature effectively limits the inrush current during startup (see the Step-Up Regulator Soft-Start Waveforms in the *Typical Operating Characteristics*).

Positive Charge-Pump Power Good (GPGD)

The GPGD power-good block is an open-drain type design. The block monitors the positive charge-pump feedback FBP with a 1.15V threshold. The threshold has a 125mV (typ) hysteresis. GPGD goes low when FBP is below the threshold.

Positive Charge-Pump Linear Regulator

The positive linear regulator controller is an analog gain block with an open-drain n-channel output. It drives an external pnp pass transistor (P1) with a 510Ω base-to-emitter resistor. Its guaranteed base-drive sink current is at least 10mA. The output voltage is set with an external resistive voltage-divider from the charge-pump output to AGND, with the midpoint connected to FBP. The regulator in Figure 1 uses a 1µF ceramic output capacitor and is designed to deliver 100mA at 28V. Other output voltages and currents are possible with the proper pass transistor, output capacitor, number of charge-pump stages, and the setting of the feedback divider. The positive charge-pump regulator output (V_{GON}) is typically used to generate the positive supply rail for the TFT LCD gate-driver ICs.

The regulator utilizes the step-up regulator switching node (LX1) to toggle the charge-pump flying capacitor. Therefore, to have a good output regulation, it requires LX1 to toggle with a known duty cycle. In other words, the step-up regulator needs to be working in continuous mode. The regulator achieves its loop control by limiting the current available through P1 to charge the flying capacitor (C_{FLY}). This topology eliminates the high-voltage stress on the DRVP pin. However, flying capacitor charging-current pulses could cause early termination of the step-up regulator switching pulses and cause unstable performance of the step-up regulator. A small resistor (R_P) in series with charging diode D4 can reduce the magnitude of these current pulses and prevent this behavior. The value of this small resistor is determined by the available headroom loss.

The positive linear regulator is enabled after the step-down regulator finishes its soft-start and EN2 is pulled high. Each time it is enabled, the regulator goes through a soft-start routine by ramping up its internal reference voltage from 0 to 1.25V in 128 steps. The soft-start period is 3ms (typ) and FBP fault detection is disabled during this period. The soft-start feature effectively limits the inrush current during startup.

Negative Linear Regulator

The negative linear-regulator controller is an analog gain block with an open-drain p-channel output. It drives an external npn pass transistor (N1) with a 510Ω base-to-emitter resistor. Its guaranteed base-drive source current is at least 10mA. The output voltage is set with an external resistive voltage-divider from its output to 3.3V reference with the midpoint connected to FBN. The regulator in Figure 1 uses a 1µF ceramic output capacitor and is designed to deliver 100mA at -7.5V. Other output voltages and currents are possible with the proper pass transistor, output capacitor, and the setting of the feedback divider. The negative linear-regulator output (GOFF1) is typically used to linearly derive a negative gate-driver supply between the boost-buck regulator's output GOFF2 and ground.

The negative linear regulator is enabled after the step-down regulator finishes its soft-start and EN2 is pulled high.

Step-Up, Step-Down Regulator, Gate-On Charge Pump, and Boost-Buck Regulator for TV TFT LCD Display

Temperature-Compensated Boost-Buck Regulator

The boost-buck regulator employs a current-mode, fixed-frequency PWM architecture to maximize loop bandwidth and provide fast-transient response to pulsed loads typical of TFT LCD panel source drivers. The integrated MOSFET and the built-in digital soft-start function reduce the number of external components required while controlling inrush currents. The maximum negative output voltage can be set to -36V relative to V_{IN3} with an external resistive voltage-divider. The regulator controls the output voltage and the power delivered to the output by modulating duty cycle D of the internal power MOSFET in each switching cycle. The duty cycle of the MOSFET is approximated by:

$$D_{BB} \approx \frac{-V_{GOFF2} + V_{D3}}{V_{IN3} + V_{D3} - V_{GOFF2} - V_{LX3}}$$

where V_{GOFF2} is the output voltage of the boost-buck regulator, V_{D3} is the voltage drop across diode D3, and V_{LX3} is the voltage drop across the internal MOSFET.

PWM Control Block

An error amplifier compares the signal at FB3 to a reference voltage, which is determined by temperature-compensation logic, and changes the COMP3 output. The voltage at COMP3 sets the peak inductor current. As the load varies, the error amplifier sources or sinks current to the COMP3 output accordingly to produce the inductor peak current necessary to service the load. To maintain stability at high duty cycles, a slope-compensation signal is summed with the current-sense signal.

On the rising edge of the internal clock, the controller sets a flip-flop, turning on the p-channel MOSFET and applying the input voltage across the inductor. The current through the inductor ramps up linearly, storing energy in its magnetic field. Once the sum of the current-feedback signal and the slope compensation exceed the COMP3 voltage, the controller resets the flip-flop and turns off the MOSFET. Since the inductor current is continuous, a transverse potential develops across the inductor that turns on diode D3. The voltage across the inductor then becomes the negative output voltage. This discharge condition forces the current through the inductor to ramp back down, transferring the energy stored in the magnetic field to the output capacitor and the load. The MOSFET remains off for the rest of the clock cycle.

Temperature Compensation

The GOFF2 boost-buck regulator output varies with temperature to compensate for lower TFT mobility at cold temperatures. The output voltage is typically -12V at +25°C and warmer, and -20V at 0°C and colder, with a gradual change between +25°C and 0°C.

The circuit involves two constant voltages and one temperature-dependent voltage. The first constant voltage is internally fixed at half of 3.3V (1.65V). The other constant voltage should be less than 1.65V and is chosen by connecting resistor R_{SET} from the 100µA current source at the SET pin to AGND. The temperature-dependent voltage is developed by the network attached to the 100µA current source at the NTC pin. The NTC voltage is subtracted from the 3.3V reference to provide the variable voltage with the correct temperature slope.

If the differential voltage between the 3.3V reference and the NTC pin is greater than 1.65V, then the 1.65V voltage is used as the reference for the error amplifier at FB3. This sets the warm-range output of the boost-buck regulator. If the differential voltage between 3.3V reference and the NTC pin is less than the voltage at the SET pin, then the SET pin voltage is used as the reference for the error amplifier at FB3. This sets the cool-range output of the boost-buck regulator. If neither is true, then the differential voltage itself is used as the reference for the error amplifier at FB3.

These conditions are mutually exclusive as long as the SET pin voltage is less than 1.65V. If the SET pin voltage is greater than 1.65V, which would be true if SET was left open, then 1.65V is used as the reference for the error amplifier at FB3 regardless of the differential voltage between 3.3V reference and the NTC pin. This ensures a defined behavior of operation and provides a “disable” mode for the function. The minimum voltage on SET is 0.1V.

The thermistor network and resistor on SET can be adjusted to program almost any temperature variation desired, limited to two output levels with a smooth transition between. Figure 4 shows the block diagram of the temperature-compensation function and Figure 5 shows the reference voltages and output voltage behavior for the typical application components.

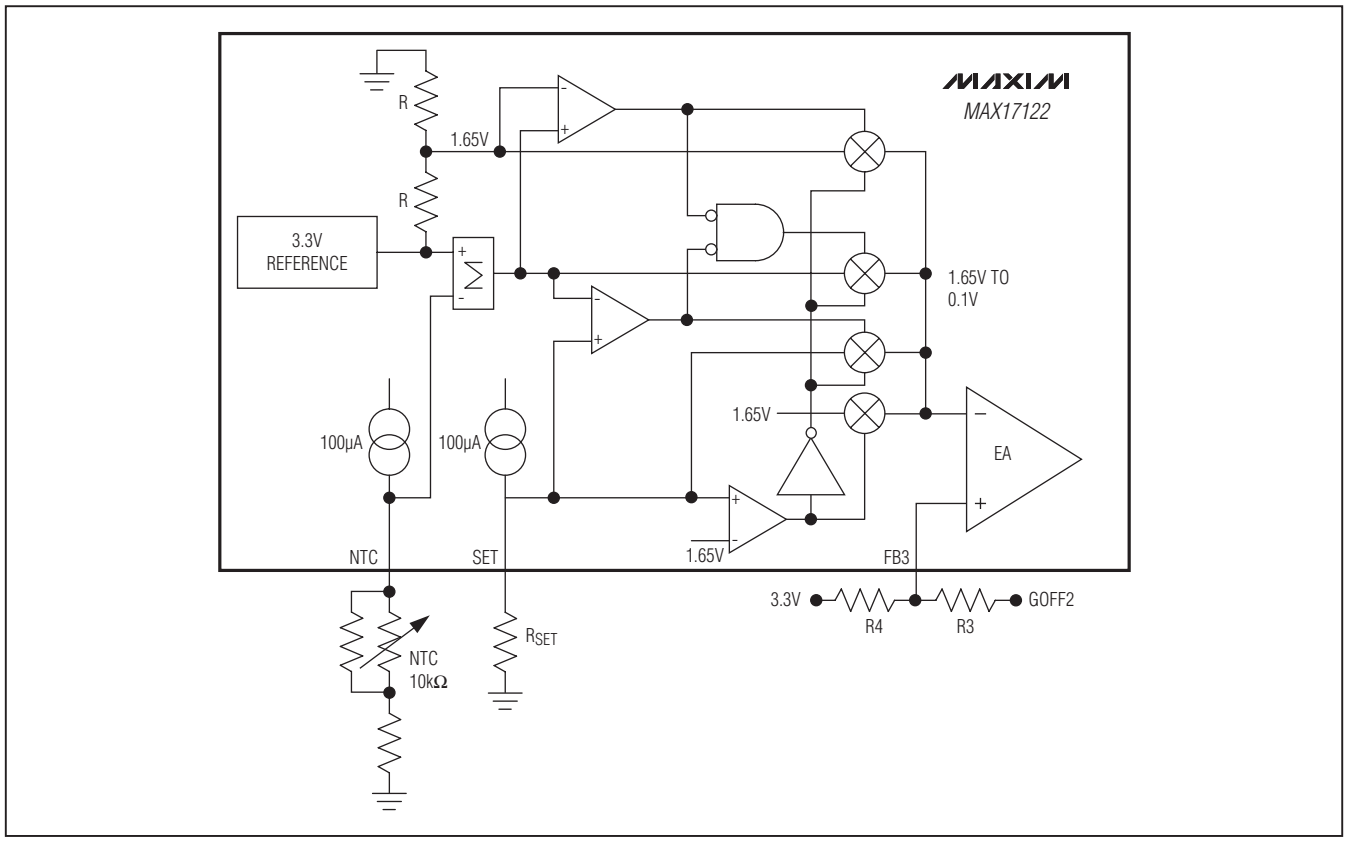


Figure 4. Switching Frequency vs. R_{FOSC}

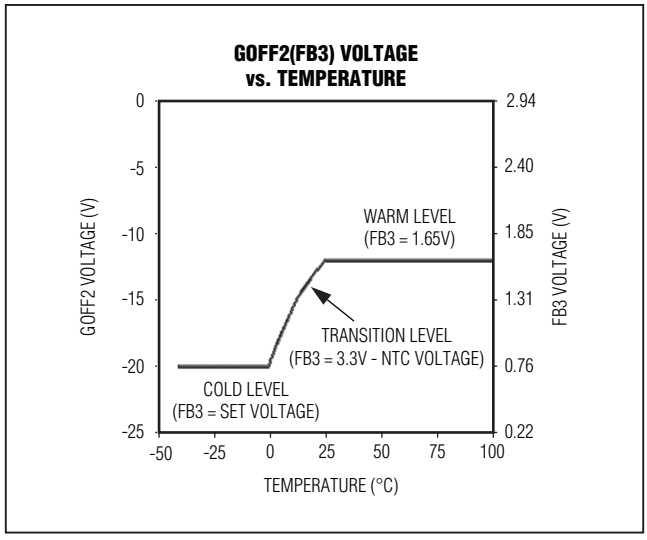


Figure 5. Compensation Network

Soft-Start

The boost-buck regulator includes a 7-bit soft-start DAC that steps its internal reference voltage from 3.3V to the reference voltage determined by temperature-compensation logic in 128 steps. The soft-start period is 3ms (typ) and FB3 fault detection is disabled during this period. The soft-start feature effectively limits the inrush current during startup (see the Boost-Buck Regulator Soft-Start Waveforms in the *Typical Operating Characteristics*).

Linear Regulator (VL)

The MAX17122 includes an internal linear regulator. IN is the input of the linear regulator. The input voltage range is between 8V and 16.5V. The output voltage is set to 5V. The regulator powers the internal MOSFET drivers, PWM controllers, charge-pump regulators, and logic circuitry. The total external load capability is 25mA. Bypass VL to AGND with a minimum 1µF ceramic capacitor.

Step-Up, Step-Down Regulator, Gate-On Charge Pump, and Boost-Buck Regulator for TV TFT LCD Display

Power-Up Sequence

The step-down regulator starts up when the MAX17122's internal linear-regulator output VL is above its undervoltage lockout (UVLO) threshold and EN1 is high. Figure 6 shows the power-up sequence. Once the step-down regulator soft-start is done, the FB2 fault-detection circuit is enabled. The step-down regulator power-good timing control signal (DEL) is enabled after OUTB is above its designed threshold (see the *Step-Down Regulator Power Good (RESET)* section). Once DEL passes above 1.25V, RESET is passively pulled up high through a resistor. Set the delay time using the following equation:

$$C_{DEL} = DELAY_TIME \times \frac{8\mu A}{1.25V}$$

The negative linear regulator and the boost-buck regulator are enabled after the step-down regulator finishes its soft-start and EN2 is high. In the same time, both of the delay control signals (DLY1 and DLY2) for the step-up regulator and the positive charge-pump linear regulator are also enabled.

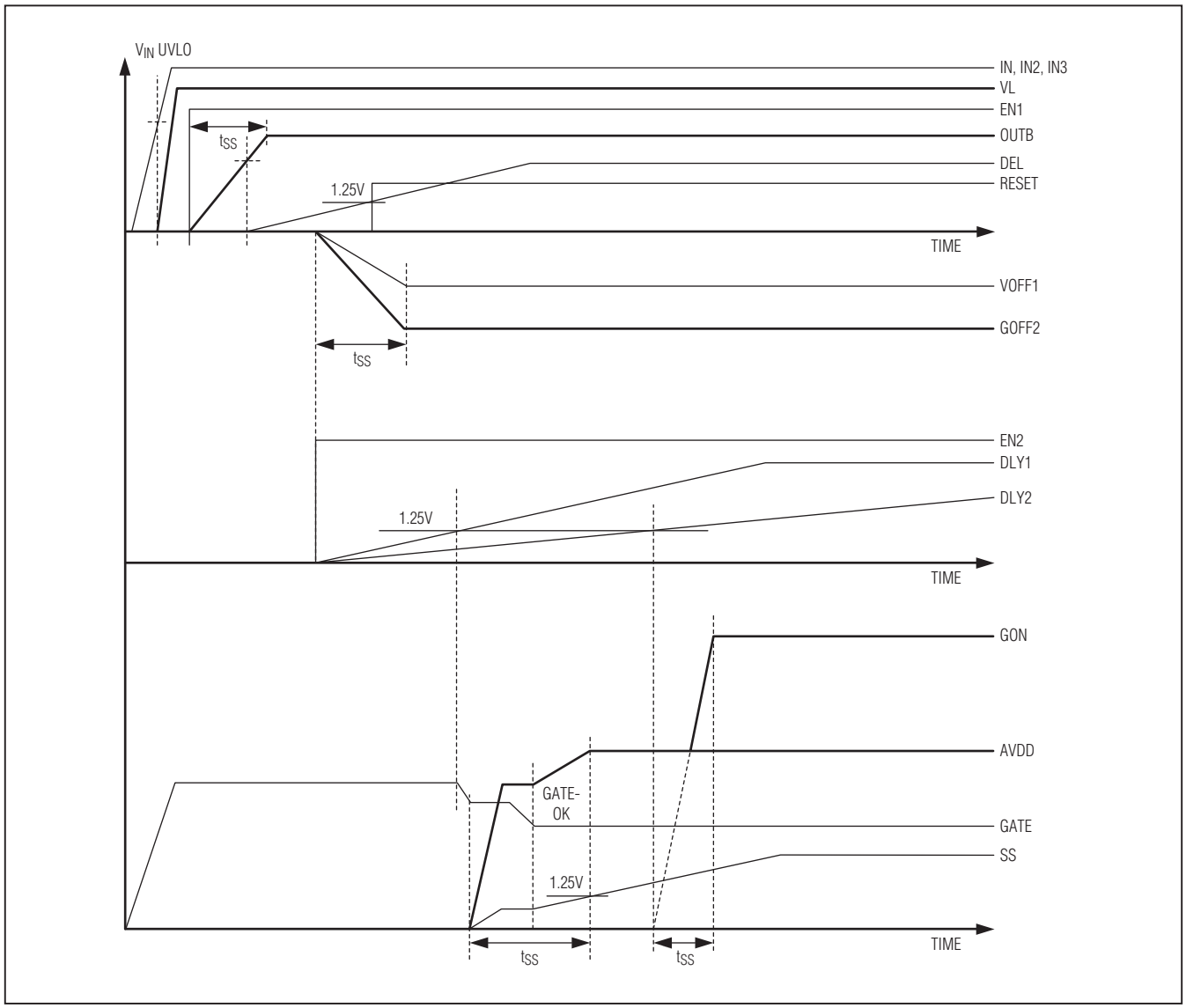


Figure 6. Power-Up Sequence

GATE is resistively pulled up towards IN2 during initial startup. Once DLY1 passes above 1.25V, a 160µA current source starts to pull down on GATE, turning on external pMOS switch Q1 and enabling the step-up regulator. When V_{GATE} reaches its GATE_OK threshold (V_{IN} - 5.5V), the step-up regulator switch is allowed to toggle. A 10µA current source charges the SS capacitor pin and when the SS voltage reaches 1.25V, soft-start is done. The FB1 fault-detection circuit is enabled after the step-up regulator finishes its soft-start.

The positive charge-pump linear regulator is enabled after the step-up regulator finishes its soft-start and DLY2 is above 1.25V. The FBP fault-detection circuit is enabled after the positive linear regulator finishes its soft-start.

Fault Protection

During steady-state operation, if any of the five regulators' output (step-down regulator, step-up regulator, positive linear regulator, boost-buck regulator, and gate-off linear regulator) goes lower than its respective fault-detection threshold, the MAX17122 activates an internal fault timer. If any condition, or the combination of conditions, indicates a continuous fault for the fault-timer duration (50ms typ), the MAX17122 shuts down temporarily for approximately 160ms (typ) and then restarts. During restart, if any output voltage is below its fault threshold at the end of its soft-start period, the IC immediately shuts down again. This feature is only active after a fault shutdown has occurred. It does not apply to the initial startup, where the 50ms timer always applies. Once all outputs have started properly after a restart, the 50ms fault timer is reenabled. The IC restarts indefinitely for a continuous fault condition and never shuts down permanently or waits for power cycling.

If a short to ground occurs on the step-down regulator, step-up regulator, positive linear regulator, or boost-buck regulator, no fault timer is applied and the IC immediately shuts down. No harm occurs if the gate-off linear regulator is shorted to ground, so this feature is omitted for that output.

Thermal-Overload Protection

The thermal-overload protection prevents excessive power dissipation from overheating the MAX17122. When the junction temperature exceeds T_J = +160°C, a thermal sensor immediately activates the fault protection, which shuts down all the outputs. Cycle the input voltage to clear the fault latch and restart the MAX17122.

The thermal-overload protection protects the controller in the event of fault conditions. For continuous operation, do not exceed the absolute maximum junction temperature rating of T_J = +150°C.

Design Procedure

Step-Down Regulator

Inductor Selection

Three key inductor parameters must be specified: inductance value (L), peak current (I_{PEAK}), and DC resistance (R_{DC}). The following equation includes a constant (LIR), which is the ratio of peak-to-peak inductor ripple current to DC load current. A higher LIR value allows smaller inductance, but results in higher losses and higher ripple. A good compromise between size and losses is typically found at a 30% ripple-current-to-load-current ratio (LIR = 0.3), which corresponds to a peak inductor current 1.15 times the DC load current:

$$L_2 = \frac{V_{OUTB} \times (V_{IN2} - V_{OUTB})}{V_{IN2} \times f_{SW} \times I_{OUTB(MAX)} \times LIR}$$

where $I_{OUTB(MAX)}$ is the maximum DC load current, and the switching frequency (f_{SW}) is 750kHz. The exact inductor value is not critical and can be adjusted to make trade-offs among size, cost, and efficiency. Lower inductor values minimize size and cost, but they also increase the output ripple and reduce the efficiency due to higher peak currents. On the other hand, higher inductor values increase efficiency, but at some point resistive losses due to extra turns of wire will exceed the benefit gained from lower AC current levels.

The inductor's saturation current must exceed the peak inductor current. The peak current can be calculated by:

$$I_{OUTB_RIPPLE} = \frac{V_{OUTB} \times (V_{IN2} - V_{OUTB})}{f_{SW} \times L_2 \times V_{IN2}}$$

$$I_{OUTB_PEAK} = I_{OUTB(MAX)} + \frac{I_{OUTB_RIPPLE}}{2}$$

The inductor's DC resistance should be low for good efficiency. Find a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. Ferrite cores are often the best choice. Shielded-core geometries help keep noise, EMI, and switching waveform jitter low.

Step-Up, Step-Down Regulator, Gate-On Charge Pump, and Boost-Buck Regulator for TV TFT LCD Display

Considering the typical operating circuit in Figure 1, the maximum load current $I_{OUT(MAX)}$ is 2.0A with a 3.3V output and a 12V (typ) input voltage. Choosing an LIR of 0.4 at this operation point:

$$L2 = \frac{3.3V \times (12V - 3.3V)}{12V \times 750kHz \times 2A \times 0.3} \approx 5.3\mu H$$

Pick L2 = 4.7µH. At that operation point, both the ripple current and peak current are:

$$I_{OUTB_RIPPLE} = \frac{3.3V \times (12V - 3.3V)}{750kHz \times 4.7\mu H \times 12V} = 0.68A$$

$$I_{OUTB_PEAK} = 2A + \frac{0.68A}{2} = 2.34A$$

Input Capacitors

The input filter capacitors reduce peak currents drawn from the power source and reduce noise and voltage ripple on the input caused by the regulator's switching. They are usually selected according to input ripple-current requirements and voltage rating, rather than capacitance value. The input voltage and load current determine the RMS input ripple current (I_{RMS}):

$$I_{RMS} = I_{OUTB} \times \frac{\sqrt{V_{OUTB} \times (V_{IN2} - V_{OUTB})}}{V_{IN2}}$$

The worst case is $I_{RMS} = 0.5 \times I_{OUTB}$, which occurs at $V_{IN2} = 2 \times V_{OUT}$.

For most applications, ceramic capacitors are used because of their high-ripple-current and surge-current capabilities. For optimal circuit long-term reliability, choose an input capacitor that exhibits less than +10°C temperature rise at the RMS input current corresponding to the maximum load current.

Output Capacitor Selection

Since the MAX17122's step-down regulator is internally compensated, it is stable with any reasonable amount of output capacitance. However, the actual capacitance and ESR affect the regulator's output-voltage ripple and transient response. The rest of this section deals with how to determine the output capacitance and ESR needs according to the ripple voltage and load-transient requirements.

The output-voltage ripple has two components: variations in the charge stored in the output capacitor, and the voltage drop across the capacitor's ESR caused by the current into and out of the capacitor:

$$V_{OUTB_RIPPLE} = V_{OUTB_RIPPLE(ESR)} + V_{OUTB_RIPPLE(C)}$$

$$V_{OUTB_RIPPLE(ESR)} = I_{OUTB_RIPPLE} \times R_{ESR_OUTB}$$

$$V_{OUTB_RIPPLE(C)} = \frac{I_{OUTB_RIPPLE}}{8 \times C_{OUTB} \times f_{SW}}$$

where I_{OUTB_RIPPLE} is defined in the *Step-Down Regulator* and *Inductor Selection* sections, C_{OUTB} (C5 in Figure 1) is the output capacitance, and R_{ESR_OUTB} is the ESR of output capacitor C_{OUT}. In Figure 1's circuit, the inductor ripple current is 0.68A. If the voltage-ripple requirement of Figure 1's circuit is ±1% of the 3.3V output, then the total peak-to-peak ripple voltage should be less than 66mV. Assuming that the ESR ripple and the capacitive ripple each should be less than 50% of the total peak-to-peak ripple, then the ESR should be less than 48.5mΩ and the output capacitance should be greater than 3.4µF to meet the total ripple requirement. A 22µF capacitor with ESR (including PCB trace resistance) of 10mΩ is selected for the typical operating circuit in Figure 1, which easily meets the voltage-ripple requirement.

The step-down regulator's output capacitor and ESR also affect the voltage undershoot and overshoot when the load steps up and down abruptly. The undershoot and overshoot also have two components: the voltage steps caused by ESR and voltage sag, and soar due to the finite capacitance and inductor slew rate. Use the following formulas to check if the ESR is low enough and the output capacitance is large enough to prevent excessive soar and sag.

The amplitude of the ESR step is a function of the load step and the ESR of the output capacitor:

$$V_{OUTB_ESR_STEP} = \Delta I_{OUTB} \times R_{ESR_OUTB}$$

The amplitude of the capacitive sag is a function of the load step, the output capacitor value, the inductor value, the input-to-output voltage differential, and the maximum duty cycle:

$$V_{OUTB_SAG} = \frac{L_2 \times (\Delta I_{OUTB})^2}{2 \times C_{OUTB} \times (V_{IN2(MIN)} \times D_{MAX} - V_{OUTB})}$$

The amplitude of the capacitive soar is a function of the load step, the output capacitor value, the inductor value, and the output voltage:

$$V_{OUTB_SOAR} = \frac{L_2 \times (\Delta I_{OUTB})^2}{2 \times C_{OUTB} \times V_{OUTB}}$$

Given the component values in the circuit of Figure 1, during a full 2A step load transient, the voltage step due to capacitor ESR is negligible. The voltage sag and soar are 138mV and 129mV, respectively.

Rectifier Diode

The MAX17122's high switching frequency demands a high-speed rectifier. Schottky diodes are recommended for most applications because of their fast recovery time and low forward voltage. In general, a 3A Schottky diode works well in the MAX17122's step-down regulator.

Step-Up Regulator

Inductor Selection

The inductance value, peak current rating, and series resistance are factors to consider when selecting the inductor. These factors influence the converter's efficiency, maximum output-load capability, transient-response time, and output-voltage ripple. Physical size and cost are also important factors to be considered.

The maximum output current, input voltage, output voltage, and switching frequency determine the inductor value. Very high inductance values minimize the current ripple and therefore reduce the peak current, which decreases core losses in the inductor and I^2R losses in the entire power path. However, large inductor values also require more energy storage and more turns of wire, which increase physical size and can increase I^2R losses in the inductor. Low inductance values decrease the physical size but increase the current ripple and peak current. Finding the best inductor involves choosing the best compromise between circuit efficiency, inductor size, and cost.

The equations used here include a constant (LIR), which is the ratio of the inductor peak-to-peak ripple current to the average DC inductor current at the full load current. The best trade-off between inductor size and circuit efficiency for step-up regulators generally has an LIR between 0.3 and 0.5. However, depending on the AC characteristics of the inductor core material and ratio of inductor resistance to other power-path resistances, the best LIR can shift up or down. If the inductor resistance is relatively high, more ripple can be accepted to reduce the number of turns required and increase the wire diameter. If the inductor resistance is relatively low, increasing inductance to lower the peak current can decrease losses throughout the power path. If extremely thin high-resistance inductors are used, as is common for LCD panel applications, the best LIR can increase to between 0.5 and 1.0.

Once a physical inductor is chosen, higher and lower values of the inductor should be evaluated for efficiency improvements in typical operating regions.

Calculate the approximate inductor value using the typical input voltage (V_{IN}), the maximum output current ($I_{AVDD(MAX)}$), the expected efficiency (η_{TYP}) taken from an appropriate curve in the *Typical Operating Characteristics*, and an estimate of LIR based on the above discussion:

$$L_1 = \left(\frac{V_{IN}}{V_{AVDD}}\right)^2 \left(\frac{V_{AVDD} - V_{IN}}{I_{AVDD(MAX)} \times f_{SW}}\right)\left(\frac{\eta_{TYP}}{LIR}\right)$$

Choose an available inductor value from an appropriate inductor family. Calculate the maximum DC input current at the minimum input voltage $V_{IN(MIN)}$ using conservation of energy and the expected efficiency at that operating point (η_{MIN}) taken from an appropriate curve in the *Typical Operating Characteristics*:

$$I_{IN(DC,MAX)} = \frac{I_{AVDD(MAX)} \times V_{AVDD}}{V_{IN(MIN)} \times \eta_{MIN}}$$

Calculate the ripple current at that operating point and the peak current required for the inductor:

$$I_{AVDD_RIPPLE} = \frac{V_{IN(MIN)} \times \left(V_{AVDD} - V_{IN(MIN)}\right)}{L_{AVDD} \times V_{AVDD} \times f_{SW}}$$

$$I_{AVDD_PEAK} = I_{IN(DC,MAX)} + \frac{I_{AVDD_RIPPLE}}{2}$$

The inductor's saturation current rating and the MAX17122's LX1 current limit should exceed I_{AVDD_PEAK} and the inductor's DC current rating should exceed $I_{IN(DC,MAX)}$. For good efficiency, choose an inductor with less than 0.1Ω series resistance.

Considering the typical operating circuit in Figure 1, the maximum load current ($I_{AVDD(MAX)}$) is 2.2A with a 15V output and a typical input voltage of 12V. Choosing an LIR of 0.3 and estimating efficiency of 90% at this operating point:

$$L_1 = \left(\frac{12V}{15V}\right)^2 \left(\frac{15V - 12V}{2.2A \times 750kHz}\right)\left(\frac{90\%}{0.3}\right) = 3.49\mu H$$

Step-Up, Step-Down Regulator, Gate-On Charge Pump, and Boost-Buck Regulator for TV TFT LCD Display

Using the circuit's minimum input voltage under normal operation (12V) and estimating efficiency of 85% at that operating point:

$$I_{IN(DC,MAX)} = \frac{2.2A \times 15V}{12V \times 85\%} \approx 3.235A$$

The ripple current and the peak current are:

$$I_{AVDD_RIPPLE} = \frac{12V \times (15V - 12V)}{4.7\mu H \times 15V \times 750kHz} \approx 0.68A$$

$$I_{AVDD_PEAK} = 3.235A + \frac{0.68A}{2} \approx 3.575A$$

Output Capacitor Selection

The total output-voltage ripple has two components: the capacitive ripple caused by the charging and discharging of the output capacitance, and the ohmic ripple due to the capacitor's ESR:

$$V_{AVDD_RIPPLE} = V_{AVDD_RIPPLE(C)} + V_{AVDD_RIPPLE(ESR)}$$

$$V_{AVDD_RIPPLE(C)} \approx \frac{I_{AVDD}}{C_{AVDD}}\left(\frac{V_{AVDD} - V_{IN}}{V_{AVDD} f_{SW}}\right)$$

and:

$$V_{AVDD_RIPPLE(ESR)} \approx I_{AVDD_PEAK} R_{ESR_AVDD}$$

where I_{AVDD_PEAK} is the peak inductor current (see the *Inductor Selection* section). For ceramic capacitors, the output voltage ripple is typically dominated by $V_{AVDD_RIPPLE(C)}$. The voltage rating and temperature characteristics of the output capacitor must also be considered. Note that all ceramic capacitors typically have large temperature coefficient and bias voltage coefficients. The actual capacitor value in circuit is typically significantly less than the stated value.

Input Capacitor Selection

The input capacitor reduces the current peaks drawn from the input supply and reduces noise injection into the IC. A 22µF ceramic capacitor is used in the typical operating circuit (Figure 1) because of the high source impedance seen in typical lab setups. Actual applications usually have much lower source impedance since the step-up regulator often runs directly from the output of another regulated supply. Typically, the input capacitance can be reduced below the values used in the typical operating circuit.

Rectifier Diode

The MAX17122's high switching frequency demands a high-speed rectifier. Schottky diodes are recommended for most applications because of their fast recovery time and low forward voltage. In general, a 3A Schottky diode complements the internal MOSFET well.

Output Voltage Selection

The output voltage of the step-up regulator can be adjusted by connecting a resistive voltage-divider from the output (V_{AVDD}) to AGND with the center tap connected to FB1 (see Figure 1). Select R2 in the 10kΩ to 50kΩ range. Calculate R1 with the following equation:

$$R1 = R2 \times \left(\frac{V_{AVDD}}{V_{FB1}} - 1\right)$$

where V_{FB1}, the step-up regulator's feedback set point, is 1.25V. Place R1 and R2 close to the IC.

HVS Function

When HVS exceeds its logic-high threshold, R_{HVS} connects to AGND, effectively placing R_{HVS} in parallel with the low-side resistor-divider (R2) and regulates V_{AVDD} to a higher voltage $V_{AVDD(HIGH)}$. Connect the HVS pin to ground to disable this function. Calculate R_{HVS} with the following equation:

$$R_{HVS} = \frac{R1 \times R2}{R2\left(\frac{V_{AVDD(HIGH)}}{V_{FB1}} - 1\right) - R1}$$

Loop Compensation

Choose R_{COMP1} to set the high-frequency integrator gain for fast-transient response. Choose C_{COMP1} to set the integrator zero to maintain loop stability. Add a small capacitor (C_{P1}) from COMP1 to AGND to reduce jitter and improve stability. Usually 10pF is enough for this purpose.

For low-ESR output capacitors, use the following equations to obtain stable performance and good transient response:

$$R_{COMP1} \approx \frac{100 \times V_{IN} \times V_{AVDD} \times C_{AVDD}}{L_{AVDD} \times I_{AVDD(MAX)}}$$

$$C_{COMP1} \approx \frac{V_{AVDD} \times C_{AVDD}}{10 \times I_{AVDD(MAX)} \times R_{COMP}}$$

To further optimize transient response, vary R_{COMP1} in 20% steps and C_{COMP1} in 50% steps while observing transient-response waveforms.

Step-Up, Step-Down Regulator, Gate-On Charge Pump, and Boost-Buck Regulator for TV TFT LCD Display

Temperature-Compensated Boost-Buck Regulator

Inductor Selection

The inductance value, peak current rating, and series resistance are factors to consider when selecting the inductor. These factors influence the converter's efficiency, maximum output-load capability, transient-response time, and output-voltage ripple. Physical size and cost are also important factors to be considered.

The maximum output current, input voltage, output voltage, and switching frequency determine the inductor value. Very high inductance values minimize the current ripple and therefore reduce the peak current, which decreases core losses in the inductor and I^2R losses in the entire power path. However, large inductor values also require more energy storage and more turns of wire, which increase physical size and can increase I^2R losses in the inductor. Low inductance values decrease the physical size but increase the current ripple and peak current. Finding the best inductor involves choosing the best compromise between circuit efficiency, inductor size, and cost.

The equations used here include a constant (LIR), which is the ratio of the inductor peak-to-peak ripple current to the average DC inductor current at the full load current. The best trade-off between inductor size and circuit efficiency for step-up regulators generally has an LIR between 0.3 and 0.5. However, depending on the AC characteristics of the inductor core material and ratio of inductor resistance to other power-path resistances, the best LIR can shift up or down. If the inductor resistance is relatively high, more ripple can be accepted to reduce the number of turns required and increase the wire diameter. If the inductor resistance is relatively low, increasing inductance to lower the peak current can decrease losses throughout the power path. If extremely thin high-resistance inductors are used, as is common for LCD panel applications, the best LIR can increase to between 0.5 and 1.0.

Once a physical inductor is chosen, higher and lower values of the inductor should be evaluated for efficiency improvements in typical operating regions.

Calculate the approximate inductor value using the typical input voltage (V_{IN3}), the typical output voltage (V_{GOFF2}), the maximum output current ($I_{VOFF2(MAX)}$), the assumed efficiency (η_{TYP}) of 85%, and an estimate of LIR based on the above discussion:

$$L_3 = \frac{V_{IN3}(-V_{GOFF2})}{I_{VOFF2(MAX)} f_{SW} (V_{IN3} - V_{GOFF2})} \frac{\eta_{TYP}}{LIR}$$

Choose an available inductor value from an appropriate inductor family. Calculate the maximum DC inductor current at the minimum input voltage ($V_{IN3(MIN)}$) and cold temperature output voltage (V_{GOFF2_COLD}) using conservation of energy and the expected efficiency at that operating point (η_{MIN}) taken from an appropriate curve in the *Typical Operating Characteristics*:

$$I_{L3(DC,MAX)} = \frac{I_{GOFF2(MAX)} \times (-V_{GOFF2_COLD})}{V_{IN3(MIN)} \times \eta_{MIN}}$$

Calculate the ripple current at that operating point and the peak current required for the inductor:

$$I_{GOFF2_RIPPLE} = \frac{-V_{IN3} V_{GOFF2_COLD}}{L_3 (V_{IN3} - V_{GOFF2_COLD}) f_{SW}}$$

$$I_{GOFF2_PEAK} = I_{L3(DC,MAX)} + \frac{I_{GOFF2_RIPPLE}}{2}$$

The inductor's saturation current rating and the MAX17122's LX3 current limit should exceed I_{GOFF2_PEAK} and the inductor's DC current rating should exceed $I_{L3(DC,MAX)}$. For good efficiency, choose an inductor with less than 0.1Ω series resistance.

Considering the typical operating circuit in Figure 1, the maximum load current ($I_{GOFF2(MAX)}$) is 450mA with a -12V typical output and a typical input voltage of 12V. The estimated efficiency is 85% at this operating point. Because the inductor is large, so is the series resistance; choose an LIR of 0.5 to minimize power loss:

$$L_3 = \frac{12V \times 12V}{0.45A \times 750kHz \times (12V + 12V)} \frac{85\%}{0.5} = 30\mu H$$

A 22µH inductor is used in the typical operating circuit (Figure 1). Using the circuit's minimum input voltage (8V), cold-temperature output voltage (-20V), and estimating efficiency of 85% at that operating point:

$$I_{L3(DC,MAX)} = \frac{450mA \times 20V}{8V \times 85\%} \approx 1.32A$$

The ripple current and the peak current are:

$$I_{GOFF2_RIPPLE} = \frac{12V \times 20V}{22\mu H \times (12V + 20V) \times 750kHz} \approx 0.46A$$

$$I_{GOFF2_PEAK} = 1.32A + \frac{0.46A}{2} \approx 1.55A$$

Step-Up, Step-Down Regulator, Gate-On Charge Pump, and Boost-Buck Regulator for TV TFT LCD Display

Output Capacitor Selection

The total output-voltage ripple has two components: the capacitive ripple caused by the charging and discharging of the output capacitance, and the ohmic ripple due to the capacitor's ESR:

$$V_{GOFF2_RIPPLE} = V_{GOFF2_RIPPLE(C)} + V_{GOFF2_RIPPLE(ESR)}$$

$$V_{GOFF2_RIPPLE(C)} \approx \frac{I_{GOFF2}}{C_{GOFF2}} \times \frac{(-V_{GOFF2})}{f_{SW}(V_{IN3} - V_{GOFF2})}$$

and:

$$V_{GOFF2_RIPPLE(ESR)} \approx I_{GOFF2_PEAK} R_{ESR_AVDD}$$

where I_{GOFF2_PEAK} is the peak inductor current (see the *Inductor Selection* section). For ceramic capacitors, the output-voltage ripple is typically dominated by $V_{GOFF2_RIPPLE(C)}$. The voltage rating and temperature characteristics of the output capacitor must also be considered. Note that all ceramic capacitors typically have large temperature coefficient and bias voltage coefficients. The actual capacitor value in the circuit is typically significantly less than the stated value.

Input Capacitor Selection

The input capacitor reduces the current peaks drawn from the input supply and reduces noise injection into the IC. A 10µF ceramic capacitor is used in the typical operating circuit (Figure 1) because of the high source impedance seen in typical lab setups. Actual applications usually have much lower source impedance since the step-up regulator often runs directly from the output of another regulated supply. Typically, the input capacitance can be reduced below the values used in the typical operating circuit.

Rectifier Diode

The MAX17122's high switching frequency demands a high-speed rectifier. Schottky diodes are recommended for most applications because of their fast recovery time and low forward voltage. In general, a 1A Schottky diode complements the internal MOSFET well.

Output-Voltage Selection

The output voltage of the step-up regulator is temperature compensated. From the warm temperature range ((3.3V - V_{NTC}) > 1.65V), the output voltage is set by connecting a resistive voltage-divider from the output (V_{GOFF2}) to the 3.3V reference with the center tap connected to FB3 (see Figure 1). Select R4 in the 10kΩ to 50kΩ range. Calculate R3 with the following equation:

$$R3 = R4 \times \frac{V_{GOFF2_WARM} - V_{FB3}}{V_{FB3} - 3.3V}$$

where V_{FB3}, the step-up regulator's feedback set point, is 1.65V. Place R3 and R4 close to the IC.

For cold temperatures ((3.3V - V_{NTC}) < V_{SET}), the output voltage is set by:

$$V_{SET} = \frac{R4 \times V_{GOFF2_COLD} + R3 \times 3.3V}{R3 + R4}$$

If the above calculated V_{SET} voltage is larger than 1.65V, then temperature compensation is disabled and the boost-buck regulator output is V_{GOFF2_WARM} at all temperatures.

Calculate the SET pin resistor R_{SET} as follows:

$$R_{SET} = \frac{V_{SET}}{100\mu A}$$

The temperature-compensation network is usually a thermistor in series with a resistor as in Figure 1. A parallel resistor is often added to linearize the network's resistance-temperature characteristic.

Loop Compensation

Choose R_{COMP3} to set the high-frequency integrator gain for fast-transient response. Choose C_{COMP3} to set the integrator zero to maintain loop stability. Typically, a low bandwidth is expected for normal operation. In that case, choosing C_{COMP3} = 4.7nF and R_{COMP3} between 1kΩ and 5kΩ gives a good combination of stability and startup timing. Using greater than 4.7nF for C_{COMP3} can cause an excessive startup delay due to the time required to charge C_{COMP3}.

Positive Charge-Pump Linear Regulators

Selecting the Number of Charge-Pump Stages

For highest efficiency, always choose the lowest number of charge-pump stages that meet the output requirement.

The number of positive charge-pump stages is given by:

$$n_{POS} = \frac{V_{GON} + V_{PNP} - V_{AVDD}}{V_{AVDD} - 2 \times V_D}$$

where n_{POS} is the number of positive charge-pump stages, V_{GON} is the output of the positive charge-pump

regulator, V_{AVDD} is the step-up regulator output and is also the supply voltage of the charge-pump regulators, V_D is the forward voltage drop of charge-pump diode D4, and V_{PNP} is the voltage across the pnp transistor P1 emitter and collector. For a doubler configuration, $n_{POS} = 1$.

The previous equation is derived based on the assumption that the first stage of the positive charge pump is connected to V_{AVDD}. Sometimes fractional stages are more desirable for better efficiency. This can be done by connecting the first stage to another available supply V_{INCP}. If the first charge-pump stage is powered from V_{INCP}, then the previous equation becomes:

$$n_{POS} = \frac{V_{GON} + V_{PNP} - V_{INCP}}{V_{AVDD} - 2 \times V_D}$$

Flying Capacitors

Increasing the flying capacitor C_{FLY} (connected to LX1) value lowers the effective source impedance and increases the output-current capability. Increasing the capacitance indefinitely has a negligible effect on output current capability because the internal switch resistance and diode impedance place a lower limit on the source impedance. A 0.1µF ceramic capacitor works well in most low-current applications. The flying capacitor's voltage rating must exceed the following:

$$V_{CFLY} > n_{POS} \times V_{AVDD}$$

where n_{POS} is the number of stages in which the flying capacitor appears. It is the same as the number of charge-pump stages.

Charge-Pump Output Capacitor

Increasing the output capacitance, or decreasing the ESR, reduces the output-voltage ripple and the peak-to-peak transient voltage. With ceramic capacitors, the output-voltage ripple is dominated by the capacitance value. Use the following equation to approximate the required capacitor value:

$$C_{GON} \geq \frac{I_{GON}}{2 \times f_{SW} \times V_{RIPPLE_GON}}$$

where C_{GON} is the output capacitor of the charge pump, I_{GON} is the load current of the charge pump, and V_{RIPPLE_GON} is the peak-to-peak value of the output ripple.

Output-Voltage Selection

Adjust the charge-pump regulator's output voltage by connecting a resistive voltage-divider from the V_{GON} output to AGND with the center tap connected to FBP (Figure 1). Select the lower resistor of divider R6 in the 10kΩ to 30kΩ range. Calculate upper resistor R5 with the following equation:

$$R5 = R6 \times \left(\frac{V_{GON}}{V_{FBP}} - 1 \right)$$

where V_{FBP} = 1.25V (typical).

Charge-Pump Rectifier Diodes

Use low-cost silicon switching diodes with a current rating equal to or greater than two times the average charge-pump input current. If it helps avoid an extra stage, some or all of the diodes can be replaced with Schottky diodes with an equivalent current rating. A small resistor (R_P) in series with charging diode D4 is usually required to reduce the magnitude of the current pulses into the step-up regulator switching node LX, which can cause its current mode control to terminate LX1 pulses too early. The value of this small resistor is determined by the available charge-pump headroom according to the following question:

$$V_{HEADROOM} = I_{CP} \times R_P$$

where I_{CP} is the charging current and R_P is the series resistor. Normally, a 2Ω to 5Ω resistor is sufficient for this purpose.

Pass-Transistor Selection

The pass transistor must meet specifications for current gain (h_{FEP}), input capacitance, collector-emitter saturation voltage, and power dissipation. The transistor's current gain limits the guaranteed maximum output current to:

$$I_{CP(MAX)} = (I_{DRVP} - \frac{V_{BEP}}{R_{BEP}}) \times h_{FEP(MIN)}$$

where I_{DRVP} is the minimum guaranteed base-drive current, V_{BEP} is the pnp transistor's base-to-emitter forward-voltage drop, and R_{BEP} is the pullup resistor connected between the pnp transistor's base and emitter. Furthermore, the transistor's current gain increases the linear regulator's DC loop gain so excessive gain destabilizes the output. Therefore, transistors with current gain over 100 at the maximum output current can be difficult to stabilize and are not recommended unless the high gain is needed to meet the load-current requirements.

Step-Up, Step-Down Regulator, Gate-On Charge Pump, and Boost-Buck Regulator for TV TFT LCD Display

The transistor's saturation voltage at the maximum output current determines the minimum input-to-output voltage differential that the regulator can support. Also, the package's power dissipation limits the usable maximum input-to-output voltage differential. The maximum power-dissipation capability of the transistor's package and mounting must exceed the actual power dissipated in the device. The power dissipated equals the maximum charge current ($I_{CP_DC(MAX)}$) multiplied by the maximum input-to-output voltage differential:

$$P = I_{CP_DC(MAX)} \times V_{PNP}$$

where V_{PNP} is the voltage across the pnp emitter and collector and can be calculated as:

$$V_{PNP} = V_{INCP} - (V_{GON} - \eta_{POS}(V_{AVDD} - 2V_D))$$

where $I_{CP_DC(MAX)}$ is the maximum average DC input current of the pnp pass transistor and can be estimated as:

$$I_{CP_DC(MAX)} \approx \frac{V_{GON} + V_D}{V_{GON} - \eta_{POS}(V_{AVDD} - 2V_D) + V_D} \times I_{LOAD}$$

where I_{LOAD} is the charge pump average DC load current.

A collector capacitor (CP) can increase the current injection to the step-up regulator switching node, LX1, and should be avoided unless stable operation of the charge pump cannot be achieved otherwise. If installed, the capacitor value should be 0.1µF.

Negative Linear Regulator

Output-Voltage Selection

Adjust the negative linear-regulator output voltage (GOFF1) by connecting a resistive voltage-divider from V_{GOFF1} to 3.3V with the center tap connected to FBN (Figure 1). Select R8 in the 20kΩ to 50kΩ range. Calculate R7 with the following equation:

$$R7 = R8 \times \frac{V_{GOFF1} - V_{FBN}}{V_{FBN} - 3.3V}$$

where V_{FBN} = 250mV.

Pass-Transistor Selection

The pass transistor must meet specifications for current gain (h_{FEN}), input capacitance, collector-emitter saturation voltage, and power dissipation. The transistor's current gain limits the guaranteed maximum output current to:

$$I_{GOFF1(MAX)} = (I_{DRVN} - \frac{V_{BEN}}{R_{BEN}}) \times h_{FEN(MIN)}$$

where I_{DRVN} is the minimum guaranteed base-drive current, V_{BEN} is the npn transistor's base-to-emitter forward voltage drop, and R_{BEN} is the pullup resistor connected between the npn transistor's base and emitter. Furthermore, the transistor's current gain increases the linear regulator's DC loop gain, so excessive gain destabilizes the output. Therefore, transistors with current gain over 100 at the maximum output current can be difficult to stabilize and are not recommended unless the high gain is needed to meet the load-current requirements.

The transistor's saturation voltage at the maximum output current determines the minimum input-to-output voltage differential that the linear regulator can support. Also, the package's power dissipation limits the usable maximum input-to-output voltage differential. The maximum power-dissipation capability of the transistor's package and mounting must exceed the actual power dissipated in the device. The power dissipated equals the maximum load current ($I_{GOFF1(MAX)}$) multiplied by the maximum input-to-output voltage differential:

$$P = I_{GOFF1(MAX)} \times (-V_{GOFF1(MAX)})$$

where $I_{GOFF1(MAX)}$ is the maximum average DC output of the negative linear regulator, and $V_{GOFF1(MAX)}$ is the maximum negative output voltage of the linear regulator.

PCB Layout and Grounding

Careful PCB layout is important for proper operation. Use the following guidelines for good PCB layout:

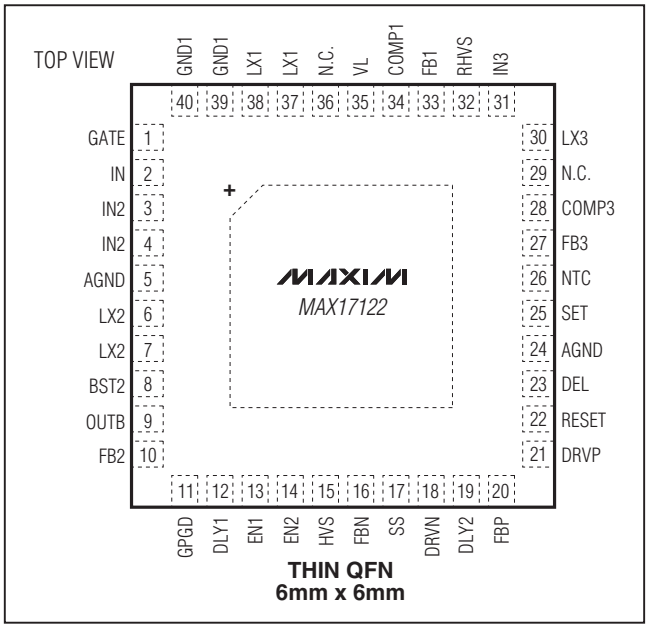
- Minimize the area of respective high-current loops by placing each DC-DC converter's inductor, diode, and output capacitors near its input capacitors and its LX_ and power grounds. For the step-down regulator, the high-current input loop goes from the positive terminal of the input capacitor to the IC's IN2 pin, out of LX2, to the inductor, to the positive terminals of the output capacitors, reconnecting the output capacitor and input capacitor ground terminals. The high-current output loop is from the inductor to the positive terminals of the output capacitors, to the negative terminals of the output capacitors, and to the Schottky diode (D2). For the step-up regulator, the high-current input loop goes from the positive terminal of the input capacitor to the inductor, to the IC's LX1 pin, out of GND1, and to the input capacitor's negative terminal. The high-current output loop is from the positive terminal of the input capacitor to the inductor, to the output diode (D1), to the positive terminal of the output capacitors, reconnecting between the output capacitor and input capacitor ground terminals. For

the boost-buck regulator, the high-current input loop goes from the positive terminal of the input capacitor to the IC's LX3 pin, inductor, out of GND1, and to the input capacitor's negative terminal. The high-current output loop is from the ground terminal to inductor, to the IC's LX3 pin, to the output diode (D3), the negative terminal of the output capacitor, reconnecting between the output capacitor/input capacitor ground terminals. Connect these loop components with short, wide connections. Avoid using vias in the high-current paths. If vias are unavoidable, use many vias in parallel to reduce resistance and inductance.

- Create a power ground island for the step-down regulator, consisting of the input and output capacitor grounds and the diode ground. Connect all these together with short, wide traces or a small ground plane. Similarly, create a power ground island (GND1) for the step-up regulator, consisting of the input and output capacitor grounds and the GND1 pin. Create a power ground island for the boost-buck regulator, consisting of the input and output capacitor grounds and inductor ground. Connect the step-down regulator ground plane, GND1 ground plane, boost-buck ground plane, charge-pump power ground, and negative linear-regulator power ground together with wide traces. Maximizing the width of the power ground traces improves efficiency and reduces output voltage ripple and noise spikes.
- Create an analog ground plane (AGND) consisting of the AGND pin, all the feedback-divider ground connections, the COMP1, COMP3, DEL, SS, DLY1, DLY2, EN1, and EN2 capacitor ground connections, and the device's exposed backside pad. Connect the GND1 and AGND islands by connecting the two ground pins directly to the exposed backside pad. Make no other connections between these separate ground planes.
- Place all feedback voltage-divider resistors as close as possible to their respective feedback pins. The divider's center trace should be kept short. Placing the resistors far away causes their FB traces to become antennas that can pick up switching noise. Care should be taken to avoid running any feedback trace near LX1, LX2, and LX3.
- Place IN pin, IN2 pin, and VL pin bypass capacitors as close as possible to the device. The ground connection of the VL bypass capacitor should be connected directly to the AGND pin with a wide trace.
- Minimize the length and maximize the width of the traces between the output capacitors and the load for best transient responses.
- Minimize the size of the LX1, LX2, and LX3 nodes while keeping them wide and short. Keep the LX1, LX2, and LX3 nodes away from feedback nodes (FB1, FB2, FB3, FBP, and FBN) and analog ground. Use DC traces as a shield if necessary.

Refer to the MAX17122 evaluation kit data sheet for an example of proper board layout.

Pin Configuration



Step-Up, Step-Down Regulator, Gate-On Charge Pump, and Boost-Buck Regulator for TV TFT LCD Display

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
40 TQFN-EP	T4066+3	21-0141	90-0054

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
1	9/09	Initial release	—
2	11/09	Corrected EC table parameter; only typical is relevant at high temperature	1, 2, 7

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