3-Channel Digital Power Supply Controller

Data Sheet

ADP1053

FEATURES

Configurable 8-PWM engine with up to 3 channels
2 independent digitally controlled channel outputs
Voltage mode PWM control with 625 ps resolution
Remote voltage sensing on both channels
Programmable compensation filters
Voltage feedforward option
Flexible start-up sequencing and tracking
Switching frequency: 50 kHz to 625 kHz
Frequency synchronization
Independent channel protections: OVP and OCP
2 independent OTP circuits
Programmable fault protection sequence
Volt-second balance and dual-phase current balance for interleaved configurations
On-board EEPROM
PMBus-compliant
Graphical user interface (GUI) for ease of programming
Available in a 40-lead, 6 mm × 6 mm LFCSP

APPLICATIONS

AC-to-DC power supplies
Isolated dc-to-dc power supplies
Intermediate rail power supplies
Nonisolated dc-to-dc power converter

GENERAL DESCRIPTION

The ADP1053, based on a voltage mode PWM architecture, is a flexible, application dedicated digital controller designed for isolated and nonisolated dc-to-dc power supply applications. The ADP1053 enables highly efficient power supply design and facilitates the introduction of intelligent power management techniques to improve energy efficiency at a system level.

The ADP1053 provides control, monitoring, and protection of up to three independent channel outputs. The eight flexible PWM outputs can be configured as three independent channels: two regulated channels with feedback control plus one additional unregulated channel with a fixed duty cycle. The frequency of these three channels can be programmed individually from 50 kHz to 625 kHz; all channels can be synchronized internally or to an external signal.

All eight PWM outputs can also be assigned to enable a single-channel solution, which may be required in high power, high efficiency applications.

Features include differential voltage sensing, fast current sensing, flexible start-up sequencing and tracking, and synchronization between devices to reduce low frequency system noise. Protection and monitoring features include overcurrent protection (OCP), undervoltage protection (UVP), overvoltage protection (OVP), and overtemperature protection (OTP).

SIMPLIFIED TYPICAL APPLICATION CIRCUIT

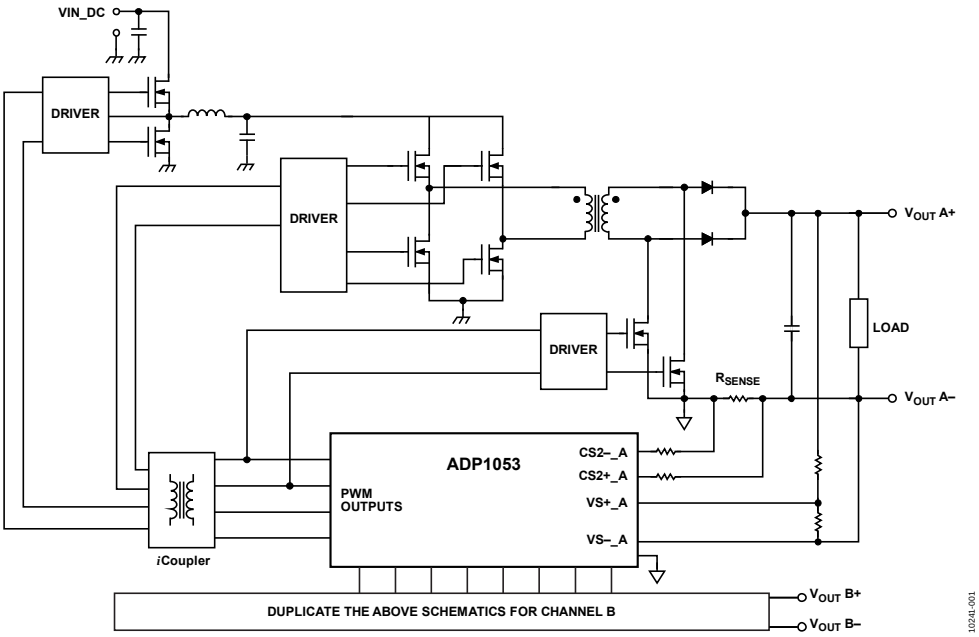

Figure 1.

Rev. A

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6/12—Rev. 0 to Rev. A

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1/12—Revision 0: Initial Version

The ADP1053 provides local and remote differential sensing of the output voltage, which is converted to the digital domain using high speed, high resolution Σ-Δ converters. The proprietary conversion system maximizes the bandwidth of the converter and minimizes output noise due to digital quantization error, thus dramatically reducing the power consumption of the digital controller.

Configurable compensation networks provide three poles and two zeros to control feedback loop stability and optimize output response. In addition, a programmable feedforward feature can be enabled to enhance input voltage response.

The ADP1053 provides extensive protection and monitoring capabilities. For example, each regulated output has its own independent voltage threshold, and overvoltage protection is provided for each regulated output. The protection and monitoring features combine to eliminate the possibility of a single point of failure.

Fast overcurrent protection is provided to protect the system from short circuits. Accurate current sensing and overcurrent limit protections are also included. In addition, two overtemperature protection circuits are provided for use with 100 kΩ thermistors to sense the hot spots.

Other protection and monitoring features include a programmable power-on (PSON) function and power-good monitoring for Channel A and Channel B.

All these features are programmable through the PMBus/I²C interface. This interface is also used for calibration. Additional information, such as input current, output current, and fault flag status, can be read via the PMBus/I²C interface.

The built-in EEPROM is used to store programmed values and instructions. System reliability is improved through a built-in checksum and redundancy of critical circuits. In the event of a system fault, the EEPROM can be configured to capture the first instance of failure; this stored fault data can be analyzed to improve overall system reliability and reduce failure mode analysis time.

The ADP1053 is designed to maximize ease of use and reduce time to market with the provision of a comprehensive, easy to use graphical user interface (GUI) that allows programming of most parameters and protection and monitoring limits.

The ADP1053 is available in a 40-lead LFCSP package and operates from a single 3.3 V supply.

FUNCTIONAL BLOCK DIAGRAM

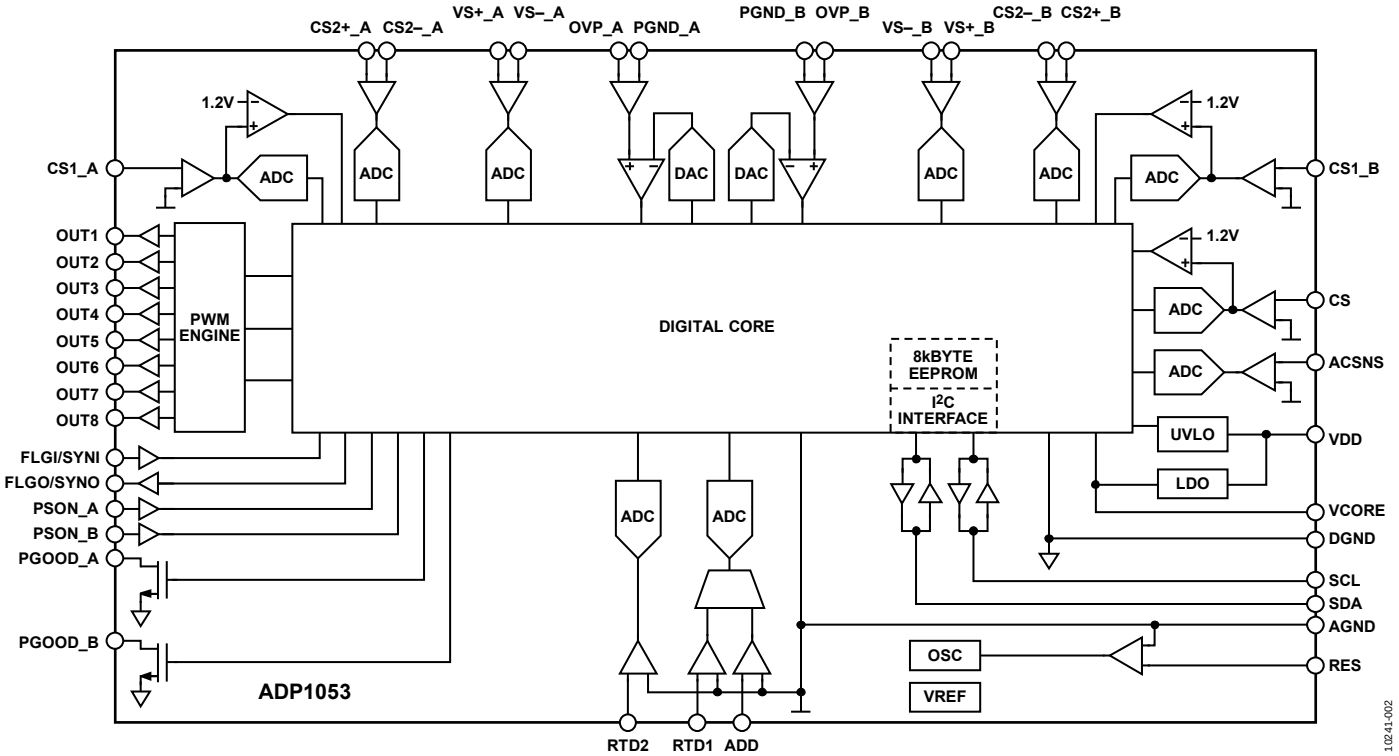


Figure 2.

SPECIFICATIONS

V_{DD} = 3.0 V to 3.6 V, T_A = −40°C to +125°C, unless otherwise noted. FSR = full-scale range.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SUPPLY					
V_{DD}		3.0	3.3	3.6	V
I_{DD}	PWM pins unloaded				
	Normal operation (PSON high)		30		mA
	Power supply off (PSON low)		30		mA
	Shutdown (V_{DD} below UVLO)		100		µA
	During EEPROM programming		I_{DD} + 8		mA
POWER-ON RESET					
UVLO Threshold					
V_{DD} Rising				3.0	V
V_{DD} Falling		2.750	2.85	2.975	V
OVLO Threshold		3.7	3.9	4.1	V
OVLO Debounce	When set to 2 µs		2		µs
	When set to 500 µs		500		µs
VCORE PIN					
Output Voltage	330 nF capacitor between VCORE and DGND	2.3	2.5	2.7	V
OSCILLATOR AND PLL					
PLL Frequency	RES = 10 kΩ		200		MHz
DPWM Resolution			625		ps
VS_A, VS_B VOLTAGE SENSE					
Input Voltage	Differential voltage from VS+_A to VS−_A and from VS+_B to VS−_B	0	1	1.6	V
Input Voltage FSR			1.6		V
VS_A, VS_B Accurate ADCs					
Valid Input Voltage Range		0		1.5	V
ADC Register Update Rate			100		Hz
Resolution			12		Bits
Measurement Accuracy	From 0% to 100% of valid input voltage	−2.8		+2.1	% FSR
		−44.8		+33.6	mV
	From 10% to 90% of valid input voltage	−1.35		+2.1	% FSR
		−21.6		+33.6	mV
	From 900 mV to 1.1 V	−1.2		+1.65	% FSR
		−19.2		+26.4	mV
Temperature Stability	From 900 mV to 1.1 V	−0.1		+0.1	mV/°C
Common-Mode Voltage Offset	Voltage from VS−_A and VS−_B to AGND to achieve measurement accuracy	−200	0	+200	mV
VS_A, VS_B High Speed ADCs					
Equivalent Resolution	At 390.6 kHz switching frequency		6		Bits
Dynamic Range	Regulation voltage 300 mV to 1.4 V		±10		mV
VS_A, VS_B UVP	Based on VS_A, VS_B accurate ADC				
Threshold Accuracy	Same as accurate ADC measurement accuracy specifications				
Comparator Update Speed			10		ms
OVP_A, OVP_B PINS					
Threshold Accuracy		−1.7		+1.6	%
Propagation Delay (Latency)	Debounce time not included		58	110	ns

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
AC SENSE					
Input Voltage	Voltage from ACSNS to AGND	0	1	1.6	V
Input Voltage FSR			1.6		V
ACSNS ADC					
Valid Input Voltage Range		0	1	1.4	V
ADC Register Update Rate			800		Hz
Resolution			11		Bits
Measurement Accuracy	From 10% to 90% of valid input voltage	−1.25		+1.8	% FSR
		−20		+28.8	mV
	From 0% to 100% of valid input voltage	−5.4		+1.9	% FSR
		−86.4		+30.4	mV
ACSNS					
Threshold Accuracy	Same as ACSNS ADC measurement accuracy specifications				
Comparator Update Speed			1		ms
CS, CS1_A, CS1_B CURRENT SENSE					
Input Voltage	Voltage from CS/CS1_A/CS1_B to AGND	0		1.6	V
Input Voltage FSR			1.6		V
CS, CS1_A, CS1_B ADCs					
Valid Input Voltage Range		0	1	1.4	V
ADC Register Update Rate			100		Hz
Resolution			12		Bits
Measurement Accuracy	From 10% to 90% of valid input voltage	−1.3		+1.8	% FSR
		−20.8		+28.8	mV
	From 0% to 100% of valid input voltage	−5.6		+1.8	% FSR
		−89.6		+28.8	mV
Fast OCP					
Threshold Value		1.18	1.2	1.22	V
Propagation Delay (Latency)	Debounce/blanking time not included		58	110	ns
CS2_A, CS2_B CURRENT SENSE					
Input Voltage	Differential voltage from CS2+_A to CS2−_A and from CS2+_B to CS2−_B	0		120	mV
Input Voltage FSR			120		mV
Common-Mode Voltage	Common-mode voltage from CS2+_A/CS2−_A and CS2+_B/CS2−_B to AGND to achieve measurement accuracy	0.8	1	1.3	V
CS2_A, CS2_B ADCs					
Valid Input Voltage Range		0		120	mV
Resolution			12		Bits
Measurement Accuracy					
Low-Side Mode with User Trim	V_{OUT} = 0 V, 5 kΩ level-shifting resistor				
	From 0 mV to 110 mV	−1.85		+2.1	% FSR
		−2.22		+2.52	mV
	From 110 mV to 120 mV	−6.1		+1.5	% FSR
		−6.36		+0.84	mV
High-Side Mode with User Trim	V_{OUT} = 11 V, 5 kΩ level-shifting resistor				
	From 0 mV to 110 mV	−1.6		+2.3	% FSR
		−1.92		+2.76	mV
	From 110 mV to 120 mV	−5.3		+0.7	% FSR
		−6.36		+0.84	mV

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Accurate OCP					
Threshold Accuracy	Same as ADC accuracy				
ADC Register Update Rate			100		Hz
Current Sink (High Side)	V_{OUT} = 11 V, 5 kΩ level-shifting resistor	1.81	1.9	1.99	mA
Current Source (Low Side)	V_{OUT} = 0 V, 5 kΩ level-shifting resistor	180	230	280	µA
Fast Reverse Current Threshold (CS2+, CS2−)					
Threshold Accuracy	−17 mV setting	−23.2	−17	−9.6	mV
	−27 mV setting	−34.7	−27	−18.1	mV
Threshold Speed	Debounce time = 40 ns		110	150	ns
RTD1, RTD2 TEMPERATURE SENSE PINS					
Input Voltage	Voltage from RTDx to AGND	0		1.6	V
Input Voltage FSR			1.6		V
Source Current	Set to 46 µA	44.3	46	47.3	µA
	Set to 40 µA	38.6	40	42	µA
	Set to 30 µA	28.8	30	31.7	µA
	Set to 20 µA	18.8	20	21.5	µA
	Set to 10 µA (factory default setting)	9.1	10	11	µA
RTD1, RTD2 ADCs					
Valid Input Voltage Range		0		1.28	V
ADC Register Update Rate			100		Hz
Resolution			12		Bits
Measurement Accuracy	From 2% to 20% of valid input voltage	−0.3		+0.45	% FSR
		−4.8		+7.2	mV
	From 0% to 100% of valid input voltage	−2.6		+1.6	% FSR
		−41.6		+25.6	mV
Temperature Readings According to Internal Linearization Scheme	Factory trimmed to 10 µA; Register 0xFE80 and Register 0xFE81 = 0x00; NTC R_0 = 100 kΩ, 1%; beta = 4250, 1%; R_{EXT} = 16.5 kΩ, 1%				
	T = 25°C to 100°C			7	°C
	T = 100°C to 125°C			5	°C
OTP1, OTP2, OTW1, OTW2					
Threshold Accuracy	T = 85°C with 100 kΩ‖16.5 kΩ	−0.9		+0.25	% FSR
		−14.4		+4	mV
	T = 100°C with 100 kΩ‖16.5 kΩ	0.5		1.1	% FSR
		8		17.6	mV
Comparator Update Speed			10		ms
OUT1 TO OUT8, FLGO/SYNO PINS	Digital output pins				
Output Low Voltage, V_{OL}	Source current = 10 mA			0.4	V
Output High Voltage, V_{OH}	Source current = 10 mA	V_{DD} − 0.4			V
Rise Time	C_{LOAD} = 50 pF		4.5		ns
Fall Time	C_{LOAD} = 50 pF		2.5		ns
PGOOD_A, PGOOD_B PINS	Open-drain output pins				
Output Low Voltage, V_{OL}				0.4	V
PSON_A, PSON_B, FLGI/SYNI PINS	Digital input pins				
Input Low Voltage, V_{IL}				0.8	V
Input High Voltage, V_{IH}		V_{DD} − 0.8			V
SDA/SCL PINS					
Input Low Voltage, V_{IL}				0.8	V
Input High Voltage, V_{IH}		V_{DD} − 0.8			V
Output Low Voltage, V_{OL}				0.8	V
Leakage Current		−5		+5	µA

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SERIAL BUS TIMING	See Figure 3				
Clock Frequency			100	400	kHz
Glitch Immunity, t_{SW}				50	ns
Bus Free Time, t_{BUF}		1.3			µs
Start Setup Time, $t_{SU;STA}$		0.6			µs
Stop Setup Time, $t_{SU;STO}$		0.6			µs
Start Hold Time, $t_{HD;STA}$		0.6			µs
SCL Low Time, t_{LOW}		0.6			µs
SCL High Time, t_{HIGH}		0.6			µs
SCL, SDA Rise Time, t_R				20	ns
SCL, SDA Fall Time, t_F				20	ns
Data Setup Time, $t_{SU;DAT}$		100			ns
Data Hold Time, $t_{HD;DAT}$					
Read		125			ns
Write		300			ns
EEPROM					
EEPROM Update Time	Time from update command to EEPROM update completed (T_J = 25°C)		40		ms
Reliability					
Endurance[1]	T_J = 85°C	10,000			Cycles
	T_J = 125°C	1000			Cycles
Data Retention[2]	T_J = 85°C	20			Years
	T_J = 125°C	10			Years

[1] Endurance is qualified as per JEDEC Standard 22, Method A117, and is measured at −40°C, +25°C, +85°C, and +125°C. Endurance conditions are subject to change pending EEPROM qualification.
[2] Retention lifetime equivalent at junction temperature (T_J) = 125°C as per JEDEC Standard 22, Method A117. The derated lifetime is subject to change pending EEPROM qualification.

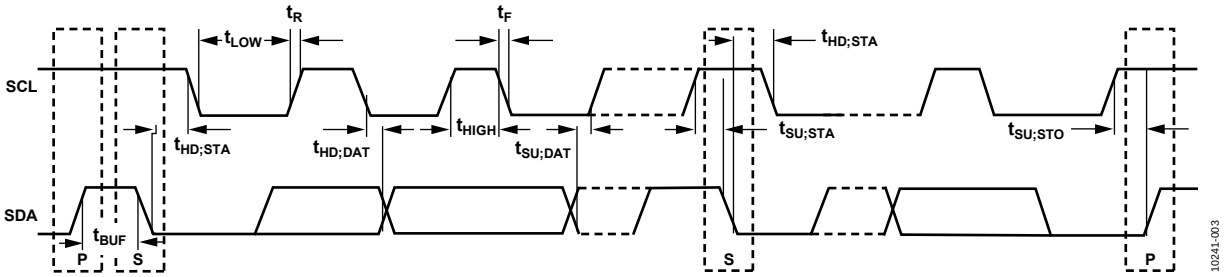


Figure 3. Serial Bus Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage (Continuous), V_{DD}	4.2 V
Digital Pins	−0.3 V to V_{DD} + 0.3 V
VS−_A, VS−_B, PGND_A, PGND_B to AGND, DGND	−0.3 V to +0.3 V
Other Analog Pins to AGND	3.6 V
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Peak Solder Reflow Temperature	
SnPb Assemblies (10 sec to 30 sec)	240°C
RoHS Compliant Assemblies (20 to 40 sec)	260°C
ESD	
Charged Device Model	1.0 kV
Human Body Model	2.5 kV

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
40-Lead LFCSP (CP-40-10)	28.36	2.1	°C/W

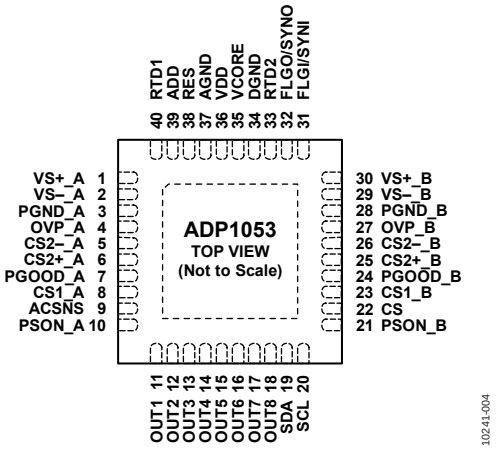
SOLDERING

It is important to follow the correct guidelines when laying out the PCB footprint for the ADP1053 and when soldering the part onto the PCB. For detailed information about these guidelines, see the AN-772 Application Note.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. THE EXPOSED PAD ON THE UNDERSIDE OF THE PACKAGE SHOULD BE SOLDERED TO AGND.

Figure 4. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VS+_A	Noninverting Input of the Voltage Sense ADC for Channel A Loop Control. This signal is referenced to VS−_A.
2	VS−_A	Inverting Input of the Voltage Sense ADC for Channel A Loop Control. There should be a low ohmic connection to AGND.
3	PGND_A	Reference Pin for Channel A Overvoltage Protection (OVP_A).
4	OVP_A	Overvoltage Protection Comparator Input for Channel A. This signal is referenced to PGND_A.
5	CS2−_A	Inverting Input of the Differential Current Sense ADC for Channel A. The nominal voltage at this pin should be 1 V for optimal operation.
6	CS2+_A	Noninverting Input of the Differential Current Sense ADC for Channel A. The nominal voltage at this pin should be 1 V for optimal operation.
7	PGOOD_A	Power-Good Output (Open-Drain) for Channel A. This signal is referenced to AGND. This pin is controlled by the PGOOD_A flag and is driven low when the flag is set. The PGOOD_A flag is set when the POWER_SUPPLY_A, UVP_A, EEPROM_CRC, or SOFTSTART_FILTER_A flag is set. The ACSNS and OTW1 flags can also be programmed to be included.
8	CS1_A	CS1 ADC Input and Fast Current Sense Input for Channel A. This signal is referenced to AGND.
9	ACSNS	AC Sense ADC and Feedforward Operation Input. This pin is connected upstream of the main inductor through a resistor divider network. The nominal voltage at this pin should be 1 V. This signal is referenced to AGND.
10	PSON_A	Power Supply On Input for Channel A. This signal is referenced to AGND.
11	OUT1	OUT1 PWM Logic Output Drive. This pin is connected to the input of a FET driver; it can be disabled when not in use. This signal is referenced to AGND.
12	OUT2	OUT2 PWM Logic Output Drive. This pin is connected to the input of a FET driver; it can be disabled when not in use. This signal is referenced to AGND.
13	OUT3	OUT3 PWM Logic Output Drive. This pin is connected to the input of a FET driver; it can be disabled when not in use. This signal is referenced to AGND.
14	OUT4	OUT4 PWM Logic Output Drive. This pin is connected to the input of a FET driver; it can be disabled when not in use. This signal is referenced to AGND.
15	OUT5	OUT5 PWM Logic Output Drive. This pin is connected to the input of a FET driver; it can be disabled when not in use. This signal is referenced to AGND.
16	OUT6	OUT6 PWM Logic Output Drive. This pin is connected to the input of a FET driver; it can be disabled when not in use. This signal is referenced to AGND.
17	OUT7	OUT7 PWM Logic Output Drive. This pin is connected to the input of a FET driver; it can be disabled when not in use. This signal is referenced to AGND.
18	OUT8	OUT8 PWM Logic Output Drive. This pin is connected to the input of a FET driver; it can be disabled when not in use. This signal is referenced to AGND.

Pin No.	Mnemonic	Description
19	SDA	PMBus/I²C Serial Data Input and Output (Open-Drain). This signal is referenced to AGND.
20	SCL	PMBus/I²C Serial Clock Input and Output (Open-Drain). This signal is referenced to AGND.
21	PSON_B	Power Supply On Input for Channel B. This signal is referenced to DGND.
22	CS	CS ADC Input and Fast Current Sense Input for Overcurrent Protection and Current Monitoring. This signal is referenced to AGND.
23	CS1_B	CS1 ADC Input and Fast Current Sense Input for Channel B. This signal is referenced to AGND.
24	PGOOD_B	Power-Good Output (Open-Drain) for Channel B. This signal is referenced to AGND. This pin is controlled by the PGOOD_B flag and is driven low when the flag is set. The PGOOD_B flag is set when the POWER_SUPPLY_B, UVP_B, EEPROM_CRC, or SOFTSTART_FILTER_B flag is set. The ACSNS and OTW2 flags can also be programmed to be included.
25	CS2+_B	Noninverting Input of the Differential Current Sense ADC for Channel B. The nominal voltage at this pin should be 1 V for optimal operation.
26	CS2−_B	Inverting Input of the Differential Current Sense ADC for Channel B. The nominal voltage at this pin should be 1 V for optimal operation.
27	OVP_B	Overvoltage Protection Comparator Input for Channel B. This signal is referenced to PGND_B.
28	PGND_B	Reference Pin for Channel B Overvoltage Protection (OVP_B).
29	VS−_B	Inverting Input of the Voltage Sense ADC for Channel B Loop Control. There should be a low ohmic connection to AGND.
30	VS+_B	Noninverting Input of the Voltage Sense ADC for Channel B Loop Control. This signal is referenced to VS−_B.
31	FLGI/SYNI	Flag Input/Synchronization Input. When this pin is programmed as a flag input, an external signal can be input to generate a flag condition. The polarity is configurable. When this pin is programmed as a synchronization input, the input signal is used as a reference for the internal PWM frequencies. This signal is referenced to AGND.
32	FLGO/SYNO	Flag Output/Synchronization Output. When this pin is programmed as a flag output, it can be used to indicate the light load mode operation. The polarity is configurable. When this pin is programmed as a synchronization output, it can be used as a frequency reference for synchronization. This signal is referenced to AGND.
33	RTD2	Thermistor ADC Input from Zone 2. Typically, a 100 kΩ thermistor in parallel with a 16.5 kΩ resistor are placed from this pin to AGND. This signal is referenced to AGND.
34	DGND	IC Digital Ground. Reference ground for the digital circuitry of the ADP1053. This pin should be star-connected to AGND.
35	VCORE	Output of 2.5 V Regulator. Connect a 330 nF capacitor between this pin and DGND.
36	VDD	Positive Supply Voltage, 3.0 V to 3.6 V. This signal is referenced to AGND. Connect a 330 nF capacitor from VDD to AGND.
37	AGND	IC Common Analog Ground. This pin should be star-connected to DGND.
38	RES	Resistor Input. This pin sets the internal voltage reference for the ADP1053. Connect a 10 kΩ resistor (±1%) from RES to AGND. This signal is referenced to AGND.
39	ADD	PMBus/I²C Address Select Input. Connect a resistor from ADD to AGND (see the PMBus/I²C Address section). This signal is referenced to AGND.
40	RTD1	Thermistor ADC Input from Zone 1. Typically, a 100 kΩ thermistor in parallel with a 16.5 kΩ resistor are placed from this pin to AGND. This signal is referenced to AGND.
EP	Exposed Pad	The exposed pad on the underside of the package should be soldered to AGND.

APPLICATION CIRCUITS

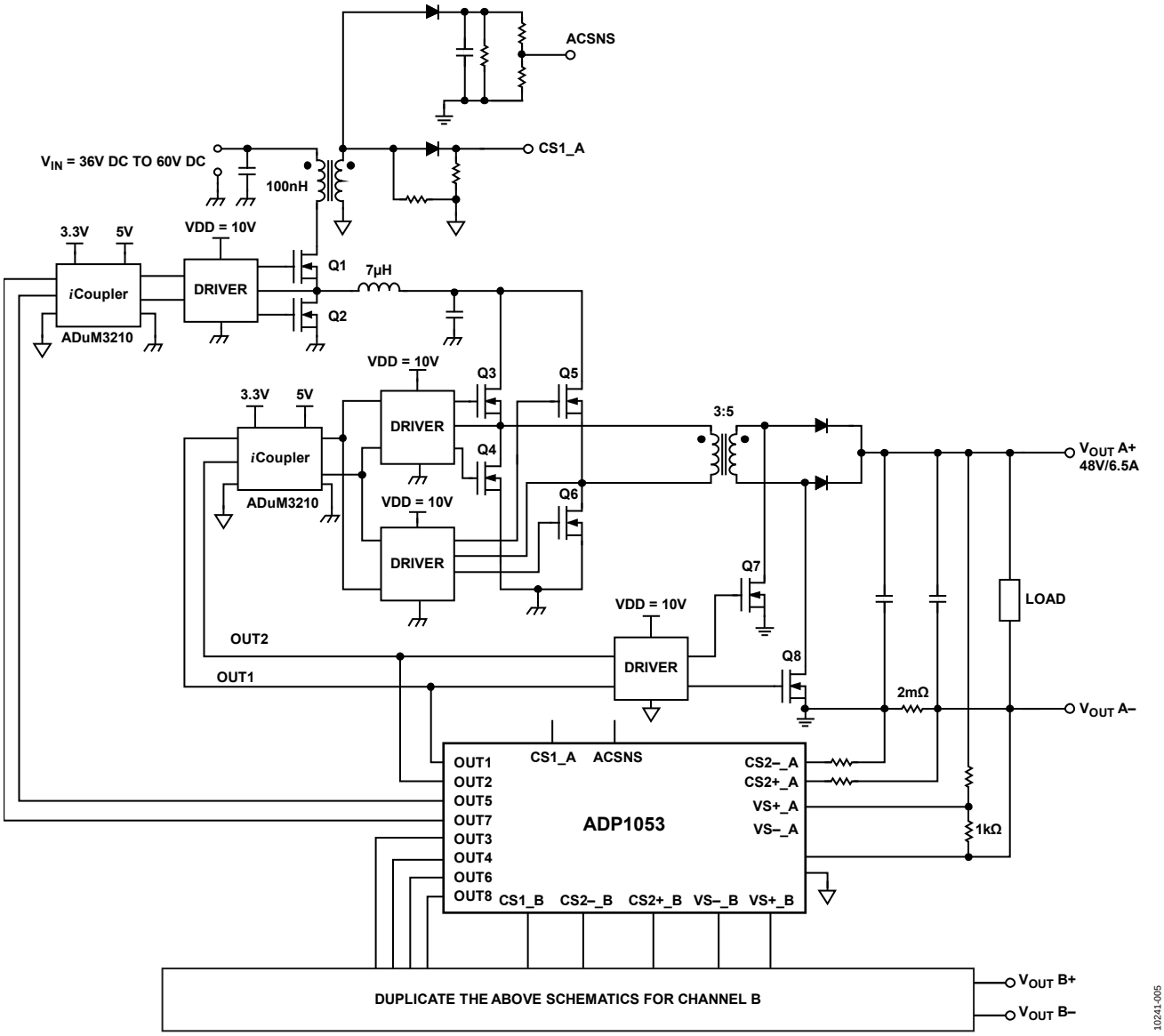


Figure 5. Application Circuit 1—Buck Preregulator Followed by a Fixed PWM Full-Bridge Topology with Synchronous Rectification

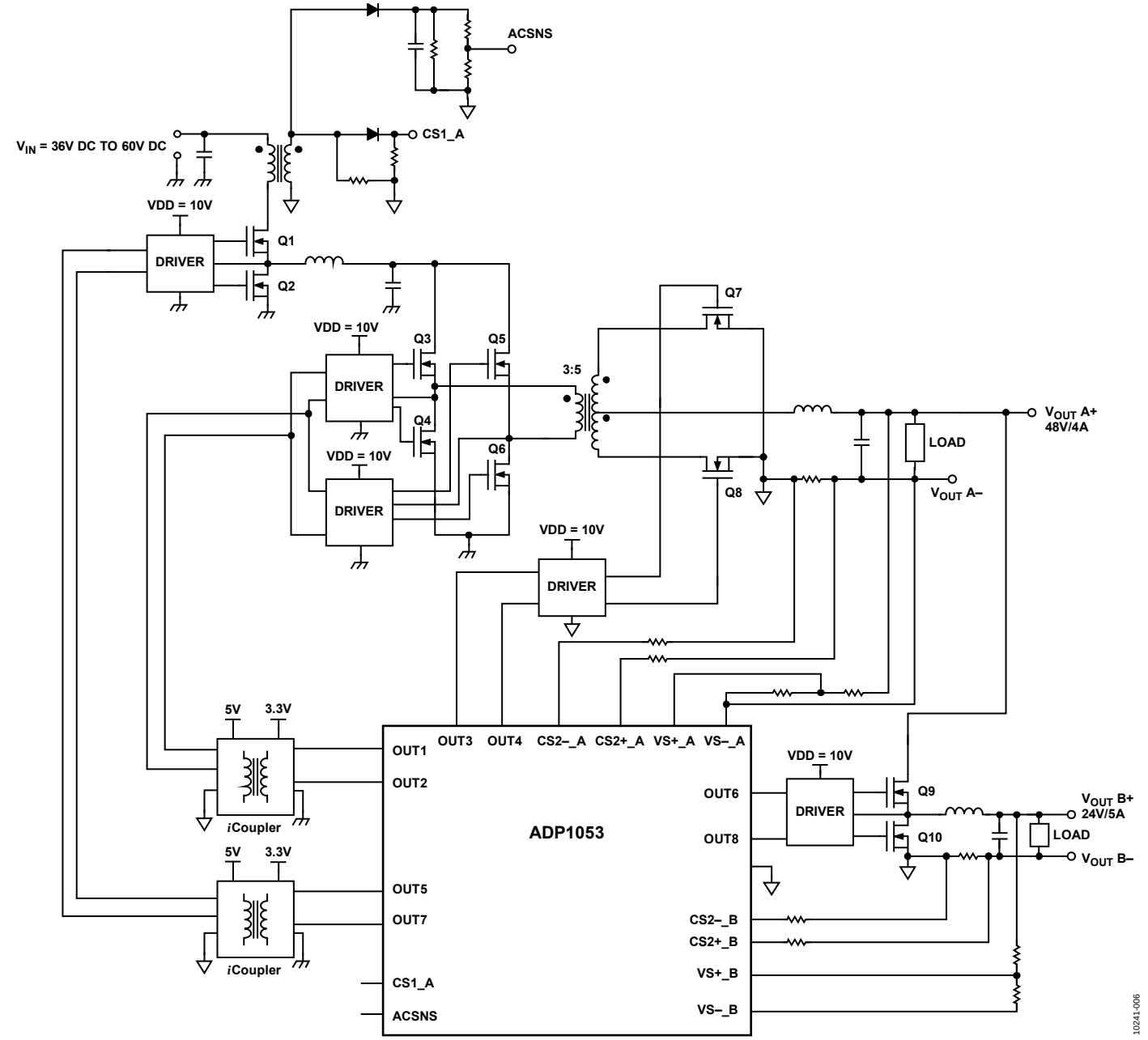


Figure 6. Application Circuit 2—Two Output Channels with Only One Full-Bridge Rectifier

THEORY OF OPERATION

PWM OUTPUTS (OUT1 TO OUT8)

The eight PWM outputs of the ADP1053 can be configured as two regulated channels with feedback control (Channel A and Channel B) and one additional unregulated channel with a fixed duty cycle (Channel C). The frequency of these channels can be individually programmed from 50 kHz to 625 kHz using Register 0xFE0A, Register 0xFE0B, and Register 0xFE0C, respectively.

The PWM engine in the ADP1053 is highly flexible. For example, the user can assign two PWM outputs to Channel A, two PWM outputs to Channel B, and four PWM outputs to Channel C. The user can also assign seven PWM outputs to Channel A and the remaining PWM output to Channel B. Alternatively, all eight PWM outputs can be assigned to Channel A for a single-channel solution.

As an example, Figure 5 shows a typical application circuit consisting of a buck preregulator followed by a fixed PWM full-bridge topology with synchronous rectification. In this example, only Channel A and Channel B are configured. As shown in Figure 5, the OUT1, OUT2, OUT5, and OUT7 PWM outputs are assigned to Channel A, and the OUT3, OUT4, OUT6, and OUT8 PWM outputs are assigned to Channel B. The Analog Devices, Inc., ADuM3210 *i*Coupler® device is used for isolation between the primary and secondary power stages.

All three channels can be enabled to support soft start. Channel A and Channel B use a closed-loop soft start scheme, which increases the reference voltage linearly and uses the feedback to increase the duty cycle gradually. When PWM outputs are assigned to Channel C with a fixed duty cycle, the duty cycle increases linearly until it reaches the preset value. For more information, see the Soft Start and Shutdown section.

Four of the eight PWM outputs (OUT3, OUT4, OUT7, and OUT8) can also be enabled for use as synchronous rectifier (SR) PWM control signals. These SR signals can be disabled during the power supply soft start ramp time. In addition, the SR PWM outputs can be programmed to initiate soft start when the outputs are enabled. For more information, see the Synchronous Rectifier (SR) Soft Start section.

All eight PWM outputs can be enabled or disabled using Register 0xFE60.

Timing of PWM Rising and Falling Edges

The timing of the rising and falling edges of the PWM outputs can be individually programmed. Special care must be taken to avoid shootthrough and cross-conduction. It is recommended that the ADP1053 graphical user interface (GUI) be used to program these outputs.

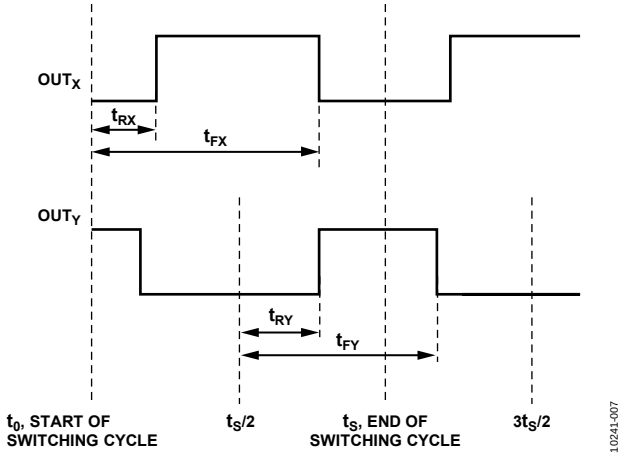


Figure 7. PWM Output Timing Diagram

Register 0xFE40 through Register 0xFE5F set the rising edge timing, falling edge timing, channel assignment, modulation schemes, and balance controls for the PWM outputs. For more information, see the PWM Output Timing Registers section.

One bit sets the 180° phase shift for each PWM output. When this bit is not set, the rising edge timing and the falling edge timing are referenced to the start of the switching cycle of the assigned channel (see t_{RX} and t_{FX} in Figure 7). When this bit is set, the rising edge timing and the falling edge timing are referred to half the switching cycle (see t_{RY} and t_{FY} in Figure 7).

Each LSB in the timing registers corresponds to a 5 ns step. The edge timing cannot exceed one switching cycle. Therefore, when the 180° phase shift is disabled, the edges are always located between t_0 and t_S; when the 180° phase shift is enabled, the edges are located between $t_S/2$ and $3t_S/2$.

Example Configuration of PWM Outputs

Table 6 provides example register settings that configure the OUT1 and OUT2 outputs for Channel A. In this example, the switching frequency of Channel A is 208.3 kHz, that is, a 4.8 µs switching cycle (Register 0xFE0A = 0x15).

GO Command

All eight PWM outputs work together. Therefore, when reprogramming more than one of these outputs, it is important to first update all the registers and then latch the information into the ADP1053 at the same time using the GO command (Bit 2 of Register 0xFE61). During reprogramming, the outputs are temporarily disabled. A special instruction is sent to the ADP1053 to ensure that new timing information is programmed simultaneously. It is recommended that unused PWM outputs be disabled.

Modulation Settings

Bits[3:0] in each PWM output setting register enable/disable rising and falling edge modulation and set the modulation sign. When the modulation sign is positive, an increase of the feedback filter output moves the edge to the right. When the sign is negative, an increase of the filter output moves the edge to the left.

For example, one of the most widely used modulation schemes is trailing edge modulation. To realize this scheme, Bits[3:0] of the PWM output setting registers are set to 0010.

Modulation Limits

Register 0xFE3C and Register 0xFE3D can be programmed to apply a maximum duty cycle modulation limit to PWM signals in Channel A and Channel B, respectively. As shown in Figure 8, this limit is the maximum time variation for the modulated edges from the default timing, following the configured modulation direction. There is no minimum duty cycle limit setting. Therefore, the user must set the rising edges and falling edges based on the case with the least modulation.

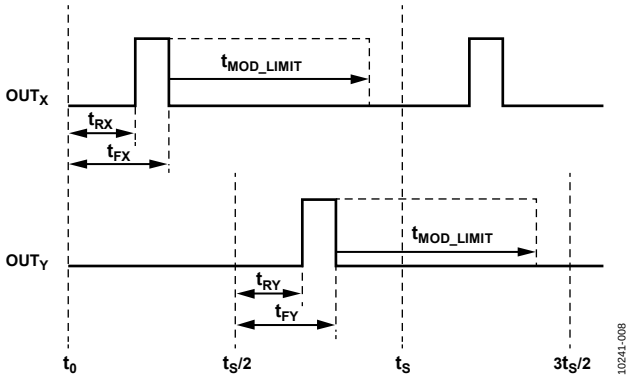


Figure 8. Setting Modulation Limits

The step size of an LSB in Register 0xFE3C and Register 0xFE3D depends on the switching frequency (see Table 5).

Table 5. LSB Step Size and Switching Frequency

Switching Frequency	LSB Step Size
48.8 kHz to 86.8 kHz	80 ns
97.7 kHz to 183.8 kHz	40 ns
195.3 kHz to 378.8 kHz	20 ns
390.6 kHz to 625.0 kHz	10 ns

The modulated edges cannot exceed one switching cycle. For PWM outputs without the 180° phase shift, such as OUT_X in Figure 7, the edges before and after modulation are always from t_0 to t_S. For PWM outputs with the 180° phase shift, such as OUT_Y in Figure 7, the edges before and after modulation are always from $t_S/2$ to $3t_S/2$.

The GUI provided with the ADP1053 is recommended for evaluating this feature.

Table 6. Example OUT1 and OUT2 Configuration

Register Setting	Configuration
Register 0xFE43, Bits[6:5] = 00	The PWM output OUT1 is assigned to Channel A with a frequency of 208.3 kHz.
Register 0xFE43, Bit 7 = 0	The reference for the rising and falling edges of OUT1 is the start of the switching cycle (180° phase shift disabled).
Register 0xFE40 = 0x01 and Register 0xFE42 = 0x00	The rising edge value is 0x010 (16 decimal), and the timing is set to 16 × 5 ns = 80 ns.
Register 0xFE41 = 0x20	The falling edge value is 0x200 (512 decimal), and the timing is set to 512 × 5 ns = 2.56 µs.
Register 0xFE47, Bits[6:5] = 00	The PWM output OUT2 is also assigned to Channel A with a frequency of 208.3 kHz.
Register 0xFE47, Bit 7 = 1	The reference for the rising and falling edges of OUT2 is half the switching cycle, $t_S/2$ (180° phase shift enabled).
Register 0xFE44 = 0x01 and Register 0xFE46 = 0x00	The rising edge value is 0x010 (16 decimal). Due to the 180° phase shift, the timing is set to 16 × 5 ns + 2.4 µs = 2.48 µs.
Register 0xFE45 = 0x20	The falling edge value is 0x200 (512 decimal), and the timing is set to 512 × 5 ns + 2.48 µs = 5.04 µs.

FREQUENCY SYNCHRONIZATION

Synchronization Output

The FLGO/SYNO pin can be programmed to generate a synchronization reference output using Bit 3 of Register 0xFE0F. The pin outputs a 320 ns pulse-width signal, whose frequency follows either Channel A or Channel C (programmable using Bit 3 of Register 0xFE0E).

To compensate for the propagation delays in the ADP1053 synchronization scheme, the SYNO signal has a 760 ns lead time before the start of the switching cycle.

Figure 9 shows an example of the SYNO timing when using Channel A as the reference.

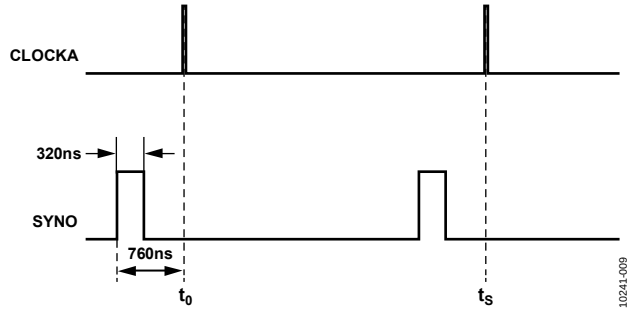


Figure 9. SYNO Timing

Synchronization Input

When the FLGI/SYNI pin is configured as a synchronization input, the external clock frequency at the pin must be between 90% and 110% of the internal switching frequency set by the channel's internal switching frequency register. If the switching cycle is out of this range or if there is no rising edge detected for 80 µs, the part exits synchronization mode, and each channel operates at its preset internal switching frequency. The maximum external synchronization clock frequency should be less than 625 kHz. If the FLGI/SYNI pin is programmed for the FLGI function, the synchronization function is disabled.

If two or more channels are enabled for synchronization, the valid synchronization frequency range is determined by the channel with the lowest synchronization multiple. The multiple is set using Bits[7:6] of Register 0xFE0A (Channel A), Register 0xFE0B (Channel B), and Register 0xFE0C (Channel C). If the multiple value is the same for two or more channels, the value set for Channel A has the highest priority and the value set for Channel C has the lowest priority.

Note that if Channel A or Channel C is synchronized with an external clock at the SYNI pin, the SYNO frequency is the preset internal frequency but not the operating switching frequency. For example, if the preset frequency of Channel A is 100 kHz and the SYNO frequency is configured to follow Channel A, the SYNO frequency is still 100 kHz even when the external synchronization clock is at 105 kHz.

To ensure proper operation of the synchronization mode, the synchronization multiple for at least one channel must be set to 1 (Bits[7:6] = 00).

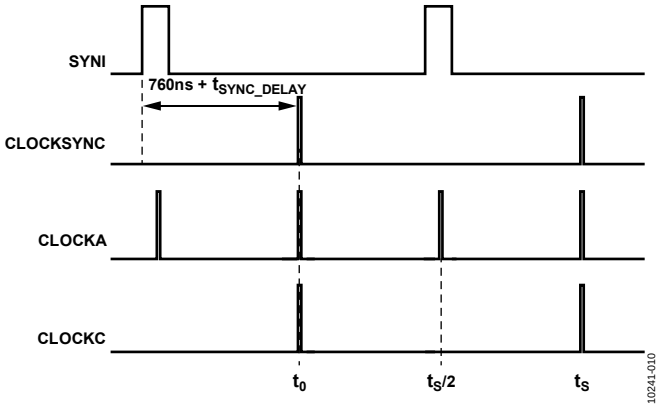


Figure 10. Synchronization Timing

VOLTAGE SENSE

Multiple voltage sense inputs on the ADP1053 are used for the monitoring, control, and protection of the power supply output. The voltage information is available through the PMBus/I²C interface. All voltage sense points can be calibrated digitally to remove any errors due to external components. This calibration can be performed in the production environment, and the settings saved in the EEPROM of the ADP1053. For more information, see the Power Supply Calibration and Trim section.

The update rate of the ADC from a control loop standpoint is set to the switching frequency. For example, if the switching frequency is set to 100 kHz, the ADC outputs a signal at a rate of 100 kHz to the control loop. Because the Σ-Δ ADC samples at 1.6 MHz, the output of the ADC is the average of the 16 readings per switching cycle.

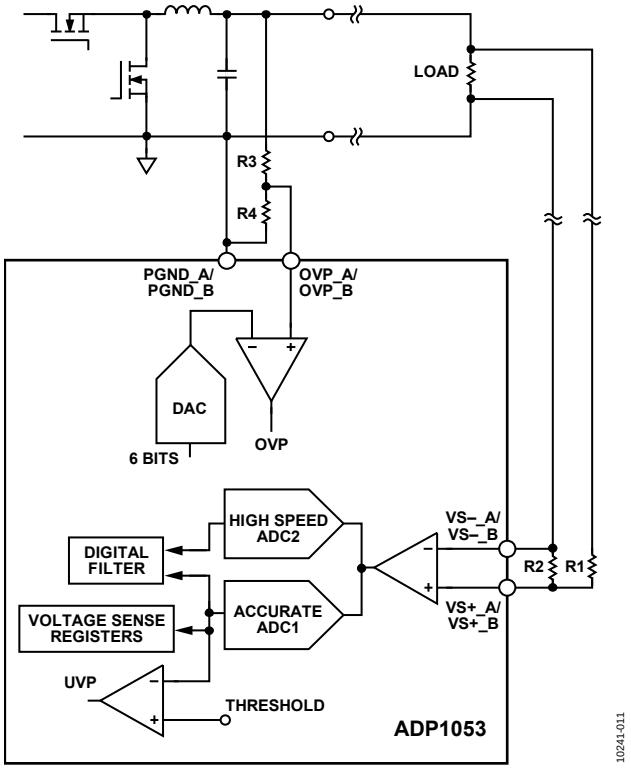


Figure 11. Voltage Sense Configuration

Voltage Feedback Sensing (VS+_A/VS+_B, VS−_A/VS−_B)

VS_A and VS_B are used for the control, monitoring, and undervoltage protection (UVP) of the remote output voltage of Channel A and Channel B, respectively. VS_A and VS_B are differential inputs; they function as the main feedback sense points for the control loop.

The VS_A/VS_B sense points on the power rail require an external resistor divider to bring the nominal voltage to 1 V at the VS pins (see Figure 11). This voltage provides the best accuracy for the ADC reading.

VS_A/VS_B use ADC1 for the high accuracy feedback loop and ADC2 for the high speed feedback loop.

ADCs

Σ-Δ ADCs have a resolution of one bit and operate differently from traditional flash ADCs. The equivalent resolution obtainable depends on how long the output bit stream of the Σ-Δ ADC is sampled.

Σ-Δ ADCs also differ from Nyquist rate ADCs in that the quantization noise is not uniform across the frequency spectrum. At lower frequencies the noise is lower, and at higher frequencies the noise is higher (see Figure 12).

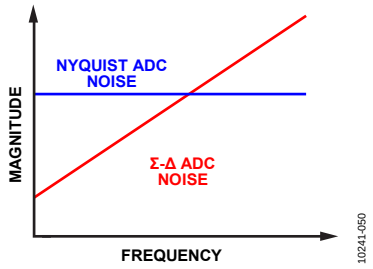


Figure 12. Noise Performance for Nyquist Rate and Σ-Δ ADCs

Two types of Σ-Δ ADCs are used in the feedback loop of the ADP1053: a low frequency ADC and a high frequency ADC.

The low frequency ADC runs at approximately 1.56 MHz. For a specified bandwidth, the equivalent resolution can be calculated as follows:

$$\ln(1.56\ \text{M}/BW)/\ln(2) = N\ \text{bits}$$

For example, at a bandwidth of 95 Hz, the equivalent resolution/noise is

$$\ln(1.5\ \text{M}/95)/\ln(2) = 14\ \text{bits}$$

At a bandwidth of 1.5 kHz, the equivalent resolution/noise is

$$\ln(1.56\ \text{M}/1.5\ \text{k})/\ln(2) = 10\ \text{bits}$$

The high frequency ADC has a clock of 25 MHz. It is comb filtered and outputs at the switching frequency (f_{SW}) into the digital filter.

The equivalent resolution for some sample frequencies is listed in Table 7.

Table 7. Equivalent Resolution for High Frequency ADC at Various Switching Frequencies

f_{SW} (kHz)	High Frequency ADC Resolution
48.8	9 bits
97.7	8 bits
195.3	7 bits
390.6	6 bits

The high frequency ADC has a range of ±10 mV. With the switching frequency (f_{SW}) set to 200 kHz, the quantization noise is 0.156 mV, which is one LSB ($2 \times 10\ \text{mV}/2^7 = 0.156\ \text{mV}$). Increasing f_{SW} to 400 kHz increases the quantization noise to 0.3125 mV (1 LSB = $2 \times 10\ \text{mV}/2^6 = 0.3125\ \text{mV}$).

OVP Sensing (OVP_A, OVP_B)

OVP_A and OVP_B are used for overvoltage protection of Channel A and Channel B, respectively. They are referenced to PGND_A and PGND_B.

The OVP_A/OVP_B sense points on the power rail require an external resistor divider to bring the nominal voltage to 1 V at the OVP_A/OVP_B pins (see Figure 11). This divided-down signal is internally fed into a comparator. The output of the comparator goes to the OVP fault flags. The OVP threshold level can be programmed from 0.75 V to 1.5 V. For more information about the OVP flags, see the Overvoltage Protection (OVP) Flags section.

CURRENT SENSE

The ADP1053 has five separate current sense inputs: CS, CS1_A, CS1_B, CS2_A, and CS2_B. These inputs are used to protect the power supply when the current exceeds the preset current limit. The registers that configure the current sensing inputs must be calibrated to remove errors due to external components. For more information, see the Power Supply Calibration and Trim section.

CS and CS1 (CS1_A/CS1_B) Sensing

CS1_A and CS1_B are typically used for the monitoring and protection of Channel A and Channel B, respectively, whereas CS is used for the unregulated Channel C. Generally, the current inputs are sensed through a current transformer (CT). The input signals at the pins are fed into ADCs for current monitoring. The valid input range of these ADCs is from 0 V to 1.4 V. The input signal is also fed into a comparator for fast overcurrent protection (fast OCP). Typical configurations for current sensing are shown in Figure 13 and Figure 14.

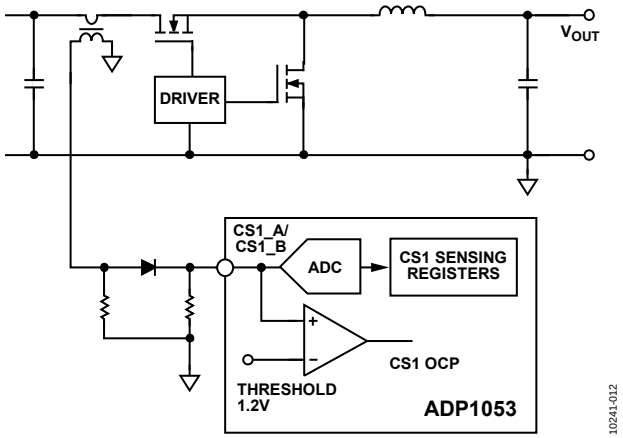


Figure 13. Current Sense 1 (CS1) Operation

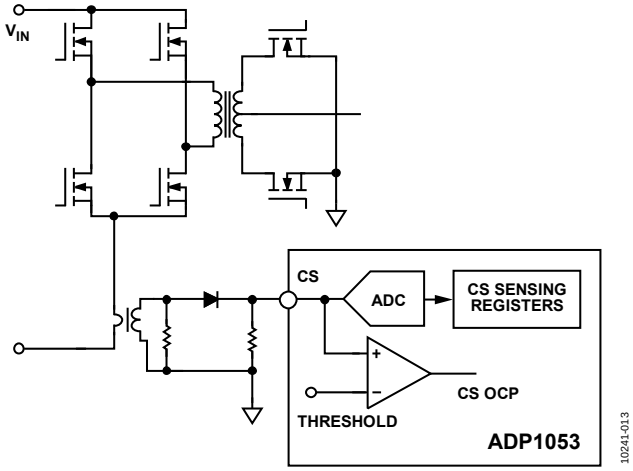


Figure 14. Current Sense (CS) Operation

The CS ADCs measure the average current information, which can be read via the PMBus/I²C interface. This information can also be used for volt-second balance or current balance control. For more information, see the Volt-Second Balance and Current Balance section.

CS2 (CS2+_A/CS2+_B, CS2−_A/CS2−_B) Sensing

CS2_A and CS2_B are typically used for the monitoring and protection of Channel A and Channel B, respectively. CS2_A/CS2_B provide accurate current sensing and monitoring of OCP conditions.

CS2_A/CS2_B current sensing can be configured using a low-side sense resistor or a high-side sense resistor. Depending on the common-mode voltage of the current sensing resistor, the part must be programmed for low-side or high-side mode using Bit 7 of Register 0xFE1A and Register 0xFE1B.

Typical configurations are shown in Figure 15 and Figure 16. The differential inputs are fed into an ADC through a pair of external resistors. Internal matching current sources (nominal value of 200 µA for low-side sensing and 2 mA for high-side sensing) are used to regulate the common-mode voltage of the CS2 pins at approximately 1 V.

For both high-side and low-side current sensing, it is recommended that a 500 pF to 1000 pF capacitor be connected from the CS2_A/CS2_B pins to AGND.

When using low-side resistor current sensing, as shown in Figure 15, the common-mode voltage at the sensing resistor is approximately 0 V. The current sources are 200 µA in low-side current sensing mode. Two matching 5 kΩ resistors are recommended.

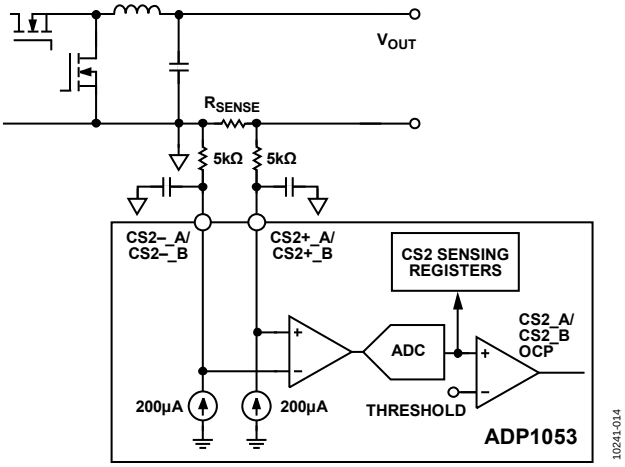


Figure 15. CS2 Low-Side Resistive Current Sensing

When high-side resistor current sensing is required, as shown in Figure 16, the resistor value is calculated based on a 2 mA high-side current source, as follows:

$$R = (V_{OUT} - 1\text{ V})/2\text{ mA}$$

For example, in a 28 V system with high-side current sensing, the value of the resistors used at the CS2 pins is calculated by

$$R = (28\text{ V} - 1\text{ V})/2\text{ mA} = 13.5\text{ k}\Omega$$

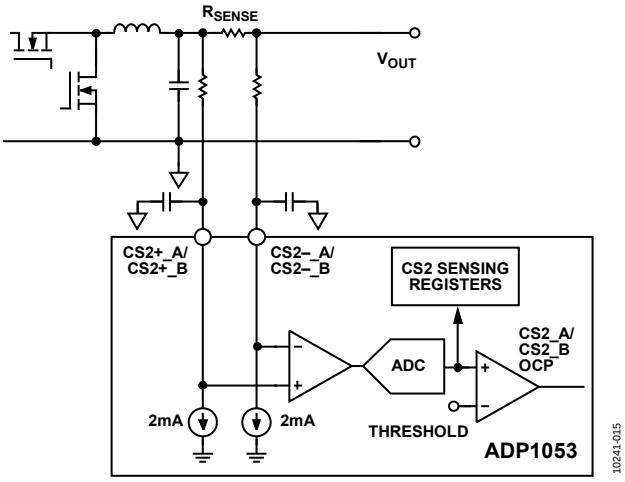


Figure 16. CS2 High-Side Resistive Current Sensing

Matching resistors with 0.1% or better accuracy are recommended to achieve the accuracy specifications.

The full-scale range of the CS2_A/CS2_B ADC is 120 mV. The ADC registers have an update rate of 100 Hz with 12-bit resolution.

The accurate ADC reading is used for CS2 overcurrent protection (OCP) and monitoring. For more information, see the CS2_A and CS2_B Accurate OCP Flags section and the CS2 (CS2_A/CS2_B) Readings section.

SR FETs REVERSE CURRENT PROTECTION

In synchronous rectification applications, reverse current may flow from V_{OUT} through an output inductor, SR FETs, and a sense resistor to the power ground. If the SR FETs are kept on, the large reverse current can damage the SR FETs or the gate driver circuit under extreme conditions.

SR FET reverse current protection is implemented using analog comparators. The reverse current protection threshold can be set using Register 0xFE84 and Register 0xFE85. If the voltage difference between CS2− and CS2+ is greater than the reverse current protection threshold programmed in these registers, the flag (REVERSE_A or REVERSE_B) is triggered. The action taken when the threshold is triggered can be programmed in Register 0xFE83.

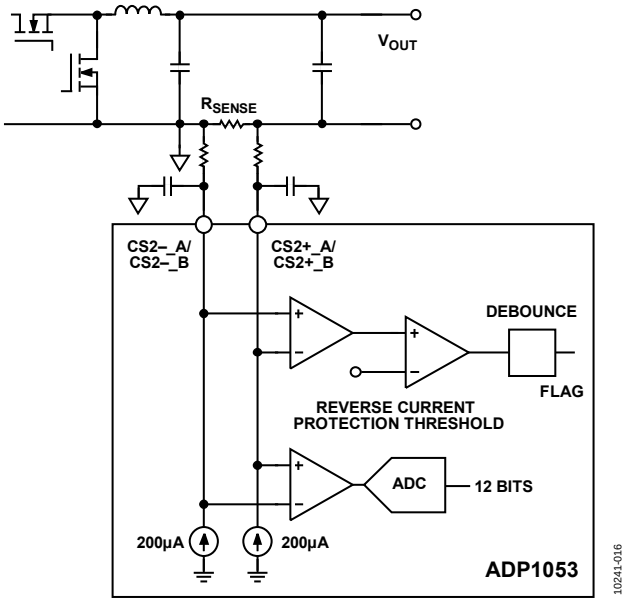


Figure 17. SR FET Reverse Current Protection

CONTROL LOOPS AND FEEDBACK REFERENCES

Channel A and Channel B each have an independent voltage feedback control loop. The feedback uses the sensed signals from VS+_A and VS−_A (for Channel A) and VS+_B and VS−_B (for Channel B).

Register 0xFE22 and Register 0xFE24 set the reference voltage for Channel A; Register 0xFE23 and Register 0xFE25 set the reference voltage for Channel B. Each LSB corresponds to the LSB of the VS_A/VS_B accurate ADC, which is 390.6 µV (see the VS_A and VS_B Readings section).

The output voltage must be divided down using a resistor divider network (R1 and R2 in Figure 11) to set up a feedback voltage at the VS_A/VS_B pins. To convert the register value to an output voltage reference, use the following equation:

$$V_{OUT} = VS_Ref_Voltage_Value \times 390.6\ \mu V \times (R1 + R2)/R2$$

For example, in a 12 V system with an 11 kΩ and 1 kΩ resistor divider, the reference voltage register value for Channel A is 0xB00 (2816 decimal). This register value is converted as follows:

$$V_{OUT} = 2816 \times 390.6\ \mu V \times (11\ k\Omega + 1\ k\Omega)/1\ k\Omega = 13.2\ V$$

To prevent the writing of invalid voltage reference values to the registers, the value written to the registers does not take effect in the closed-loop operation until the GO command is executed. For Channel A, the GO command is executed by writing 1 to Bit 0 in Register 0xFE61. For Channel B, the GO command is executed by writing 1 to Bit 1 in Register 0xFE61. This function allows the user to read back and confirm the reference register value before implementing it for closed-loop operation.

In addition, to prevent a channel from outputting a voltage that is outside its capability, Register 0xFE1E through Register 0xFE21 can be used to set the high and low limits for the feedback references. The reference registers can only be set to values between the low and high limits. If the user attempts to write a value that is out of range to the reference register, the value is ignored and the voltage setting error flag (VS_SET_ERR_A or VS_SET_ERR_B) is set.

Note that the VS_SET_ERR_x flag is set during the writing of the invalid value and is cleared when the write fails; the latched flag is also set but is not cleared.

If the reference register value is not modified but the reference limit register is modified such that the reference is out of range, the write is successful. However, the reference value remains unchanged, and the VS_SET_ERR_x flag is set.

VOLTAGE SETTING WITH SLEW RATE

The ADP1053 provides a method for output voltage adjustment with slew rate control. The slew rate is set using Bits[3:1] of Register 0xFE86 (for VS_A) and Register 0xFE87 (for VS_B). The slew rate function is enabled by setting Bit 0 in Register 0xFE86 or Register 0xFE87. When a slew rate is enabled and the ADP1053 receives an output voltage adjustment command, the ADP1053 adjusts the voltage setting with the preset slew rate.

DIGITAL FILTERS

Channel A and Channel B each have an internal programmable digital filter. A Type III filter architecture is implemented in both digital filters. The low frequency gain, zero location, pole location, and high frequency gain can all be set individually to optimize the loop response.

It is recommended that the ADP1053 GUI be used to program the digital filter. The GUI displays the filter and loop response in Bode plot format. Together with the parameters from the power stages, all stability criteria can be evaluated.

From sensed voltage to the duty cycle, the transfer function of the filter in z-domain is

$$H(z) = \frac{d}{204.8 \times m} \times \frac{z}{z-1} + \frac{c}{5.12} \times \frac{z-b}{z-a}$$

where:
a = filter_pole_register_value/256.
b = filter_zero_register_value/256.
c = high_frequency_gain_register_value.
d = low_frequency_gain_register_value.
m = 1 when 48.8 kHz ≤ f_{SW} < 97.7 kHz.
m = 2 when 97.7 kHz ≤ f_{SW} < 195.3 kHz.
m = 4 when 195.3 kHz ≤ f_{SW} < 390.6 kHz.
m = 8 when 390.6 kHz ≤ f_{SW}.

where f_{SW} is the switching frequency.

To transfer the z-domain value to the s-domain, plug the following equation into Equation 1:

$$z(s) = \frac{2f_S + s}{2f_S - s}$$

Another set of registers configures the filter parameters for light load mode (see the Light Load Mode and Phase Shedding section). These separate registers allow the controller to regulate properly at different load conditions and to move smoothly between normal mode and light load mode.

ACSNS AND INPUT FEEDFORWARD

ACSNS has a low speed, high resolution ADC. This ADC samples at the same PWM switching frequency as Channel C. The ACSNS ADC has an update rate of 800 Hz with 11-bit resolution. The ACSNS value register (Register 0xFED9) provides information for the ACSNS monitoring and flag functions.

To improve line transient performance, a feedforward function is implemented in the ADP1053 using the ACSNS voltage. As shown in Figure 19, the input voltage signal is filtered by an RCD network. The ACSNS value is used to modify the output of the digital filter, and the modified result is fed to the PWM engine.

When the ACSNS input is set to a nominal voltage of 1 V (1280 decimal in the ACSNS value register), there is no effect on the modulation value.

When the output of the ACSNS ADC is below 0x280 (640 decimal), the feedforward function uses 0x280 as the effective input value. This means that the digital filter modulation value can be increased up to twice the original value.

For example, if the digital filter output remains unchanged and the ACSNS voltage changes to 50% of its original value (under an input voltage dip condition), the modulation value of OUT_X doubles (see Figure 18). The modulation edge is still limited by the maximum modulation limit.

The feedforward function is optional. It can be enabled or disabled using Bit 2 of Register 0xFE3E (for Channel A) and Register 0xFE3F (for Channel B).

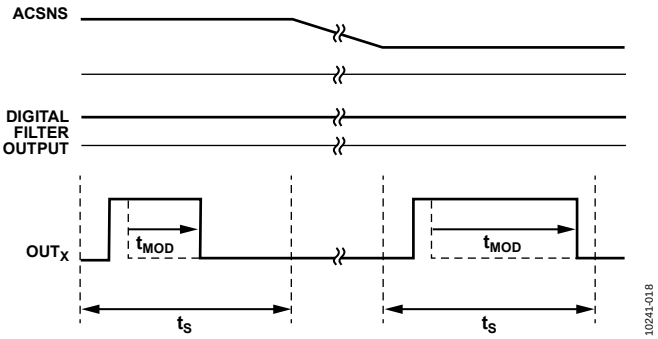


Figure 18. Feedforward Changes Modulation Values

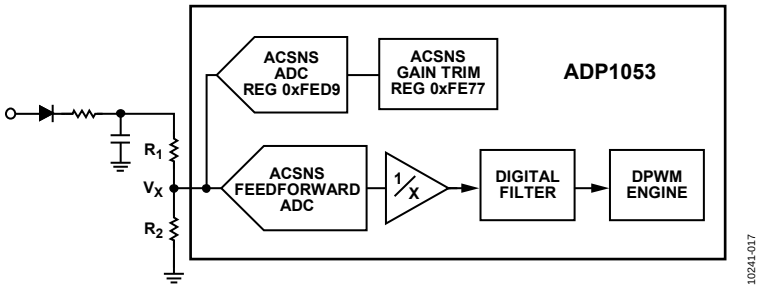


Figure 19. Feedforward Configuration

LIGHT LOAD MODE AND PHASE SHEDDING

The ADP1053 can be configured to disable PWM outputs under light load conditions based on the value of CS2_A and CS2_B. This function is programmed in Register 0xFE69 (for Channel A) and Register 0xFE6A (for Channel B) and can be used to implement phase shedding for multiphase operation. The light load condition flags, LIGHTLOAD_A (Bit 1 of Register 0xFEC0) and LIGHTLOAD_B (Bit 1 of Register 0xFEC1), are based on the reading of CS2_A and CS2_B, respectively.

The light load current thresholds can be programmed independently with Bits[3:0] of Register 0xFE1A and Register 0xFE1B. Each LSB of the threshold setting represents 64 LSBs of the 12-bit CS2_A/CS2_B readings. Because the input range of the CS2_A/CS2_B ADCs is 120 mV, each LSB of the threshold is equal to 1.875 mV. When Bits[3:0] are set to 0, the light load flag remains cleared.

Hysteresis is added to avoid switching between normal mode and light load mode. The threshold setting is the value that causes the part to enter light load mode. The value to exit light load mode is 2.8125 mV (96 LSBs) greater than the threshold to enter light load mode.

For example, in a system with a 2 mΩ sensing resistor, Bits[3:0] of Register 0xFE1A are set to 1001 (9 decimal). Therefore, the threshold to enter light load mode is

$$I_{LIGHTLOAD_IN} = 9 \times 1.875\ \text{mV}/2\ \text{m}\Omega = 8.44\ \text{A}$$

where $I_{LIGHTLOAD_IN}$ is the output current below which the part enters light load mode.

The threshold to exit light load mode and enter forced PWM mode is

$$I_{LIGHTLOAD_OUT} = (9 \times 1.875\ \text{mV} + 2.8125\ \text{mV})/2\ \text{m}\Omega = 9.84\ \text{A}$$

where $I_{LIGHTLOAD_OUT}$ is the output current above which the part exits light load mode.

When a channel enters light load mode, the following actions take place:

- The LIGHTLOAD_A/LIGHTLOAD_B flag is set.
- The configured PWM outputs (programmable using Register 0xFE69 and Register 0xFE6A) are disabled.
- The feedback digital filter changes to the values for the light load condition.

When a channel exits light load mode, the light load flag is cleared, the disabled PWM outputs are reenabled, and the feedback filter changes back to the values for normal mode.

The signal at the FLGO/SYNO pin can be configured as a flag output by setting Bit 3 of Register 0xFE0F. This signal can be programmed to respond to either the LIGHTLOAD_A or LIGHTLOAD_B flag using Bit 4 of Register 0xFE0F. The polarity of the FLGO/SYNO pin can be set to inverted or noninverted using Bit 5 of Register 0xFE0F.

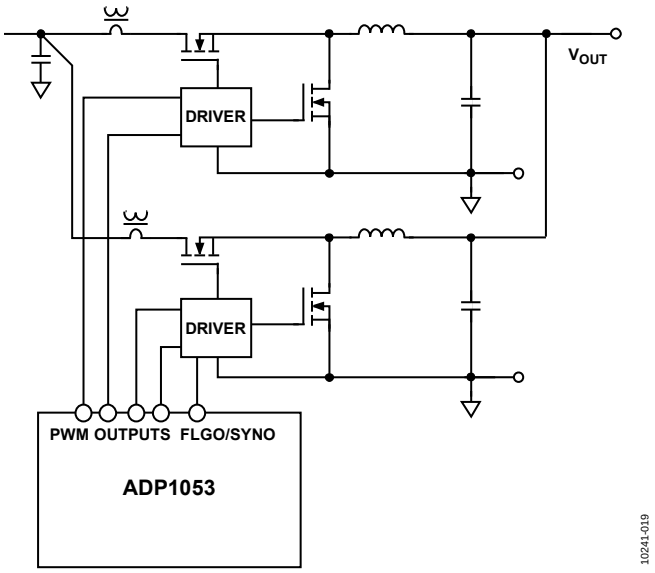


Figure 20. Phase Shedding in Dual-Phase Buck Controller

POWER-GOOD SIGNALS

Each regulated channel of the ADP1053 has a power-good pin: PGOOD_A for Channel A and PGOOD_B for Channel B. The PGOOD_A or PGOOD_B fault flag (Bit 6 of Register 0xFEC0 or Register 0xFEC1) is set when the EEPROM_CRC, POWER_SUPPLY_x, UVP_x, or SOFTSTART_FILTER_x flag is set. The ACSNS and OTWx flags can also be included in the setting of the PGOOD_A and PGOOD_B flags.

An overvoltage or overcurrent event does not directly trigger PGOOD_x, but it can trigger a POWER_SUPPLY_x fault that in turn triggers PGOOD_x. For example, if an overcurrent condition sets the OCP flag and the configured response to the OCP flag is to disable the appropriate PWM outputs, thus causing the power supply output to fall, a POWER_SUPPLY_x fault can be triggered that in turn triggers PGOOD_x. In the same way, an overvoltage condition can also indirectly trigger PGOOD_x.

The PGOOD_A and PGOOD_B pins are open-drain, active low pins. The on and off debounce times for the PGOOD_A and PGOOD_B fault flags are programmable for each flag at 0 ms, 200 ms, 320 ms, or 600 ms using Register 0xFE09.

SOFT START AND SHUTDOWN

PSON Control

The turning on and off of regulated Channel A is controlled by the hardware PSON_A pin and/or the software PSON_A register, depending on the configured settings in Register 0xFE79. In the same way, the turning on and off of regulated Channel B is controlled by the hardware PSON_B pin and/or the software PSON_B register, depending on the configured settings in Register 0xFE7A.

The PSON_A and PSON_B pins and registers can be controlled independently by different enable signals. The pins can also be tied together and triggered by the same signal.

The unregulated Channel C can be programmed to be always on, or it can be programmed to be on when either PSON_A or PSON_B is on. This option is configured using Bit 4 of Register 0xFE7B.

Software Reset

The user can reset the ADP1053 power supply by writing the GO command to Register 0xFE88 (Bit 0 for Channel A; Bit 1 for Channel B). When the GO bit is written, the power supply for Channel A or Channel B is immediately turned off, and the channel is restarted with a soft start after a preset delay. The delay can be programmed to 0 ms, 500 ms, 1 sec, or 2 sec using Bits[3:2] of Register 0xFE88.

PSON Sequencing

For both the regulated Channel A and Channel B and the unregulated Channel C, the turn-on delay, turn-off delay, and ramp rate can be independently configured. The register settings can be used to set up the sequencing of the channels.

Figure 21 shows a typical sequencing diagram.

- The turn-on delays (t_{DON_A}, t_{DON_B}, and t_{DON_C}) are the delay times between the activation of the PSON_A/PSON_B pins or commands that trigger the turn-on signal and the start of the output ramp-up.
- The turn-off delays (t_{DOFF_A}, t_{DOFF_B}, t_{DOFF_C}) are the delay times between the activation of the PSON_A/PSON_B pins or commands that trigger the turn-off signal and the start of the output shutdown.

The turn-on and turn-off delays for Channel A, Channel B, and Channel C can be set to 0 ms, 50 ms, 250 ms, or 1 sec using Register 0xFE79, Register 0xFE7A, and Register 0xFE7B, respectively.

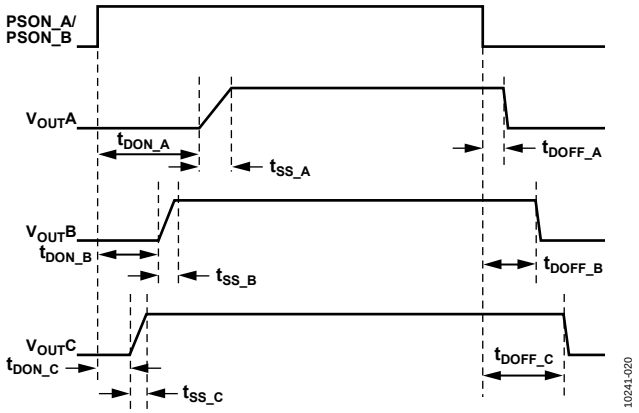


Figure 21. PSON Sequencing Diagram

The PGOOD signal of a master controller can be configured to trigger the PSON signals of multiple slave controllers.

The ADP1053 also has fault link functionality; that is, the part can be configured to shut down an output after another output is shut down.

Soft Start Ramp

For either regulated channel of the ADP1053, the VS_A/VS_B reference voltage increases from 0 V to the regulated reference voltage after the PSON signal is received and after the turn-on delay. The ramp rate for the reference voltage is set in Register 0xFE2A for Channel A and Register 0xFE2B for Channel B. The first column of Table 8 shows the possible ramp rates for the VS_A and VS_B references.

A non-zero prebias may result in a longer turn-on delay and shorter rise time.

Table 8. Soft Start Ramp Timing

VS_A/VS_B Reference Ramp Rate	Channel C Duty Cycle Ramp Rate
1 V/1.75 ms	40 ns/1 switching cycle
1 V/10.5 ms	40 ns/2 switching cycles
1 V/21.0 ms	40 ns/4 switching cycles
1 V/40.2 ms	40 ns/8 switching cycles

For the unregulated Channel C, the duty cycle can be programmed to increase or decrease at a rate set by Bits[5:4] of Register 0xFE68. The duty cycle variation can be set to 40 ns per one, two, four, or eight switching cycles. The soft start time for Channel C is usually faster than the soft start time for the regulated channels.

Two variation values are used for Channel C soft start:

$$t_{SS_C1} = |t_{F1} - t_{R1}|$$

$$t_{SS_C2} = |t_{F2} - t_{R2}|$$

where:
t_{R1} and t_{R2} are the timing values for the rising edges of OUT1 and OUT2, respectively.
t_{F1} and t_{F2} are the timing values for the falling edges of OUT1 and OUT2, respectively.
t_{SS_C1} sets the variation for OUT1, OUT3, OUT5, and OUT7 if these PWM outputs are assigned to Channel C.
t_{SS_C2} sets the variation for OUT2, OUT4, OUT6, and OUT8 if these PWM outputs are assigned to Channel C.

Both edges of a PWM signal assigned to Channel C can implement modulation during soft start. At the initiation of soft start, a modulated edge assigned to Channel C behaves as follows:

- If the edge is configured for positive modulation, the edge timing is the preset value plus the variation value. During soft start, the edge moves to the left until it reaches the preset value.
- If the edge is configured for negative modulation, the edge timing is the preset value minus the variation value. During soft start, the edge moves to the right until it reaches the preset value.

Example

In a fixed duty cycle, full-bridge application, OUT1 through OUT 4 are assigned to Channel C with soft start enabled. The switching frequency is 104.2 kHz, the switching cycle is 9.6 µs, t_{R1} = 0 µs, t_{F1} = 4 µs, t_{R2} = 4.8 µs, t_{F2} = 8.8 µs, t_{R3} = 4.2 µs, t_{F3} = 9.4 µs, t_{R4} = 9 µs, and t_{F4} = 4.6 µs. Therefore, $t_{SS_C1} = t_{SS_C2}$ = 4 µs.

For soft start, the falling edges of OUT1 and OUT2 are configured for negative modulation, and the rising edges of OUT3 and OUT4 are configured for negative modulation.

Given this setup, soft start for Channel C operates as follows:

- OUT1: The rising edge is fixed. At the beginning of soft start, the falling edge is located at $t_{F1} - t_{SS_C1} = 0$, which means a zero duty cycle. The edge moves to the right during soft start and stops at the t_{F1} value of 4 µs.
- OUT2: The rising edge is fixed. At the beginning of soft start, the falling edge is located at $t_{F2} - t_{SS_C2}$ = 4.8 µs, which means a zero duty cycle. The edge moves to the right during soft start and stops at the t_{F2} value of 8.8 µs.
- OUT3: The falling edge is fixed. At the beginning of soft start, the rising edge is located at $t_{R3} - t_{SS_C1}$ = 0.2 µs. The edge moves to the right during soft start and stops at the t_{R3} value of 4.2 µs.
- OUT4: The falling edge is fixed. At the beginning of soft start, the rising edge is located at $t_{R4} - t_{SS_C2}$ = 5 µs. The edge moves to the right during soft start and stops at the t_{R4} value of 9 µs.

To implement soft start for Channel C using a different PWM timing configuration, the user can configure additional bit settings in Register 0xFE68.

- When Bit 3 is set, t_{SS_C1} is forced to follow t_{SS_C2}.
- When Bit 2 is set, $t_{SS_C2} = |t_S - t_{R2}|$, where t_S is the switching cycle for Channel C.
- When Bit 1 is set, $t_{SS_C1} = |t_{F3} - t_{R3}|$.
- When Bit 0 is set, $t_{SS_C2} = |t_{F4} - t_{R4}|$.

Bits[7:6] of Register 0xFE68 are used to prevent the unintentional overlap of the PWM outputs, especially when synchronization is enabled.

When Bit 7 is set, the falling edges of OUT1, OUT2, OUT5, and OUT6 are always after the rising edges in one cycle during soft start.

Bit 6 is valid only when Bit 7 of Register 0xFE68 is set to 1. If Bit 6 is set to 0, the rising edges of OUT3, OUT4, OUT7, and OUT8 are always after the falling edges in one cycle during soft start. If Bit 6 is set to 1, the falling edges of OUT3, OUT4, OUT7, and OUT8 are always after the rising edges in one cycle during soft start.

Flag Timing During Soft Start

The user can program which flags are active during the soft start. All flags are active at the end of the soft start. For more information, see the Flag Blanking During Soft Start section.

For either regulated channel of the ADP1053, the following procedure occurs after the user turns on the power supply (enables PSON_A or PSON_B). See Figure 22.

1. The PSON signal is enabled at t = t_0. The ADP1053 checks that initial flags are OK.
2. The ADP1053 waits for the t_{DON} time before it begins to ramp up the power stage reference voltage at t_1.
3. When the output voltage reaches a steady state, the soft start is completed, and the SOFTSTART_FILTER_A or SOFTSTART_FILTER_B flag is cleared.
4. The PGOOD signal waits for the t_{DGOOD} time before it is enabled at t_3.

The values for t_{DON_A}, t_{DON_B}, t_{DGOOD_A}, and t_{DGOOD_B} are all programmable.

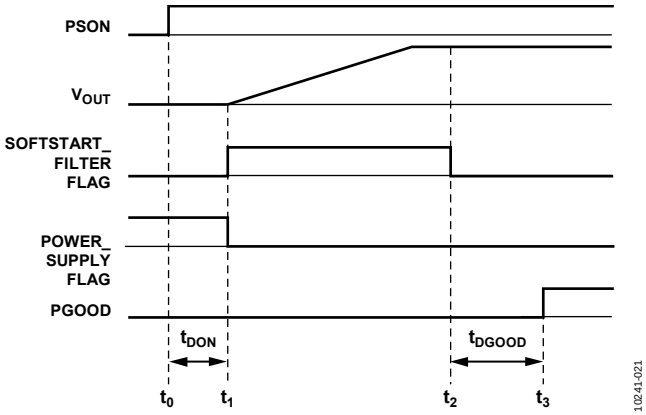


Figure 22. Soft Start Timing Diagram

The restart delay time can be programmed using Register 0xFE88. For example, in the case of a short circuit, the ADP1053 restarts in a soft start sequence every restart delay time. This restart feature, also called "hiccup mode," helps to minimize power dissipation in the event of a short circuit. For more information, see the Protection Actions section.

The SR PWM outputs and the current balance function can be disabled during soft start. For more information, see the PWM Outputs (OUT1 to OUT8) section and the Synchronous Rectifier (SR) Soft Start section.

Flag Timing During Shutdown

When a fault condition occurs, the following flags are set:

- The PGOOD_A or PGOOD_B fault flag is set.
- Depending on the fault and how it is configured, the POWER_SUPPLY_A or POWER_SUPPLY_B flag is enabled after a programmed time.

Digital Filters During Soft Start

A dedicated filter is used during soft start. The filter is disabled at the end of the soft start routine, after which the voltage loop digital filter is used. The soft start filter gain is programmable using Bits[1:0] of Register 0xFE3E and Register 0xFE3F.

The soft start filter is used during the reference ramp time until the high frequency ADCs of VS_A/VS_B are settled. The user can program a debounce time for detecting the settling of the high frequency ADC using Bits[5:4] of Register 0xFE3E and Register 0xFE3F. The debounce time can be set to 5 ms or 10 ms with Bit 5. During the time that the soft start filter is used, the SOFTSTART_FILTER_x flag is set.

SYNCHRONOUS RECTIFIER (SR) SOFT START

The turning on of the synchronous rectification (SR) signals (OUT3, OUT4, OUT7, and OUT8) during a soft start can be programmed in two ways. The SR signals can either be turned on to their full PWM values immediately, or they can be turned on in a soft start fashion, which ensures a smooth output ramp during the soft start.

SR soft start changes the rising edge of the PWM output. Note that the falling edge of an SR PWM output should not be modulated. When turned on in a soft start, the rising edge of the SR PWM output starts at the same instant as the falling edge, which means a zero duty cycle. The rising edge moves left in a step of 40 ns per 1, 4, 16, or 64 switching cycles (programmable using Register 0xFE67). In this way, the SR output ramps up from a zero duty cycle to the desired duty cycle. When the rising edge reaches 0, it wraps to restart at the end of the switching cycle.

When the ADP1053 is programmed to use SR during soft start, the falling edge of SR outputs must be set to a lower value than the rising edge of the following PWM output.

VOLT-SECOND BALANCE AND CURRENT BALANCE

The ADP1053 has two dedicated circuits to maintain current balance/volt-second balance. To configure a PWM output for volt-second balance or current balance, program Bit 4 in the appropriate PWM output setting register. (The PWM output setting registers are Register 0xFE43, Register 0xFE47, Register 0xFE4B, Register 0xFE4F, Register 0xFE53, Register 0xFE57, Register 0xFE5B, and Register 0xFE5F.) Volt-second balance control can be disabled during soft start using Bit 3 of Register 0xFE08.

The balance control gains are programmable in Register 0xFE72. The maximum modulation limit on the duty cycles is programmable at 80 ns and 160 ns using Bit 6 of Register 0xFE72.

When OUT1, OUT2, OUT3, and OUT4 are used for balance control, the user can enable or disable the rising and falling edges using Register 0xFE62 and Register 0xFE63. The direction of the modulation is also programmable.

When OUT5, OUT6, OUT7, and OUT8 are used for balance control, the user can enable or disable the rising and falling edges using Register 0xFE64. The modulation direction is fixed.

When OUT5 and OUT7 are used and edge modulation for balance control is enabled, increasing the balance control modulation moves the edge to the right. For OUT6 and OUT8, increasing the balance control modulation moves the edge to the left.

Volt-Second Balancing (Based on CS Pin Signal)

Volt-second balance control is based on the sensed signal at the CS pin following the rising edge of the OUT1 and OUT2 signals. When enabled, volt-second balance control makes the programmed adjustment to the enabled PWM edges. This feature can be effectively used in full-bridge applications, eliminating the need for a dc blocking capacitor. The circuit monitors the dc current flowing in both halves of the full bridge, stores this information, and compensates the PWM drive signals to ensure equal current flow in both halves of the full bridge. The time required for the circuit to operate effectively can be programmed and is typically in the range of 100 ms. Therefore, during a transient condition, the volt-second balance relies on the overcurrent condition to limit the PWM duty cycle.

Volt-second balance control uses the CS signal; it can be assigned to Channel A or Channel C using Bit 7 of Register 0xFE72. When volt-second balance control is used, OUT1 and OUT2 must be assigned to the appropriate channel (Channel A or Channel C) because the balance control circuit looks only for the rising edges of OUT1 and OUT2 to start the balance control integration.

When the CS signal in the half cycle after the rising edge of OUT1 is higher than the signal in the half cycle after the rising edge of OUT2, the modulation value increases. The PWM output edges move according to the values programmed in Register 0xFE62.

Leading edge blanking functions can also be used at the sensed CS signals for more accurate control results. The blanking time follows the CS OCP blanking time. For more information, see the Overcurrent Protection (OCP) Flags section.

Current Balancing (Based on CS1/CS2 Pin Signals)

Current balancing with regulated feedback is designed for operation in dual-phase, single-output topologies. Current balancing is implemented to control the balance between CS1_A and CS1_B or between CS2_A and CS2_B (use Bit 3 of Register 0xFE72 to select CS1_A/CS1_B or CS2_A/CS2_B).

For dual-phase current balance control, when the CS1_A or CS2_A value is larger than the CS1_B or CS2_B value, the modulation value increases. The actions for different PWM output edges are programmable using Register 0xFE62, Register 0xFE63, and Register 0xFE64.

POWER MONITORING AND FLAGS

The ADP1053 has extensive system and fault monitoring capabilities for the sensed signals. The system monitoring functions include voltage, current, power, and temperature readings. The fault conditions include out-of-limit values for current, voltage, power, and temperature. The limits for the fault conditions are programmable.

The ADP1053 has an extensive set of flags that are set when certain thresholds or limits are reached. For information about the thresholds and limits, see the Flag Registers section.

MONITORING FUNCTIONS

The ADP1053 monitors and reports several signals, including voltages, currents, power, and temperature. All these values are stored in individual registers and can be read through the PMBus/I²C interface.

The accuracy of the ADP1053 is specified relative to the full-scale range (FSR) of the signal that is measured.

VOLTAGE READINGS

VS_A and VS_B Readings

The VS_A and VS_B voltage value registers (Register 0xFED5 and Register 0xFED6, respectively) are updated every 10 ms. The VS_A and VS_B ADCs have an input range of 0 V to 1.6 V and a resolution of 12 bits, which means that the LSB size is 1.6 V/4096 = 390.6 µV. The valid input range is 1.5 V, which means that the maximum ADC output code is limited to 1.5 V/390.6 µV = 3840.

The equation to calculate the ADC code at a specified voltage (V_X) is given by the following formula:

$$ADC\ CODE = V_X/390.6\ \mu V$$

For example, when there is 1 V on the input of the VS_A ADC,

$$VS_A\ ADC\ CODE = 1\ V/390.6\ \mu V = 2560$$

ACSNS Readings

The ACSNS voltage value register (Register 0xFED9) is updated every 1 ms. The ACSNS ADC has an input range of 0 V to 1.6 V and a resolution of 11 bits, which means that the LSB size is 1.6 V/2048 = 781.25 µV. The valid input range is 1.4 V, which means that the ADC output code is limited to 1.4 V/781.25 µV = 1792.

The equation to calculate the ADC code at a specified voltage (V_X) is given by the following formula:

$$ADC\ CODE = V_X/781.25\ \mu V$$

For example, when there is 1 V on the input of the ACSNS ADC,

$$ACSNS\ ADC\ CODE = 1\ V/781.25\ \mu V = 1280$$

CURRENT READINGS

By default, the current reading ADCs are updated every 10 ms. However, Register 0xFE89 can be used to change the update rate to 50 ms, 100 ms, or 200 ms.

CS and CS1 (CS1_A/CS1_B) Readings

The CS, CS1_A, and CS1_B value registers (Register 0xFED0, Register 0xFED1, and Register 0xFED2, respectively) are updated every 10 ms. The CS, CS1_A, and CS1_B ADCs have an input range of 0 V to 1.6 V and a resolution of 12 bits, which means that the LSB size is 1.6 V/4096 = 390.6 µV.

The equation to calculate the ADC code at a specified voltage (V_X) is given by the following formula:

$$ADC\ CODE = V_X/390.6\ \mu V$$

For example, when there is 1 V on the input of the CS ADC,

$$CS\ ADC\ CODE = 1\ V/390.6\ \mu V = 2560$$

CS2 (CS2_A/CS2_B) Readings

The CS2_A and CS2_B value registers (Register 0xFED3 and Register 0xFED4, respectively) are updated every 10 ms. The CS2_A and CS2_B ADCs have an input range of 0 mV to 120 mV and a resolution of 12 bits, which means that the LSB size is 120 mV/4096 = 29.3 µV.

The equation to calculate the ADC code at a specified voltage (V_X) is given by the following formula:

$$ADC\ CODE = V_X \times 4096/Sensing\ Range$$

For example, when there is 40 mV on the input of the CS2_A ADC and the sensing range is 120 mV,

$$CS2_A\ ADC\ CODE = 40\ mV \times 4096/120\ mV = 1365$$

TEMPERATURE READINGS (RTD1 AND RTD2 PINS)

The RTD1 and RTD2 pins are provided for use with an external 100 kΩ NTC thermistor. An internal current source of 10 µA, 20 µA, 30 µA, or 40 µA can be selected. Therefore, with a 100 kΩ thermistor, the voltage on the RTDx pin is 1 V at 25°C.

An ADC on the ADP1053 monitors the voltage on each RTDx pin. The ADC has a 1 kHz bandwidth and 12-bit resolution. The ADC reading is used for overtemperature protection and monitoring. For more information, see the Overtemperature Protection (OTP) and Overtemperature Warning (OTW) Flags section and the Temperature Linearization Scheme section.

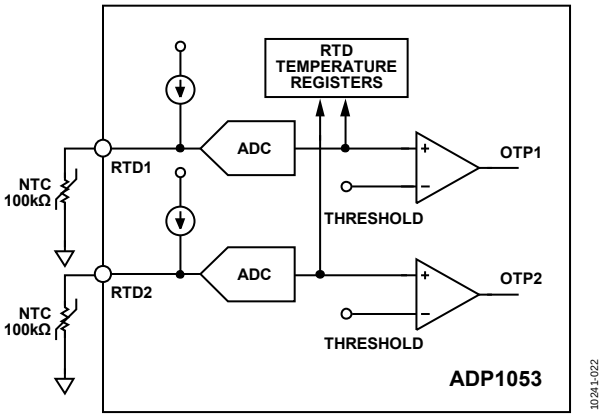


Figure 23. RTD Pin Internal Details

The RTD1 and RTD2 value registers (Register 0xFED7 and Register 0xFED8, respectively) are updated every 10 ms. The ADP1053 stores every ADC sample for 10 ms and then outputs the average value at the end of the 10 ms period.

The RTD1 and RTD2 ADCs have an input range of 0 V to 1.6 V and a resolution of 12 bits, which means that the LSB size is 1.6 V/4096 = 390.6 µV. The valid input range is 1.28 V, which means that the maximum ADC output code is limited to 1.28 V/390.6 µV = 3277.

The output of the RTD ADC is linearly proportional to the voltage on the RTDx pin. However, thermistors exhibit a nonlinear function of resistance vs. temperature. Therefore, the user must perform postprocessing on the RTD ADC reading to accurately read the temperature.

By connecting an external resistor (R_{EXT}) in parallel with the NTC thermistor (TH), a constant current can be used to achieve linearization (see Figure 24).

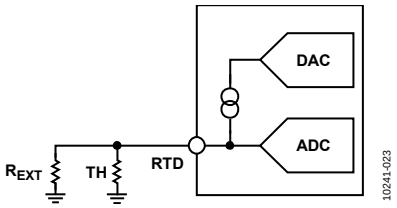


Figure 24. Temperature Measurement Using Thermistor

An internal, precision current source of 10 µA, 20 µA, 30 µA, or 40 µA can be selected. This current source can be fine-tuned by means of an internal DAC to compensate for thermistor accuracy (see the Calibrating for Accuracy section).

The user can select the output current source using Bits[7:6] of the RTD1 and RTD2 current source settings registers (Register 0xFE80 and Register 0xFE81, respectively).

The ADP1053 implements a linearization scheme based on a preselected combination of external components and current selection for best performance when linearizing measured temperatures in the industrial range.

For more information about the required thermistor and selecting and trimming the precision current sources, see the Temperature Linearization Scheme section.

Optionally, the user can process the RTD reading and perform postprocessing in the form of a lookup table or polynomial equation to match the specific NTC thermistor used.

With the internal current source set to 46 µA, the equation to calculate the ADC code at a specified NTC value (R_X) is given by the following formula:

$$ADC\ CODE = 46\ \mu A \times R_X/1.6 \times 4096$$

For example, at 60°C, the NTC at the RTDx pin is 21.82 kΩ.

$$RTD\ ADC\ CODE = 46\ \mu A \times 21.82\ k\Omega/1.6 \times 4096 = 2570$$

TEMPERATURE LINEARIZATION SCHEME

The ADP1053 implements a linearization scheme based on a preselected combination of thermistor (100 kΩ), external resistor (16.5 kΩ, 1%), and the 46 µA current source for best performance when linearizing measured temperatures in the industrial range.

The required NTC thermistor should have a resistance of 100 kΩ, 1%, such as the NCP15WF104F03RC (beta = 4250, 1%). It is recommended that 1% tolerance be used for both the resistor and beta value.

Calibrating for Accuracy

Register 0xFE80 and Register 0xFE81 set the value of the current source on the RTD1 and RTD2 pins, respectively. Bits[7:6] set the value of the current source to 10 µA, 20 µA, 30 µA, or 40 µA. Bits[5:0] can be used to fine-tune the current value. By fine-tuning the internal current source, component tolerance can be compensated for and errors can be minimized. One LSB in Bits[5:0] = 156.25 nA. A decimal value of 1 adds 156.25 nA to the current source set by Bits[7:6]; a decimal value of 63 adds 9.84375 µA. There is no negative adjustment to the current source.

To calibrate the part, a known reference value can be used, such as the RTDx ADC code at 25°C. For an ideal thermistor with a resistance of R_0, the ADC code reading should be the value derived from the following equation:

$$ADC\ CODE = 46\ \mu A \times (R_{EXT}//R_0)/390.6\ \mu V$$

This fine-tuning adjusts the output current slightly to null out any inaccuracies on the thermistor (for example, tolerance on R_0 causing error curves to shift accordingly).

Reading the Linearized Temperature

The PMBus READ_TEMPERATURE_1 and READ_TEMPERATURE_2 commands (Command 0x8D and Command 0x8E) return the current temperature for RTD1 and RTD2 according to an internal linearization scheme. See Table 1 for the specified accuracy of these measurements.

As per the PMBus specification, the temperature reading result is a word in the following format:

$$X = Y \times 2^N$$

where:
X is the temperature value in °C.
Y is the twos complement mantissa (Bits[10:0]). Bit 10 is the sign bit, which is always equal to 0.
N is the twos complement integer exponent (Bits[15:11]).

In the ADP1053, N is always equal to 0. The register value represents temperature readings in degrees Celsius (°C). The temperature reading result is represented in 8-bit decimal format in °C.

Note that in the PMBus read format implemented in the ADP1053, the lowest possible temperature that can be read is 0°C. Reading Bits[9:0] gives the actual positive temperature in °C. To read the actual unconverted temperature, the user can read the ADC code from Register 0xFED7 and Register 0xFED8.

CHANNEL A AND CHANNEL B DUTY CYCLE READINGS

The Channel A and Channel B duty cycle value registers (Register 0xFEDA and Register 0xFEDB, respectively) are updated every 10 ms. The duty cycle for Channel A and Channel B is calculated using the rising and falling edge timings of OUT1, OUT2, OUT5, or OUT6, depending on which PWM output is assigned to the corresponding channel. If more than one of these PWM outputs is assigned to a channel, the PWM output used in the duty cycle calculation is selected in the following order: OUT1, OUT2, OUT5, OUT6.

FLAGS

The ADP1053 has an extensive set of flags (Register 0xFEC0 to Register 0xFECB) that are set when certain limits, conditions, and thresholds are reached. These flags include

- Housekeeping flags, such as VDD_OV, EEPROM_CRC, and EEPROM_UNLOCKED.
- Flags that can be programmed for protection responses, such as OVP_A, OVP_B, UVP_A, UVP_B, ACSNS, CS_OCP, CS1_A_OCP, CS1_B_OCP, CS2_A_OCP, CS2_B_OCP, OTP1, OTP2, FLAGIN, REVERSE_A, and REVERSE_B.
- Status flags, such as PGOOD_A, PGOOD_B, POWER_SUPPLY_A, POWER_SUPPLY_B, POWER_SUPPLY_C, MODULATION_A, MODULATION_B, SOFTSTART_FILTER_A, SOFTSTART_FILTER_B, VS_SET_ERR_A, VS_SET_ERR_B, LIGHTLOAD_A, LIGHTLOAD_B, FLAGOUT, OTW1, and OTW2.

For detailed descriptions of the flags, see the Flag Registers section.

The debounce time of some flags is programmable (see Table 9). The debounce time is the time during which the fault condition must be continuously triggered before the flag is set. Refer to the corresponding register settings for details.

Table 9. Debounce Time of Flags

Flags	Debounce Time
VDD_OV	2 µs or 500 µs
OVP_A, OVP_B	0 µs, 0.96 µs, 2.24 µs, or 8 µs
UVP_A, UVP_B	0 ms or 100 ms
ACSNS	0 ms, 2.6 ms, 10.4 ms, or 100 ms
CS_OCP, CS1_A_OCP, CS1_B_OCP	0 ns, 40 ns, 80 ns, or 120 ns
CS2_A_OCP, CS2_B_OCP	0 ms, 20 ms, 200 ms, or 1 sec
OTP1, OTP2	100 ms
OTW1, OTW2	0 ms or 100 ms
FLAGIN	0 µs or 100 µs
REVERSE_A, REVERSE_B	40 ns or 200 ns

The debounce time is for flag setting. There is no debounce time for flag clearing, which means that when the flag condition no longer exists, the flag is cleared immediately. However, the reenable delay time functions as the debounce time for flag clearing. For more information, see the Protection Actions section.

HOUSEKEEPING FLAGS

The VDD_OV flag (Bit 6 of Register 0xFEC2) is set when the VDD voltage is higher than the 3.9 V OVLO threshold. The debounce time can be set to 2 µs or 500 µs using Bit 4 of Register 0xFE06. When the VDD_OV flag is set, the ADP1053 shuts down. If Bit 5 of Register 0xFE06 is set, the flag is always cleared regardless of the VDD voltage.

The EEPROM_CRC flag (Bit 1 of Register 0xFEC2) indicates that an error has occurred when downloading the EEPROM contents to the internal registers. The part shuts down and requires a PSON_A/PSON_B reset to restart.

The EEPROM_UNLOCKED flag (Bit 4 in Register 0xFEC3) indicates that the EEPROM is in the unlocked state and can be updated.

OVERVOLTAGE PROTECTION (OVP) FLAGS

The ADP1053 has two OVP analog comparators for Channel A and Channel B, as shown in Figure 11. The OVP threshold for each channel can be programmed from 0.75 V to 1.5 V using Register 0xFE26 for Channel A and Register 0xFE27 for Channel B.

The OVP_A and OVP_B flags (Bit 2 in Register 0xFEC0 and Register 0xFEC1, respectively) are set when the sensed voltage between the OVP_A and PGND_A pins (or between the OVP_B and PGND_B pins) exceeds the programmed threshold. The debounce time of the flag can be set to 0 µs, 1 µs, 2 µs, or 8 µs using Register 0xFE26 and Register 0xFE27. There is also a 40 ns propagation delay, which is measured from when the OVP_A or OVP_B voltage exceeds the threshold to when the comparator output status is changed.

The response to the OVP_A and OVP_B flags can be programmed using Register 0xFE02. For more information, see the Protection Actions section and the Flag Configuration Registers section.

UNDERVOLTAGE PROTECTION (UVP) FLAGS

The UVP_A and UVP_B flags (Bit 3 in Register 0xFEC0 and Register 0xFEC1, respectively) are set when the voltage reading at VS_A and VS_B goes below the UVLO threshold (programmable in Register 0xFE28 and Register 0xFE29). The UVP circuits compare Bits[6:0] with the seven MSBs of the VS_A/VS_B value registers, which means that each LSB of the UVP threshold corresponds to 1.6 V × 32/4096 = 12.5 mV.

For example, with an 11 kΩ/1 kΩ divider and with Bits[6:0] of Register 0xFE28 = 0x30 (48 decimal), the UVP_A threshold is

$$12.5\ \text{mV} \times 48 \times 12 = 7.2\ \text{V}$$

Note that UVP is ignored when its threshold value is set to 0.

The debounce time of the flag can be set to 0 ms or 100 ms using Bit 7 of Register 0xFE28 and Register 0xFE29. Because the VS_A/VS_B reading is the average value over every 10 ms, there is an additional debounce and delay time of up to 10 ms.

The response to the UVP_A and UVP_B flags can be programmed using Register 0xFE03. For more information, see the Protection Actions section and the Flag Configuration Registers section. During the soft start, PSON delay, and flag reenable time, the UVP_A and UVP_B flags are blanked.

ACSNS FLAG

The ACSNS flag (Bit 2 in Register 0xFEC2) is set when the voltage reading at ACSNS goes below the threshold that is programmed using Bits[5:2] of Register 0xFE78. The value in Bits[5:2] is compared with the four MSBs of the ACSNS value.

For example, with an 11 kΩ/1 kΩ divider, Bits[5:2] of Register 0xFE78 are set to 0101 (5 decimal). These bits are compared with the four MSBs of the 8-bit ACSNS value. The ACSNS threshold is

$$(1.6\ V/16) \times 5 \times 12 = 6.00\ V$$

The debounce time of the flag can be set to 0 ms, 2.6 ms, 10.4 ms, or 100 ms using Bits[1:0] of Register 0xFE78. Because the ACSNS reading is the average value over every 1 ms, there is an additional debounce and delay time of up to 1 ms.

The response to the ACSNS flag can be programmed using Register 0xFE04. For more information, see the Protection Actions section and the Flag Configuration Registers section.

In addition, the user can optionally include the ACSNS flag in the PGOOD_A/PGOOD_B flags using Bit 7 of Register 0xFE78. The debounce time for the ACSNS flag when it is included in the PGOOD_A/PGOOD_B flags is different from that of the ACSNS flag itself. The debounce time can be set to 0 ms or 2.6 ms using Bit 6 of Register 0xFE78.

OVERCURRENT PROTECTION (OCP) FLAGS

The ADP1053 has a fast OCP function for CS, CS1_A, and CS1_B and an accurate OCP function for CS2_A and CS2_B. CS, CS1_A, CS1_B, CS2_A, and CS2_B have separate OCP circuits to provide protection for all three channels. The response to the OCP flags can be programmed using Register 0xFE00, Register 0xFE01, and Register 0xFE04.

CS, CS1_A, and CS1_B Fast OCP Flags

CS1_A OCP, CS1_B OCP, and CS OCP provide fast overcurrent protection for Channel A, Channel B, and Channel C, respectively. OCP protection is implemented with internal analog comparators, as shown in Figure 13 and Figure 14. When the voltage at the CS, CS1_A, or CS1_B pin exceeds the fixed 1.2 V threshold, the corresponding OCP flag is set (Bit 5 in Register 0xFEC0 for Channel A, Register 0xFEC1 for Channel B, and Register 0xFEC2 for Channel C). There is a 110 ns (max) propagation delay in the comparators.

A blanking time of 0 ns, 40 ns, 80 ns, 120 ns, 200 ns, 400 ns, 600 ns, or 800 ns can be set to ignore the current spike at the beginning of the current signal. The blanking time is set using Register 0xFE6F, Register 0xFE70, and Register 0xFE71. During the blanking time, the OCP comparator output is ignored. The blanking time of the CS comparator is referenced to the rising edges of OUT1 and OUT2. The blanking time of the CS1_A and CS1_B comparators is referenced to the rising edge of OUT1, OUT2, OUT5, or OUT6 (programmable with Register 0xFE6B and Register 0xFE6C).

A debounce time of 0 ns, 40 ns, 80 ns, or 120 ns (programmable with Register 0xFE6F, Register 0xFE70, and Register 0xFE71) can also be added to improve the noise immunity of the OCP circuit. The debounce time is the minimum time that the CS, CS1_A, or CS1_B signal must be continuously above the OCP threshold before the flag triggers an action.

Figure 25 shows an example of CS OCP timing with the rising edge of OUT1 as the blanking time reference. After the CS_OCP flag is set, it is not cleared until the beginning of the next switching cycle. The latched CS_OCP flag is not cleared at the beginning of the switching cycle. The CS1_A_OCP and CS1_B_OCP flags function in the same way for Channel A and Channel B, respectively.

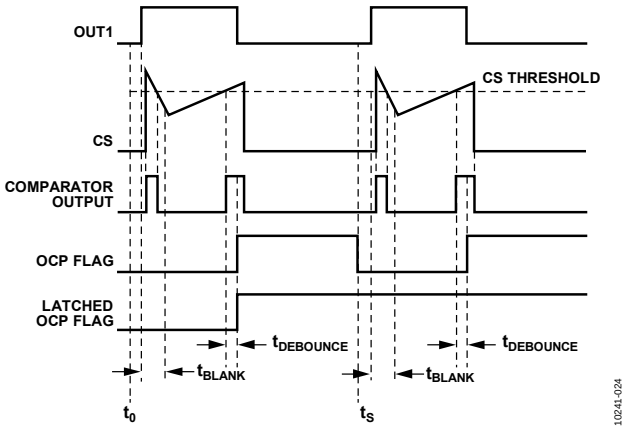


Figure 25. Fast OCP Flag Timing

A flag timeout value can also be programmed using Bits[3:2] of Register 0xFE6F, Register 0xFE70, and Register 0xFE71. This timeout specifies the number of consecutive switching cycles with OCP triggered that must occur before the OCP flag can be set. In Figure 26, the flag timeout value is set to eight cycles.

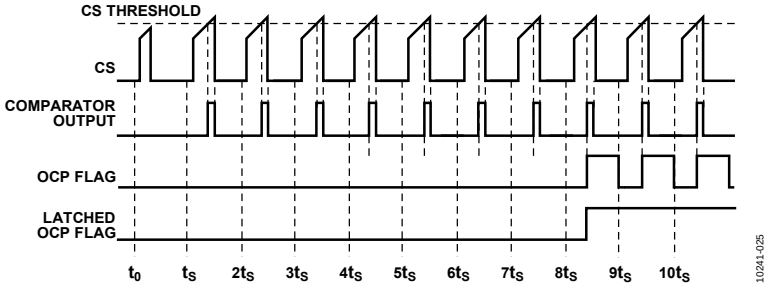


Figure 26. Fast OCP Timeout

The actions triggered by the CS_OCP, CS1_A_OCP, and CS1_B_OCP flags can be programmed with Register 0xFE00 and Register 0xFE04. For more information, see the Protection Actions section and the Flag Configuration Registers section.

Cycle-by-Cycle Limit Function for SR Outputs

In addition to the CS_OCP, CS1_A_OCP, and CS1_B_OCP flags, a cycle-by-cycle limit function can be used. This function is triggered by the CS, CS1_A, and CS1_B OCP comparator output. For example, when the CS OCP comparator output is high, all PWM outputs assigned to Channel C are disabled for the remainder of the switching cycle. The outputs are reenabled at the start of the next switching cycle. During a switching cycle, if the rising edge of a PWM output occurs after the flag is cleared, the PWM output is not disabled.

To avoid current overstress of the body diode of the synchronous rectifiers, the cycle-by-cycle OCP actions of the SR PWM outputs (OUT3, OUT4, OUT7, and OUT8) can be programmed with Register 0xFE6D. The SR PWM outputs can be programmed the same way as other PWM outputs (see the CS, CS1_A, and CS1_B Fast OCP Flags section), or they can be programmed so that when an OCP condition occurs on the channel, the output is turned on. There is a 145 ns to 180 ns delay (dead time) between the comparator output going high and the turning on of the SR PWM outputs. The falling edge of the SR PWM outputs still follows the programmed value.

Note that cycle-by-cycle protection is not affected by the flag timeout settings (the flag timeout values are set in Register 0xFE6F, Register 0xFE70, and Register 0xFE71).

The comparator output can be completely ignored by setting Bit 7 in Register 0xFE6F, Register 0xFE70, and Register 0xFE71.

CS2_A and CS2_B Accurate OCP Flags

The CS2_A_OCP and CS2_B_OCP flags (Bit 4 in Register 0xFEC0 and Register 0xFEC1, respectively) are set when the current reading at CS2_A or CS2_B exceeds the threshold programmed in Register 0xFE18 and Register 0xFE19, respectively. A flag debounce time of 0 ms, 20 ms, 200 ms, or 1 sec can be set using Register 0xFE1A and Register 0xFE1B. Because the CS2_A/CS2_B reading is the average value over every 10 ms, there is an additional debounce and delay time of up to 10 ms.

The response to the CS2_A_OCP and CS2_B_OCP flags can be programmed using Register 0xFE01. For more information, see the Protection Actions section and the Flag Configuration Registers section.

OVERTEMPERATURE PROTECTION (OTP) AND OVERTEMPERATURE WARNING (OTW) FLAGS

The ADP1053 provides overtemperature protection flags (OTP1 and OTP2) and overtemperature warning flags (OTW1 and OTW2) for each thermistor input, RTD1 and RTD2. The OTW1/OTW2 flag is set when the temperature exceeds a programmable threshold above the OTP1/OTP2 threshold; the OTW1/OTW2 threshold can be set to 3.125 mV (1 LSB), 6.25 mV (2 LSBs), 9.375 mV (3 LSBs), or 12.5 mV (4 LSBs) using Register 0xFE8A. The OTW1/OTW2 flag is cleared when the temperature falls below the OTW1/OTW2 threshold. The OTW1/OTW2 flag can also be configured to activate the PGOOD_A/PGOOD_B flag using Bit 6 and Bit 2 in Register 0xFE8A. The OTW1 and OTW2 flags are Bits[3:2] of Register 0xFEC4.

If the temperature sensed at the RTD1 pin exceeds the threshold programmed using Register 0xFE75, the OTP1 flag (Bit 3) is set in Register 0xFEC2. If the temperature sensed at the RTD2 pin exceeds the threshold programmed using Register 0xFE76, the OTP2 flag (Bit 4) is set in Register 0xFEC2. These flags are cleared when the OTP1/OTP2 condition is cleared, that is, when the temperature falls below the temperature threshold set in the OTW1/OTW2 settings register (Register 0xFE8A).

The overtemperature hysteresis is the difference between the OTPx and OTWx temperature thresholds. Note that the threshold voltage is in inverse relationship to the temperature. Figure 27 illustrates the OTPx and OTWx temperature settings.

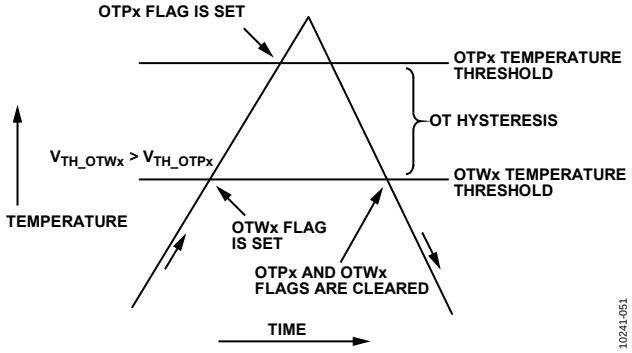


Figure 27. OTP, OTW, and OT Hysteresis

The debounce time of the flag is fixed at 100 ms. Because the RTD1/RTD2 reading is the average value over every 10 ms, there is an additional debounce and delay time of up to 10 ms.

The response to the OTP1/OTP2 flags can be programmed using Register 0xFE05. For more information, see the Protection Actions section and the Flag Configuration Registers section.

The RTD trim is required to make accurate temperature readings at the lower end of the RTD ADC range. This results in a more accurate measurement for determining the OTP threshold (see the RTD1, RTD2, OTP1, and OTP2 Trim section).

EXTERNAL FLAG INPUT (FLGI/SYNI PIN)

The FLGI/SYNI pin can be configured as a synchronization reference or as an external flag input. When this pin is configured as a flag input, an external fault signal can be sent to the pin. This flag is Bit 0 of Register 0xFEC2. The debounce time for this flag can be set to 0 µs or 100 µs using Register 0xFE0F.

The response to the FLAGIN flag can be programmed using Register 0xFE06. For more information, see the Protection Actions section and the Flag Configuration Registers section.

PROTECTION ACTIONS

The VDD_OV flag can be programmed to be ignored or to shut down the part and restart it using Bit 5 of Register 0xFE06.

The following flags can be configured to trigger protection actions: OVP_A, OVP_B, UVP_A, UVP_B, ACSNS, CS_OCP, CS1_A_OCP, CS1_B_OCP, CS2_A_OCP, CS2_B_OCP, OTP1, OTP2, FLAGIN, REVERSE_A, and REVERSE_B.

Each of these flags can be individually programmed to trigger one of the following actions:

- No action (flag ignored).
- Disable PWM outputs in Channel A.
- Disable PWM outputs in Channel B.
- Disable all PWM outputs.

After the condition that triggered one of these flags is resolved and the flag is cleared, the ADP1053 can be programmed to respond as follows:

- Reenable the disabled PWM outputs immediately with no soft start.
- After the reenable delay time elapses, reenable the disabled PWM outputs with a soft start sequence.
- Keep the PWM outputs disabled; the PSON signal must be used to reenable the PWM outputs with a soft start sequence.
  - If the flag action is to disable the PWM outputs in Channel A, resetting PSON_A reenables the disabled PWM outputs.
  - If the flag action is to disable the PWM outputs in Channel B, resetting PSON_B reenables the disabled PWM outputs.
  - If the flag action is to disable all PWM outputs, resetting both PSON_A and PSON_B reenables all PWM outputs.

The first flag with an action that causes the PWM outputs to be disabled and a resolution that includes a soft start is recorded as the first flag ID. For more information, see the First Flag ID Recording section.

A reenable delay can be set for all flags; this delay is used if the configured action for a flag is to reenable the PWM outputs after the reenable delay. This delay can be set to 250 ms, 500 ms, 1 sec, or 2 sec using Bits[7:6] of Register 0xFE06 (see Figure 28).

An additional PSON delay can be added to the reenable delay for each channel using Bits[7:5] of Register 0xFE7B. This delay is used to control the turn-on timing of different channels.

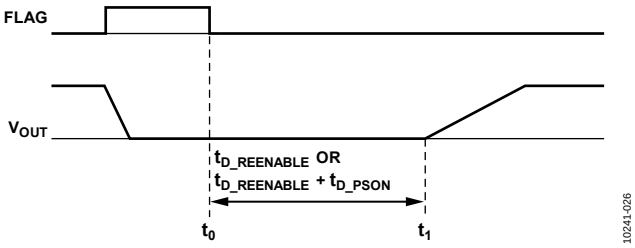


Figure 28. Flag Reenable Delay

During the reenable delay time and the PSON delay time, the UVP_A and UVP_B flags are blanked. The ACSNS flag can also be programmed to be blanked using Bit 6 of Register 0xFE08. Other flags can be individually programmed to be ignored during the soft start (see the Flag Blanking During Soft Start section).

FLAG BLANKING DURING SOFT START

Flag blanking means that when the fault condition is met, the corresponding flag is set but there are no related actions.

The following flags are always blanked during soft start:

- FLAGIN, OTP1, OTP2, and ACSNS flags (all channels)
- UVP_A and REVERSE_A (Channel A)
- UVP_B and REVERSE_B (Channel B)

The following flags can be programmed to be blanked during soft start using Register 0xFE07.

- CS_OCP flag (Channel C)
- OVP_A, CS1_A_OCP, and CS2_A_OCP flags (Channel A)
- OVP_B, CS1_B_OCP, and CS2_B_OCP flags (Channel B)

Note that if a flag is blanked during soft start, it is also blanked during the PSON delay time.

LATCHED FLAGS

The ADP1053 also has a set of latched flag registers (Register 0xFEC5 to Register 0xFEC9). Flags in a latched flag register remain set so that intermittent faults can be detected.

Reading a latched flag register resets the flags in that register (provided that the fault no longer exists). A PSON signal can also reset the latched flags.

- PSON_A resets the flags in Register 0xFEC5, Register 0xFEC7, Register 0xFEC8, and Register 0xFEC9.
- PSON_B resets the flags in Register 0xFEC6 through Register 0xFEC9.

FIRST FLAG ID RECORDING

When the ADP1053 registers one or more fault conditions, it stores the first flag in a dedicated register (Register 0xFECA for Channel A and Register 0xFECB for Channel B). The first flag ID represents the first flag that triggers a response and requires a soft start after the fault is resolved. The following types of flags are not recorded in the first flag ID register:

- Flags that are configured to be ignored
- Flags whose configured action causes PWM outputs to be disabled but which do not use a soft start to reenable the PWM outputs after the fault is resolved

For more information, see the Protection Actions section.

The first flag ID registers give the user more information for fault diagnosis than a simple flag. These registers also store the previous first flag ID. The status of the first flag ID registers can be downloaded to the EEPROM (set Bit 5 of Register 0xFE08).

The contents of the first flag ID registers are stored until read by the user. The flag ID is also saved in EEPROM. In this way, the user can read the flag information even if the ADP1053 is powered off.

The Channel A first flag ID register (Register 0xFECA) records the first flag ID of the fault that shut down Channel A; the Channel B first flag ID register (Register 0xFECB) records the first flag ID of the fault that shut down Channel B.

Figure 29 shows the timing of the first flag ID recording scheme. Table 10 describes the actions shown in Figure 29.

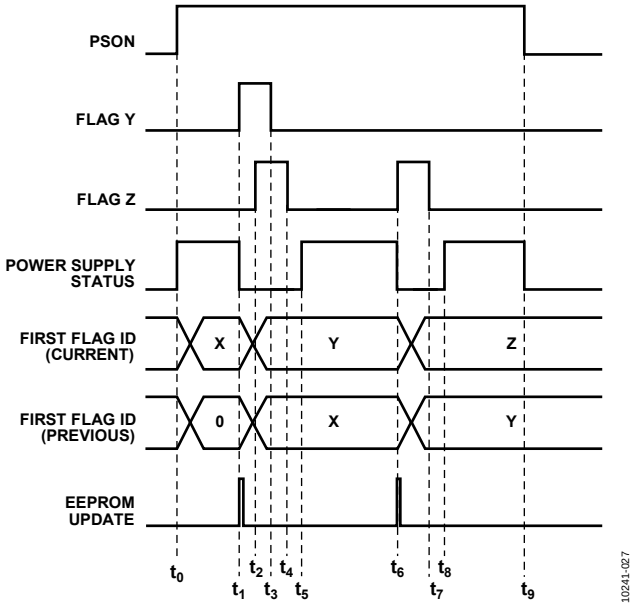


Figure 29. First Flag ID Timing

The first flag ID recording function can be disabled by setting Bit 5 to 0 in Register 0xFE08.

Table 10. First Flag ID Timing

Step	Action	Power Supply	First Flag ID Register	
			Previous Flag ID	Current Flag ID
t_0	The PSON signal turns on the power supply. The ADP1053 reads the first flag ID from the EEPROM and saves it to the first flag ID register as both the current ID and the previous ID.	On	Flag X	Flag X
t_1	A fault (Flag Y) shuts down the power supply. Flag Y is now the current flag ID, and Flag X is the previous flag ID. The first flag ID register is updated accordingly; the EEPROM is then updated to save this information.	Off	Flag X	Flag Y
t_2	Another fault (Flag Z) occurs while the power supply is off. Because Flag Z is not the first flag that caused the shutdown, neither the first flag ID register nor the EEPROM is updated.	Off	Flag X	Flag Y
t_3	Flag Y is cleared, but Flag Z keeps the power supply off. The first flag ID register is not updated.	Off	Flag X	Flag Y
t_4	Flag Z is cleared. The first flag ID register is not updated.	Off	Flag X	Flag Y
t_5	The power supply is turned on again after the reenable delay. The first flag ID register is not updated.	On	Flag X	Flag Y
t_6	The fault indicated by Flag Z shuts down the power supply. Flag Z is now the current flag ID, and Flag Y is the previous flag ID. The first flag ID register is updated accordingly; the EEPROM is then updated to save this information.	Off	Flag Y	Flag Z
t_7	Flag Z is cleared. The first flag ID register is not updated.	Off	Flag Y	Flag Z
t_8	The power supply is turned on again after the reenable delay. The first flag ID register is not updated.	On	Flag Y	Flag Z
t_9	PSON turns off the power supply.	Off		

POWER SUPPLY CALIBRATION AND TRIM

The ADP1053 allows the entire power supply to be calibrated and trimmed digitally in the production environment. It can calibrate items such as output voltage and trim for tolerance errors introduced by sense resistors, current transformers, and resistor dividers, as well as for its own internal circuitry. The part comes factory trimmed, but it can be retrimmed by the user to compensate for the errors introduced by external components in the system.

To unlock the trim registers for write access, write to the TRIM_PASSWORD register (Command 0xD6). Write the trim password twice (the factory default password is 0xFF).

The trim registers are Register 0xFE10 through Register 0xFE17, Register 0xFE1C, Register 0xFE1D, Register 0xFE6E, Register 0xFE73, Register 0xFE74, Register 0xFE77, and Register 0xFE7C through Register 0xFE7F. For complete information about these registers, see the Manufacturer-Specific Extended Command Register Descriptions section.

CS, CS1_A, AND CS1_B GAIN TRIM

To calibrate the CS, CS1_A, and CS1_B ADCs, 1 V is applied between the CS/CS1_A/CS1_B pin and AGND. The CS/CS1_A/CS1_B gain trim register (Register 0xFE6E, Register 0xFE10, or Register 0xFE11, respectively) is altered until the CS/CS1_A/CS1_B value in the appropriate value register reads 2560 decimal (0xA00). The CS, CS1_A, and CS1_B value registers are Register 0xFED0, Register 0xFED1, and Register 0xFED2, respectively.

CS2_A AND CS2_B OFFSET AND GAIN TRIM

CS2_A and CS2_B Offset Trim

Offset errors are caused by the combined mismatch of the external level-shifting resistors and internal current sources. The offset trim has both an analog and a digital component. With 0 V at the CS2 input, the desired ADC reading is 0 LSB.

The analog offset trim is performed to achieve a differential input voltage of 0 V. The digital offset trim is performed to achieve an ADC reading of 0 LSB. It is important to perform the offset trim in the following order.

1. Select high-side or low-side current sensing using Register 0xFE1A or Register 0xFE1B.
2. Set the digital offset trim setting to 0x00 using Register 0xFE14 or Register 0xFE15.
3. Adjust the CS2 analog offset trim value (Register 0xFE16 or Register 0xFE17) until the CS2 value in Register 0xFED3 or Register 0xFED4 reads as close to 100 decimal as possible.
4. Increase the CS2 digital offset trim register value (Register 0xFE14 or Register 0xFE15) until the CS2 value in Register 0xFED3 or Register 0xFED4 reads 0.

The offset trim is now complete. With 0 V at the CS2 input, the ADC code now reads 0.

CS2_A and CS2_B Gain Trim

The gain trim removes any errors introduced by the sense resistor tolerance.

1. Apply a known current (I_{OUT}) across the sense resistor.
2. Adjust the CS2 gain trim value in Register 0xFE12 or Register 0xFE13 until the CS2 value in Register 0xFED3 or Register 0xFED4 reads the value calculated by this formula:

   $$CS2\ Value = I_{OUT} \times R_{SENSE} \times (4096/120\ \text{mV})$$

   where R_{SENSE} is the sense resistor value.

   For example, if I_{OUT} = 4.64 A and R_{SENSE} = 20 mΩ,

   $$CS2\ Value = 4.64\ \text{A} \times 20\ \text{m}\Omega \times (4096/120\ \text{mV}) = 3168\ (\text{decimal}).$$

The CS2 circuit is now trimmed. After the current sense trim is performed, the OCP limits and settings should be configured.

VS_A AND VS_B GAIN TRIM

The voltage sense inputs are optimized for sensing signals at 1 V and cannot sense a signal greater than 1.5 V. In a 28 V system, a resistor divider is required to reduce the 28 V signal to below 1.5 V. It is recommended that the 28 V signal be reduced to 1 V for best performance. The resistor divider can introduce errors, which need to be trimmed.

The ADCs output a digital word of 2560 decimal (0xA00) when there is exactly 1 V at their inputs.

ACSNS GAIN TRIM

The voltage sense inputs are optimized for ACSNS pin signals at 1 V and cannot sense a signal greater than 1.5 V. A resistor divider is required to reduce the sensed voltage signal to below 1.5 V. It is recommended that the ACSNS voltage signal be reduced to 1 V for best performance. The resistor divider can introduce errors, which need to be trimmed.

The following procedure should be used:

1. Apply nominal voltage at the sense point to achieve a voltage of approximately 1 V at the ACSNS pin.
2. Adjust the ACSNS gain trim register (Register 0xFE77) until the ACSNS reading in Register 0xFED9 is 0x500 (1280 decimal).

RTD1, RTD2, OTP1, AND OTP2 TRIM

The following procedure should be used:

1. Heat the thermistor or power supply to a known temperature that is equal to the OTP threshold.
2. Adjust the RTD1 or RTD2 gain trim register (Register 0xFE73 or Register 0xFE74) until the RTD1 or RTD2 value register (Register 0xFED7 or Register 0xFED8) gives the correct temperature reading at this temperature.
3. Adjust the OTP1 or OTP2 threshold register (Register 0xFE75 or Register 0xFE76) until the OTP1 or OTP2 flag is set.

This procedure achieves the most accurate OTP, because it takes into account the part-to-part variations of the ADP1053 and the thermistor used.

LAYOUT GUIDELINES

This section explains best practices that should be followed to ensure optimal performance of the ADP1053. In general, all related control components should be placed as close to the ADP1053 as possible.

CS2+_A, CS2+_B, CS2−_A, and CS2−_B

The routing of the tracks from the sense resistor to the ADP1053 should be laid out in parallel to each other. The tracks should be kept close together and as far from switch nodes as possible.

VS+_A, VS+_B, VS−_A, and VS−_B

The routing of the tracks from the remote voltage sense point to the ADP1053 should be laid out in parallel to each other. The tracks should be kept close together and as far from switch nodes as possible.

VDD

Place decoupling capacitors as close to the part as possible. A 330 nF capacitor from VDD to AGND is recommended.

SDA and SCL

The routing of the tracks should be laid out in parallel to each other. The tracks should be kept close together and as far from switch nodes as possible.

CS, CS1_A, and CS1_B

Run the tracks from the current sense transformer to the ADP1053 in parallel to each other. The tracks should be kept close together and as far from switch nodes as possible.

Exposed Pad

The exposed pad underneath the ADP1053 should be soldered to AGND.

VCORE

Place the 330 nF capacitor to DGND as close to the part as possible.

RES

Place the 10 kΩ resistor to AGND as close to the part as possible.

RTD1 and RTD2

Route a single trace to the ADP1053 from the thermistors. Place the thermistors close to the hottest part of the power supply.

AGND

Create an AGND ground plane and make a single-point (star) connection to the power supply system ground.

PMBus/I²C COMMUNICATION

The PMBus slave allows a device to interface to a PMBus-compliant master device, as specified by the *PMBus Power System Management Protocol Specification* (Revision 1.1, February 5, 2007). The PMBus slave is a 2-wire interface that can be used to communicate with other PMBus-compliant devices and is compatible in a multimaster, multislave bus configuration.

FEATURES

The function of the PMBus slave is to decode the command sent from the master device and respond as requested. Communication is established using an I²C-like 2-wire interface with a clock line (SCL) and data line (SDA). The PMBus slave is designed to externally move chunks of 8-bit data (bytes) while maintaining compliance with the PMBus protocol. The PMBus protocol is based on the *SMBus Specification* (Version 2.0, August 2000). The SMBus specification is, in turn, based on the Philips *I²C Bus Specification* (Version 2.1, January 2000). The PMBus incorporates the following features:

- Slave operation on multiple device systems
- 7-bit addressing
- 100 kHz and 400 kHz data rates
- General call address support
- Support for clock low extension (clock stretching)
- Separate multibyte receive and transmit FIFO
- Extensive fault monitoring

OVERVIEW

The PMBus slave module is a 2-wire interface that can be used to communicate with other PMBus-compliant devices. Its transfer protocol is based on the Philips I²C transfer mechanism. The ADP1053 is always configured as a slave device in the overall system. The ADP1053 communicates with the master device using one data pin (SDA) and one clock pin (SCL). Because the ADP1053 is a slave device, it cannot generate the clock signal. However, it is capable of clock-stretching the SCL line to put the master device in a wait state when it is not ready to respond to the master's request.

Communication is initiated when the master device sends a command to the PMBus slave device. Commands can be read or write commands, in which case data is transferred between the devices in a byte wide format. Commands can also be send commands, in which case the command is executed by the slave device upon receiving the stop bit. The stop bit is the last bit in a complete data transfer, as defined in the PMBus/I²C communication protocol. During communication, the master and slave devices send acknowledge (A) or not-acknowledge ($\overline{A}$) bits as a method of handshaking between devices. See the PMBus specification for a more detailed description of the communication protocol.

When communicating with the master device, it is possible for illegal or corrupted data to be received by the PMBus slave device. In this case, the PMBus slave device should respond to the invalid command or data, as defined by the PMBus specification, and indicate to the master device that an error or fault condition has occurred. This method of handshaking can be used as a first level of defense against inadvertent programming of the slave device that can potentially damage the chip or system.

The PMBus specification defines a set of generic PMBus commands that is recommended for a power management system. However, each PMBus device manufacturer can choose to implement and support certain commands as it deems fit for its system. In addition, the PMBus device manufacturer can choose to implement manufacturer-specific commands whose functions are not included in the generic PMBus command set. The list of standard PMBus and manufacturer-specific commands can be found in the PMBUS Command Set (Supported by the ADP1053) section and the Manufacturer-Specific Extended Command List section.

PMBus/I²C ADDRESS

The PMBus address of the ADP1053 is set by connecting an external resistor from the ADD pin to AGND. Table 11 lists the recommended resistor values and associated PMBus addresses. Seven different addresses can be used.

Table 11. PMBus Address Settings and Resistor Values

PMBus Address	ADD Pin Resistor Value (kΩ)
0x60	10 (or connect directly to AGND)
0x61	28.7
0x62	48.7
0x63	68.1
0x64	88.7
0x65	109
0x67	200 (or connect directly to VDD)

The recommended resistor values in Table 11 can vary by ±2 kΩ. Therefore, it is recommended that 1% tolerance resistors be used on the ADD pin.

The part responds to the standard PMBus broadcast address (general call) of 0x00. However, it is not recommended that the general call address be used when more than one ADP1053 is connected to the master device because the data returned by multiple slave devices will be corrupted.

For more information, see the General Call Support section.

DATA TRANSFER

Format Overview

The PMBus slave follows the transfer protocol of the SMBus specification, which is based on the fundamental transfer protocol format of the *Philips I²C Bus Specification*, dated January 2000. Data transfers are byte wide, lower byte first. Each byte is transmitted serially, most significant bit (MSB) first. A typical transfer is diagrammed in Figure 30. See the SMBus and I²C specifications for an in-depth discussion of the transfer protocols.

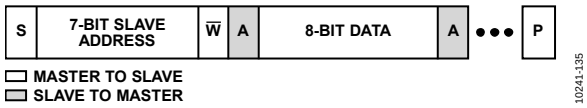


Figure 30. Basic Data Transfer

Figure 30 through Figure 37 use the following abbreviations:

S = start condition
P = stop condition
Sr = repeated start condition
$\overline{W}$ = write bit (0)
R = read bit (1)
A = acknowledge bit (0)
$\overline{A}$ = not-acknowledge bit (1)

Command Overview

Data transfer using the PMBus slave is established using PMBus commands. The PMBus specification requires that all PMBus commands start with a slave address with the R/$\overline{W}$ bit cleared (set to 0), followed by the command code. All PMBus commands supported by the ADP1053 follow one of the protocol types shown in Figure 31 through Figure 37.

The ADP1053 also supports manufacturer-specific extended commands. These commands follow the same protocol as the standard PMBus commands. However, the command code consists of two bytes that range from 0xFE00 to 0xFFFF.

Using the manufacturer-specific extended commands, the PMBus device manufacturer can add an additional 256 manufacturer-specific commands to its PMBus command set.

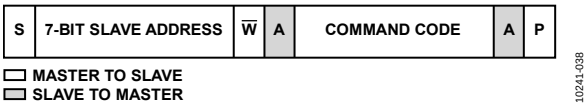


Figure 31. Send Byte Protocol

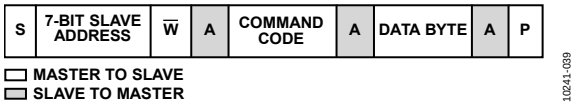


Figure 32. Write Byte Protocol

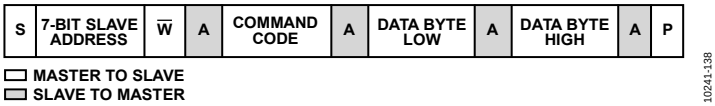


Figure 33. Write Word Protocol

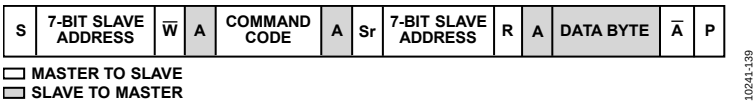


Figure 34. Read Byte Protocol

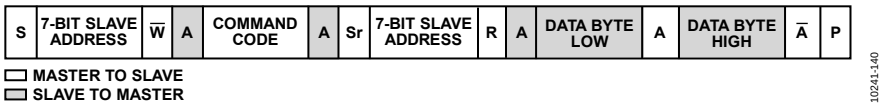


Figure 35. Read Word Protocol

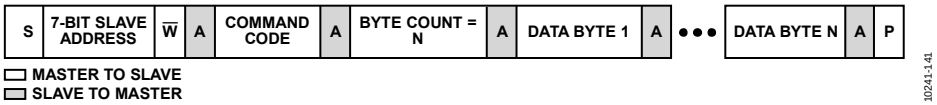


Figure 36. Block Write Protocol

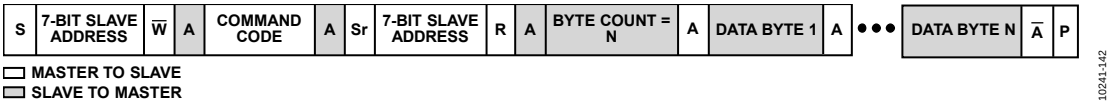


Figure 37. Block Read Protocol

Clock Generation and Stretching

The ADP1053 is always a PMBus slave device in the overall system; therefore, the device never needs to generate the clock, which is done by the master device in the system. However, the PMBus slave device is capable of clock stretching to put the master in a wait state. By stretching the SCL signal during the low period, the slave device communicates to the master device that it is not ready and that the master device must wait.

Conditions where the PMBus slave device stretches the SCL line low include the following:

- The master device is transmitting at a higher baud rate than the slave device.
- The receive buffer of the slave device is full and must be read before continuing. This prevents a data overflow condition.
- The slave device is not ready to send data that the master has requested.

Note that the slave device can stretch the SCL line only during the low period. Also, whereas the I^2C specification allows indefinite stretching of the SCL line, the PMBus specification limits the maximum time that the SCL line can be stretched, or held low, to 25 ms, after which the device must release the communication lines and reset its state machine.

GENERAL CALL SUPPORT

The PMBus slave is capable of decoding and acknowledging a general call address. The PMBus device responds to both its own address and the general call address (0x00). The general call address enables all devices on the PMBus to be written to simultaneously.

Note that all PMBus commands must start with the slave address with the R/$\overline{W}$ bit cleared (set to 0), followed by the command code. This is also true when using the general call address to communicate with the PMBus slave device.

FAST MODE

Fast mode (400 kHz) uses essentially the same mechanics as the standard mode of operation; the electrical specifications and timing are most affected. The PMBus slave is capable of communicating with a master device operating in standard mode (100 kHz) or fast mode.

FAULT CONDITIONS

The PMBus protocol provides a comprehensive set of fault conditions that must be monitored and reported. These fault conditions can be grouped into two major categories: communication faults and monitoring faults.

Communication faults are error conditions associated with the data transfer mechanism of the PMBus protocol. Monitoring faults are error conditions associated with the operation of the ADP1053, such as output overvoltage protection. These fault conditions are described in the Power Monitoring and Flags section.

TIMEOUT CONDITIONS

The SMBus specification, Version 2.0, includes three clock stretching specifications related to timeout conditions.

$T_{TIMEOUT}$

A timeout condition occurs if any single SCL clock pulse is held low for longer than the $t_{TIMEOUT}$ of 25 ms (min). Upon detecting the timeout condition, the PMBus slave device has 10 ms to abort the transfer, release the bus lines, and be ready to accept a new start condition. The device initiating the timeout is required to hold the SCL clock line low for at least $t_{TIMEOUT\ MAX}$ = 35 ms, guaranteeing that the slave device is given enough time to reset its communication protocol.

$T_{LOW:SEXT}$

This condition is not supported by the ADP1053.

$T_{LOW:MEXT}$

This condition is not supported by the ADP1053.

DATA TRANSMISSION FAULTS

Data transmission faults occur when two communicating devices violate the PMBus communication protocol, as specified in the PMBus specification. See the PMBus specification for more information about each fault condition.

Corrupted Data, PEC (Item 10.8.1)

Parity error checking. Not supported.

Sending Too Few Bits (Item 10.8.2)

Transmission is interrupted by a start or stop condition before a complete byte (eight bits) has been sent. Not supported; any transmitted data is ignored.

Reading Too Few Bits (Item 10.8.3)

Transmission is interrupted by a start or stop condition before a complete byte (eight bits) has been read. Not supported; any received data is ignored.

Host Sends or Reads Too Few Bytes (Item 10.8.4)

If a host ends a packet with a stop condition before the required bytes are sent/received, it is assumed that the host intended to stop the transfer. Therefore, the PMBus does not consider this to be an error and takes no action, except to flush any remaining bytes in the transmit FIFO.

Host Sends Too Many Bytes (Item 10.8.5)

If a host sends more bytes than are expected for the corresponding command, the PMBus slave considers this a data transmission fault and responds as follows:

- NACKs all unexpected bytes as they are received
- Flushes and ignores the received command and data
- Sets the CML bit in the STATUS_BYTE register

Host Reads Too Many Bytes (Item 10.8.6)

If a host reads more bytes than are expected for the corresponding command, the PMBus slave considers this a data transmission fault and responds as follows:

- Sends all 1s (0xFF) as long as the host continues to request data
- Sets the CML bit in the STATUS_BYTE register

Device Busy (Item 10.8.7)

The PMBus slave device is too busy to respond to a request from the master device. Not supported.

DATA CONTENT FAULTS

Data content faults occur when data transmission is successful, but the PMBus slave device cannot process the data that is received from the master device.

Improperly Set Read Bit in the Address Byte (Item 10.9.1)

All PMBus commands start with a slave address with the R/$\overline{W}$ bit cleared (set to 0), followed by the command code. If a host starts a PMBus transaction with R/$\overline{W}$ set in the address phase (equivalent to an I^2C read), the PMBus slave considers this a data content fault and responds as follows:

- ACKs the address byte
- NACKs the command and data bytes
- Sends all 1s (0xFF) as long as the host continues to request data
- Sets the CML bit in the STATUS_BYTE register

Invalid or Unsupported Command Code (Item 10.9.2)

If an invalid or unsupported command code is sent to the PMBus slave, the code is considered to be a data content fault, and the PMBus slave responds as follows:

- NACKs the illegal/unsupported command byte and data bytes
- Flushes and ignores the received command and data
- Sets the CML bit in the STATUS_BYTE register

Reserved Bits (Item 10.9.5)

Accesses to reserved bits are not a fault. Writes to reserved bits are ignored, and reads from reserved bits return 0.

Write to Read-Only Commands

If a host performs a write to a read-only command, the PMBus slave considers this a data content fault and responds as follows:

- NACKs all unexpected data bytes as they are received
- Flushes and ignores the received command and data
- Sets the CML bit in the STATUS_BYTE register

Note that this is the same error described in the Host Sends Too Many Bytes (Item 10.8.5) section.

Read from Write-Only Commands

If a host performs a read from a write-only command, the PMBus slave considers this a data content fault and responds as follows:

- Sends all 1s (0xFF) as long as the host continues to request data
- Sets the CML bit in the STATUS_BYTE register

Note that this is the same error described in the Host Reads Too Many Bytes (Item 10.8.6) section.

EEPROM

The ADP1053 has a built-in EEPROM controller that is used to communicate with the embedded 8K × 8-byte EEPROM. The EEPROM, also called Flash®/EE, is partitioned into two major blocks: the INFO block and the main block. The INFO block contains 128 8-bit bytes, and the main block contains 8K 8-bit bytes. The main block is further partitioned into 16 pages, each page containing 512 bytes.

FEATURES

The function of the EEPROM controller is to decode the operation that is requested by the ADP1053 and to provide the required timing to the EEPROM interface. Data is written to or read from the EEPROM, as requested by the decoded command. Features of the EEPROM controller include

- Separate page erase functions for each page in the EEPROM
- Single-byte and multibyte (block) read of the INFO block with up to 128 bytes at a time
- Single-byte and multibyte (block) write and read of the main block with up to 256 bytes at a time
- Automatic upload on start-up from the user settings to the internal registers
- Separate commands to upload and download data from the factory default or user settings to the internal registers

OVERVIEW

The EEPROM controller provides an interface between the ADP1053 core logic and the built-in EEPROM. The user can control data access to and from the EEPROM through this controller interface. Separate PMBus commands are available for the read, write, and erase operations to the EEPROM.

Communication is initiated by the master device sending a command to the PMBus slave device to access data from or send data to the EEPROM. Read, write, and erase commands are supported. Data is transferred between devices in a byte wide format. Using a read command, data is received from the EEPROM and transmitted to the master device. Using a write command, data is received from the master device and stored in the EEPROM through the EEPROM controller.

PAGE ERASE OPERATION

INFO Block Page Erase

The INFO block consists of 128 bytes organized as a single page. The page erase operation to the INFO block erases (sets high) all bits of the 128-byte page. The INFO block erase operation is part of a sequence of actions that occurs when the first flag information is saved into the EEPROM. Essentially, the page is first erased before the contents of the first flag registers are written to the erased page. There is no separate command to erase the INFO block.

Main Block Page Erase

The main block consists of 16 equivalent pages of 512 bytes each, numbered Page 0 to Page 15. Page 0 and Page 1 of the main block are reserved for storing the default settings and user settings, respectively. The user cannot perform a page erase operation to Page 0 or Page 1. Page 2 and Page 3 are reserved for internal use, and their contents should not be erased.

Only Page 4 to Page 15 of the main block should be used to store data. To erase any page from Page 4 to Page 15, the EEPROM must first be unlocked for access. For instructions on how to unlock the EEPROM, see the Unlock the EEPROM section.

Page 4 to Page 15 of the main block can be individually erased using the EEPROM_PAGE_ERASE command (Command 0xD4). For example, to perform a page erase of Page 10, execute the following command:

Figure 38. Example Erase Command

In this example, Command Code = 0xD4 and Data Byte = 0x0A. Note that it is important to wait at least 35 ms for the page erase operation to complete before executing the next PMBus command.

The EEPROM allows erasing of whole pages only; therefore, to change the data of any single byte in a page, the entire page must first be erased (set high) for that byte to be writable. Subsequent writes to any bytes in that page are allowed as long as that byte has not been written to a low previously.

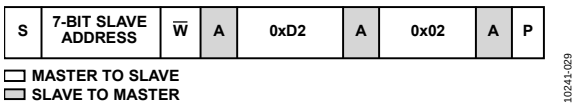
READ OPERATION (BYTE READ AND BLOCK READ)

Read from INFO Block

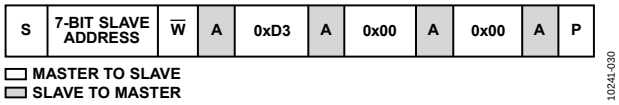
The data in the EEPROM INFO block can be read one byte at a time or in multiple bytes in series using the EEPROM_INFO command (Command 0xF1). Before executing this command, the user must program the number of bytes to read using the EEPROM_NUM_RD_BYTES command (Command 0xD2). The user can also program the offset from the page boundary where the first read byte is returned using the EEPROM_ADDR_OFFSET command (Command 0xD3).

In the following example, two bytes from the INFO block are read, starting from the first byte of the page.

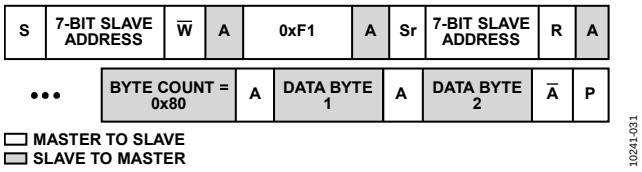
1. Set number of return bytes = 2.



2. Set address offset = 0.



3. Read two bytes from the INFO block.



Note that the block read command to the INFO block can read a maximum of 128 bytes. However, only the first two bytes are used to store the first flag information.

Read from Main Block, Page 0 and Page 1

Page 0 and Page 1 of the main block are reserved for storing the default settings and user settings, respectively, and are meant to prevent third-party access to this data. To read from Page 0 or Page 1, the user must first unlock the EEPROM (see the Unlock the EEPROM section). After the EEPROM is unlocked, Page 0 and Page 1 are readable using the EEPROM_DATA_xx commands, as described in the Read from Main Block, Page 2 to Page 15 section. Note that when the EEPROM is locked, a read from Page 0 or Page 1 returns invalid data.

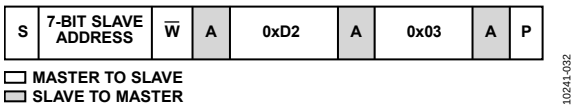
Read from Main Block, Page 2 to Page 15

Data in Page 2 to Page 15 of the main block is always readable, even with the EEPROM locked. The data in the EEPROM main block can be read one byte at a time or in multiple bytes in series using the EEPROM_DATA_xx commands (Command 0xB0 to Command 0xBF).

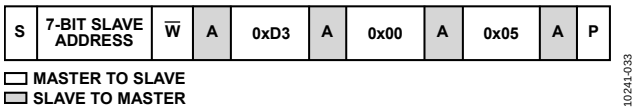
Before executing this command, the user must program the number of bytes to read using the EEPROM_NUM_RD_BYTES command (Command 0xD2). The user can also program the offset from the page boundary where the first read byte is returned using the EEPROM_ADDR_OFFSET command (Command 0xD3).

In the following example, three bytes from Page 4 are read from the EEPROM, starting from the fifth byte of that page.

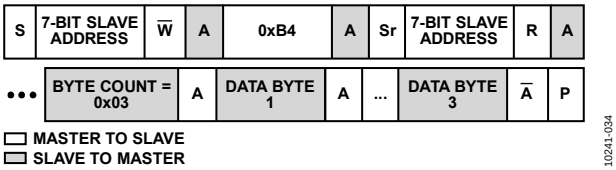
1. Set number of return bytes = 3.



2. Set address offset = 5.



3. Read three bytes from Page 4.



Note that the block read command can read a maximum of 256 bytes for any single transaction.

WRITE OPERATION (BYTE WRITE AND BLOCK WRITE)

Write to INFO Block

The user cannot write directly to the INFO block; this block is used by the ADP1053 to store the first flag information (see the First Flag ID Recording section).

Write to Main Block, Page 0 and Page 1

Page 0 and Page 1 of the main block are reserved for storing the default settings and user settings, respectively. The user cannot perform a direct write operation to Page 0 or Page 1 using the EEPROM_DATA_xx commands. A user write to Page 0 or Page 1 returns a not-acknowledge. To program the register contents of Page 1 of the main block, it is recommended that the STORE_USER_ALL command be used (Command 0x15). See the Save Register Settings to User Settings section.

Write to Main Block, Page 2 and Page 3

Page 2 and Page 3 of the main block are reserved for internal use and their contents should not be written to. Only Page 4 to Page 15 should be used to store data.

Write to Main Block, Page 4 to Page 15

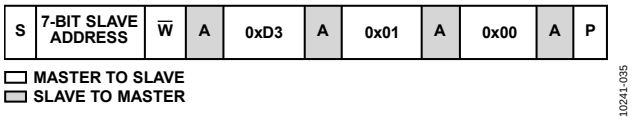
Before performing a write to Page 4 through Page 15 of the main block, the user must first unlock the EEPROM (see the Unlock the EEPROM section).

Data in Page 4 to Page 15 of the EEPROM main block can be programmed (written to) one byte at a time or in multiple bytes in series using the EEPROM_DATA_xx commands (Command 0xB0 to Command 0xBF). Before executing this command, the user can program the offset from the page boundary where the first byte is written using the EEPROM_ADDR_OFFSET command (Command 0xD3).

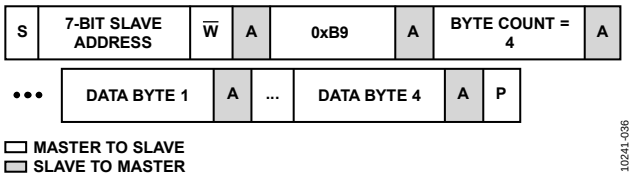
If the targeted page has not yet been erased, the user can erase the page as described in the Main Block Page Erase section.

In the following example, four bytes are written to Page 9, starting from the 256th byte of that page.

1. Set address offset = 256.



2. Write four bytes to Page 9.



Note that the block write command can write a maximum of 256 bytes for any single transaction.

EEPROM PASSWORD

On power-up, the EEPROM is locked and protected from accidental writes or erases. Only reads from Page 2 to Page 15 are allowed when the EEPROM is locked. Before any data can be written (programmed) to the EEPROM, the EEPROM must be unlocked for write access. After it is unlocked, the EEPROM is opened for reading, writing, and erasing.

On power-up, Page 0 and Page 1 are also protected from read access, and the EEPROM must first be unlocked to read these pages.

Unlock the EEPROM

To unlock the EEPROM, perform two consecutive writes with the correct password (default = 0xFF) using the EEPROM_PASSWORD command (Command 0xD5). The EEPROM_UNLOCKED flag (Bit 4 of Register 0xFEC3) is set to indicate that the EEPROM is unlocked for write access.

Lock the EEPROM

To lock the EEPROM, write any byte other than the correct password using the EEPROM_PASSWORD command (Command 0xD5). The EEPROM_UNLOCKED flag is cleared to indicate that the EEPROM is locked from write access.

Change the EEPROM Password

To change the EEPROM password, first write the correct password using the EEPROM_PASSWORD command (Command 0xD5). Immediately write the new password using the same command. The password is now changed to the new password.

DOWNLOADING EEPROM SETTINGS TO INTERNAL REGISTERS

Download User Settings to Registers

The user settings are stored in Page 1 of the EEPROM main block. These settings are downloaded from the EEPROM into the registers under the following conditions:

- On power-up. The user settings are automatically downloaded into the internal registers, powering the part up in a state previously saved by the user.
- On execution of the RESTORE_USER_ALL command (Command 0x16). This command allows the user to force a download of the user settings from Page 1 of the EEPROM main block into the internal registers.

Download Factory Default Settings to Registers

The factory default settings are stored in Page 0 of the EEPROM main block. The factory default settings can be downloaded from the EEPROM into the internal registers using the RESTORE_DEFAULT_ALL command (Command 0x12).

When this command is executed, the EEPROM password is also reset to the factory default setting of 0xFF.

SAVING REGISTER SETTINGS TO THE EEPROM

The register settings cannot be saved to the factory default settings located in Page 0 of the EEPROM main block. This is to prevent the user from accidentally overriding the factory trim settings and default register settings.

Save Register Settings to User Settings

The register settings can be saved to the user settings located in Page 1 of the EEPROM main block using the STORE_USER_ALL command (Command 0x15). Before this command can be executed, the EEPROM must first be unlocked for writing (see the Unlock the EEPROM section).

After the register settings are saved to the user settings, any subsequent power cycle automatically downloads the latest stored user information from the EEPROM into the internal registers.

Note that execution of the STORE_USER_ALL command automatically performs a page erase to Page 1 of the EEPROM main block, after which the register settings are stored in the EEPROM. Therefore, it is important to wait at least 35 ms for the operation to complete before executing the next PMBus command.

EEPROM CRC CHECKSUM

As a simple method of checking that the values downloaded from the EEPROM are consistent with the internal registers, a CRC checksum is implemented.

- When the data from the internal registers is saved to the EEPROM (Page 1 of the main block), the total number of 1s from all the registers is counted and written into the EEPROM as the last byte of information. This is called the CRC checksum.
- When the data is downloaded from the EEPROM into the internal registers, a similar counter that sums all 1s from the values loaded into the registers is saved. This value is compared with the CRC checksum from the previous upload operation.

If the values match, the download operation was successful. If the values differ, the EEPROM download operation failed, and the EEPROM_CRC fault flag is set (Bit 1 of Register 0xFEC2).

To read the EEPROM CRC checksum value, execute the EEPROM_CRC_CHKSUM command (Command 0xD1). This command returns the CRC checksum accumulated in the counter during the download operation.

Note that the CRC checksum is an 8-bit cyclical accumulator that wraps around to 0 when 255 is reached.

SOFTWARE GUI

A free software GUI is available for programming and configuring the ADP1053. The GUI is designed to be intuitive and dramatically reduces power supply design and development time.

The software includes filter design and power supply PWM topology windows. The GUI is also an information center, displaying the status of all readings, monitoring, and flags on the ADP1053.

For more information about the GUI, contact Analog Devices for the latest software and a user guide.

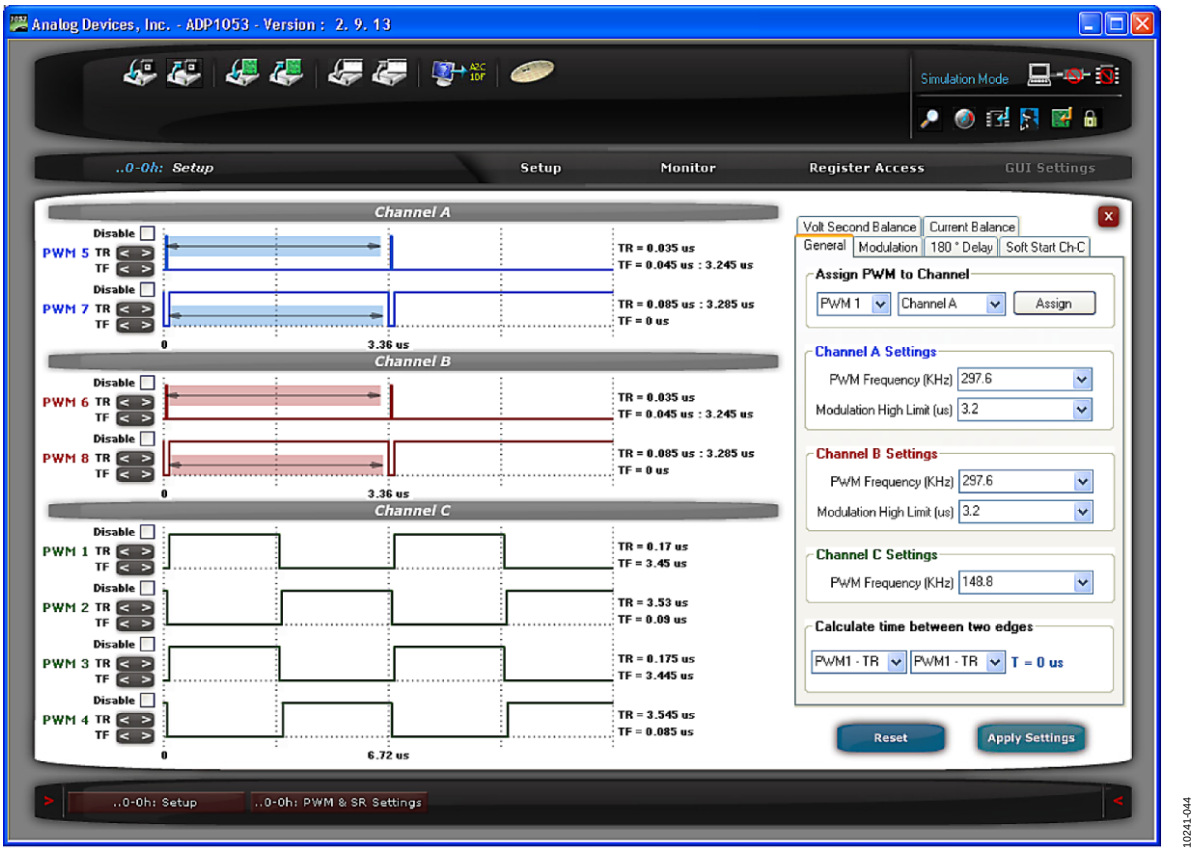


Figure 39. ADP1053 GUI, PWM Setup Window

PMBus COMMAND SET (SUPPORTED BY THE ADP1053)

Table 12 lists the standard PMBus commands that are implemented on the ADP1053. Many of these commands are implemented in registers, which share the same hexadecimal value as the PMBus command code.

Table 12. PMBus Command List

Command Code	Command Name	SMBus Transaction Type	Number of Data Bytes	Description
0x03	CLEAR_FAULTS	Send byte	0	Clear all fault bits in the STATUS_WORD register.
0x10	WRITE_PROTECT	Read/write byte	1	Protect against accidental writes to the PMBus device; reads allowed.
0x12	RESTORE_DEFAULT_ALL	Send byte	0	Download factory default settings from EEPROM (Page 0) to registers.
0x15	STORE_USER_ALL	Send byte	0	Save user settings from registers to EEPROM (Page 1). EEPROM must first be unlocked.
0x16	RESTORE_USER_ALL	Send byte	0	Download user settings from EEPROM (Page 1) to registers.
0x19	CAPABILITY	Read byte	1	Allow host system to determine capabilities of PMBus device.
0x78	STATUS_BYTE	Read byte	1	Return low byte of STATUS_WORD.
0x79	STATUS_WORD	Read word	2	Return low byte and high byte of STATUS_WORD.
0x8D	READ_TEMPERATURE_1	Read word	2	Return temperature reading (in degrees Celsius). READ_TEMPERATURE_1 = $Y \times 2^N$.
0x8E	READ_TEMPERATURE_2	Read word	2	Return temperature reading (in degrees Celsius). READ_TEMPERATURE_2 = $Y \times 2^N$.
0x98	PMBUS_REVISION	Read byte	1	Read PMBus revision that device is compliant with.
0x99	MFR_ID	Read block	1	Read manufacturer's ID.
0x9A	MFR_MODEL	Read block	1	Read manufacturer's device model number.
0x9B	MFR_REVISION	Read block	1	Read manufacturer's device revision number.
0xB0	EEPROM_DATA_00	Read block	Variable	Block read from Page 0. EEPROM must first be unlocked.
0xB1	EEPROM_DATA_01	Read block	Variable	Block read from Page 1. EEPROM must first be unlocked.
0xB2	EEPROM_DATA_02	Read/write block	Variable	Block read/write to Page 2. EEPROM must first be unlocked for write. Page 2 should not be written to.
0xB3	EEPROM_DATA_03	Read/write block	Variable	Block read/write to Page 3. EEPROM must first be unlocked for write. Page 3 should not be written to.
0xB4	EEPROM_DATA_04	Read/write block	Variable	Block read/write to Page 4. EEPROM must first be unlocked for write.
0xB5	EEPROM_DATA_05	Read/write block	Variable	Block read/write to Page 5. EEPROM must first be unlocked for write.
0xB6	EEPROM_DATA_06	Read/write block	Variable	Block read/write to Page 6. EEPROM must first be unlocked for write.
0xB7	EEPROM_DATA_07	Read/write block	Variable	Block read/write to Page 7. EEPROM must first be unlocked for write.
0xB8	EEPROM_DATA_08	Read/write block	Variable	Block read/write to Page 8. EEPROM must first be unlocked for write.
0xB9	EEPROM_DATA_09	Read/write block	Variable	Block read/write to Page 9. EEPROM must first be unlocked for write.
0xBA	EEPROM_DATA_10	Read/write block	Variable	Block read/write to Page 10. EEPROM must first be unlocked for write.
0xBB	EEPROM_DATA_11	Read/write block	Variable	Block read/write to Page 11. EEPROM must first be unlocked for write.
0xBC	EEPROM_DATA_12	Read/write block	Variable	Block read/write to Page 12. EEPROM must first be unlocked for write.
0xBD	EEPROM_DATA_13	Read/write block	Variable	Block read/write to Page 13. EEPROM must first be unlocked for write.
0xBE	EEPROM_DATA_14	Read/write block	Variable	Block read/write to Page 14. EEPROM must first be unlocked for write.
0xBF	EEPROM_DATA_15	Read/write block	Variable	Block read/write to Page 15. EEPROM must first be unlocked for write.

Command Code	Command Name	SMBus Transaction Type	Number of Data Bytes	Description
0xD1	EEPROM_CRC_CHKSUM	Read byte	1	Return CRC checksum value from EEPROM download operation.
0xD2	EEPROM_NUM_RD_BYTES	Read/write byte	1	Set number of read bytes returned when using the EEPROM_DATA_xx commands.
0xD3	EEPROM_ADDR_OFFSET	Read/write word	2	Set address offset of current EEPROM page.
0xD4	EEPROM_PAGE_ERASE	Write byte	1	Perform page erase on selected page (Page 4 to Page 15). Wait 35 ms for each page erase operation. EEPROM must first be unlocked. Page 0 and Page 1 erase is not allowed.
0xD5	EEPROM_PASSWORD	Write byte	1	Write the password to this register twice to unlock the EEPROM and/or change the EEPROM password.
0xD6	TRIM_PASSWORD	Write byte	1	Write the password to this register twice to unlock the trim registers for write access.
0xF1	EEPROM_INFO	Read/write block	Variable	Read first flag information.

MANUFACTURER-SPECIFIC EXTENDED COMMAND LIST

Table 13. Manufacturer-Specific Extended Command List

Command	Name
Flag Configuration Registers	
0xFE00	CS1_A_OCP/CS1_B_OCP flag configuration
0xFE01	CS2_A_OCP/CS2_B_OCP flag configuration
0xFE02	OVP_A/OVP_B flag configuration
0xFE03	UVP_A/UVP_B flag configuration
0xFE04	CS_OCP/ACSNS flag configuration
0xFE05	OTP1/OTP2 flag configuration
0xFE06	Flag reenable delay, VDD_OV, and FLAGIN configuration
0xFE07	Flag blanking during soft start
0xFE08	Volt-second balance blanking and SR disable during soft start
0xFE09	PGOOD debounce
Switching Frequency Registers	
0xFE0A	Switching frequency for Channel A
0xFE0B	Switching frequency for Channel B
0xFE0C	Switching frequency for Channel C
0xFE0D	Frequency synchronization delay time
0xFE0E	SYNO selection and synchronization enable
0xFE0F	Flag/synchronization pin functions
Channel A/Channel B Current Sense and Limit Setting Registers	
0xFE10	CS1_A gain trim
0xFE11	CS1_B gain trim
0xFE12	CS2_A gain trim
0xFE13	CS2_B gain trim
0xFE14	CS2_A digital offset trim
0xFE15	CS2_B digital offset trim
0xFE16	CS2_A analog offset trim
0xFE17	CS2_B analog offset trim
0xFE18	CS2_A OCP threshold
0xFE19	CS2_B OCP threshold
0xFE1A	CS2_A high-side/low-side setting and Channel A light load threshold
0xFE1B	CS2_B high-side/low-side setting and Channel B light load threshold
Channel A/Channel B Voltage Sense and Limit Setting Registers	
0xFE1C	VS_A gain trim
0xFE1D	VS_B gain trim
0xFE1E	VS_A reference maximum limit
0xFE1F	VS_B reference maximum limit
0xFE20	VS_A reference minimum limit
0xFE21	VS_B reference minimum limit
0xFE22	VS_A reference setting (MSBs)
0xFE23	VS_B reference setting (MSBs)
0xFE24	VS_A reference setting (LSBs)
0xFE25	VS_B reference setting (LSBs)
0xFE26	OVP_A setting
0xFE27	OVP_B setting
0xFE28	UVP_A setting
0xFE29	UVP_B setting

Command	Name
Soft Start, Digital Filter, and Modulation Setting Registers	
0xFE2A	Channel A soft start ramp rate
0xFE2B	Channel B soft start ramp rate
0xFE2C	Channel A normal mode low frequency gain
0xFE2D	Channel B normal mode low frequency gain
0xFE2E	Channel A normal mode zero setting
0xFE2F	Channel B normal mode zero setting
0xFE30	Channel A normal mode pole setting
0xFE31	Channel B normal mode pole setting
0xFE32	Channel A normal mode high frequency gain
0xFE33	Channel B normal mode high frequency gain
0xFE34	Channel A light load mode low frequency gain
0xFE35	Channel B light load mode low frequency gain
0xFE36	Channel A light load mode zero setting
0xFE37	Channel B light load mode zero setting
0xFE38	Channel A light load mode pole setting
0xFE39	Channel B light load mode pole setting
0xFE3A	Channel A light load mode high frequency gain
0xFE3B	Channel B light load mode high frequency gain
0xFE3C	Channel A modulation limit
0xFE3D	Channel B modulation limit
0xFE3E	Channel A feedforward and soft start digital filter setting
0xFE3F	Channel B feedforward and soft start digital filter setting
PWM Output Timing Registers	
0xFE40	OUT1 rising edge timing (MSBs)
0xFE41	OUT1 falling edge timing (MSBs)
0xFE42	OUT1 rising and falling edge timing (LSBs)
0xFE43	OUT1 settings
0xFE44	OUT2 rising edge timing (MSBs)
0xFE45	OUT2 falling edge timing (MSBs)
0xFE46	OUT2 rising and falling edge timing (LSBs)
0xFE47	OUT2 settings
0xFE48	OUT3 rising edge timing (MSBs)
0xFE49	OUT3 falling edge timing (MSBs)
0xFE4A	OUT3 rising and falling edge timing (LSBs)
0xFE4B	OUT3 settings
0xFE4C	OUT4 rising edge timing (MSBs)
0xFE4D	OUT4 falling edge timing (MSBs)
0xFE4E	OUT4 rising and falling edge timing (LSBs)
0xFE4F	OUT4 settings
0xFE50	OUT5 rising edge timing (MSBs)
0xFE51	OUT5 falling edge timing (MSBs)
0xFE52	OUT5 rising and falling edge timing (LSBs)
0xFE53	OUT5 settings
0xFE54	OUT6 rising edge timing (MSBs)
0xFE55	OUT6 falling edge timing (MSBs)
0xFE56	OUT6 rising and falling edge timing (LSBs)
0xFE57	OUT6 settings

Command	Name
0xFE58	OUT7 rising edge timing (MSBs)
0xFE59	OUT7 falling edge timing (MSBs)
0xFE5A	OUT7 rising and falling edge timing (LSBs)
0xFE5B	OUT7 settings
0xFE5C	OUT8 rising edge timing (MSBs)
0xFE5D	OUT8 falling edge timing (MSBs)
0xFE5E	OUT8 rising and falling edge timing (LSBs)
0xFE5F	OUT8 settings
0xFE60	PWM output pin disable
GO Command Register	
0xFE61	GO commands
Balance Control Registers	
0xFE62	Balance control on OUT1 and OUT2
0xFE63	Balance control on OUT3 and OUT4
0xFE64	Balance control on OUT5, OUT6, OUT7, and OUT8
Synchronization Setting Registers	
0xFE65	OUT1 and OUT2 shutdown in Channel C synchronization
0xFE66	OUT1 through OUT8 dead time adjustment in synchronization
SR and Channel C Soft Start Setting Registers	
0xFE67	Synchronous rectifier (SR) soft start
0xFE68	Channel C soft start
Light Load PWM Disable Registers	
0xFE69	Channel A light load mode PWM output disable
0xFE6A	Channel B light load mode PWM output disable
Fast OCP and Channel C Current Sense Setting Registers	
0xFE6B	CS1_A blanking reference edge
0xFE6C	CS1_B blanking reference edge
0xFE6D	OUT3, OUT4, OUT7, and OUT8 cycle-by-cycle OCP response
0xFE6E	CS gain trim
0xFE6F	CS OCP settings
0xFE70	CS1_A OCP settings
0xFE71	CS1_B OCP settings
0xFE72	Balance control settings
Temperature Sense and Protection Setting Registers	
0xFE75	OTP1 threshold
0xFE76	OTP2 threshold
ACSNS and Feedforward Setting Registers	
0xFE77	ACSNS gain trim
0xFE78	ACSNS setting
PSON Registers	
0xFE79	Channel A PSON setting
0xFE7A	Channel B PSON setting
0xFE7B	Additional flag reenable delay and Channel C PSON setting

Command	Name
RTD Trim Registers	
0xFE73	RTD1 gain trim
0xFE74	RTD2 gain trim
0xFE7C	RTD1 offset trim (MSB)
0xFE7D	RTD1 offset trim (LSBs)
0xFE7E	RTD2 offset trim (MSB)
0xFE7F	RTD2 offset trim (LSBs)
0xFE80	RTD1 current source settings
0xFE81	RTD2 current source settings
Customized Registers	
0xFE82	Custom register
0xFE83	REVERSE_A/REVERSE_B flag configuration
0xFE84	REVERSE_A flag settings
0xFE85	REVERSE_B flag settings
0xFE86	VS_A slew rate for output voltage adjustment
0xFE87	VS_B slew rate for output voltage adjustment
0xFE88	Power supply software reset control
0xFE89	CS, CS1, and CS2 ADC update rate
0xFE8A	OTW1/OTW2 settings
Flag Registers	
0xFEC0	Flag Register 1
0xFEC1	Flag Register 2
0xFEC2	Flag Register 3
0xFEC3	Flag Register 4
0xFEC4	Flag Register 5
0xFEC5	Latched Flag Register 1
0xFEC6	Latched Flag Register 2
0xFEC7	Latched Flag Register 3
0xFEC8	Latched Flag Register 4
0xFEC9	Latched Flag Register 5
0xFECA	Channel A first flag ID
0xFECB	Channel B first flag ID
Value Registers	
0xFED0	CS value
0xFED1	CS1_A value
0xFED2	CS1_B value
0xFED3	CS2_A value
0xFED4	CS2_B value
0xFED5	VS_A value
0xFED6	VS_B value
0xFED7	RTD1 value
0xFED8	RTD2 value
0xFED9	ACSNS value
0xFEDA	Channel A duty cycle value
0xFEDB	Channel B duty cycle value

PMBus COMMAND DESCRIPTIONS

CLEAR_FAULTS COMMAND

Command 0x03, send byte, no data. This command clears all fault bits in the STATUS_WORD register.

WRITE_PROTECT COMMAND

Table 14. Command 0x10—WRITE_PROTECT

Bits	Bit Name	R/W	Description
7	Write Protect 1	R/W	Setting this bit disables writes to all commands except for WRITE_PROTECT.
6	Write Protect 2	R/W	Setting this bit disables writes to all commands except for WRITE_PROTECT, OPERATION, and PAGE.
5	Write Protect 3	R/W	Setting this bit disables writes to all commands except for WRITE_PROTECT, OPERATION, PAGE, ON_OFF_CONFIG, and VOUT_COMMAND.
[4:0]	Reserved	R	Reserved.

RESTORE_DEFAULT_ALL COMMAND

Command 0x12, send byte, no data. This command downloads the factory default settings from EEPROM (Page 0) into operating memory.

STORE_USER_ALL COMMAND

Command 0x15, send byte, no data. This command copies the entire contents of operating memory into EEPROM (Page 1 of the main block). The EEPROM must first be unlocked.

RESTORE_USER_ALL COMMAND

Command 0x16, send byte, no data. This command downloads the stored user settings from EEPROM (Page 1 of the main block) into operating memory.

CAPABILITY COMMAND

This command allows host systems to determine the capabilities of the PMBus device.

Table 15. Command 0x19—CAPABILITY (Default Value = 0x20)

Bits	Bit Name	R/W	Description
7	Packet error checking	R	Always reads 0. Packet error checking (PEC) is not supported.
[6:5]	Maximum bus speed	R	Return the device PMBus speed capability. Always reads 01 (maximum bus speed is 400 kHz).
4	SMBALERT#	R	Always reads 0. SMBALERT# pin and SMBus alert response protocol are not supported.
[3:0]	Reserved	R	Reserved.

STATUS_BYTE COMMAND

This command returns the lower byte of the STATUS_WORD command. A value of 1 in this command indicates that a fault has occurred.

Table 16. Command 0x78—STATUS_BYTE

Bits	Bit Name	R/W	Description
7	BUSY	R	Always reads 0. Not supported.
6	PSON_OFF	R	Always reads 0. Not supported.
5	VOUT_OV	R	Always reads 0. Not supported.
4	IOUT_OC	R	Always reads 0. Not supported.
3	VIN_UV	R	Always reads 0. Not supported.
2	TEMPERATURE	R	Always reads 0. Not supported.
1	CML	R	1 = communications, memory, or logic fault.
0	NONE_OF_THE_ABOVE	R	Always reads 0. Not supported.

STATUS_WORD COMMAND

A value of 1 in this command indicates that a fault has occurred.

Table 17. Command 0x79—STATUS_WORD

Bits	Bit Name	R/W	Description
15	VOUT	R	Always reads 0. Not supported.
14	IOUT/POUT	R	Always reads 0. Not supported.
13	INPUT	R	Always reads 0. Not supported.
12	MFR	R	Always reads 0. Not supported.
11	POWER_GOOD#	R	Always reads 0. Not supported.
10	FANS	R	Always reads 0. Not supported.
9	OTHER	R	Always reads 0. Not supported.
8	UNKNOWN	R	Always reads 0. Not supported.
7	BUSY	R	Always reads 0. Not supported.
6	PSON_OFF	R	Always reads 0. Not supported.
5	VOUT_OV	R	Always reads 0. Not supported.
4	IOUT_OC	R	Always reads 0. Not supported.
3	VIN_UV	R	Always reads 0. Not supported.
2	TEMPERATURE	R	Always reads 0. Not supported.
1	CML	R	1 = communications, memory, or logic fault.
0	NONE_OF_THE_ABOVE	R	Always reads 0. Not supported.

READ TEMPERATURE COMMANDS

The READ_TEMPERATURE_1 and READ_TEMPERATURE_2 commands return the temperature for RTD1 and RTD2, respectively, in linear mode format ($X = Y \times 2^N$).

Table 18. Command 0x8D—READ_TEMPERATURE_1

Bits	Bit Name	R/W	Description
[15:11]	Exponent	R	Return the exponent (N) used in linear mode format ($X = Y \times 2^N$).
[10:8]	High bits	R	Mantissa high bits (Y[10:8]) used in linear mode format ($X = Y \times 2^N$).
[7:0]	Low byte	R	Mantissa low byte (Y[7:0]) used in linear mode format ($X = Y \times 2^N$).

Table 19. Command 0x8E—READ_TEMPERATURE_2

Bits	Bit Name	R/W	Description
[15:11]	Exponent	R	Return the exponent (N) used in linear mode format ($X = Y \times 2^N$).
[10:8]	High bits	R	Mantissa high bits (Y[10:8]) used in linear mode format ($X = Y \times 2^N$).
[7:0]	Low byte	R	Mantissa low byte (Y[7:0]) used in linear mode format ($X = Y \times 2^N$).

PMBUS_REVISION COMMAND

Table 20. Command 0x98—PMBUS_REVISION (Default Value = 0x11)

Bits	Bit Name	R/W	Description
[7:0]	Revision	R	Return the revision of PMBus that the device is compliant with.

MFR_ID COMMAND

Table 21. Command 0x99—MFR_ID (Default Value = 0x41)

Bits	Bit Name	R/W	Description
[7:0]	MFR_ID	R	Return the manufacturer's ID.

MFR_MODEL COMMAND

Table 22. Command 0x9A—MFR_MODEL (Default Value = 0x53)

Bits	Bit Name	R/W	Description
[7:0]	Model	R	Return the manufacturer's model number.

MFR_REVISION COMMAND

Table 23. Command 0x9B—MFR_REVISION

Bits	Bit Name	R/W	Description
[7:0]	Revision	R	Return the manufacturer's revision number.

EEPROM_DATA_00 THROUGH EEPROM_DATA_15 COMMANDS

Command 0xB0 through Command 0xBF, read/write block. The EEPROM_DATA_00 through EEPROM_DATA_15 commands are used to read data from the EEPROM (Page 0 through Page 15) and to write data to the EEPROM (Page 4 through Page 15). For example, EEPROM_DATA_04 reads from and writes to Page 4 of the EEPROM main block; EEPROM_DATA_11 reads from and writes to Page 11 of the EEPROM main block. For more information, see the EEPROM section.

EEPROM_CRC_CHKSUM COMMAND

Table 24. Command 0xD1—EEPROM_CRC_CHKSUM

Bits	Bit Name	R/W	Description
[7:0]	CRC checksum	R	Return the CRC checksum value from the EEPROM download operation.

EEPROM_NUM_RD_BYTES COMMAND

Table 25. Command 0xD2—EEPROM_NUM_RD_BYTES

Bits	Bit Name	R/W	Description
[7:0]	Number of read bytes returned	R/W	Set the number of read bytes returned when using the EEPROM_DATA_xx commands.

EEPROM_ADDR_OFFSET COMMAND

Table 26. Command 0xD3—EEPROM_ADDR_OFFSET

Bits	Bit Name	R/W	Description
[15:0]	Address offset	R/W	Set the address offset of the current EEPROM page.

EEPROM_PAGE_ERASE COMMAND

Table 27. Command 0xD4—EEPROM_PAGE_ERASE

Bits	Bit Name	R/W	Description
[7:0]	Page erase	W	Perform a page erase on the selected EEPROM page (Page 4 to Page 15). Wait 35 ms after each page erase operation. The EEPROM must first be unlocked. Page 0 and Page 1 are reserved for storing the default settings and user settings, respectively. The user cannot perform a page erase of Page 0 or Page 1. Page 2 and Page 3 are reserved for internal use and their contents should not be erased.

EEPROM_PASSWORD COMMAND

Table 28. Command 0xD5—EEPROM_PASSWORD

Bits	Bit Name	R/W	Description
[7:0]	EEPROM password	W	Write the password using this command two consecutive times to unlock the EEPROM and/or to change the EEPROM password. The factory default password is 0xFF.

TRIM_PASSWORD COMMAND

Table 29. Command 0xD6—TRIM_PASSWORD

Bits	Bit Name	R/W	Description
[7:0]	Trim password	W	Write the password using this command to unlock the trim registers for write access. Write the trim password twice to unlock the register; write any other value to exit. The trim password is the same as the EEPROM password.

EEPROM_INFO COMMAND

Command 0xF1, read/write block. This command reads the first flag data from the EEPROM.

MANUFACTURER-SPECIFIC EXTENDED COMMAND REGISTER DESCRIPTIONS

FLAG CONFIGURATION REGISTERS

Register 0xFE00 to Register 0xFE05 and Bits[3:0] of Register 0xFE06 are used to set the flag response and the resolution after the flag is cleared. Bits[7:6] of Register 0xFE06 set the global flag reenable delay time.

Table 30. Register 0xFE00 to Register 0xFE06—Flag Configuration Registers

Registers	Bits	Flag	Other Flag Configuration Registers	Flag Registers (Read-Only Status Registers)
0xFE00	[7:4]	CS1_B_OCP	0xFE71	0xFEC1, 0xFEC6
0xFE00	[3:0]	CS1_A_OCP	0xFE70	0xFEC0, 0xFEC5
0xFE01	[7:4]	CS2_B_OCP	0xFE19	0xFEC1, 0xFEC6
0xFE01	[3:0]	CS2_A_OCP	0xFE18	0xFEC0, 0xFEC5
0xFE02	[7:4]	OVP_B	0xFE27	0xFEC1, 0xFEC6
0xFE02	[3:0]	OVP_A	0xFE26	0xFEC0, 0xFEC5
0xFE03	[7:4]	UVP_B	0xFE29	0xFEC1, 0xFEC6
0xFE03	[3:0]	UVP_A	0xFE28	0xFEC0, 0xFEC5
0xFE04	[7:4]	ACSNS	0xFE78	0xFEC2, 0xFEC7
0xFE04	[3:0]	CS_OCP	0xFE6F	0xFEC2, 0xFEC7
0xFE05	[7:4]	OTP2	0xFE76	0xFEC2, 0xFEC7
0xFE05	[3:0]	OTP1	0xFE75	0xFEC2, 0xFEC7
0xFE06	[3:0]	FLAGIN	0xFE0F	0xFEC2, 0xFEC7

Table 31. Register 0xFE00 to Register 0xFE05—Flag Configuration Register Bit Descriptions

Bits	Bit Name	R/W	Description		
[7:6]	Flag action	R/W	These bits specify the action to take when the flag is set.		
			Bit 7	**Bit 6**	**Flag Action**
			0	0	None
			0	1	Disable PWM outputs in Channel A
			1	0	Disable PWM outputs in Channel B
			1	1	Disable all PWM outputs (Channel A, Channel B, and Channel C)
[5:4]	Action after flag is cleared	R/W	These bits specify the action to take after the flag is cleared.		
			Bit 5	**Bit 4**	**Action After Flag Is Cleared**
			0	0	After the reenable delay time, the PWM outputs are reenabled using the soft start process
			0	1	The PWM outputs are reenabled immediately without a soft start
			1	0	A PSON signal is needed to reenable the PWM outputs
			1	1	A PSON signal is needed to reenable the PWM outputs
[3:2]	Flag action	R/W	These bits specify the action to take when the flag is set.		
			Bit 3	**Bit 2**	**Flag Action**
			0	0	None
			0	1	Disable PWM outputs in Channel A
			1	0	Disable PWM outputs in Channel B
			1	1	Disable all PWM outputs (Channel A, Channel B, and Channel C)
[1:0]	Action after flag is cleared	R/W	These bits specify the action to take after the flag is cleared.		
			Bit 1	**Bit 0**	**Action After Flag Is Cleared**
			0	0	After the reenable delay time, the PWM outputs are reenabled using the soft start process
			0	1	The PWM outputs are reenabled immediately without a soft start
			1	0	A PSON signal is needed to reenable the PWM outputs
			1	1	A PSON signal is needed to reenable the PWM outputs

Table 32. Register 0xFE06—Flag Reenable Delay, VDD_OV, and FLAGIN Configuration

Bits	Bit Name	R/W	Description		
[7:6]	Flag reenable delay	R/W	These bits specify the global delay from when a flag is cleared to the soft start process.		
			Bit 7	**Bit 6**	**Typical Delay Time**
			0	0	250 ms
			0	1	500 ms
			1	0	1 sec
			1	1	2 sec
5	VDD_OV flag ignore	R/W	This bit enables or disables the VDD_OV flag. 0 = VDD_OV flag enabled. When there is a VDD overvoltage condition, the flag is set and the part shuts down. When the flag is cleared, the part restarts. 1 = VDD_OV flag is always cleared.		
4	VDD_OV flag debounce	R/W	This bit sets the debounce time for the VDD_OV flag. 0 = 500 µs debounce time. 1 = 2 µs debounce time.		
[3:2]	FLAGIN action	R/W	These bits specify the action to take when the FLAGIN flag is set.		
			Bit 3	**Bit 2**	**FLAGIN Action**
			0	0	None
			0	1	Disable PWM outputs in Channel A
			1	0	Disable PWM outputs in Channel B
			1	1	Disable all PWM outputs (Channel A, Channel B, and Channel C)
[1:0]	Action after FLAGIN is cleared	R/W	These bits specify the action to take after the FLAGIN flag is cleared.		
			Bit 1	**Bit 0**	**Action After FLAGIN Is Cleared**
			0	0	After the reenable delay time, the PWM outputs are reenabled using the soft start process
			0	1	The PWM outputs are reenabled immediately without a soft start
			1	0	A PSON signal is needed to reenable the PWM outputs
			1	1	A PSON signal is needed to reenable the PWM outputs

Register 0xFE07 selects flags to be blanked during soft start. When a flag is blanked, the flag is set but no action takes place. During the soft start of any channel, the following flags are always blanked: FLAGIN, OTP1, OTP2, and ACSNS. During the soft start of Channel A, these flags are also blanked: REVERSE_A and UVP_A. During the soft start of Channel B, these flags are also blanked: REVERSE_B and UVP_B.

Table 33. Register 0xFE07—Flag Blanking During Soft Start

Bits	Bit Name	R/W	Description
7	Reserved	R/W	Reserved.
6	CS_OCP blanking	R/W	0 = blank CS_OCP flag during Channel C soft start. 1 = do not blank CS_OCP flag.
5	OVP_B blanking	R/W	0 = blank OVP_B flag during Channel B soft start. 1 = do not blank OVP_B flag.
4	OVP_A blanking	R/W	0 = blank OVP_A flag during Channel A soft start. 1 = do not blank OVP_A flag.
3	CS2_B_OCP blanking	R/W	0 = blank CS2_B_OCP flag during Channel B soft start. 1 = do not blank CS2_B_OCP flag.
2	CS2_A_OCP blanking	R/W	0 = blank CS2_A_OCP flag during Channel A soft start. 1 = do not blank CS2_A_OCP flag.
1	CS1_B_OCP blanking	R/W	0 = blank CS1_B_OCP flag during Channel B soft start. 1 = do not blank CS1_B_OCP flag.
0	CS1_A_OCP blanking	R/W	0 = blank CS1_A_OCP flag during Channel A soft start. 1 = do not blank CS1_A_OCP flag.

Register 0xFE08 specifies whether volt-second balance control is blanked during the soft start of the channel that is configured for volt-second balance (Channel A or Channel C). Bit 7 of Register 0xFE72 selects the channel for volt-second balance control. Register 0xFE08 also specifies whether to disable the SR outputs (OUT3, OUT4, OUT7, and OUT8) during the soft start of their assigned channel. When synchronous rectification is not disabled on a channel during soft start, the PWM output disable settings in Register 0xFE60 determine whether the output is disabled.

Table 34. Register 0xFE08—Volt-Second Balance Blanking and SR Disable During Soft Start

Bits	Bit Name	R/W	Description
7	Reserved	R/W	Reserved.
6	ACSNS reenable blank	R/W	This bit specifies whether the ACSNS flag is blanked during the flag reenable time. 0 = do not blank the ACSNS flag during the flag reenable time. 1 = blank the ACSNS flag during the flag reenable time.
5	First flag ID update	R/W	This bit specifies whether the first flag ID is saved in the EEPROM. 0 = first flag ID is not saved in the EEPROM. 1 = first flag ID is saved in the EEPROM.
4	Flag shutdown timing	R/W	This bit specifies when the PWM outputs are shut down after a flag is triggered. 0 = PWM outputs are shut down at the end of the PWM cycle. 1 = PWM outputs are shut down immediately.
3	Volt-second balance blanking	R/W	This bit specifies whether volt-second balance control is blanked during the soft start of the channel that is enabled for volt-second balance control (Channel A or Channel C, as specified by Bit 7 of Register 0xFE72). 0 = do not blank volt-second balance control during Channel A or Channel C soft start. 1 = blank volt-second balance control during Channel A or Channel C soft start.
2	Channel C SR disable	R/W	This bit specifies whether the SR outputs (OUT3, OUT4, OUT7, and OUT8) are disabled during the soft start of Channel C, if these outputs are assigned to Channel C. 0 = do not disable OUT3, OUT4, OUT7, and OUT8 during soft start of Channel C. 1 = disable OUT3, OUT4, OUT7, and OUT8 during soft start of Channel C.
1	Channel B SR disable	R/W	This bit specifies whether the SR outputs (OUT3, OUT4, OUT7, and OUT8) are disabled during the soft start of Channel B, if these outputs are assigned to Channel B. 0 = do not disable OUT3, OUT4, OUT7, and OUT8 during soft start of Channel B. 1 = disable OUT3, OUT4, OUT7, and OUT8 during soft start of Channel B.
0	Channel A SR disable	R/W	This bit specifies whether the SR outputs (OUT3, OUT4, OUT7, and OUT8) are disabled during the soft start of Channel A, if these outputs are assigned to Channel A. 0 = do not disable OUT3, OUT4, OUT7, and OUT8 during soft start of Channel A. 1 = disable OUT3, OUT4, OUT7, and OUT8 during soft start of Channel A.

Table 35. Register 0xFE09—PGOOD Debounce

Bits	Bit Name	R/W	Description		
[7:6]	PGOOD_B on debounce	R/W	These bits set the PGOOD_B on debounce time, that is, the time from when the PGOOD_B on condition is met to when the PGOOD_B flag is set.		
			Bit 7	**Bit 6**	**Typical PGOOD_B On Debounce Time**
			0	0	0 ms
			0	1	200 ms
			1	0	320 ms
			1	1	600 ms
[5:4]	PGOOD_B off debounce	R/W	These bits set the PGOOD_B off debounce time, that is, the time from when the PGOOD_B off condition is met to when the PGOOD_B flag is cleared.		
			Bit 5	**Bit 4**	**Typical PGOOD_B Off Debounce Time**
			0	0	0 ms
			0	1	200 ms
			1	0	320 ms
			1	1	600 ms

Bits	Bit Name	R/W	Description		
[3:2]	PGOOD_A on debounce	R/W	These bits set the PGOOD_A on debounce time, that is, the time from when the PGOOD_A on condition is met to when the PGOOD_A flag is set.		
			Bit 3	**Bit 2**	**Typical PGOOD_A On Debounce Time**
			0	0	0 ms
			0	1	200 ms
			1	0	320 ms
			1	1	600 ms
[1:0]	PGOOD_A off debounce	R/W	These bits set the PGOOD_A off debounce time, that is, the time from when the PGOOD_A off condition is met to when the PGOOD_A flag is cleared.		
			Bit 1	**Bit 0**	**Typical PGOOD_A Off Debounce Time**
			0	0	0 ms
			0	1	200 ms
			1	0	320 ms
			1	1	600 ms

SWITCHING FREQUENCY REGISTERS

Table 36. Register 0xFE0A, Register 0xFE0B, and Register 0xFE0C—Switching Frequency for Channel A, Channel B, and Channel C

Bits	Bit Name	R/W	Description						
[7:6]	Frequency synchronization setting	R/W	These bits set the switching frequency to a multiple of the synchronization input frequency.						
			Bit 7	**Bit 6**	**Multiple of Synchronization Input Frequency**				
			0	0	1				
			0	1	2				
			1	0	Reserved				
			1	1	Reserved				
[5:0]	Switching frequency	R/W	These bits set the switching frequency.						
			Bit 5	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Frequency (kHz)**
			0	0	0	0	0	0	48.8
			0	0	0	0	0	1	55.8
			0	0	0	0	1	0	60.1
			0	0	0	0	1	1	65.1
			0	0	0	1	0	0	71.0
			0	0	0	1	0	1	78.1
			0	0	0	1	1	0	86.8
			0	0	0	1	1	1	97.7
			0	0	1	0	0	0	104.2
			0	0	1	0	0	1	111.6
			0	0	1	0	1	0	120.2
			0	0	1	0	1	1	130.2
			0	0	1	1	0	0	135.9
			0	0	1	1	0	1	142.0
			0	0	1	1	1	0	148.8
			0	0	1	1	1	1	156.3
			0	1	0	0	0	0	164.5
			0	1	0	0	0	1	173.6
			0	1	0	0	1	0	183.8
			0	1	0	0	1	1	195.3
			0	1	0	1	0	0	201.6
			0	1	0	1	0	1	208.3
			0	1	0	1	1	0	215.5
			0	1	0	1	1	1	223.2
			0	1	1	0	0	0	231.5

Bits	Bit Name	R/W	Description						
[5:0]	Switching frequency	R/W	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Frequency (kHz)**
			0	1	1	0	0	1	240.4
			0	1	1	0	1	0	250.0
			0	1	1	0	1	1	260.4
			0	1	1	1	0	0	271.7
			0	1	1	1	0	1	284.1
			0	1	1	1	1	0	297.6
			0	1	1	1	1	1	312.5
			1	0	0	0	0	0	320.5
			1	0	0	0	0	1	328.9
			1	0	0	0	1	0	337.8
			1	0	0	0	1	1	347.2
			1	0	0	1	0	0	357.1
			1	0	0	1	0	1	367.6
			1	0	0	1	1	0	378.8
			1	0	0	1	1	1	390.6
			1	0	1	0	0	0	396.8
			1	0	1	0	0	1	403.2
			1	0	1	0	1	0	409.8
			1	0	1	0	1	1	416.7
			1	0	1	1	0	0	423.7
			1	0	1	1	0	1	431.0
			1	0	1	1	1	0	438.6
			1	0	1	1	1	1	446.4
			1	1	0	0	0	0	454.5
			1	1	0	0	0	1	463.0
			1	1	0	0	1	0	471.7
			1	1	0	0	1	1	480.8
			1	1	0	1	0	0	490.2
			1	1	0	1	0	1	500.0
			1	1	0	1	1	0	510.2
			1	1	0	1	1	1	520.8
			1	1	1	0	0	0	531.9
			1	1	1	0	0	1	543.5
			1	1	1	0	1	0	555.6
			1	1	1	0	1	1	568.2
			1	1	1	1	0	0	581.4
			1	1	1	1	0	1	595.2
			1	1	1	1	1	0	609.8
			1	1	1	1	1	1	625.0

When synchronization is enabled, the controller takes the SYNI signal, adds the t_{SYNC_DELAY}, together with the 760 ns propagation delay, to generate the internal synchronization reference clock, as shown in Figure 40. Each channel then uses the reference clock (or a multiple of the reference clock if programmed in Register 0xFE0A, Register 0xFE0B, or Register 0xFE0C) to generate its own clock. Register 0xFE0D is used to set the t_{SYNC_DELAY} time.

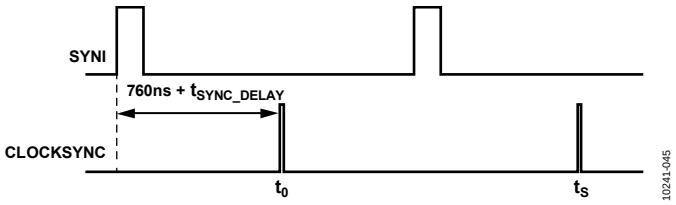


Figure 40. Synchronization Timing

Table 37. Register 0xFE0D—Frequency Synchronization Delay Time

Bits	Bit Name	R/W	Description
[7:0]	t_{SYNC_DELAY}	R/W	This register sets the additional delay of the synchronization reference clock to the rising edge of the SYNI pin signal. Each LSB corresponds to 80 ns resolution.

Table 38. Register 0xFE0E—SYNO Selection and Synchronization Enable

Bits	Bit Name	R/W	Description
[7:4]	Reserved	R/W	Reserved.
3	SYNO selection	R/W	0 = select Channel C as the SYNO reference. 1 = select Channel A as the SYNO reference.
2	Enable Channel C synchronization	R/W	Setting this bit enables frequency synchronization for Channel C.
1	Enable Channel B synchronization	R/W	Setting this bit enables frequency synchronization for Channel B.
0	Enable Channel A synchronization	R/W	Setting this bit enables frequency synchronization for Channel A.

Table 39. Register 0xFE0F—Flag/Synchronization Pin Functions

Bits	Bit Name	R/W	Description
7	Reserved	R/W	Reserved.
6	Channel B filter 180° interleaving	R/W	Setting this bit enables 180° interleaving on the clock for the ADC and filter of Channel B. This setting prevents additional delays when the PWM outputs in Channel B use 180° interleaving.
5	FLAGOUT polarity	R/W	Setting this bit inverts the polarity of the FLGO/SYNO pin signal when the pin is programmed as a flag output (FLAGOUT). 0 = normal mode. A high signal on the FLGO/SYNO pin sets FLAGOUT. 1 = inverted. A low signal on the FLGO/SYNO pin sets FLAGOUT.
4	FLAGOUT selection	R/W	This bit configures the FLGO/SYNO pin to respond to the LIGHTLOAD_A or LIGHTLOAD_B flag. 0 = LIGHTLOAD_A flag triggers FLAGOUT. 1 = LIGHTLOAD_B flag triggers FLAGOUT.
3	FLGO/SYNO pin function selection	R/W	This bit configures the FLGO/SYNO pin as a flag output or a synchronization output. 0 = FLGO/SYNO pin used as a synchronization output (SYNO). 1 = FLGO/SYNO pin used as a flag output (FLAGOUT).
2	FLAGIN polarity	R/W	Setting this bit inverts the polarity of the FLGI/SYNI pin signal when the pin is programmed as a flag input (FLAGIN). 0 = normal mode. A high signal on the FLGI/SYNI pin sets FLAGIN. 1 = inverted. A low signal on the FLGI/SYNI pin sets FLAGIN.
1	FLAGIN debounce time	R/W	This bit sets the debounce time for FLAGIN. 0 = 0 µs debounce time for FLAGIN. 1 = 100 µs debounce time for FLAGIN.
0	FLGI/SYNI pin function selection	R/W	This bit configures the FLGI/SYNI pin as a flag input or a synchronization input. 0 = FLGI/SYNI pin used as a synchronization input (SYNI). 1 = FLGI/SYNI pin used as a flag input (FLAGIN).

CHANNEL A/CHANNEL B CURRENT SENSE AND LIMIT SETTING REGISTERS

Table 40. Register 0xFE10—CS1_A Gain Trim

Bits	Bit Name	R/W	Description
7	Gain polarity	R/W	1 = negative gain is introduced. 0 = positive gain is introduced.
[6:0]	CS1_A gain trim	R/W	This value calibrates the CS1_A current sense gain. For more information, see the CS, CS1_A, and CS1_B Gain Trim section.

Table 41. Register 0xFE11—CS1_B Gain Trim

Bits	Bit Name	R/W	Description
7	Gain polarity	R/W	1 = negative gain is introduced. 0 = positive gain is introduced.
[6:0]	CS1_B gain trim	R/W	This value calibrates the CS1_B current sense gain. For more information, see the CS, CS1_A, and CS1_B Gain Trim section.

Table 42. Register 0xFE12—CS2_A Gain Trim

Bits	Bit Name	R/W	Description
7	Gain polarity	R/W	1 = negative gain is introduced. 0 = positive gain is introduced.
[6:0]	CS2_A gain trim	R/W	This value calibrates the CS2_A current sense gain. For more information, see the CS2_A and CS2_B Gain Trim section.

Table 43. Register 0xFE13—CS2_B Gain Trim

Bits	Bit Name	R/W	Description
7	Gain polarity	R/W	1 = negative gain is introduced. 0 = positive gain is introduced.
[6:0]	CS2_B gain trim	R/W	This value calibrates the CS2_B current sense gain. For more information, see the CS2_A and CS2_B Gain Trim section.

Table 44. Register 0xFE14—CS2_A Digital Offset Trim

Bits	Bit Name	R/W	Description
[7:0]	CS2_A digital offset trim	R/W	This register contains the CS2_A digital offset trim level. This value is used to calibrate the CS2_A value. For more information, see the CS2_A and CS2_B Offset Trim section.

Table 45. Register 0xFE15—CS2_B Digital Offset Trim

Bits	Bit Name	R/W	Description
[7:0]	CS2_B digital offset trim	R/W	This register contains the CS2_B digital offset trim level. This value is used to calibrate the CS2_B value. For more information, see the CS2_A and CS2_B Offset Trim section.

Table 46. Register 0xFE16—CS2_A Analog Offset Trim

Bits	Bit Name	R/W	Description
7	Reserved	R/W	Reserved.
6	Analog trim polarity	R/W	1 = negative gain is introduced. 0 = positive gain is introduced.
[5:0]	CS2_A analog offset trim	R/W	This value calibrates the CS2_A value. For more information, see the CS2_A and CS2_B Offset Trim section.

Table 47. Register 0xFE17—CS2_B Analog Offset Trim

Bits	Bit Name	R/W	Description
7	Reserved	R/W	Reserved.
6	Analog trim polarity	R/W	1 = negative gain is introduced. 0 = positive gain is introduced.
[5:0]	CS2_B analog offset trim	R/W	This value calibrates the CS2_B value. For more information, see the CS2_A and CS2_B Offset Trim section.

Register 0xFE18 sets the CS2_A OCP threshold, and Register 0xFE19 sets the CS2_B OCP threshold.

Table 48. Register 0xFE18 and Register 0xFE19—CS2_A OCP Threshold and CS2_B OCP Threshold

Bits	Bit Name	R/W	Description
[7:0]	CS2_A/CS2_B OCP threshold	R/W	The 8-bit OCP threshold set in this register is compared with Bits[15:8] in the CS2_A or CS2_B value register (Register 0xFED3 or Register 0xFED4). If the eight MSBs in the value register are higher, the CS2_A_OCP or CS2_B_OCP flag is set. When the OCP threshold is set to 0xFF (255 decimal), the CS2_A_OCP or CS2_B_OCP flag is always cleared. The range of the CS2 ADC is 0 mV to 120 mV, so the step size is 120 mV/4096 = 29.3 µV. Therefore, the threshold step size is 29.3 µV × 16 = 468.8 µV. The OCP threshold can be calculated as follows: *Threshold Target* (V) = (*Threshold Code* + 1) × 468.8 µV The GUI converts the voltage to current based on the value of the current sensing resistor. The valid range of the register code is from 2 to 241 decimal.

Register 0xFE1A selects the CS2_A high-side/low-side setting, sets the CS2_A_OCP flag debounce time, and sets the light load threshold for Channel A. Register 0xFE1B sets the same values for Channel B.

Table 49. Register 0xFE1A and Register 0xFE1B—CS2_A/CS2_B High-Side/Low-Side Setting and Channel A/Channel B Light Load Threshold

Bits	Bit Name	R/W	Description
7	High-side/low-side sensing	R/W	This bit configures the part for high-side resistor current sensing or low-side current sensing. 0 = CS2_A or CS2_B is configured for low-side sensing. 1 = CS2_A or CS2_B is configured for high-side sensing.
[6:5]	CS2_A_OCP/CS2_B_OCP flag debounce	R/W	These bits set the CS2_A_OCP/CS2_B_OCP flag debounce time.

Bit 6	Bit 5	Typical Debounce Time
0	0	0 ms
0	1	20 ms
1	0	200 ms
1	1	1 sec

Bits	Bit Name	R/W	Description
4	LIGHTLOAD_A/LIGHTLOAD_B flag blanking in soft start	R/W	This bit specifies whether to blank the LIGHTLOAD_A/LIGHTLOAD_B flag during soft start. 0 = do not blank the LIGHTLOAD_A/LIGHTLOAD_B flag during Channel A/Channel B soft start. 1 = blank the LIGHTLOAD_A/LIGHTLOAD_B flag during Channel A/Channel B soft start.
[3:0]	CS2_A/CS2_B light load threshold	R/W	These bits set the CS2_A/CS2_B ADC light load threshold value, below which the LIGHTLOAD_A or LIGHTLOAD_B flag is set and Channel A or Channel B enters light load mode. Each LSB corresponds to 64 LSBs of the 12-bit CS2_A/CS2_B reading, which is 1.56% of the full range (1.875 mV). Hysteresis is included to exit light load mode; the threshold to exit light load mode is 96 LSBs greater than the threshold to enter light load mode (96 LSBs = 2.34% of the full range, that is, 2.8125 mV). When these bits are set to 0, the LIGHTLOAD_A/LIGHTLOAD_B flag is always cleared.

CHANNEL A/CHANNEL B VOLTAGE SENSE AND LIMIT SETTING REGISTERS

Table 50. Register 0xFE1C—VS_A Gain Trim

Bits	Bit Name	R/W	Description
7	Trim polarity	R/W	1 = negative gain is introduced. 0 = positive gain is introduced.
[6:0]	VS_A gain trim	R/W	These bits set the amount of gain trim that is applied to the VS_A ADC reading. This register trims the voltage at the VS_A pin for external resistor tolerances. For more information, see the VS_A and VS_B Gain Trim section.

Table 51. Register 0xFE1D—VS_B Gain Trim

Bits	Bit Name	R/W	Description
7	Trim polarity	R/W	1 = negative gain is introduced. 0 = positive gain is introduced.
[6:0]	VS_B gain trim	R/W	These bits set the amount of gain trim that is applied to the VS_B ADC reading. This register trims the voltage at the VS_B pin for external resistor tolerances. For more information, see the VS_A and VS_B Gain Trim section.

Table 52. Register 0xFE1E—VS_A Reference Maximum Limit

Bits	Bit Name	R/W	Description
[7:6]	Reserved	R/W	Reserved.
[5:0]	VS_A maximum reference	R/W	This register sets the maximum limit of the Channel A output voltage reference. It sets the six MSBs for the reference limit. The factory default setting is 0x3F.

Table 53. Register 0xFE1F—VS_B Reference Maximum Limit

Bits	Bit Name	R/W	Description
[7:6]	Reserved	R/W	Reserved.
[5:0]	VS_B maximum reference	R/W	This register sets the maximum limit of the Channel B output voltage reference. It sets the six MSBs for the reference limit. The factory default setting is 0x3F.

Table 54. Register 0xFE20—VS_A Reference Minimum Limit

Bits	Bit Name	R/W	Description
[7:6]	Reserved	R/W	Reserved.
[5:0]	VS_A minimum reference	R/W	This register sets the minimum limit of the Channel A output voltage reference. It sets the six MSBs for the reference limit. The factory default setting is 0x00.

Table 55. Register 0xFE21—VS_B Reference Minimum Limit

Bits	Bit Name	R/W	Description
[7:6]	Reserved	R/W	Reserved.
[5:0]	VS_B minimum reference	R/W	This register sets the minimum limit of the Channel B output voltage reference. It sets the six MSBs for the reference limit. The factory default setting is 0x00.

Table 56. Register 0xFE22—VS_A Reference Setting (MSBs)

Bits	Bit Name	R/W	Description
[7:0]	VS_A voltage reference MSBs	R/W	This register sets the eight MSBs of the output voltage reference for Channel A. Together with Bits[3:0] of Register 0xFE24, this register sets the 12-bit reference. In a steady state, closed-loop operation, the output of the VS_A ADC is regulated to the reference setting value.

Table 57. Register 0xFE23—VS_B Reference Setting (MSBs)

Bits	Bit Name	R/W	Description
[7:0]	VS_B voltage reference MSBs	R/W	This register sets the eight MSBs of the output voltage reference for Channel B. Together with Bits[3:0] of Register 0xFE25, this register sets the 12-bit reference. In a steady state, closed-loop operation, the output of the VS_B ADC is regulated to the reference setting value.

Table 58. Register 0xFE24—VS_A Reference Setting (LSBs)

Bits	Bit Name	R/W	Description
[7:4]	Reserved	R/W	Reserved.
[3:0]	VS_A voltage reference LSBs	R/W	This register sets the four LSBs of the output voltage reference for Channel A. Together with Register 0xFE22, this register sets the 12-bit reference. In a steady state, closed-loop operation, the output of the VS_A ADC is regulated to the reference setting value.

Table 59. Register 0xFE25—VS_B Reference Setting (LSBs)

Bits	Bit Name	R/W	Description
[7:4]	Reserved	R/W	Reserved.
[3:0]	VS_B voltage reference LSBs	R/W	This register sets the four LSBs of the output voltage reference for Channel B. Together with Register 0xFE23, this register sets the 12-bit reference. In a steady state, closed-loop operation, the output of the VS_B ADC is regulated to the reference setting value.

Table 60. Register 0xFE26—OVP_A Setting

Bits	Bit Name	R/W	Description		
[7:6]	OVP_A flag debounce time	R/W	These bits set the OVP_A flag debounce time.		
			Bit 7	**Bit 6**	**Typical Debounce Time**
			0	0	0 µs
			0	1	0.96 µs
			1	0	2.24 µs
			1	1	8 µs
[5:0]	OVP_A threshold	R/W	These bits set the threshold for the OVP_A analog comparator. This threshold is programmable from 0.75 V to 1.5 V. A setting of 0x00 corresponds to a 0.75 V threshold. A setting of 0x3F corresponds to a 1.5 V threshold. Each LSB increments the threshold by 11.904 mV, as follows: *OVP Threshold* = (*Code* × 0.75/63) + 0.75		

Table 61. Register 0xFE27—OVP_B Setting

Bits	Bit Name	R/W	Description		
[7:6]	OVP_B flag debounce time	R/W	These bits set the OVP_B flag debounce time.		
			Bit 7	**Bit 6**	**Typical Debounce Time**
			0	0	0 µs
			0	1	0.96 µs
			1	0	2.24 µs
			1	1	8 µs
[5:0]	OVP_B threshold	R/W	These bits set the threshold for the OVP_B analog comparator. This threshold is programmable from 0.75 V to 1.5 V. A setting of 0x00 corresponds to a 0.75 V threshold. A setting of 0x3F corresponds to a 1.5 V threshold. Each LSB increments the threshold by 11.904 mV, as follows: *OVP Threshold* = (*Code* × 0.75/63) + 0.75		

Table 62. Register 0xFE28—UVP_A Setting

Bits	Bit Name	R/W	Description
7	UVP_A flag debounce time	R/W	This bit sets the UVP_A flag debounce time. 0 = 0 ms. 1 = 100 ms.
[6:0]	UVP_A threshold	R/W	These bits set the UVP_A threshold. The UVP_A flag is set when the UVP_A threshold is larger than the seven MSBs of the VS_A value register (Register 0xFED5). Each LSB of the UVP_A threshold corresponds to 12.5 mV. When these bits are set to 0, the UVP_A flag is always cleared.

Table 63. Register 0xFE29—UVP_B Setting

Bits	Bit Name	R/W	Description
7	UVP_B flag debounce time	R/W	This bit sets the UVP_B flag debounce time. 0 = 0 ms. 1 = 100 ms.
[6:0]	UVP_B threshold	R/W	These bits set the UVP_B threshold. The UVP_B flag is set when the UVP_B threshold is larger than the seven MSBs of the VS_B value register (Register 0xFED6). Each LSB of the UVP_B threshold corresponds to 12.5 mV. When these bits are set to 0, the UVP_B flag is always cleared.

SOFT START, DIGITAL FILTER, AND MODULATION SETTING REGISTERS

Table 64. Register 0xFE2A—Channel A Soft Start Ramp Rate

Bits	Bit Name	R/W	Description		
[7:2]	Reserved	R/W	Reserved.		
[1:0]	Channel A soft start ramp time	R/W	These bits set the output reference ramp rate during soft start for Channel A. The ramp time is based on V_{REF} = 2/3 full-scale range (FSR).		
			Bit 1	**Bit 0**	**Typical Soft Start Ramp Rate**
			0	0	1.75 ms
			0	1	10.5 ms
			1	0	21.0 ms
			1	1	40.2 ms

Table 65. Register 0xFE2B—Channel B Soft Start Ramp Rate

Bits	Bit Name	R/W	Description		
[7:2]	Reserved	R/W	Reserved.		
[1:0]	Channel B soft start ramp time	R/W	These bits set the output reference ramp rate during soft start for Channel B. The ramp time is based on V_{REF} = 2/3 full-scale range (FSR).		
			Bit 1	**Bit 0**	**Typical Soft Start Ramp Rate**
			0	0	1.75 ms
			0	1	10.5 ms
			1	0	21.0 ms
			1	1	40.2 ms

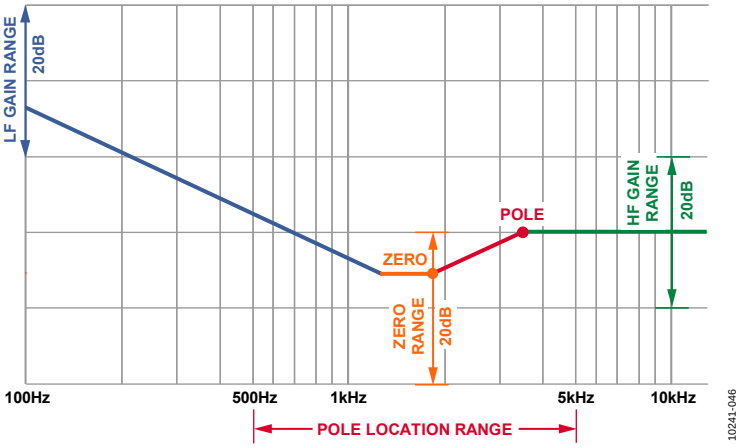


Figure 41. Digital Filter Programmability

Table 66. Register 0xFE2C—Channel A Normal Mode Low Frequency Gain

Bits	Bit Name	R/W	Description
[7:0]	Channel A normal mode low frequency gain	R/W	This register specifies the low frequency gain of the feedback filter for Channel A in normal mode. The gain is programmable over a 20 dB range (see Figure 41). Each LSB corresponds to a 0.3 dB increase.

Table 67. Register 0xFE2D—Channel B Normal Mode Low Frequency Gain

Bits	Bit Name	R/W	Description
[7:0]	Channel B normal mode low frequency gain	R/W	This register specifies the low frequency gain of the feedback filter for Channel B in normal mode. The gain is programmable over a 20 dB range (see Figure 41). Each LSB corresponds to a 0.3 dB increase.

Table 68. Register 0xFE2E—Channel A Normal Mode Zero Setting

Bits	Bit Name	R/W	Description
[7:0]	Channel A normal mode zero setting	R/W	This register specifies the position of the zero in the feedback filter for Channel A in normal mode (see Figure 41).

Table 69. Register 0xFE2F—Channel B Normal Mode Zero Setting

Bits	Bit Name	R/W	Description
[7:0]	Channel B normal mode zero setting	R/W	This register specifies the position of the zero in the feedback filter for Channel B in normal mode (see Figure 41).

Table 70. Register 0xFE30—Channel A Normal Mode Pole Setting

Bits	Bit Name	R/W	Description
[7:0]	Channel A normal mode pole setting	R/W	This register specifies the position of the pole in the feedback filter for Channel A in normal mode (see Figure 41).

Table 71. Register 0xFE31—Channel B Normal Mode Pole Setting

Bits	Bit Name	R/W	Description
[7:0]	Channel B normal mode pole setting	R/W	This register specifies the position of the pole in the feedback filter for Channel B in normal mode (see Figure 41).

Table 72. Register 0xFE32—Channel A Normal Mode High Frequency Gain

Bits	Bit Name	R/W	Description
[7:0]	Channel A normal mode high frequency gain	R/W	This register specifies the high frequency gain of the feedback filter for Channel A in normal mode. The gain is programmable over a 20 dB range (see Figure 41). Each LSB corresponds to a 0.3 dB increase.

Table 73. Register 0xFE33—Channel B Normal Mode High Frequency Gain

Bits	Bit Name	R/W	Description
[7:0]	Channel B normal mode high frequency gain	R/W	This register specifies the high frequency gain of the feedback filter for Channel B in normal mode. The gain is programmable over a 20 dB range (see Figure 41). Each LSB corresponds to a 0.3 dB increase.

Table 74. Register 0xFE34—Channel A Light Load Mode Low Frequency Gain

Bits	Bit Name	R/W	Description
[7:0]	Channel A light load mode low frequency gain	R/W	This register specifies the low frequency gain of the feedback filter for Channel A in light load mode. The gain is programmable over a 20 dB range (see Figure 41). Each LSB corresponds to a 0.3 dB increase.

Table 75. Register 0xFE35—Channel B Light Load Mode Low Frequency Gain

Bits	Bit Name	R/W	Description
[7:0]	Channel B light load mode low frequency gain	R/W	This register specifies the low frequency gain of the feedback filter for Channel B in light load mode. The gain is programmable over a 20 dB range (see Figure 41). Each LSB corresponds to a 0.3 dB increase.

Table 76. Register 0xFE36—Channel A Light Load Mode Zero Setting

Bits	Bit Name	R/W	Description
[7:0]	Channel A light load mode zero setting	R/W	This register specifies the position of the zero in the feedback filter for Channel A in light load mode (see Figure 41).

Table 77. Register 0xFE37—Channel B Light Load Mode Zero Setting

Bits	Bit Name	R/W	Description
[7:0]	Channel B light load mode zero setting	R/W	This register specifies the position of the zero in the feedback filter for Channel B in light load mode (see Figure 41).

Table 78. Register 0xFE38—Channel A Light Load Mode Pole Setting

Bits	Bit Name	R/W	Description
[7:0]	Channel A light load mode pole setting	R/W	This register specifies the position of the pole in the feedback filter for Channel A in light load mode (see Figure 41).

Table 79. Register 0xFE39—Channel B Light Load Mode Pole Setting

Bits	Bit Name	R/W	Description
[7:0]	Channel B light load mode pole setting	R/W	This register specifies the position of the pole in the feedback filter for Channel B in light load mode (see Figure 41).

Table 80. Register 0xFE3A—Channel A Light Load Mode High Frequency Gain

Bits	Bit Name	R/W	Description
[7:0]	Channel A light load mode high frequency gain	R/W	This register specifies the high frequency gain of the feedback filter for Channel A in light load mode. The gain is programmable over a 20 dB range (see Figure 41). Each LSB corresponds to a 0.3 dB increase.

Table 81. Register 0xFE3B—Channel B Light Load Mode High Frequency Gain

Bits	Bit Name	R/W	Description
[7:0]	Channel B light load mode high frequency gain	R/W	This register specifies the high frequency gain of the feedback filter for Channel B in light load mode. The gain is programmable over a 20 dB range (see Figure 41). Each LSB corresponds to a 0.3 dB increase.

Figure 42 illustrates the modulation limit settings. Register 0xFE3C and Register 0xFE3D configure the modulation limit for Channel A and Channel B.

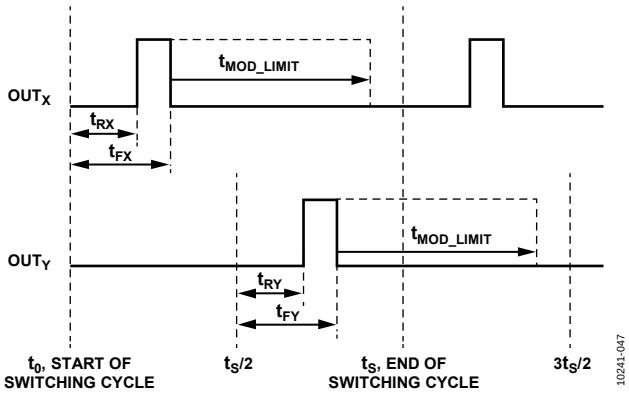


Figure 42. Setting Modulation Limits

Table 82. Register 0xFE3C—Channel A Modulation Limit

Bits	Bit Name	R/W	Description	
[7:0]	Channel A modulation limit	R/W	This register sets the maximum duty cycle modulation limit for PWM outputs in Channel A. The modulation limit is the maximum time variation for the modulated edges from the default timing (see Figure 42). The step size of an LSB depends on the switching frequency.	
			Switching Frequency	**LSB Step Size**
			48.8 kHz to 86.8 kHz	80 ns
			97.7 kHz to 183.8 kHz	40 ns
			195.3 kHz to 378.8 kHz	20 ns
			390.6 kHz to 625.0 kHz	10 ns

Table 83. Register 0xFE3D—Channel B Modulation Limit

Bits	Bit Name	R/W	Description	
[7:0]	Channel B modulation limit	R/W	This register sets the maximum duty cycle modulation limit for PWM outputs in Channel B. The modulation limit is the maximum time variation for the modulated edges from the default timing (see Figure 42). The step size of an LSB depends on the switching frequency.	
			Switching Frequency	**LSB Step Size**
			48.8 kHz to 86.8 kHz	80 ns
			97.7 kHz to 183.8 kHz	40 ns
			195.3 kHz to 378.8 kHz	20 ns
			390.6 kHz to 625.0 kHz	10 ns

Table 84. Register 0xFE3E—Channel A Feedforward and Soft Start Digital Filter Setting

Bits	Bit Name	R/W	Description		
[7:6]	Reserved	R/W	Reserved.		
5	High frequency ADC debounce time	R/W	This bit sets the debounce time for detecting the settling of the VS_A high frequency ADC. Bit 4 must be set to 1. 0 = 5 ms. 1 = 10 ms.		
4	High frequency ADC debounce enable	R/W	Setting this bit enables a debounce time for detecting the settling of the VS_A high frequency ADC at the end of a soft start. The debounce time is set using Bit 5.		
3	Feedforward ADC selection	R/W	This bit should be set to 1 (factory default setting). This bit selects the 11-bit ACSNS ADC for feedforward control of Channel A. Do not set this bit to 0.		
2	Feedforward enable	R/W	This bit enables or disables feedforward control on Channel A. 0 = feedforward control disabled on Channel A. 1 = feedforward control enabled on Channel A.		
[1:0]	Soft start filter gain	R/W	These bits set the low-pass filter gain for Channel A during soft start.		
			Bit 1	**Bit 0**	**Soft Start Filter Gain**
			0	0	1
			0	1	2
			1	0	4
			1	1	8

Table 85. Register 0xFE3F—Channel B Feedforward and Soft Start Digital Filter Setting

Bits	Bit Name	R/W	Description		
[7:6]	Reserved	R/W	Reserved.		
5	High frequency ADC debounce time	R/W	This bit sets the debounce time for detecting the settling of the VS_B high frequency ADC. Bit 4 must be set to 1. 0 = 5 ms. 1 = 10 ms.		
4	High frequency ADC debounce enable	R/W	Setting this bit enables a debounce time for detecting the settling of the VS_B high frequency ADC at the end of a soft start. The debounce time is set using Bit 5.		
3	Feedforward ADC selection	R/W	This bit should be set to 1 (factory default setting). This bit selects the 11-bit ACSNS ADC for feedforward control of Channel B. Do not set this bit to 0.		
2	Feedforward enable	R/W	This bit enables or disables feedforward control on Channel B. 0 = feedforward control disabled on Channel B. 1 = feedforward control enabled on Channel B.		
[1:0]	Soft start filter gain	R/W	These bits set the low-pass filter gain for Channel B during soft start.		
			Bit 1	**Bit 0**	**Soft Start Filter Gain**
			0	0	1
			0	1	2
			1	0	4
			1	1	8

PWM OUTPUT TIMING REGISTERS

Figure 43 shows the timing of the rising and falling edges of the PWM outputs. Register 0xFE40 to Register 0xFE5F describe the implementation and programming of the eight PWM signals that are output from the ADP1053. In Figure 43, OUT_X is an example of PWM timing without the 180° phase shift setting, and OUT_Y is an example of PWM timing with the 180° phase shift setting.

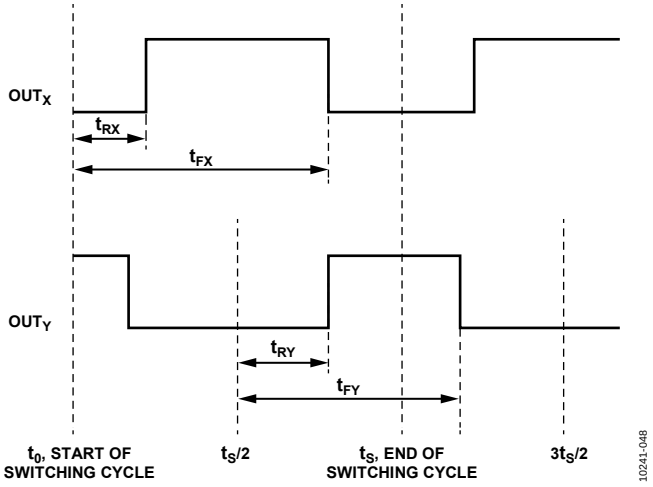


Figure 43. PWM Output Timing Diagram

Table 86. Register 0xFE40/0xFE44/0xFE48/0xFE4C/0xFE50/0xFE54/0xFE58/0xFE5C—OUT1 to OUT8 Rising Edge Timing (MSBs)

Bits	Bit Name	R/W	Description
[7:0]	OUT_X rising edge timing (t_{RX}), MSBs	R/W	This register contains the eight MSBs of the 12-bit t_{RX} time. This value is always used with Bits[7:4] of Register 0xFE42/0xFE46/0xFE4A/0xFE4E/0xFE52/0xFE56/0xFE5A/0xFE5E, which contains the four LSBs of the t_{RX} time. Each LSB corresponds to 5 ns resolution.

Table 87. Register 0xFE41/0xFE45/0xFE49/0xFE4D/0xFE51/0xFE55/0xFE59/0xFE5D—OUT1 to OUT8 Falling Edge Timing (MSBs)

Bits	Bit Name	R/W	Description
[7:0]	OUT_X falling edge timing (t_{FX}), MSBs	R/W	This register contains the eight MSBs of the 12-bit t_{FX} time. This value is always used with Bits[3:0] of Register 0xFE42/0xFE46/0xFE4A/0xFE4E/0xFE52/0xFE56/0xFE5A/0xFE5E, which contains the four LSBs of the t_{FX} time. Each LSB corresponds to 5 ns resolution.

Table 88. Register 0xFE42/0xFE46/0xFE4A/0xFE4E/0xFE52/0xFE56/0xFE5A/0xFE5E—OUT1 to OUT8 Rising and Falling Edge Timing (LSBs)

Bits	Bit Name	R/W	Description
[7:4]	OUT_X rising edge timing (t_{RX}), LSBs	R/W	These bits contain the four LSBs of the 12-bit t_{RX} time. This value is always used with the eight bits of Register 0xFE40/0xFE44/0xFE48/0xFE4C/0xFE50/0xFE54/0xFE58/0xFE5C, which contains the eight MSBs of the t_{RX} time. Each LSB corresponds to 5 ns resolution.
[3:0]	OUT_X falling edge timing (t_{FX}), LSBs	R/W	These bits contain the four LSBs of the 12-bit t_{FX} time. This value is always used with the eight bits of Register 0xFE41/0xFE45/0xFE49/0xFE4D/0xFE51/0xFE55/0xFE59/0xFE5D, which contains the eight MSBs of the t_{FX} time. Each LSB corresponds to 5 ns resolution.

Table 89. Register 0xFE43/0xFE47/0xFE4B/0xFE4F/0xFE53/0xFE57/0xFE5B/0xFE5F—OUT1 to OUT8 Settings

Bits	Bit Name	R/W	Description
7	OUT_X 180° delay	R/W	Setting this bit adds a 180° delay to the timing of the OUT_X edges.
[6:5]	Channel assignment	R/W	These bits assign the PWM output to a channel (OUT_X = OUT1, OUT2, OUT3, OUT4, OUT5, OUT6, OUT7, or OUT8).
			Bit 6 / **Bit 5** / **PWM Output Assignment**
			0 / 0 / OUT_X assigned to Channel A.
			0 / 1 / OUT_X assigned to Channel B.
			1 / 0 / OUT_X assigned to Channel C with soft start enabled.
			1 / 1 / OUT_X assigned to Channel C with soft start disabled.
4	Current/volt-second balance enable	R/W	If current balance control or volt-second balance control is enabled, this bit enables the feature on the specific PWM output (OUT_X = OUT1, OUT2, OUT3, OUT4, OUT5, OUT6, OUT7, or OUT8). 0 = OUT_X modulated by volt-second balance control. 1 = OUT_X modulated by dual-phase current balance control.
3	t_{RX} modulation enable	R/W	0 = no PWM modulation of the t_{RX} edge. 1 = PWM modulation acts on the t_{RX} edge.
2	t_{RX} modulation sign	R/W	0 = positive sign. Increase of PWM modulation moves t_{RX} right. 1 = negative sign. Increase of PWM modulation moves t_{RX} left.
1	t_{FX} modulation enable	R/W	0 = no PWM modulation of the t_{FX} edge. 1 = PWM modulation acts on the t_{FX} edge.
0	t_{FX} modulation sign	R/W	0 = positive sign. Increase of PWM modulation moves t_{FX} right. 1 = negative sign. Increase of PWM modulation moves t_{FX} left.

Table 90. Register 0xFE60—PWM Output Pin Disable

Bits	Bit Name	R/W	Description
7	OUT8 disable	R/W	Setting this bit disables the OUT8 output.
6	OUT7 disable	R/W	Setting this bit disables the OUT7 output.
5	OUT6 disable	R/W	Setting this bit disables the OUT6 output.
4	OUT5 disable	R/W	Setting this bit disables the OUT5 output.
3	OUT4 disable	R/W	Setting this bit disables the OUT4 output.
2	OUT3 disable	R/W	Setting this bit disables the OUT3 output.
1	OUT2 disable	R/W	Setting this bit disables the OUT2 output.
0	OUT1 disable	R/W	Setting this bit disables the OUT1 output.

GO COMMAND REGISTER

Table 91. Register 0xFE61—GO Commands

Bits	Bit Name	R/W	Description
[7:4]	Reserved	R/W	Reserved.
3	Frequency GO	R/W	This bit synchronously latches the contents of Register 0xFE0A to Register 0xFE0C into the shadow registers used to calculate the switching frequency.
2	PWM setting GO	R/W	This bit synchronously latches the contents of Register 0xFE40 to Register 0xFE5F into the shadow registers used to calculate the PWM edge timing.
1	VS_B reference GO	R/W	This bit synchronously latches the contents of Register 0xFE23 and Register 0xFE25 into the shadow registers used to calculate the VS_B voltage reference.
0	VS_A reference GO	R/W	This bit synchronously latches the contents of Register 0xFE22 and Register 0xFE24 into the shadow registers used to calculate the VS_A voltage reference.

BALANCE CONTROL REGISTERS

Balance control is based on the modulation from volt-second balance control or dual-phase current balance control. For volt-second balance control, when the CS signal in the half cycle after the rising edge of OUT1 is higher than the CS signal in the half cycle after the rising edge of OUT2, the modulation value increases. For dual-phase current balance control, when the CS1_A or CS2_A value is larger than the CS1_B or CS2_B value, the modulation value increases.

Table 92. Register 0xFE62—Balance Control on OUT1 and OUT2

Bits	Bit Name	R/W	Description
7	t_{R2} balance setting	R/W	Setting this bit enables modulation from balance control on the rising edge of OUT2, t_{R2}.
6	t_{R2} balance direction	R/W	0 = positive sign. Increase of balance control modulation moves t_{R2} right. 1 = negative sign. Increase of balance control modulation moves t_{R2} left.
5	t_{F2} balance setting	R/W	Setting this bit enables modulation from balance control on the falling edge of OUT2, t_{F2}.
4	t_{F2} balance direction	R/W	0 = positive sign. Increase of balance control modulation moves t_{F2} right. 1 = negative sign. Increase of balance control modulation moves t_{F2} left.
3	t_{R1} balance setting	R/W	Setting this bit enables modulation from balance control on the rising edge of OUT1, t_{R1}.
2	t_{R1} balance direction	R/W	0 = positive sign. Increase of balance control modulation moves t_{R1} right. 1 = negative sign. Increase of balance control modulation moves t_{R1} left.
1	t_{F1} balance setting	R/W	Setting this bit enables modulation from balance control on the falling edge of OUT1, t_{F1}.
0	t_{F1} balance direction	R/W	0 = positive sign. Increase of balance control modulation moves t_{F1} right. 1 = negative sign. Increase of balance control modulation moves t_{F1} left.

Table 93. Register 0xFE63—Balance Control on OUT3 and OUT4

Bits	Bit Name	R/W	Description
7	t_{R4} balance setting	R/W	Setting this bit enables modulation from balance control on the rising edge of OUT4, t_{R4}.
6	t_{R4} balance direction	R/W	0 = positive sign. Increase of balance control modulation moves t_{R4} right. 1 = negative sign. Increase of balance control modulation moves t_{R4} left.
5	t_{F4} balance setting	R/W	Setting this bit enables modulation from balance control on the falling edge of OUT4, t_{F4}.
4	t_{F4} balance direction	R/W	0 = positive sign. Increase of balance control modulation moves t_{F4} right. 1 = negative sign. Increase of balance control modulation moves t_{F4} left.
3	t_{R3} balance setting	R/W	Setting this bit enables modulation from balance control on the rising edge of OUT3, t_{R3}.
2	t_{R3} balance direction	R/W	0 = positive sign. Increase of balance control modulation moves t_{R3} right. 1 = negative sign. Increase of balance control modulation moves t_{R3} left.
1	t_{F3} balance setting	R/W	Setting this bit enables modulation from balance control on the falling edge of OUT3, t_{F3}.
0	t_{F3} balance direction	R/W	0 = positive sign. Increase of balance control modulation moves t_{F3} right. 1 = negative sign. Increase of balance control modulation moves t_{F3} left.

Table 94. Register 0xFE64—Balance Control on OUT5, OUT6, OUT7, and OUT8

Bits	Bit Name	R/W	Description
7	t_{R8} balance setting	R/W	Setting this bit enables modulation from balance control on the rising edge of OUT8, t_{R8}. An increase of balance control modulation moves t_{R8} left.
6	t_{F8} balance setting	R/W	Setting this bit enables modulation from balance control on the falling edge of OUT8, t_{F8}. An increase of balance control modulation moves t_{F8} left.
5	t_{R7} balance setting	R/W	Setting this bit enables modulation from balance control on the rising edge of OUT7, t_{R7}. An increase of balance control modulation moves t_{R7} right.
4	t_{F7} balance setting	R/W	Setting this bit enables modulation from balance control on the falling edge of OUT7, t_{F7}. An increase of balance control modulation moves t_{F7} right.
3	t_{R6} balance setting	R/W	Setting this bit enables modulation from balance control on the rising edge of OUT6, t_{R6}. An increase of balance control modulation moves t_{R6} left.
2	t_{F6} balance setting	R/W	Setting this bit enables modulation from balance control on the falling edge of OUT6, t_{F6}. An increase of balance control modulation moves t_{F6} left.
1	t_{R5} balance setting	R/W	Setting this bit enables modulation from balance control on the rising edge of OUT5, t_{R5}. An increase of balance control modulation moves t_{R5} right.
0	t_{F5} balance setting	R/W	Setting this bit enables modulation from balance control on the falling edge of OUT5, t_{F5}. An increase of balance control modulation moves t_{F5} right.

SYNCHRONIZATION SETTING REGISTERS

If the synchronization cycle for Channel A, Channel B, or Channel C is t_S, and t_S is programmed to be synchronized to the switching cycle, t_{SYNC}, the on times of the PWM outputs in this channel remain the same. For example, if OUT_X and OUT_Y are assigned to Channel C and OUT_Y is programmed for a 180°C phase shift, the difference between the falling edge of OUT_X and the rising edge of OUT_Y changes to $t_{SYNC}/2 - t_{FX}$, as shown on the left side of Figure 44. If the timing of the outputs is critical—for example, when OUT_X and OUT_Y drive two switches in a totem-pole structure—the operation of the power stage may be significantly affected.

Register 0xFE66 enables PWM output edge adjustment for OUT1 to OUT8. When the appropriate bit is set in Register 0xFE66, an adjustment of $(t_S - t_{SYNC})/2$ is made on both edges of the corresponding PWM output. It is important to enable output adjustment for the complementary OUT_X/ OUT_Y pairs. With output edge adjustment set on both OUT_X and OUT_Y (as shown on the right side of Figure 44), the dead time between the falling edge of OUT_X and the rising edge of OUT_Y is kept the same at $t_S/2 - t_{FX}$.

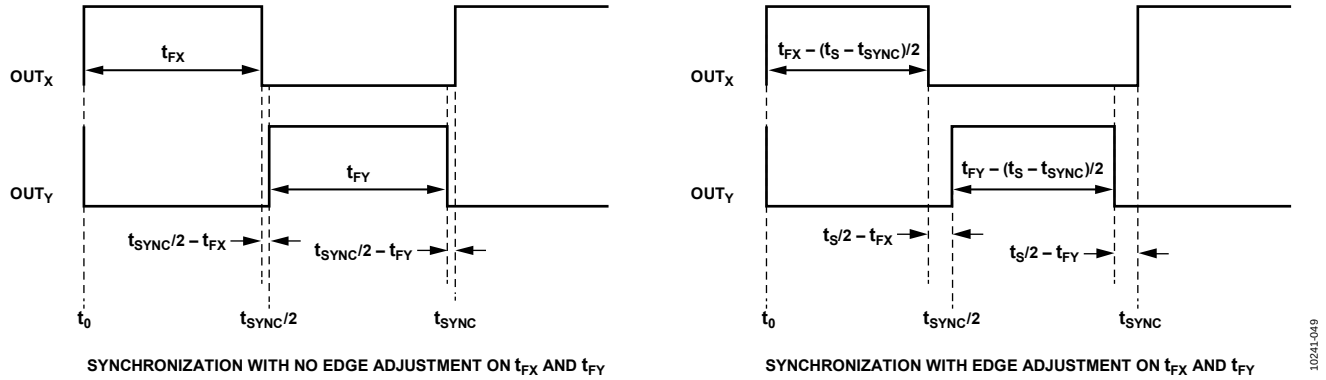


Figure 44. PWM Output Edge Adjustment in Channel C Synchronization

Table 95. Register 0xFE65—OUT1 and OUT2 Shutdown in Channel C Synchronization

Bits	Bit Name	R/W	Description
7	OUT2 shutdown	R/W	Setting this bit shuts down OUT2 at the start of the OUT1 switching cycle. If OUT2 is not assigned to Channel C, this bit must be set to 0.
6	OUT1 shutdown	R/W	Setting this bit shuts down OUT1 at the start of the OUT2 switching cycle. If OUT1 is not assigned to Channel C, this bit must be set to 0.
[5:0]	Reserved	R/W	Reserved.

Table 96. Register 0xFE66—OUT1 Through OUT8 Dead Time Adjustment in Synchronization

Bits	Bit Name	R/W	Description
7	OUT8 adjustment	R/W	Setting this bit adjusts both edges of OUT8 by $(t_S - t_{SYNC})/2$.
6	OUT7 adjustment	R/W	Setting this bit adjusts both edges of OUT7 by $(t_S - t_{SYNC})/2$.
5	OUT6 adjustment	R/W	Setting this bit adjusts both edges of OUT6 by $(t_S - t_{SYNC})/2$.
4	OUT5 adjustment	R/W	Setting this bit adjusts both edges of OUT5 by $(t_S - t_{SYNC})/2$.
3	OUT4 adjustment	R/W	Setting this bit adjusts both edges of OUT4 by $(t_S - t_{SYNC})/2$.
2	OUT3 adjustment	R/W	Setting this bit adjusts both edges of OUT3 by $(t_S - t_{SYNC})/2$.
1	OUT2 adjustment	R/W	Setting this bit adjusts both edges of OUT2 by $(t_S - t_{SYNC})/2$.
0	OUT1 adjustment	R/W	Setting this bit adjusts both edges of OUT1 by $(t_S - t_{SYNC})/2$.

SR AND CHANNEL C SOFT START SETTING REGISTERS

Table 97. Register 0xFE67—Synchronous Rectifier (SR) Soft Start

Bits	Bit Name	R/W	Description
[7:6]	Reserved	R/W	Reserved.
[5:4]	SR soft start timing	R/W	When an SR PWM output is configured to turn on in a soft start manner (using Bits[3:0]), the rising edge of the output moves left in steps of 40 ns. These bits specify how many switching cycles are required to move the SR PWM output left in 40 ns. **Bit 5 / Bit 4 / SR Soft Start Timing** 0 / 0 / SR PWM output changes 40 ns in 1 switching cycle 0 / 1 / SR PWM output changes 40 ns in 4 switching cycles 1 / 0 / SR PWM output changes 40 ns in 16 switching cycles 1 / 1 / SR PWM output changes 40 ns in 64 switching cycles
3	OUT8 SR soft start	R/W	Setting this bit enables SR soft start for OUT8.
2	OUT7 SR soft start	R/W	Setting this bit enables SR soft start for OUT7.
1	OUT4 SR soft start	R/W	Setting this bit enables SR soft start for OUT4.
0	OUT3 SR soft start	R/W	Setting this bit enables SR soft start for OUT3.

Table 98. Register 0xFE68—Channel C Soft Start

Bits	Bit Name	R/W	Description
7	OUT1, OUT2, OUT5, and OUT6 edges	R/W	When this bit is set, the falling edges of OUT1, OUT2, OUT5, and OUT6 always occur after the rising edges in one cycle during a soft start.
6	OUT3, OUT4, OUT7, and OUT8 edges	R/W	This bit is valid only when Bit 7 is set to 1. 0 = rising edges of OUT3, OUT4, OUT7, and OUT8 always occur after the falling edges in one cycle during a soft start. 1 = falling edges of OUT3, OUT4, OUT7, and OUT8 always occur after the rising edges in one cycle during a soft start.
[5:4]	Channel C soft start timing	R/W	These bits determine the duty cycle ramp rate during soft start for the PWM outputs assigned to Channel C. The duty cycle ramp rate is set to 40 ns per 1, 2, 4, or 8 switching cycles. **Bit 5 / Bit 4 / Channel C Soft Start Ramp Rate** 0 / 0 / PWM outputs change 40 ns in 1 switching cycle 0 / 1 / PWM outputs change 40 ns in 2 switching cycles 1 / 0 / PWM outputs change 40 ns in 4 switching cycles 1 / 1 / PWM outputs change 40 ns in 8 switching cycles
3	Global variation	R/W	Setting this bit enables global variation during Channel C soft start. 0 = OUT1, OUT3, OUT5, and OUT7 variation is independent of the OUT2, OUT4, OUT6, and OUT8 variation during soft start. 1 = all outputs use the time variation calculated by the OUT2 timing.
2	OUT2 soft start variation	R/W	This bit selects the variation of the OUT2 on time during Channel C soft start. 0 = variation of OUT2 during soft start is $t_{F2} - t_{R2}$. 1 = variation of OUT2 during soft start is $t_S - t_{R2}$, where t_S is the switching cycle.
1	OUT1, OUT3, OUT5, and OUT7 variation selection	R/W	This bit selects which PWM output determines the variation of OUT1, OUT3, OUT5, and OUT7 during Channel C soft start. If Bit 3 = 1, the setting of this bit is ignored. 0 = rising and falling edges of OUT1 determine OUT1, OUT3, OUT5, and OUT7 variation. 1 = rising and falling edges of OUT3 determine OUT1, OUT3, OUT5, and OUT7 variation.
0	OUT2, OUT4, OUT6, and OUT8 variation selection	R/W	This bit selects which PWM output determines the variation of OUT2, OUT4, OUT6, and OUT8 during Channel C soft start. If Bit 3 = 1, the setting of this bit is ignored. 0 = rising and falling edges of OUT2 determine OUT2, OUT4, OUT6, and OUT8 variation. 1 = rising and falling edges of OUT4 determine OUT2, OUT4, OUT6, and OUT8 variation.

LIGHT LOAD PWM DISABLE REGISTERS

Table 99. Register 0xFE69—Channel A Light Load Mode PWM Output Disable

Bits	Bit Name	R/W	Description
7	OUT8 disable	R/W	Setting this bit disables the OUT8 output when Channel A is in light load mode.
6	OUT7 disable	R/W	Setting this bit disables the OUT7 output when Channel A is in light load mode.
5	OUT6 disable	R/W	Setting this bit disables the OUT6 output when Channel A is in light load mode.
4	OUT5 disable	R/W	Setting this bit disables the OUT5 output when Channel A is in light load mode.
3	OUT4 disable	R/W	Setting this bit disables the OUT4 output when Channel A is in light load mode.
2	OUT3 disable	R/W	Setting this bit disables the OUT3 output when Channel A is in light load mode.
1	OUT2 disable	R/W	Setting this bit disables the OUT2 output when Channel A is in light load mode.
0	OUT1 disable	R/W	Setting this bit disables the OUT1 output when Channel A is in light load mode.

Table 100. Register 0xFE6A—Channel B Light Load Mode PWM Output Disable

Bits	Bit Name	R/W	Description
7	OUT8 disable	R/W	Setting this bit disables the OUT8 output when Channel B is in light load mode.
6	OUT7 disable	R/W	Setting this bit disables the OUT7 output when Channel B is in light load mode.
5	OUT6 disable	R/W	Setting this bit disables the OUT6 output when Channel B is in light load mode.
4	OUT5 disable	R/W	Setting this bit disables the OUT5 output when Channel B is in light load mode.
3	OUT4 disable	R/W	Setting this bit disables the OUT4 output when Channel B is in light load mode.
2	OUT3 disable	R/W	Setting this bit disables the OUT3 output when Channel B is in light load mode.
1	OUT2 disable	R/W	Setting this bit disables the OUT2 output when Channel B is in light load mode.
0	OUT1 disable	R/W	Setting this bit disables the OUT1 output when Channel B is in light load mode.

FAST OCP AND CHANNEL C CURRENT SENSE SETTING REGISTERS

Table 101. Register 0xFE6B—CS1_A Blanking Reference Edge

Bits	Bit Name	R/W	Description
[7:4]	Reserved	R/W	Reserved.
3	OUT6 rising edge blanking	R/W	This bit specifies whether the blanking time for the CS1_A OCP comparator is referenced to the rising edge of OUT6. 0 = no blanking at OUT6 rising edge. 1 = blanking time referenced to OUT6 rising edge.
2	OUT5 rising edge blanking	R/W	This bit specifies whether the blanking time for the CS1_A OCP comparator is referenced to the rising edge of OUT5. 0 = no blanking at OUT5 rising edge. 1 = blanking time referenced to OUT5 rising edge.
1	OUT2 rising edge blanking	R/W	This bit specifies whether the blanking time for the CS1_A OCP comparator is referenced to the rising edge of OUT2. 0 = no blanking at OUT2 rising edge. 1 = blanking time referenced to OUT2 rising edge.
0	OUT1 rising edge blanking	R/W	This bit specifies whether the blanking time for the CS1_A OCP comparator is referenced to the rising edge of OUT1. 0 = no blanking at OUT1 rising edge. 1 = blanking time referenced to OUT1 rising edge.

Table 102. Register 0xFE6C—CS1_B Blanking Reference Edge

Bits	Bit Name	R/W	Description
[7:4]	Reserved	R/W	Reserved.
3	OUT6 rising edge blanking	R/W	This bit specifies whether the blanking time for the CS1_B OCP comparator is referenced to the rising edge of OUT6. 0 = no blanking at OUT6 rising edge. 1 = blanking time referenced to OUT6 rising edge.
2	OUT5 rising edge blanking	R/W	This bit specifies whether the blanking time for the CS1_B OCP comparator is referenced to the rising edge of OUT5. 0 = no blanking at OUT5 rising edge. 1 = blanking time referenced to OUT5 rising edge.
1	OUT2 rising edge blanking	R/W	This bit specifies whether the blanking time for the CS1_B OCP comparator is referenced to the rising edge of OUT2. 0 = no blanking at OUT2 rising edge. 1 = blanking time referenced to OUT2 rising edge.
0	OUT1 rising edge blanking	R/W	This bit specifies whether the blanking time for the CS1_B OCP comparator is referenced to the rising edge of OUT1. 0 = no blanking at OUT1 rising edge. 1 = blanking time referenced to OUT1 rising edge.

Table 103. Register 0xFE6D—OUT3, OUT4, OUT7, and OUT8 Cycle-by-Cycle OCP Response

Bits	Bit Name	R/W	Description
[7:4]	Reserved	R/W	Reserved.
3	OUT8 cycle-by-cycle OCP response	R/W	When this bit is set, an OCP signal on the channel to which OUT8 is assigned causes OUT8 to turn on. The falling edge of the SR output still follows the programmed value.
2	OUT7 cycle-by-cycle OCP response	R/W	When this bit is set, an OCP signal on the channel to which OUT7 is assigned causes OUT7 to turn on. The falling edge of the SR output still follows the programmed value.
1	OUT4 cycle-by-cycle OCP response	R/W	When this bit is set, an OCP signal on the channel to which OUT4 is assigned causes OUT4 to turn on. The falling edge of the SR output still follows the programmed value.
0	OUT3 cycle-by-cycle OCP response	R/W	When this bit is set, an OCP signal on the channel to which OUT3 is assigned causes OUT3 to turn on. The falling edge of the SR output still follows the programmed value.

Table 104. Register 0xFE6E—CS Gain Trim

Bits	Bit Name	R/W	Description
7	Gain polarity	R/W	1 = negative gain is introduced. 0 = positive gain is introduced.
[6:0]	CS gain trim	R/W	This value calibrates the primary side current sense gain. For more information, see the CS, CS1_A, and CS1_B Gain Trim section.

Table 105. Register 0xFE6F—CS OCP Settings

Bits	Bit Name	R/W	Description			
7	CS OCP ignored	R/W	Setting this bit causes the CS OCP comparator output to be ignored. The flag is always cleared.			
[6:4]	Leading edge blanking	R/W	These bits specify the blanking time. During this time, the CS OCP comparator output is ignored. The CS OCP blanking time is measured from OUT1 and OUT2.			
			Bit 6	**Bit 5**	**Bit 4**	**Leading Edge Blanking Time**
			0	0	0	0 ns
			0	0	1	40 ns
			0	1	0	80 ns
			0	1	1	120 ns
			1	0	0	200 ns
			1	0	1	400 ns
			1	1	0	600 ns
			1	1	1	800 ns

Bits	Bit Name	R/W	Description		
[3:2]	CS_OCP flag timeout	R/W	These bits specify the number of consecutive switching cycles with OCP triggered that must occur before the CS_OCP flag is set.		
			Bit 3	**Bit 2**	**Fast OCP Flag Timeout**
			0	0	1 switching cycle
			0	1	8 switching cycles
			1	0	64 switching cycles
			1	1	512 switching cycles
[1:0]	CS_OCP flag debounce time	R/W	These bits set the CS_OCP flag debounce time. The debounce time is the minimum time that the CS signal must be continuously above the CS OCP threshold before the flag triggers an action. This action is programmed in Register 0xFE04, Bits[3:0].		
			Bit 1	**Bit 0**	**Flag Debounce Time**
			0	0	0 ns
			0	1	40 ns
			1	0	80 ns
			1	1	120 ns

Table 106. Register 0xFE70 and Register 0xFE71—CS1_A OCP and CS1_B OCP Settings

Bits	Bit Name	R/W	Description			
7	CS1_A/CS1_B OCP ignored	R/W	Setting this bit causes the CS1_A/CS1_B OCP comparator output to be ignored. The flag is always cleared.			
[6:4]	Leading edge blanking	R/W	These bits specify the blanking time. During this time, the CS1_A OCP/CS1_B OCP comparator output is ignored. The blanking time is measured from the rising edge of OUT1, OUT2, OUT5, or OUT6 (programmed in Register 0xFE6B and Register 0xFE6C).			
			Bit 6	**Bit 5**	**Bit 4**	**Leading Edge Blanking Time**
			0	0	0	0 ns
			0	0	1	40 ns
			0	1	0	80 ns
			0	1	1	120 ns
			1	0	0	200 ns
			1	0	1	400 ns
			1	1	0	600 ns
			1	1	1	800 ns
[3:2]	CS1_A_OCP/CS1_B_OCP flag timeout	R/W	These bits specify the number of consecutive switching cycles with OCP triggered that must occur before the CS1_A_OCP/CS1_B_OCP flag is set.			
			Bit 3	**Bit 2**	**Fast OCP Flag Timeout**	
			0	0	1 switching cycle	
			0	1	8 switching cycles	
			1	0	64 switching cycles	
			1	1	512 switching cycles	
[1:0]	CS1_A_OCP/CS1_B_OCP flag debounce time	R/W	These bits set the CS1_A_OCP/CS1_B_OCP flag debounce time. The debounce time is the minimum time that the CS1_A/CS1_B signal must be continuously above the threshold before the flag triggers an action. This action is programmed in Register 0xFE00.			
			Bit 1	**Bit 0**	**Flag Debounce Time**	
			0	0	0 ns	
			0	1	40 ns	
			1	0	80 ns	
			1	1	120 ns	

Table 107. Register 0xFE72—Balance Control Settings

Bits	Bit Name	R/W	Description
7	Channel selection for volt-second balance control	R/W	Setting this bit selects Channel A or Channel C for volt-second balance control. 0 = use Channel C for volt-second balance control. 1 = use Channel A for volt-second balance control.
6	Volt-second balance control limit	R/W	This bit sets the modulation limit on the duty cycles from the volt-second control circuit. 0 = maximum volt-second control modulation is ±160 ns. 1 = maximum volt-second control modulation is ±80 ns.
[5:4]	Volt-second balance loop gain	R/W	These bits set the volt-second balance control loop gain.
			Bit 5 / **Bit 4** / **Volt-Second Balance Control Loop Gain** 0 / 0 / 1 0 / 1 / 4 1 / 0 / 16 1 / 1 / 64
3	Sensing selection for current balance	R/W	Setting this bit selects CS1_A/CS1_B or CS2_A/CS2_B for current balance control. 0 = use CS2_A/CS2_B for current balance control. 1 = use CS1_A/CS1_B for current balance control.
2	Current balance control limit	R/W	This bit sets the modulation limit on the duty cycles from the current control circuit. 0 = maximum current control modulation is ±160 ns. 1 = maximum current control modulation is ±80 ns.
[1:0]	Current balance loop gain	R/W	These bits set the current balance control loop gain.
			Bit 1 / **Bit 0** / **Current Balance Control Loop Gain** 0 / 0 / 1 0 / 1 / 4 1 / 0 / 16 1 / 1 / 64

TEMPERATURE SENSE AND PROTECTION SETTING REGISTERS

Table 108. Register 0xFE73—RTD1 Gain Trim

Bits	Bit Name	R/W	Description
7	Gain polarity	R/W	1 = negative gain is introduced. 0 = positive gain is introduced.
[6:0]	RTD1 gain trim	R/W	This value calibrates the RTD1 sensing gain (see the RTD1, RTD2, OTP1, and OTP2 Trim section).

Table 109. Register 0xFE74—RTD2 Gain Trim

Bits	Bit Name	R/W	Description
7	Gain polarity	R/W	1 = negative gain is introduced. 0 = positive gain is introduced.
[6:0]	RTD2 gain trim	R/W	This value calibrates the RTD2 sensing gain (see the RTD1, RTD2, OTP1, and OTP2 Trim section).

Register 0xFE75 sets the OTP1 threshold value. The debounce time of the OTP1 flag is 100 ms.

Table 110. Register 0xFE75—OTP1 Threshold

Bits	Bit Name	R/W	Description							
[7:0]	OTP1 threshold	R/W	OTP1 threshold. This register, adding 0 as the MSB, results in a 9-bit threshold value. This 9-bit value is compared to the nine MSBs of the RTD1 value register (Register 0xFED7). If the OTP1 threshold is higher than the RTD1 ADC reading, the OTP1 flag is set. The eight bits of this register allow 256 threshold settings from 0 mV to 800 mV. One LSB corresponds to 800 mV/256 = 3.125 mV. However, threshold settings at the low end and the high end are not allowed. The valid range for this register value is 2 to 244 (decimal).							
			Bit 7	**Bit 6**	**…**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**OTP1 Limit (mV)**
			0	0	…	0	0	1	0	6.25
			…	…	…	…	…	…	…	…
			0	0	…	0	1	0	0	12.5
			0	0	…	0	1	0	1	15.625
			…	…	…	…	…	…	…	…
			1	1	…	0	0	1	1	459.375
			1	1	…	0	1	0	0	762.5

Register 0xFE76 sets the OTP2 threshold value. The debounce time of the OTP2 flag is 100 ms.

Table 111. Register 0xFE76—OTP2 Threshold

Bits	Bit Name	R/W	Description							
[7:0]	OTP2 threshold	R/W	OTP2 threshold. This register, adding 0 as the MSB, results in a 9-bit threshold value. This 9-bit value is compared to the nine MSBs of the RTD2 value register (Register 0xFED8). If the OTP2 threshold is higher than the RTD2 ADC reading, the OTP2 flag is set. The eight bits of this register allow 256 threshold settings from 0 mV to 800 mV. One LSB corresponds to 800 mV/256 = 3.125 mV. However, threshold settings at the low end and the high end are not allowed. The valid range for this register value is 2 to 244 (decimal).							
			Bit 7	**Bit 6**	**…**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**OTP2 Limit (mV)**
			0	0	…	0	0	1	0	6.25
			…	…	…	…	…	…	…	…
			0	0	…	0	1	0	0	12.5
			0	0	…	0	1	0	1	15.625
			…	…	…	…	…	…	…	…
			1	1	…	0	0	1	1	459.375
			1	1	…	0	1	0	0	762.5

ACSNS AND FEEDFORWARD SETTING REGISTERS

Table 112. Register 0xFE77—ACSNS Gain Trim

Bits	Bit Name	R/W	Description
7	Trim polarity	R/W	1 = negative gain is introduced. 0 = positive gain is introduced.
[6:0]	ACSNS trim	R/W	This value sets the amount of gain trim that is applied to the ACSNS ADC reading. This register trims the voltage at the ACSNS pin for external resistor tolerances. For more information, see the ACSNS Gain Trim section.

Table 113. Register 0xFE78—ACSNS Setting

Bits	Bit Name	R/W	Description		
7	ACSNS flag included in PGOOD	R/W	Setting this bit includes the ACSNS flag in the PGOOD_A and PGOOD_B flags. The debounce time for this function is set with Bit 6.		
6	Debounce of ACSNS flag included in PGOOD	R/W	This bit sets the debounce time of the ACSNS flag when it is included in the PGOOD_A and PGOOD_B flags. 0 = 0 ms. 1 = 2.6 ms.		
[5:2]	ACSNS threshold	R/W	These bits set the ACSNS threshold. This 4-bit value is compared with the four MSBs of the ACSNS value register (Register 0xFED9). The hysteresis is 75 mV. When these bits are set to 0, the ACSNS flag is always cleared. For more information, see the ACSNS Flag section.		
[1:0]	ACSNS flag debounce time	R/W	These bits set the ACSNS flag debounce time.		
			Bit 1	**Bit 0**	**Typical Debounce Time**
			0	0	0 ms
			0	1	2.6 ms
			1	0	10.4 ms
			1	1	100 ms

PSON REGISTERS

Table 114. Register 0xFE79—Channel A PSON Setting

Bits	Bit Name	R/W	Description		
7	PSON_A polarity	R/W	Setting this bit inverts the polarity of the PSON_A pin signal when hardware PSON_A is used. 0 = normal mode. A high signal on the PSON_A pin turns on Channel A. 1 = inverted. A low signal on the PSON_A pin turns on Channel A.		
6	Software PSON_A	R/W	When software PSON_A is used, setting this bit turns on Channel A.		
[5:4]	PSON_A control hardware/software selection	R/W	These bits specify which signal or signals are used as the PSON_A control.		
			Bit 5	**Bit 4**	**PSON_A Control Selection**
			0	0	Always on. Channel A is always on.
			0	1	Hardware PSON_A. The PSON_A pin turns Channel A on and off.
			1	0	Software PSON_A. Bit 6 turns Channel A on and off.
			1	1	Software and hardware PSON_A. Both the PSON_A pin and Bit 6 must be set to turn on Channel A.
[3:2]	PSON_A delay	R/W	These bits specify the delay from when the PSON_A signal is set to when the soft start of Channel A begins.		
			Bit 3	**Bit 2**	**Typical Delay Time**
			0	0	0 ms
			0	1	50 ms
			1	0	250 ms
			1	1	1 sec
[1:0]	PSOFF_A delay	R/W	These bits specify the delay from when the PSON_A signal is cleared to when Channel A is turned off.		
			Bit 1	**Bit 0**	**Typical Delay Time**
			0	0	0 ms
			0	1	50 ms
			1	0	250 ms
			1	1	1 sec

Table 115. Register 0xFE7A—Channel B PSON Setting

Bits	Bit Name	R/W	Description		
7	PSON_B polarity	R/W	Setting this bit inverts the polarity of the PSON_B pin signal when hardware PSON_B is used. 0 = normal mode. A high signal on the PSON_B pin turns on Channel B. 1 = inverted. A low signal on the PSON_B pin turns on Channel B.		
6	Software PSON_B	R/W	When software PSON_B is used, setting this bit turns on Channel B.		
[5:4]	PSON_B control hardware/software selection	R/W	These bits specify which signal or signals are used as the PSON_B control.		
			Bit 5	**Bit 4**	**PSON_B Control Selection**
			0	0	Always on. Channel B is always on.
			0	1	Hardware PSON_B. The PSON_B pin turns Channel B on and off.
			1	0	Software PSON_B. Bit 6 turns Channel B on and off.
			1	1	Software and hardware PSON_B. Both the PSON_B pin and Bit 6 must be set to turn on Channel B.
[3:2]	PSON_B delay	R/W	These bits specify the delay from when the PSON_B signal is set to when the soft start of Channel B begins.		
			Bit 3	**Bit 2**	**Typical Delay Time**
			0	0	0 ms
			0	1	50 ms
			1	0	250 ms
			1	1	1 sec
[1:0]	PSOFF_B delay	R/W	These bits specify the delay from when the PSON_B signal is cleared to when Channel B is turned off.		
			Bit 1	**Bit 0**	**Typical Delay Time**
			0	0	0 ms
			0	1	50 ms
			1	0	250 ms
			1	1	1 sec

Table 116. Register 0xFE7B—Additional Flag Reenable Delay and Channel C PSON Setting

Bits	Bit Name	R/W	Description		
7	Channel C additional flag reenable delay	R/W	This bit specifies whether an additional PSON_C delay is added to the reenable delay after a flag is cleared and before Channel C begins a soft start. 0 = no additional delay is added to the reenable delay. 1 = additional PSON_C delay is added to the reenable delay.		
6	Channel B additional flag reenable delay	R/W	This bit specifies whether an additional PSON_B delay is added to the reenable delay after a flag is cleared and before Channel B begins a soft start. 0 = no additional delay is added to the reenable delay. 1 = additional PSON_B delay is added to the reenable delay.		
5	Channel A additional flag reenable delay	R/W	This bit specifies whether an additional PSON_A delay is added to the reenable delay after a flag is cleared and before Channel A begins a soft start. 0 = no additional delay is added to the reenable delay. 1 = additional PSON_A delay is added to the reenable delay.		
4	PSON_C control selection	R/W	0 = Channel C is always on. 1 = Either PSON_A or PSON_B must be set to turn on Channel C.		
[3:2]	PSON_C delay	R/W	These bits specify the delay from when the PSON_C signal is set to when the soft start of Channel C begins.		
			Bit 3	**Bit 2**	**Typical Delay Time**
			0	0	0 ms
			0	1	50 ms
			1	0	250 ms
			1	1	1 sec
[1:0]	PSOFF_C delay	R/W	These bits specify the delay from when the PSON_C signal is cleared to when Channel C is turned off.		
			Bit 1	**Bit 0**	**Typical Delay Time**
			0	0	0 ms
			0	1	50 ms
			1	0	250 ms
			1	1	1 sec

RTD TRIM REGISTERS

Table 117. Register 0xFE7C—RTD1 Offset Trim (MSB)

Bits	Bit Name	R/W	Description
[7:2]	Reserved	R/W	Reserved.
1	Trim polarity	R/W	1 = negative gain is introduced. 0 = positive gain is introduced.
0	RTD1 offset trim (MSB)	R/W	This bit, together with Register 0xFE7D, sets the amount of offset trim that is applied to the RTD1 ADC reading.

Table 118. Register 0xFE7D—RTD1 Offset Trim (LSBs)

Bits	Bit Name	R/W	Description
[7:0]	RTD1 offset trim (LSBs)	R/W	These eight bits, together with Bit 0 of Register 0xFE7C, sets the amount of offset trim that is applied to the RTD1 ADC reading.

Table 119. Register 0xFE7E—RTD2 Offset Trim (MSB)

Bits	Bit Name	R/W	Description
[7:2]	Reserved	R/W	Reserved.
1	Trim polarity	R/W	1 = negative gain is introduced. 0 = positive gain is introduced.
0	RTD2 offset trim (MSB)	R/W	This bit, together with Register 0xFE7F, sets the amount of offset trim that is applied to the RTD2 ADC reading.

Table 120. Register 0xFE7F—RTD2 Offset Trim (LSBs)

Bits	Bit Name	R/W	Description
[7:0]	RTD2 offset trim (LSBs)	R/W	These eight bits, together with Bit 0 of Register 0xFE7E, sets the amount of offset trim that is applied to the RTD2 ADC reading.

Table 121. Register 0xFE80—RTD1 Current Source Settings

Bits	Bit Name	R/W	Description		
[7:6]	RTD1 current setting	R/W	These bits set the size of the current source on the RTD1 pin. The factory default setting is 10 µA.		
			Bit 7	**Bit 6**	**Current Source (µA)**
			0	0	10
			0	1	20
			1	0	30
			1	1	40
[5:0]	RTD1 current fine adjust	R/W	These bits are used to adjust the current source on the RTD1 pin. Each LSB corresponds to 156.25 nA, independent of the RTD1 current source setting specified by Bits[7:6].		

Table 122. Register 0xFE81—RTD2 Current Source Settings

Bits	Bit Name	R/W	Description		
[7:6]	RTD2 current setting	R/W	These bits set the size of the current source on the RTD2 pin. The factory default setting is 10 µA.		
			Bit 7	**Bit 6**	**Current Source (µA)**
			0	0	10
			0	1	20
			1	0	30
			1	1	40
[5:0]	RTD2 current fine adjust	R/W	These bits are used to adjust the current source on the RTD2 pin. Each LSB corresponds to 156.25 nA, independent of the RTD2 current source setting specified by Bits[7:6].		

CUSTOMIZED REGISTERS

Table 123. Register 0xFE82—Custom Register

Bits	Bit Name	R/W	Description
[7:0]	Custom register	R/W	This register is available to the user to store custom information. For example, this register can be used to store user software or hardware revision information.

Table 124. Register 0xFE83—REVERSE_A/REVERSE_B Flag Configuration

Bits	Bit Name	R/W	Description		
[7:6]	REVERSE_B flag action	R/W	These bits specify the action to take when the REVERSE_B flag is set.		
			Bit 7	**Bit 6**	**Flag Action**
			0	0	None
			0	1	Disable PWM outputs in Channel A
			1	0	Disable PWM outputs in Channel B
			1	1	Disable all PWM outputs (Channel A, Channel B, and Channel C)
[5:4]	Action after REVERSE_B flag is cleared	R/W	These bits specify the action to take after the REVERSE_B flag is cleared.		
			Bit 5	**Bit 4**	**Action After Flag Is Cleared**
			0	0	After the reenable delay time, the PWM outputs are reenabled using the soft start process
			0	1	The PWM outputs are reenabled immediately without a soft start
			1	0	A PSON signal is needed to reenable the PWM outputs
			1	1	A PSON signal is needed to reenable the PWM outputs
[3:2]	REVERSE_A flag action	R/W	These bits specify the action to take when the REVERSE_A flag is set.		
			Bit 3	**Bit 2**	**Flag Action**
			0	0	None
			0	1	Disable PWM outputs in Channel A
			1	0	Disable PWM outputs in Channel B
			1	1	Disable all PWM outputs (Channel A, Channel B, and Channel C)
[1:0]	Action after REVERSE_A flag is cleared	R/W	These bits specify the action to take after the REVERSE_A flag is cleared.		
			Bit 1	**Bit 0**	**Action After Flag Is Cleared**
			0	0	After the reenable delay time, the PWM outputs are reenabled using the soft start process
			0	1	The PWM outputs are reenabled immediately without a soft start
			1	0	A PSON signal is needed to reenable the PWM outputs
			1	1	A PSON signal is needed to reenable the PWM outputs

Table 125. Register 0xFE84 and Register 0xFE85—REVERSE_A/REVERSE_B Flag Settings

Bits	Bit Name	R/W	Description					
[7:4]	Reserved	R/W	Reserved.					
3	Debounce time	R/W	This bit sets the debounce time for the REVERSE_A and REVERSE_B flags. 0 = 40 ns. 1 = 200 ns.					
[2:0]	Reverse current protection threshold	R/W	These bits specify the CS2 reverse current protection threshold. When the CS2 negative current falls below this threshold, the REVERSE_A or REVERSE_B flag is triggered.					
			Bit 2	**Bit 1**	**Bit 0**	**Trigger Threshold min (mV)**	**Trigger Threshold Setting (mV)**	**Trigger Threshold max (mV)**
			0	0	X		Reserved	
			0	1	0	−15.8	−10	−3.6
			0	1	1	−19.4	−13	−6.6
			1	0	0	−23.2	−17	−9.6
			1	0	1	−27	−20	−12.4
			1	1	0	−30.8	−24	−15.3
			1	1	1	−34.7	−27	−18.1

Table 126. Register 0xFE86 and Register 0xFE87—VS_A/VS_B Slew Rate for Output Voltage Adjustment

Bits	Bit Name	R/W	Description			
[7:4]	Reserved	R/W	Reserved.			
[3:1]	Slew rate setting	R/W	These bits specify the slew rate.			
			Bit 3	**Bit 2**	**Bit 1**	**Slew Rate**
			0	0	0	1.5625 mV/ms (4 LSB/ms)
			0	0	1	3.125 mV/ms
			0	1	0	6.25 mV/ms
			0	1	1	12.5 mV/ms
			1	0	0	25 mV/ms
			1	0	1	50 mV/ms
			1	1	0	100 mV/ms
			1	1	1	200 mV/ms
0	Slew rate adjust enable	R/W	Setting this bit enables output voltage adjustment with the slew rate specified by Bits[3:1].			

Table 127. Register 0xFE88—Power Supply Software Reset Control

Bits	Bit Name	R/W	Description		
[7:4]	Reserved	R/W	Reserved.		
[3:2]	Restart delay	R/W	These bits specify the delay after the power supply is turned off and before the part is restarted.		
			Bit 3	**Bit 2**	**Restart Delay**
			0	0	0 ms
			0	1	500 ms
			1	0	1 sec
			1	1	2 sec
1	Channel B SW reset GO	R/W	Setting this bit resets the Channel B power supply with a preset delay between the turning off of the power supply and the restarting of the part. This restart delay is set using Bits[3:2].		
0	Channel A SW reset GO	R/W	Setting this bit resets the Channel A power supply with a preset delay between the turning off of the power supply and the restarting of the part. This restart delay is set using Bits[3:2].		

Table 128. Register 0xFE89—CS, CS1, and CS2 ADC Update Rate

Bits	Bit Name	R/W	Description		
[7:2]	Reserved	R/W	Reserved.		
[1:0]	CSx value update rate	R/W	These bits specify the update rate for the current value ADCs. By default, the current value ADCs are updated every 10 ms.		
			Bit 1	**Bit 0**	**Update Rate**
			0	0	10.5 ms
			0	1	52.4 ms
			1	0	104.9 ms
			1	1	209.7 ms

Table 129. Register 0xFE8A—OTW1/OTW2 Settings

Bits	Bit Name	R/W	Description		
7	OTW2 flag debounce	R/W	This bit sets the OTW2 flag debounce time. 0 = 100 ms. 1 = 0 ms.		
6	OTW2 triggers PGOOD_B	R/W	This bit specifies whether the OTW2 flag triggers PGOOD_B. 0 = OTW2 does not trigger PGOOD_B. 1 = OTW2 triggers PGOOD_B.		
[5:4]	OTW2 threshold	R/W	These bits set the OTW2 threshold.		
			Bit 5	**Bit 4**	**OTW2 Threshold**
			0	0	3.125 mV (1 LSB) above the OTP2 threshold
			0	1	6.25 mV (2 LSBs) above the OTP2 threshold
			1	0	9.375 mV (3 LSBs) above the OTP2 threshold
			1	1	12.5 mV (4 LSBs) above the OTP2 threshold
3	OTW1 flag debounce	R/W	This bit sets the OTW1 flag debounce time. 0 = 100 ms. 1 = 0 ms.		
2	OTW1 triggers PGOOD_A	R/W	This bit specifies whether the OTW1 flag triggers PGOOD_A. 0 = OTW1 does not trigger PGOOD_A. 1 = OTW1 triggers PGOOD_A.		
[1:0]	OTW1 threshold	R/W	These bits set the OTW1 threshold.		
			Bit 1	**Bit 0**	**OTW1 Threshold**
			0	0	3.125 mV (1 LSB) above the OTP1 threshold
			0	1	6.25 mV (2 LSBs) above the OTP1 threshold
			1	0	9.375 mV (3 LSBs) above the OTP1 threshold
			1	1	12.5 mV (4 LSBs) above the OTP1 threshold

FLAG REGISTERS

Register 0xFEC0 through Register 0xFEC4 are flag registers that indicate the status of the flags. Register 0xFEC5 through Register 0xFEC9 are latched flag registers. In the latched flag registers, flags are not reset when the condition disappears but remain set so that intermittent faults can be detected. Flags in the latched flag registers are cleared only by a register read (provided that the fault no longer exists) or by asserting PSON. It is recommended that the latched flag register be read again after the faults disappear to ensure that the register was reset. Note that latched flag bits are clocked on a low-to-high transition only.

Table 130. Register 0xFEC0—Flag Register 1 and Register 0xFEC5—Latched Flag Register 1 (1 = Fault, 0 = Normal Operation)

Bits	Bit Name	R/W	Description	Register	Action
7	POWER_SUPPLY_A	R	Channel A power supply is off and the PWM outputs are disabled. This bit stays high until PSON_A is asserted.		None
6	PGOOD_A	R	Power-good fault on Channel A. This flag is set when the UVP_A, POWER_SUPPLY_A, EEPROM_CRC, or SOFTSTART_FILTER_A flag is set. The ACSNS and OTW1 flags can also be programmed to be included.	0xFE09, 0xFE78, 0xFE8A	PGOOD_A pin set low
5	CS1_A_OCP	R	The voltage at CS1_A is above the 1.2 V threshold.	0xFE00, 0xFE70	Programmable
4	CS2_A_OCP	R	The voltage at CS2_A is above its threshold.	0xFE01, 0xFE18	Programmable
3	UVP_A	R	VS_A is below its threshold.	0xFE03, 0xFE28	Programmable
2	OVP_A	R	OVP_A is above its threshold.	0xFE02, 0xFE26	Programmable
1	LIGHTLOAD_A	R	Channel A is in light load mode (CS2_A current is below the light load threshold).	0xFE1A, 0xFE69	Programmable
0	VS_SET_ERR_A	R	The intended VS_A reference setting is outside the allowed range.	0xFE1E, 0xFE20	None

Table 131. Register 0xFEC1—Flag Register 2 and Register 0xFEC6—Latched Flag Register 2 (1 = Fault, 0 = Normal Operation)

Bits	Bit Name	R/W	Description	Register	Action
7	POWER_SUPPLY_B	R	Channel B power supply is off and the PWM outputs are disabled. This bit stays high until PSON_B is asserted.		None
6	PGOOD_B	R	Power-good fault on Channel B. This flag is set when the UVP_B, POWER_SUPPLY_B, EEPROM_CRC, or SOFTSTART_FILTER_B flag is set. The ACSNS and OTW2 flags can also be programmed to be included.	0xFE09, 0xFE78, 0xFE8A	PGOOD_B pin set low
5	CS1_B_OCP	R	The voltage at CS1_B is above the 1.2 V threshold.	0xFE00, 0xFE71	Programmable
4	CS2_B_OCP	R	The voltage at CS2_B is above its threshold.	0xFE01, 0xFE19	Programmable
3	UVP_B	R	VS_B is below its threshold.	0xFE03, 0xFE29	Programmable
2	OVP_B	R	OVP_B is above its threshold.	0xFE02, 0xFE27	Programmable
1	LIGHTLOAD_B	R	Channel B is in light load mode (CS2_B current is below the light load threshold).	0xFE1B, 0xFE6A	Programmable
0	VS_SET_ERR_B	R	The intended VS_B reference setting is outside the allowed range.	0xFE1F, 0xFE21	None

Table 132. Register 0xFEC2—Flag Register 3 and Register 0xFEC7—Latched Flag Register 3 (1 = Fault, 0 = Normal Operation)

Bits	Bit Name	R/W	Description	Register	Action
7	Reserved	R	Reserved.		
6	VDD_OV	R	Overvoltage condition (V_{DD} is above limit). The I^2C interface remains functional, but a PSON toggle is required to restart the power supply.	0xFE06	Programmable
5	CS_OCP	R	The voltage at CS is above the 1.2 V threshold.	0xFE04, 0xFE6F	Programmable
4	OTP2	R	Temperature of Zone 2 is above the OTP2 threshold.	0xFE05, 0xFE76	Programmable
3	OTP1	R	Temperature of Zone 1 is above the OTP1 threshold.	0xFE05, 0xFE75	Programmable
2	ACSNS	R	ACSNS is below its threshold.	0xFE04, 0xFE78	Programmable
1	EEPROM_CRC	R	The downloaded EEPROM contents are incorrect.		Immediate shutdown
0	FLAGIN	R	The external flag pin (FLGI/SYNI) is set.	0xFE06, 0xFE0F	Programmable

Table 133. Register 0xFEC3—Flag Register 4 and Register 0xFEC8—Latched Flag Register 4 (1 = Fault, 0 = Normal Operation)

Bits	Bit Name	R/W	Description	Register	Action
7	Reserved	R	Reserved.		
6	POWER_SUPPLY_C	R	Channel C power supply is off and the PWM outputs are disabled. This bit stays high until PSON_C is asserted.		None
5	FLAGOUT	R	The FLGO/SYNO pin is set in response to the LIGHTLOAD_A or LIGHTLOAD_B flag.	0xFE0F	None
4	EEPROM_UNLOCKED	R	The EEPROM is unlocked.		None
3	SOFTSTART_FILTER_B	R	Channel B soft start filter is in use.	0xFE3F	None
2	SOFTSTART_FILTER_A	R	Channel A soft start filter is in use.	0xFE3E	None
1	MODULATION_B	R	Channel B digital filter is at its minimum or maximum limit.	0xFE3D	None
0	MODULATION_A	R	Channel A digital filter is at its minimum or maximum limit.	0xFE3C	None

Table 134. Register 0xFEC4—Flag Register 5 and Register 0xFEC9—Latched Flag Register 5 (1 = Fault, 0 = Normal Operation)

Bits	Bit Name	R/W	Description	Register	Action
[7:4]	Reserved	R	Reserved.		
3	OTW2	R	Temperature of Zone 2 is above the OTW2 threshold.	0xFE8A	Programmable
2	OTW1	R	Temperature of Zone 1 is above the OTW1 threshold.	0xFE8A	Programmable
1	REVERSE_B	R	CS2_B reverse current falls below the CS2_B reverse current threshold.	0xFE85	Programmable
0	REVERSE_A	R	CS2_A reverse current falls below the CS2_A reverse current threshold.	0xFE84	Programmable

Register 0xFECA and Register 0xFECB record the first flag ID for Channel A and Channel B, respectively. The first flag ID represents the first flag that triggers a response and requires a soft start after the fault is resolved. The Channel A first flag ID register (Register 0xFECA) records the first flag ID of the fault that shut down Channel A; the Channel B first flag ID register (Register 0xFECB) records the first flag ID of the fault that shut down Channel B. For more information, see the First Flag ID Recording section.

Table 135. Register 0xFECA and Register 0xFECB—Channel A and Channel B First Flag ID

Bits	Bit Name	R/W	Description				
[7:4]	Previous first flag ID	R	These bits return the flag fault ID of the flag that caused the previous shutdown of Channel A or Channel B. This previous shutdown occurred before the shutdown caused by the fault identified in Bits[3:0].				
			Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**First Flag ID**
			0	0	0	0	No flag
			0	0	0	1	CS1_A_OCP
			0	0	1	0	CS1_B_OCP
			0	0	1	1	CS2_A_OCP
			0	1	0	0	CS2_B_OCP
			0	1	0	1	OVP_A
			0	1	1	0	OVP_B
			0	1	1	1	UVP_A
			1	0	0	0	UVP_B
			1	0	0	1	CS_OCP
			1	0	1	0	ACSNS
			1	0	1	1	OTP1
			1	1	0	0	OTP2
			1	1	0	1	FLAGIN
			1	1	1	0	CS2_A reverse current
			1	1	1	1	CS2_B reverse current
[3:0]	Current first flag ID	R	These bits return the flag fault ID of the fault that caused the shutdown of Channel A or Channel B.				
			Bit 3	**Bit 2**	**Bit 1**	**Bit 0**	**First Flag ID**
			0	0	0	0	No flag
			0	0	0	1	CS1_A_OCP
			0	0	1	0	CS1_B_OCP
			0	0	1	1	CS2_A_OCP
			0	1	0	0	CS2_B_OCP
			0	1	0	1	OVP_A
			0	1	1	0	OVP_B
			0	1	1	1	UVP_A
			1	0	0	0	UVP_B
			1	0	0	1	CS_OCP
			1	0	1	0	ACSNS
			1	0	1	1	OTP1
			1	1	0	0	OTP2
			1	1	0	1	FLAGIN
			1	1	1	0	CS2_A reverse current
			1	1	1	1	CS2_B reverse current

VALUE REGISTERS

Table 136. Register 0xFED0—CS Value

Bits	Bit Name	R/W	Description
[15:4]	CS voltage value	R	This register contains the 12-bit CS current information. The range of the CS input pin is from 0 V to 1.6 V. Each LSB corresponds to 390.6 µV. At 0 V input, the value in this register is 0. The nominal voltage at this pin is 1 V. At 1 V input, the value in these bits is 0xA00 (2560 decimal).
[3:0]	Reserved	R	Reserved.

Table 137. Register 0xFED1—CS1_A Value

Bits	Bit Name	R/W	Description
[15:4]	CS1_A voltage value	R	This register contains the 12-bit CS1_A current information. The range of the CS1_A input pin is from 0 V to 1.6 V. Each LSB corresponds to 390.6 µV. At 0 V input, the value in this register is 0. The nominal voltage at this pin is 1 V. At 1 V input, the value in these bits is 0xA00 (2560 decimal).
[3:0]	Reserved	R	Reserved.

Table 138. Register 0xFED2—CS1_B Value

Bits	Bit Name	R/W	Description
[15:4]	CS1_B voltage value	R	This register contains the 12-bit CS1_B current information. The range of the CS1_B input pin is from 0 V to 1.6 V. Each LSB corresponds to 390.6 µV. At 0 V input, the value in this register is 0. The nominal voltage at this pin is 1 V. At 1 V input, the value in these bits is 0xA00 (2560 decimal).
[3:0]	Reserved	R	Reserved.

Table 139. Register 0xFED3—CS2_A Value

Bits	Bit Name	R/W	Description
[15:4]	CS2_A voltage value	R	This register contains the 12-bit CS2_A output current information. The range of the CS2_A input pin is from 0 mV to 120 mV. Each LSB corresponds to 29.3 µV. At 0 V input, the value in this register is 0.
[3:0]	Reserved	R	Reserved.

Table 140. Register 0xFED4—CS2_B Value

Bits	Bit Name	R/W	Description
[15:4]	CS2_B voltage value	R	This register contains the 12-bit CS2_B output current information. The range of the CS2_B input pin is from 0 mV to 120 mV. Each LSB corresponds to 29.3 µV. At 0 V input, the value in this register is 0.
[3:0]	Reserved	R	Reserved.

Table 141. Register 0xFED5—VS_A Value

Bits	Bit Name	R/W	Description
[15:4]	VS_A voltage value	R	This register contains the 12-bit VS_A output voltage information. The range of the VS_A input pin is from 0 V to 1.6 V. Each LSB corresponds to 390.6 µV. At 0 V input, the value in this register is 0. The nominal voltage at this pin is 1 V. At 1 V input, the value in these bits is 0xA00 (2560 decimal).
[3:0]	Reserved	R	Reserved.

Table 142. Register 0xFED6—VS_B Value

Bits	Bit Name	R/W	Description
[15:4]	VS_B voltage value	R	This register contains the 12-bit VS_B output voltage information. The range of the VS_B input pin is from 0 V to 1.6 V. Each LSB corresponds to 390.6 µV. At 0 V input, the value in this register is 0. The nominal voltage at this pin is 1 V. At 1 V input, the value in these bits is 0xA00 (2560 decimal).
[3:0]	Reserved	R	Reserved.

Table 143. Register 0xFED7—RTD1 Value

Bits	Bit Name	R/W	Description
[15:4]	RTD1 temperature value	R	This register contains the 12-bit RTD1 temperature information as determined from the RTD1 pin. The range of the RTD1 input pin is from 0 V to 1.6 V. Each LSB corresponds to 390.6 µV. At 0 V input, the value in this register is 0. The nominal voltage at this pin is 1 V. At 1 V input, the value in these bits is 0xA00 (2560 decimal).
[3:0]	Reserved	R	Reserved.

Table 144. Register 0xFED8—RTD2 Value

Bits	Bit Name	R/W	Description
[15:4]	RTD2 temperature value	R	This register contains the 12-bit RTD2 temperature information as determined from the RTD2 pin. The range of the RTD2 input pin is from 0 V to 1.6 V. Each LSB corresponds to 390.6 µV. At 0 V input, the value in this register is 0. The nominal voltage at this pin is 1 V. At 1 V input, the value in these bits is 0xA00 (2560 decimal).
[3:0]	Reserved	R	Reserved.

Table 145. Register 0xFED9—ACSNS Value

Bits	Bit Name	R/W	Description
[15:5]	ACSNS voltage value	R	This register contains the 11-bit ACSNS voltage information. The range of the ACSNS input pin is from 0 V to 1.6 V. Each LSB corresponds to 781.25 µV. At 0 V input, the value in this register is 0. The nominal voltage at this pin is 1 V. At 1 V input, the value in these bits is 0x500 (1280 decimal).
[4:0]	Reserved	R	Reserved.

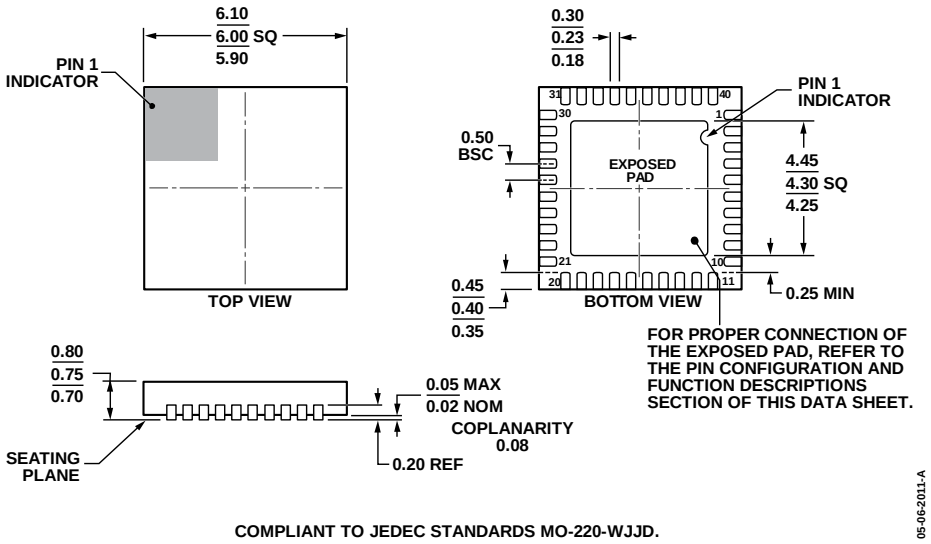
Table 146. Register 0xFEDA—Channel A Duty Cycle Value

Bits	Bit Name	R/W	Description
[15:4]	Channel A duty cycle value	R	This register contains the 12-bit duty cycle information for Channel A. The duty cycle is calculated using the rising and falling edge timings of OUT1, OUT2, OUT5, or OUT6. If more than one of these PWM outputs is assigned to Channel A, the PWM output used in the duty cycle calculation is selected in the following order: OUT1, OUT2, OUT5, OUT6. Each LSB corresponds to 0.0244% of the duty cycle. At 100% duty cycle, the value in this register is 0xFFF (4095 decimal).
[3:0]	Reserved	R	Reserved.

Table 147. Register 0xFEDB—Channel B Duty Cycle Value

Bits	Bit Name	R/W	Description
[15:4]	Channel B duty cycle value	R	This register contains the 12-bit duty cycle information for Channel B. The duty cycle is calculated using the rising and falling edge timings of OUT1, OUT2, OUT5, or OUT6. If more than one of these PWM outputs is assigned to Channel B, the PWM output used in the duty cycle calculation is selected in the following order: OUT1, OUT2, OUT5, OUT6. Each LSB corresponds to 0.0244% of the duty cycle. At 100% duty cycle, the value in this register is 0xFFF (4095 decimal).
[3:0]	Reserved	R	Reserved.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WJJD.

Figure 45. 40-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
6 mm × 6 mm Body, Very Very Thin Quad
(CP-40-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADP1053ACPZ-RL	−40°C to +125°C	40-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-40-10
ADP1053ACPZ-R7	−40°C to +125°C	40-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-40-10
ADP1053DC-EVALZ		ADP1053 Daughter Card Evaluation Board	
ADP-I2C-USB-Z		USB to I^2C Interface Connector	

[1] Z = RoHS Compliant Part.

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