

Evaluating the [ADE7978/ADE7933/ADE7932](#) Isolated Metering Chipset

FEATURES

Full featured evaluation board for the [ADE7978/ADE7933/ADE7932](#)

PC control in conjunction with the system demonstration platform ([EVAL-SDP-CB1Z](#))

PC software for control and data analysis (time and frequency domain)

Standalone capability

EVALUATION KIT CONTENTS

[ADE7978/ADE7933](#) evaluation board
SDP interface board

ADDITIONAL EQUIPMENT NEEDED

[EVAL-SDP-CB1Z](#) (must order separately)
includes a USB cable

4 current sensing shunts

Precision current and voltage signal source

SMB cables

PC running Windows XP SP2, Windows Vista, or Windows 7
with USB 2.0 port

ONLINE RESOURCES

Documents

[ADE7978/ADE7933/ADE7932](#) data sheet

[EVAL-ADE7978EBZ](#) user guide

Required Software

[EVAL-ADE7978EBZ](#) evaluation software (download from product page)

Design and Integration Files

[Schematics](#), [layout files](#), [bill of materials](#)

GENERAL DESCRIPTION

The [ADE7978/ADE7933](#) evaluation kit includes two boards that allow the performance of the isolated metering chipsets to be evaluated in a context very close to an actual three-phase meter implementation. Although this kit can also be used to test the [ADE7932](#) isolated ADC, the board is populated with only [ADE7978](#) and [ADE7933](#) devices and thus only the [ADE7978](#) and [ADE7933](#) are referred to in this user guide. The kit requires purchasing a third board, the controller board for the system demonstration platform ([EVAL-SDP-CB1Z](#)). The [ADE7978/ADE7933](#) evaluation kit includes evaluation software, written in LabVIEW®, that provides access to the registers and features of the chipsets using a PC interface.

TYPICAL SETUP

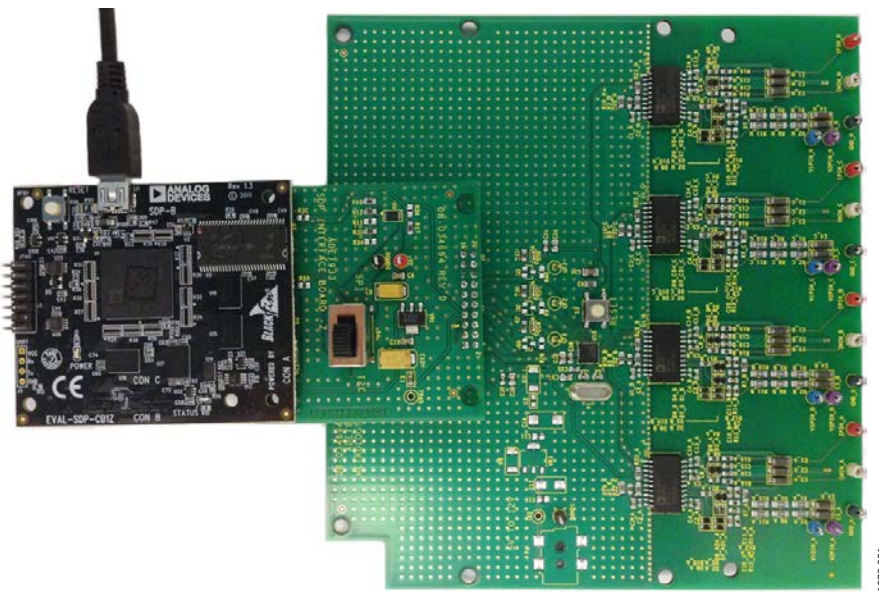


Figure 1. Connected to the SDP Interface and SDP Boards

TABLE OF CONTENTS

Features	1	Evaluation Software Functions	10
Evaluation Kit Contents.....	1	Hardware Reset.....	10
Additional Equipment Needed.....	1	Read and Write Registers	10
Online Resources.....	1	All Register Access	11
General Description	1	Waveform Sampling.....	11
Typical Setup	1	Read RMS Registers	12
Revision History	2	Read Fundamental RMS.....	12
Evaluation Board Hardware.....	3	Temperature Monitor	13
Overview.....	3	Total Active Power	13
Evaluation Kit Connection Diagram	4	CFx Configuration	14
Powering Up the Evaluation Kit Boards.....	5	Read Energy Registers	14
Analog Inputs.....	5	Total Reactive Power	15
Setting Up the Evaluation Board as an Energy Meter	7	Apparent Power	15
Evaluation Board Software	8	Total Harmonic Distortion	16
Installing the Drivers	8	Fundamental Active Power	16
Installing and Uninstalling the ADE7978/ADE7933		Fundamental Reactive Power	16
Software	8	Power Quality	17
Front Panel	8	Quick Setup	18

REVISION HISTORY

11/13—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

OVERVIEW

To evaluate the chipset, three boards are connected together (see Figure 1). The [ADE7978/ADE7933](#) evaluation board, which is populated with one [ADE7978](#) and four [ADE7933](#) isolated ADCs, can be used as an implementation example of a three-phase energy meter (see Figure 2).

The SDP interface board is provided in the kit. The 20-pin connector (P6) of the SDP interface board is connected to connector P7 of the [ADE7978/ADE7933](#) evaluation board.

The SDP interface board is connected to the SDP Blackfin board (also referred to as SDP-B or [EVAL-SDP-CB1Z](#)) using the 120-pin connector. Be sure to order [EVAL-SDP-CB1Z](#) when ordering your evaluation board; the kit and the SDP-B are purchased and packaged separately, but must be used together.

The 120-pin connector of the interface board is connected to the 120-pin connector of the SDP Blackfin board. It consists of an [ADSP-BF527](#) microcontroller that handles all the communications from the PC to the [ADE7978](#) and [ADE7933](#) devices populating the evaluation board (see Figure 3).

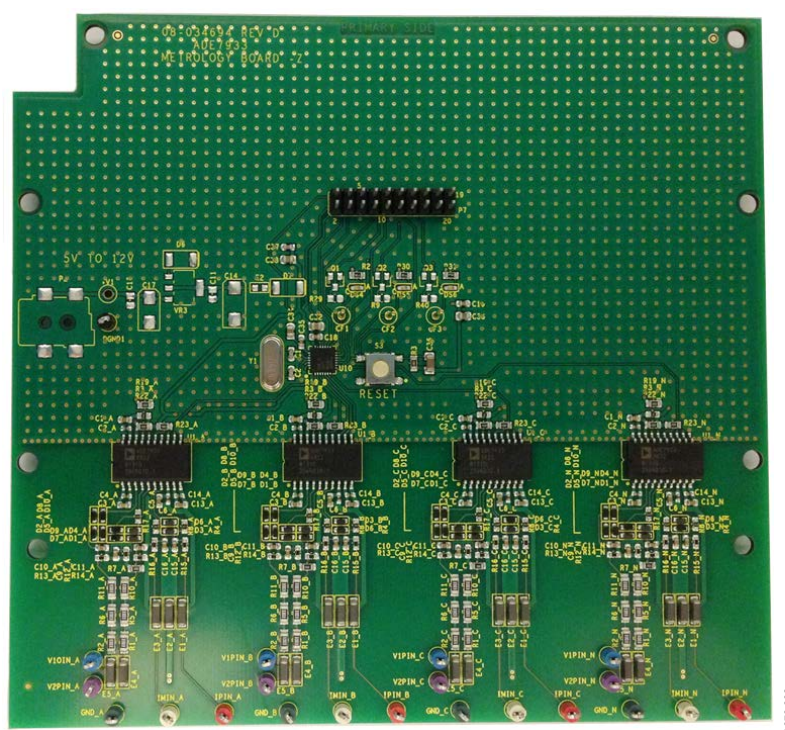


Figure 2. [ADE7978/ADE7933](#) Evaluation Board

EVALUATION KIT CONNECTION DIAGRAM

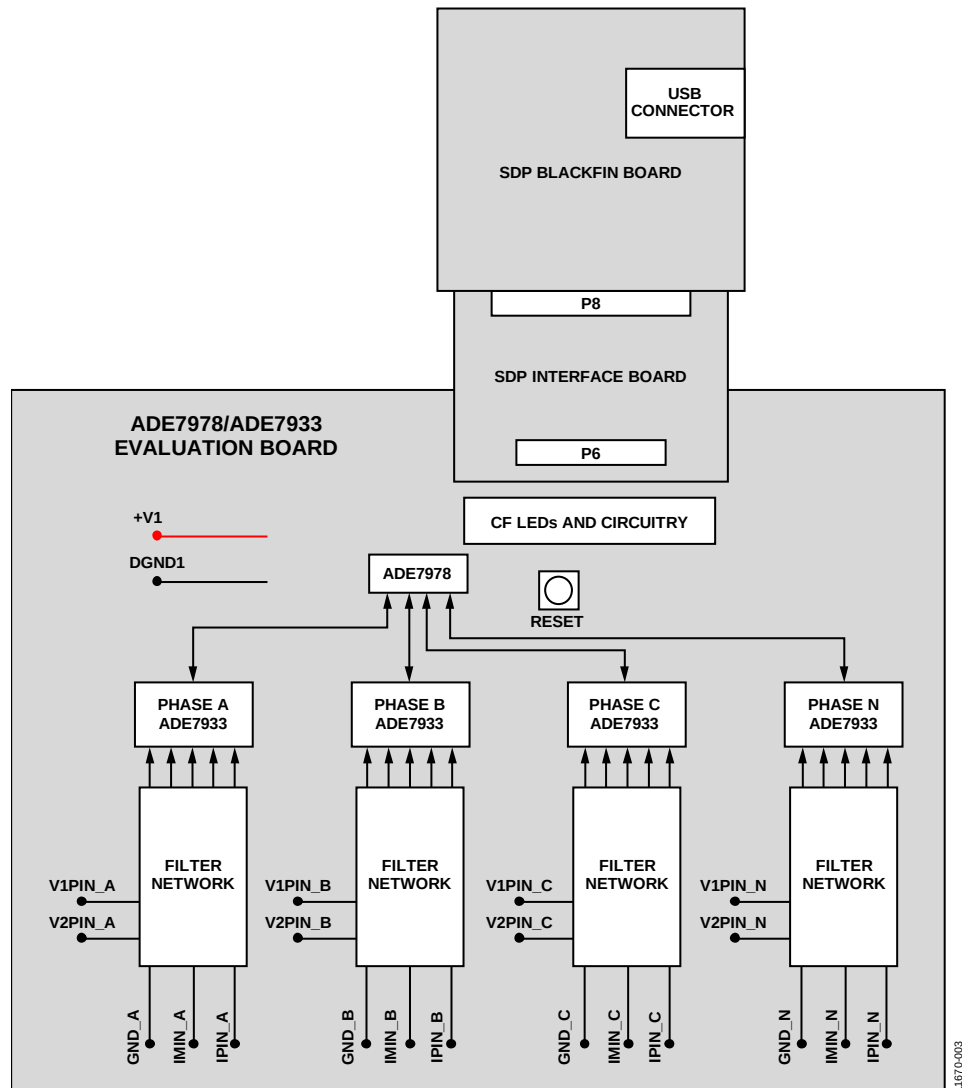


Figure 3. Evaluation Kit Connection

POWERING UP THE EVALUATION KIT BOARDS

The interface board receives power via the USB cable that is connected to the PC. A 3.3 V regulator then powers the SDP board microcontroller and the ADE7978/ADE7933 chipsets populating the evaluation board. No additional power source is required for the ADE7978/ADE7933 evaluation kit boards.

ANALOG INPUTS

Current and voltage signals are connected at the test pins placed on the evaluation board. All analog input signals are filtered using the on-board antialiasing filters before the signals are connected to the ADE7933 isolated ADCs. The components used on the board are the recommended values to be used with the ADE7978/ADE7933.

Current Sense Inputs (IMIN_A and IPIN_A, IMIN_B and IPIN_B, IMIN_C and IPIN_C, and IMIN_N and IPIN_N Test Pins)

Every ADE7933 measures the voltage across a shunt at its IP and IM pins. Figure 4 shows the structure used for the Phase A current.

The R4_A and R8_A (similarly, R4_B, R8_B for Phase B, _C for Phase C, and _N for Phase N) are 0 Ω resistors that do not need to be implemented on a real meter board. The R15_A/C15_A and R16_A/C16_A RC networks are the antialiasing filters. The default corner frequency of these low-pass filters is 4.8 kHz (1 kΩ/33 nF). These filters can easily be adjusted by replacing the components on the evaluation board.

The E1, E2, and E3 ferrite beads filter the high frequency noise that may be induced into the wires.

The absolute maximum voltage on the IP and IM pins of the ADE7933 is ±2 V. The D3_A and D6_A diodes protect the IP and IM pins against voltages greater than ±1 V. The maximum signal level permissible at the IP and IM pins of the ADE7933 is ±0.03125 V peak. The signal range should not exceed ±0.03125 V, with respect to AGND_ADC, for specified operation.

The Phase A shunt is connected between IPIN_A and IMIN_A test pins.

All the other current channels (that is, Phase B and Phase C) have an identical input structure. The Phase B shunt is connected between the IPIN_B and IMIN_B test pins, the Phase C shunt is connected between IPIN_C and IMIN_C, and the Phase N shunt is connected between IPIN_N and IMIN_N.

The shunt maximum value is function of the maximum current to be measured on every phase:

$$R = \frac{31.25 \times 10^{-3}}{\sqrt{2}} \times \frac{1}{I_{FS}}$$

where:

$$\frac{31.25 \times 10^{-3}}{\sqrt{2}}$$

is the rms value of the full-scale voltage accepted at input.

I_{FS} is the maximum current to be measured at the analog-to-digital converter (ADC) IP and IM inputs. It is called the full-scale current.

Figure 5 shows how a shunt is connected to the Phase A current input structure. The shunt is connected between P1 and P1' energy meter Phase A line inputs. IMIN_A and IPIN_A test pins are connected to the shunt measurement poles, while GND_A, the test pin that is the ground of the Phase A ADE7933 isolated side, is connected to the ground pole of the shunt.

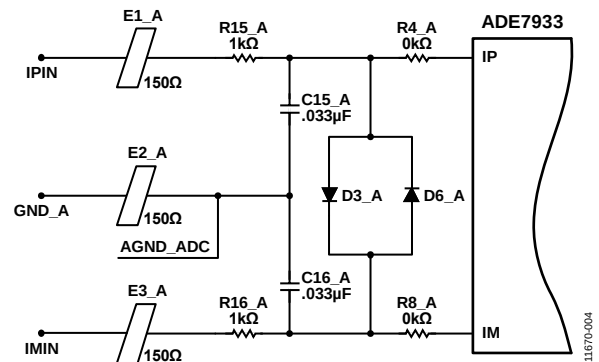


Figure 4. Phase A Current Input Structure on the Evaluation Board

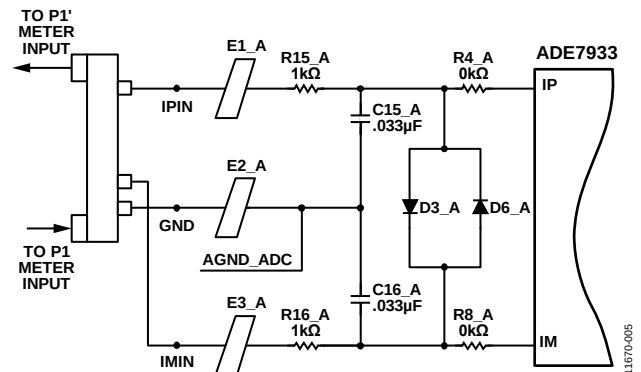


Figure 5. Example of a Shunt Connection

Phase Voltage Sense Inputs (V1PIN_A, V1PIN_B, V1PIN_C, and V1PIN_N Test Pins)

The phase-to-neutral voltage input connections on the evaluation board can be directly connected to the line voltage sources between V1PIN_A and GND_A for Phase A to neutral voltage, between V1PIN_B and GND_B for Phase B to neutral voltage, and between V1PIN_C and GND_C for Phase C to neutral voltage. These voltages are attenuated using a simple resistor divider network before they are supplied to the ADE7933. The attenuation network on the voltage channels is designed so that the corner frequency (3 dB frequency) of the network matches that of the antialiasing filters in the current channel inputs. This prevents the occurrence of large energy errors at low power factors.

The V1PIN path in Figure 6 shows a typical connection of the Phase A voltage inputs; the resistor divider consists in three 330 k Ω resistors (R1_A, R5_A, and R10_A) and one 1 k Ω resistor (R14_A). The antialiasing filter R14_A/C11_A matches the R12_A/C9_A filter in the VM path. The absolute maximum voltages on the V1P and VM pins of the ADE7933 are ± 2 V. The D1_A, D7_A, D4_A, and D9_A diodes protect the V1P and VM pins against voltages greater than ± 2 V. The maximum signal level permissible at the V1P pin of the ADE7933 is ± 0.5 V peak. The signal range should not exceed ± 0.5 V with respect to AGND_ADC for specified operation.

The E4_A and E5_A ferrite beads filter the high frequency noise that may be induced into the wires.

Auxiliary Voltage Sense Inputs (V2PIN_A, V2PIN_B, V2PIN_C, and V2PIN_N Test Pins)

The auxiliary voltage input connections on the ADE7978/ADE7933 evaluation board can be directly connected to the line voltage sources between V2PIN_A and GND_A for Phase A auxiliary voltage, between V2PIN_B and GND_B for Phase B auxiliary voltage, between V2PIN_C and GND_C for Phase C auxiliary voltage, and between V2PIN_N and GND_N for Phase N auxiliary voltage.

The V2PIN path in Figure 6 shows a typical connection of the Phase A auxiliary voltage input. It is very similar to the V1PIN path explained in the Phase Voltage Sense Inputs (V1PIN_A, V1PIN_B, V1PIN_C, and V1PIN_N Test Pins) section.

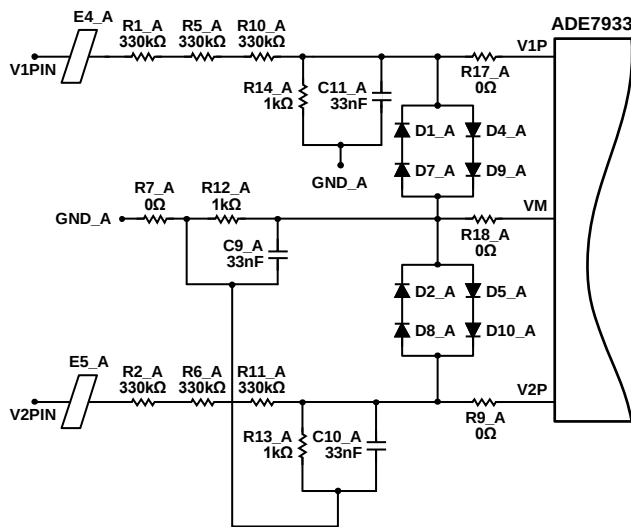


Figure 6. Phase A Voltage Input Structure on the Evaluation Board

Isolated Ground Pins Management

The ADE7933 package has two isolated ground GND_{ISO} pins: Pin 2 and Pin 10. Figure 7 shows their management in the case of a Phase ADE7933. For Figure 7, just add an “_A”, “_B”, “_C”, or “_N” for Phase A, B, C, and N, respectively (for example, Phase A C3 is “C3_A”). Internally, Pin 2 is connected to Pin 10. The decoupling capacitors, C3 and C4 on the VDD_{ISO} pin, are connected to the closest isolated ground pin, Pin 2. The decoupling capacitors, C5 and C6 on the analog LDO pin and C13 and C14 on the voltage reference pins, must be separate from the VDD_{ISO} circuitry and are connected to the isolate ground (Pin 10).

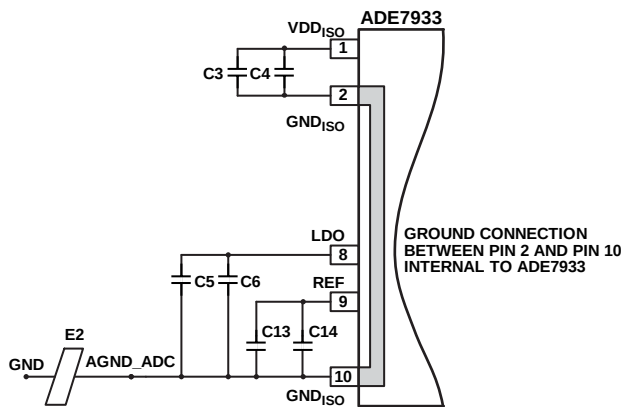


Figure 7. Isolated Ground Pins Management

The P1 meter input constitutes the AGND_ADC1 signal (see also Figure 5). AGND_ADC1 is then connected to the GND_{ISO} pin (AGND_ADC signal) through a ferrite bead, E2.

SETTING UP THE EVALUATION BOARD AS AN ENERGY METER

Figure 8 shows a typical setup for the [ADE7978/ADE7933](#) evaluation board. In this example, an energy meter for a 3-phase, 4-wire, wye distribution system is shown. Shunts are used to sense the phase currents and are connected as shown in Figure 8. The line voltages are connected directly to the board as shown. The board is supplied from one power supply provided by the PC through the USB cable.

Figure 9 shows a setup for the [ADE7978/ADE7933](#) evaluation board as an energy meter for a 3-phase, 3-wire, delta distribution system. The Phase B voltage is considered as reference and the V1PIN test pins of Phase A and Phase C [ADE7933](#) isolated ADCs are connected to it.

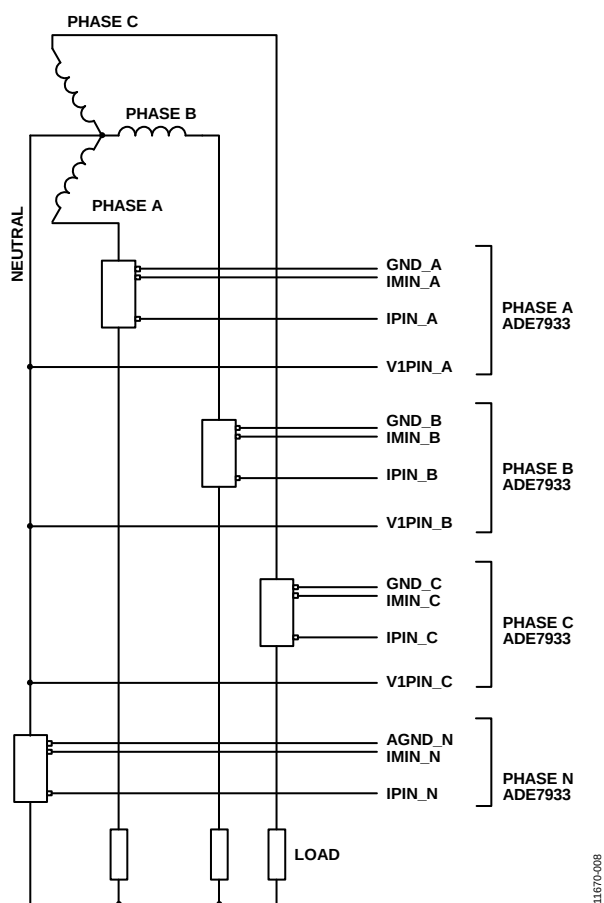


Figure 8. Typical Setup for the [ADE7978/ADE7933](#) Evaluation Board for 3-Phase, 4-Wire, Wye Distribution System

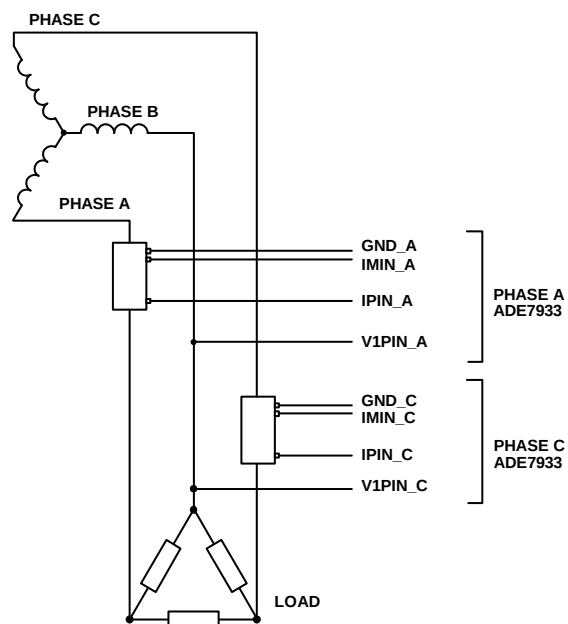


Figure 9. Typical Setup for the [ADE7978/ADE7933](#) Evaluation Board for 3-Phase, 3-Wire, Delta Distribution Systems

Using the Evaluation Board with Another Microcontroller

It is possible to manage the [ADE7978/ADE7933](#) evaluation board with a different microcontroller mounted on another board. The evaluation board can be connected to this second board through the P7 connector. The SDP interface and the SDP Blackfin boards are, in this case, unused.

EVALUATION BOARD SOFTWARE

The [ADE7978/ADE7933](#) evaluation board is supported by Windows® based software that allows the user to access all the functionality of the [ADE7978](#) and [ADE7933](#). The software communicates with the SDP Blackfin board using the USB. The microcontroller communicates with the [ADE7978](#) and [ADE7933](#) chipset placed on the evaluation board to process the requests that are sent from the PC.

INSTALLING THE DRIVERS

When using the [ADE7978/ADE7933](#) evaluation tools for the first time, a driver must be installed to allow successful communication. The driver **SDPDriversNET.exe** can be found in the evaluation software package in the **SDP drivers** folder.

To install the driver, follow this procedure:

1. When the Setup Wizard appears, click **Next**, and follow the installation instructions.

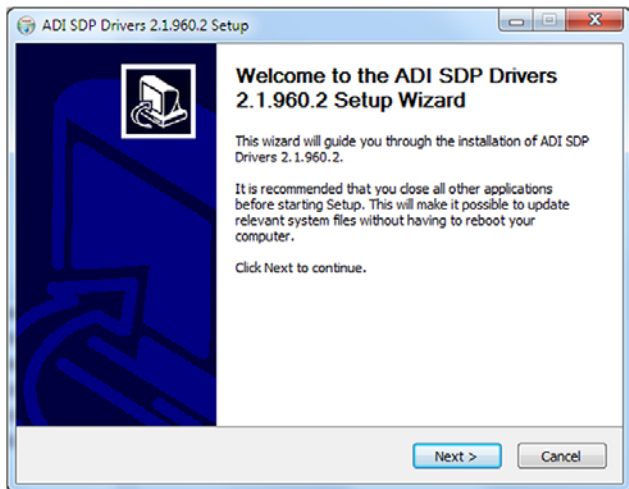


Figure 10. SDP Drivers Setup

2. When installation is complete, click **Finish** to close the window.

Connect the USB cable from the PC to the SDP-B board. Windows detects the device and locates the correct driver automatically.

INSTALLING AND UNINSTALLING THE ADE7978/ADE7933 SOFTWARE

The [ADE7978/ADE7933](#) software is supplied with the evaluation software package. It contains an installer to install the [ADE7978/ADE7933](#) evaluation software. The program to be installed is a LabVIEW™ based program that runs on the PC.

Before using LabView 2010 on the PC for the first time, run an installer prior to executing the LabView-based program. This installer is available in the **LabView\InstallationFiles** folder. If a copy of LabView 2010 is available on the PC, the executable is provided in the **executable** folder. The LabView source files are provided in the **LabView_project\source** folder.

1. To install the [ADE7978/ADE7933](#) software, double-click **InstallationFiles\setup.exe**. This launches the setup program that automatically installs all the software components, including the uninstall program, and creates the required directories.
2. To launch the software, go to **Start/All Programs/ADE7978 Eval Front Panel** and click **ADE7978_Eval_Software**.

Both the [ADE7978/ADE7933](#) evaluation software program and the NI run-time engine are uninstalled using the **Add/Remove Programs** option in the control panel.

1. Before installing a new version of the [ADE7978/ADE7933](#) evaluation software, first uninstall the previous version.
2. Select the **Add/Remove Programs** option in the Windows control panel.
3. Select the program to uninstall and click the **Add/Remove** button.

FRONT PANEL

When the software is launched, the Front Panel is opened. This panel contains three areas: the main menu on the left, a drop-down menu to select the communication mode, and a button for the **Connection Information** on the right (see Figure 11).

The software automatically detects the SDP-B board.

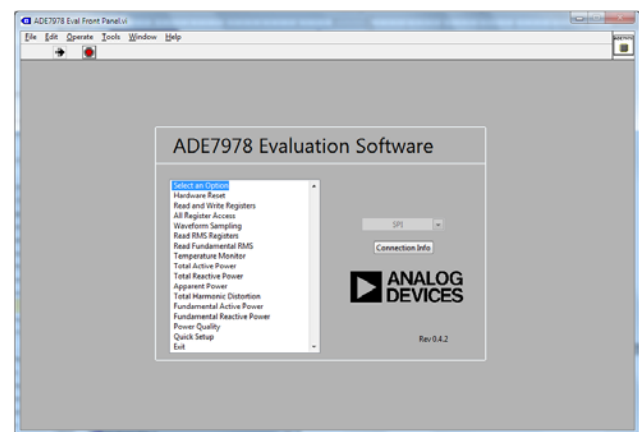


Figure 11. Front Panel of the Software

Troubleshooting SDP Detection

If the software does not detect the SDP-B board, the message shown in Figure 12 is displayed.

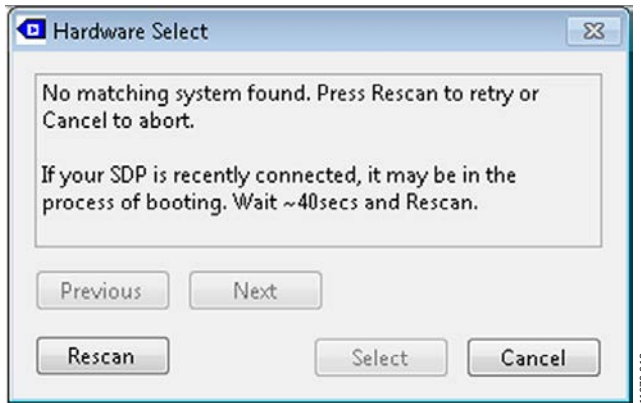


Figure 12. Hardware Select Message

If this message appears, take the following steps:

1. Verify that the SDP Blackfin board is connected to the PC using the USB cable.
The window in Figure 13 pops up on your task bar; Windows will install any other necessary drivers.
2. Once the installation is complete, click **Rescan**.
3. When another window appears, check if the LED on the board is flashing; if so, click **Select**.



Figure 13. Installing Driver Software Message

EVALUATION SOFTWARE FUNCTIONS

The [ADE7978/ADE7933](#) evaluation software allows access to all registers and features of the [ADE7978](#). The menu options available are

- Hardware Reset
- Read and Write Registers
- All Register Access
- Waveform Sampling
- Read RMS Registers
- Read Fundamental RMS
- Temperature Monitor
- Total Active Power
- Total Reactive Power
- Apparent Power
- Total Harmonic Distortion
- Fundamental Active Power
- Fundamental Reactive Power
- Power Quality
- Quick Setup
- Exit (Stops LabView)

The options provide access to all internal registers and allow the evaluation of the [ADE7978/ADE7933](#) chipset performance/features. To access these functions, click the desired option in the options list (see Figure 11).

Clicking an option in the list displays a window where the specific function can be accessed. Each window includes an **Exit** button used to return to the main window.

Note that only one option from the options list can be open at a time; click **Exit** to return to the main window before choosing another option from the list.

HARDWARE RESET

The **Hardware Reset** button of the [ADE7978/ADE7933](#) evaluation board resets the [ADE7978/ADE7933](#) chipset. Then, the Front Panel is set back to the **Select Com Mode** step, and all registers go back to their default values.

READ AND WRITE REGISTERS

The **Read and Write Registers** window is shown in Figure 14. Every register of the [ADE7978](#) can be accessed using the drop-down menu at the center of the screen. The switch above this menu is used to choose between using register names or register addresses. With **Register Name**, the name of the register can be typed into the drop-down field to find a specific register. With **Register Number**, the address of the desired register to read or write to can be input. The register can be read or written to via **Read Registers** or **Write Registers**. The bottom left has a field for entering the data to be written to the register and a **Write Successful** light.

When **Read** is clicked, the register identified in the **Register Name** box is read and its value is visualized in the **Data Read from Register** box.

When **Write** is clicked, the register identified in the **Register Name** box is written with the value from the **Data to Write to Register** box.

Exit returns the program to the main menu.



Figure 14. Read and Write Registers

ALL REGISTER ACCESS

The All Register Access window, shown in Figure 15, allows control over all the registers at one time. The **Read/Write Successful** LED lights up when all registers are accessed.

- **Exit** returns to the main menu.
- **Read All** reads all the registers as displayed in the **All Registers** table.
- **Write All** writes the data to the specified registers. The data in a column is only written to the register in the respective column; the register name cannot be changed.
- **File Output** specifies the path to save the register file to. A new path can be either typed in or the yellow folder can be clicked to search for a path.
- **Save to File** saves all registers to a .csv file.
- **Load from File** prompts you to choose a .csv file from which to load all the registers.
- An error window (bottom, right) is available. If something goes wrong, reset the board and try again.



Figure 15. All Register Access

WAVEFORM SAMPLING

The Waveform Sampling window is shown in Figure 16.

- The left side of the window, labeled **Channels**, lists the different waveforms that can be plotted. A maximum of five consecutive plots can be chosen at one time.
- **Run** continuously plots the chosen waveforms in a window the size of which is specified by **Capture Time**.
- **Single** captures the plot for the **Capture Time** specified and keeps it displayed in the window.
- **Exit** returns to the main menu.
- **File Output** is used to export the waveform captured as a .csv or .png file. The directory must be chosen by typing it into the text box or clicking to the picture of a file folder.
- **Triggering** can be enabled to align the window to start at a particular **Level** (the amplitude at which the left side of the waveform is aligned) of a waveform chosen with **Source** and **Mode**.

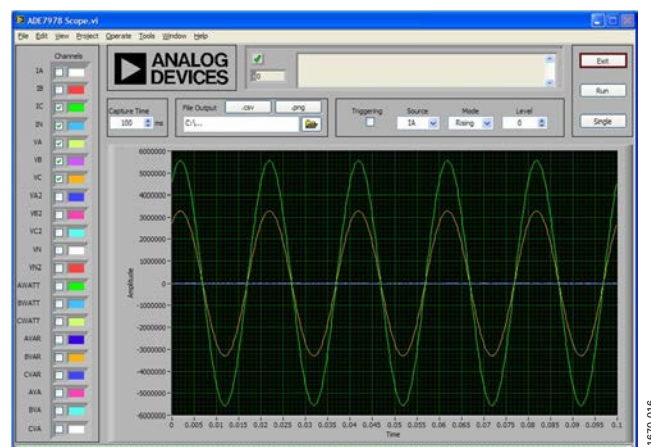


Figure 16. Waveform Sampling

READ RMS REGISTERS

The Read RMS Registers window, shown in Figure 17, shows the signal path for the two voltage signals and one current signal to get the rms value. The rms offset (xxRMSOS) register can be modified. The rms display shows a reading and cannot be modified.

- On the right side of the window is the **Active Data Path** drop-down menu. The selected data path is displayed in the window.
- When Phase N is chosen, a switch appears on the left side. This switches the NIRMS register between displaying NIRMS or ISUM RMS (The rms value of ISUM, the instantaneous sum of all three phase currents).
- At the bottom of the window, **Read RMS registers** reads the rms values in synchronization with a phase voltage or current. The source to be synchronous with can be chosen with **Zero-Crossing Source**. It is recommended to set the **Number of Averages** to a minimum of 100.
- Exit** returns to the main menu.
- Read** reads the current configuration of the part and the instantaneous rms values.
- Write** writes the current configuration to the registers.
- Total Harmonic Distortion** goes to the THD window. See the Total Harmonic Distortion section for details.

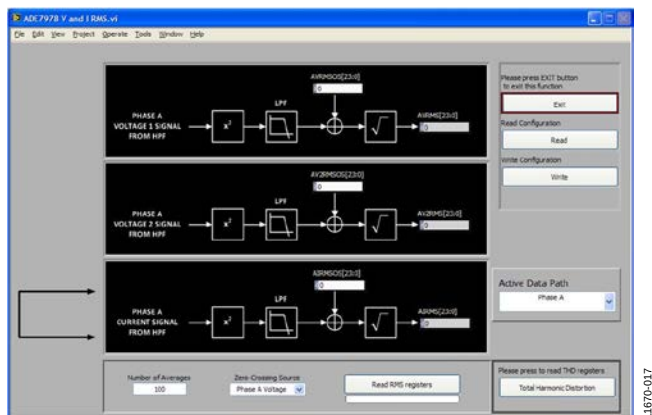


Figure 17. Read RMS Registers

READ FUNDAMENTAL RMS

The Read Fundamental RMS window is shown in Figure 18. This window shows the signal path for Voltage 1 and the current signal to calculate the fundamental rms values. The fundamental rms offset (xFxRMSOS) register can be modified in the labeled box. The rms display shows a reading and cannot be modified.

- On the right side of the window is the **Active Data Path** drop-down menu. The selected data path is displayed in the window.
- At the bottom of the window, **Read Fund. RMS registers** reads the rms values in synchronization with a phase voltage or current. The source to be synchronous with can be chosen with **Zero-Crossing Source**. It is recommended to set the **Number of Averages** to 100.
- Exit** returns to the main menu.
- Read** reads the current configuration of the part and the instantaneous rms values.
- Write** writes the current configuration to the registers.

Total Harmonic Distortion goes to the THD window. See the Total Harmonic Distortion section for details.

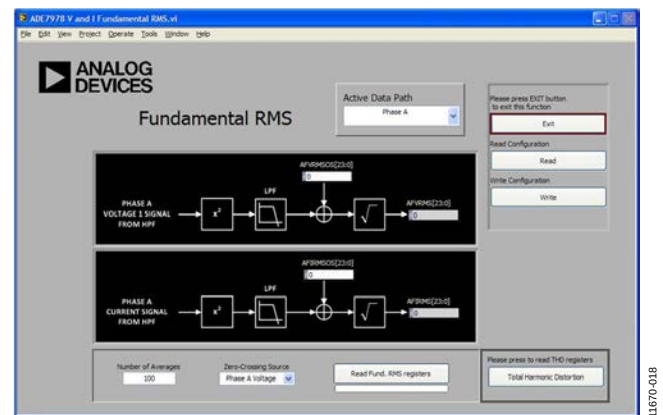


Figure 18. Read Fundamental RMS

CFx CONFIGURATION

The CFx Configuration window is shown in Figure 21. This window is used to set up the CF outputs to give out pulses.

- **COMPMODE** and **CFMODE** register indicators are at the top of the window. **CFCYC** is the number of CF pulses between two consecutive energy latches.
- The three smaller **TERMSELx** windows on the left have selections for which phases to include in the CF calculations. Hold the Shift key down to select multiple phases.
- To the right are three **CFxSEL** windows that configure the type of power output on each CF pin.
- The right side has **CFx output** switches for enabling the CF outputs and switches for enabling **CFx Latch Mode**.
- The **CFxDEN** values are used to change the frequency of the output by a certain multiple (for example, dividing CFxDEN by 2 divides the frequency by 2).

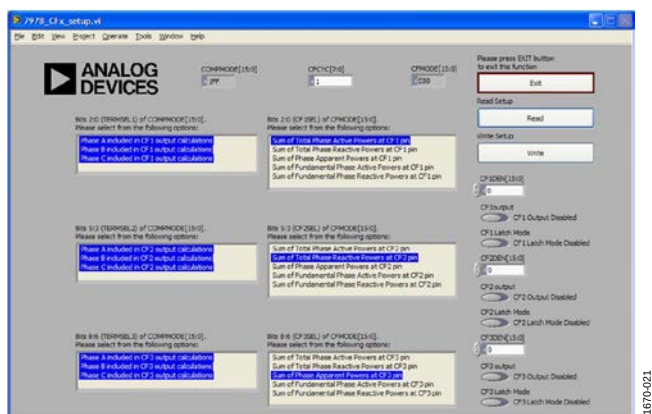


Figure 21. CFx Configuration Window

READ ENERGY REGISTERS

The Read Energy Registers window is shown in Figure 22. This window provides settings to read the energy registers in line cycle accumulation or in synchronous with CF pulses.

At the top center are the **Read energy registers synchronous with CFx pulses** buttons. When pressed, the energy registers that contribute to the CFx pin output are read when the CFx pin transitions high to low and an interrupt is triggered.

Note this function requires setting Bits[14:12] (CF3LATCH, CF2LATCH, and CF1LATCH) in the CFMODE register using the CFx Configuration window. See the CFx Configuration section for details. If these bits are not set and the **Read energy registers synchronous with CFx pulses** buttons are pressed, a message displays and the CF3LATCH, CF2LATCH, and CF1LATCH bits are set. When the buttons are depressed, the bits are cleared back to 0.

- **Read all energy registers using line accumulation mode** reads the energy registers that are set in line cycle accumulation mode. **LINECYC** is the number of half-line cycles after which to take the register reading.
- Under this button is a progress bar and **Expected Accumulation Time** box with the predicting time it takes to obtain a reading. The **Actual Accumulation Time** box gives the amount of time it took for the readings to run with the selected amount of line cycles (**LINECYC**).
- The bottom of the window displays the output of all the energy registers for the chosen phase in the drop-down box, **Choose Phase**. The selection can be changed while the **Read all energy registers using line accumulation mode** and **Read energy registers synchronous with CFx pulses** buttons are pressed.
- The switches under these drop-down boxes are used to choose the energies to be read in line cycle accumulation mode.
- The timeout boxes are used to set the amount of time in milliseconds the part waits for a zero crossing and to set the amount of time elapsed before resetting an interrupt.
- **Exit** returns to the main menu.
- **Read** reads the current setup of the part and the energy register values.
- **Write** writes the current configuration to the registers.

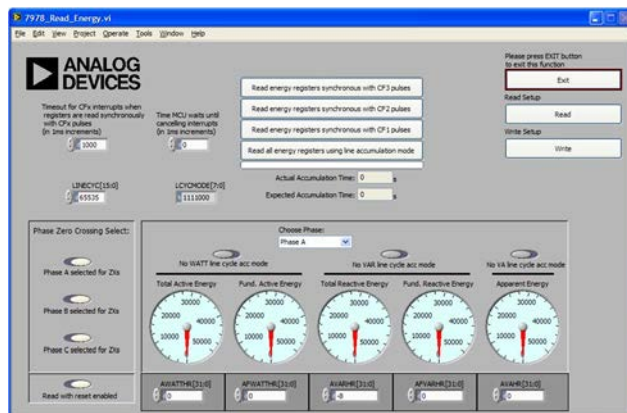


Figure 22. Read Energy Registers Window

TOTAL REACTIVE POWER

The Total Reactive Power window is shown in Figure 23. This window is very similar to the **Total Active Power** window except the registers and switches are changed to reflect the reactive power data path. This window shows the signal path for the reactive power with the diagram displaying all relevant register values.

- At the top left is **Active Data Path**. Here the desired phase to be shown in the window can be chosen and all the register values change with the phase.
- ACCMODE register settings** is where the accumulation mode can be changed with **ACCMODE.3,2**. The connection setup can be changed with **ACCMODE.5,4**. Total or fundamental power can be used to trigger interrupt registers with **ACCMODE.7**
- The **CONFIG register setting** is used to swap the voltage and current channel outputs.
- Under that is a drop-down box, **Choose a Phase Voltage**, in which a different phase voltage can be used along with the phase current to do the calculations.
- To the right of this, the **No Load Thresholds** can be set.
- CFx Configuration** opens another window to setup the CF outputs.
- Read Energy Registers** opens another window to read the energy register with multiple settings (for example, synchronous with CF, line cycle accumulation).
- Exit** returns to the main menu.
- Read** reads the current configuration of the part and the energy register values.
- Write** writes the current configuration to the registers.
- The middle left has a **Read with reset** button to enable or disable the register being reset after a read access.

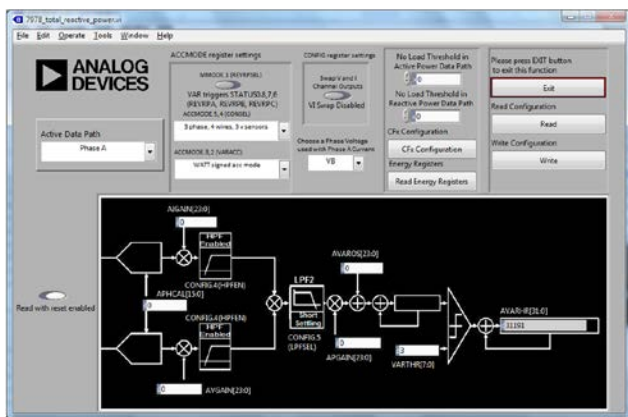
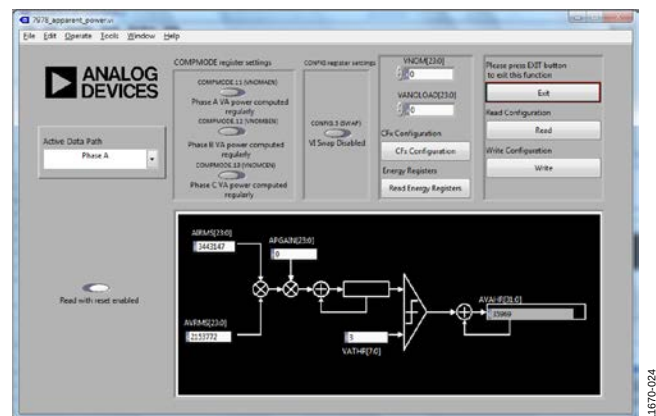


Figure 23. Total Reactive Power

APPARENT POWER

The Apparent Power window is shown in Figure 24. This window is similar to the **Total Active Power** window except the registers and switches are changed to reflect the apparent power data path. The diagram is for the apparent power signal path and shows all relevant registers.

- At the top left is **Active Data Path** where the desired phase to be shown in the window can be chosen and all the register values change with the phase.
- To the right is the **COMPMODE register settings** box and the switches are used to change the calculation of apparent power. It is calculated with either xVRMS or V_{NOM}.
- The **CONFIG register settings** is used to swap the voltage and current channel outputs.
- To the right of this, the **No Load Thresholds** can be set.
- CFx Configuration** opens another window to setup the CF outputs.
- Read Energy Registers** open another window to read the energy register with multiple settings (for example, synchronous with CF or line cycle accumulation).
- Exit** returns to the main menu.
- Read** reads the current configuration of the part and the energy register values.
- Write** writes the current configuration to the registers.
- The middle left has a **Read with reset** button to enable or disable the register being reset after a read access.



TOTAL HARMONIC DISTORTION

The Total Harmonic Distortion window is shown in Figure 25. This window shows the percentage of the harmonics in the rms reading out of the fundamental rms reading. Refer to the Total Harmonic Distortion Calculation section in the data sheet.

- Under the **Channel X** headings, the top row consists of the respective register readings. Below this row is the **Percentage Harmonics out of Fundamental**.
- **Exit** returns to the main menu.
- **Read** reads the current configuration of the part and the energy register values.

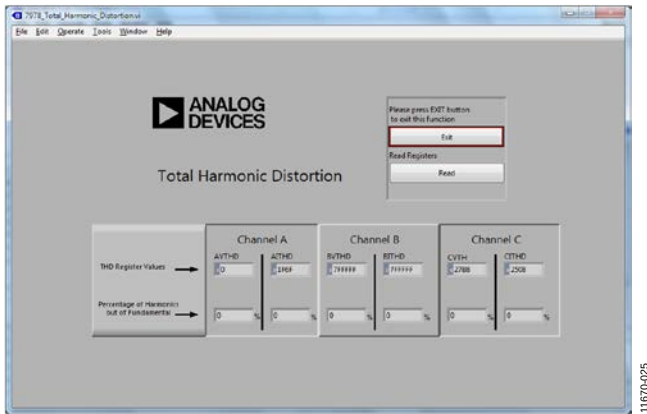


Figure 25. Total Harmonic Distortion Window

FUNDAMENTAL ACTIVE POWER

The Fundamental Active Power window is shown in Figure 26. This window is very similar to the **Total Active Power** window. The registers are setup to reflect the fundamental active power.

- On the left, **SELFREQ** is used to select the frequency of the power line being used. Setting the correct line frequency speeds up the fundamental calculations.
- **VLEVEL** is the trigger level for the fundamental based on the following equation:

$$VLEVEL = \frac{V_{FS}}{V_n} \times 4 \times 10^6$$

- **Exit** returns to the main menu.
- **Read** reads the current configuration of the part and the energy register values.
- **Write** writes the current configuration to the registers.
- See the Total Active Power section for all other settings.

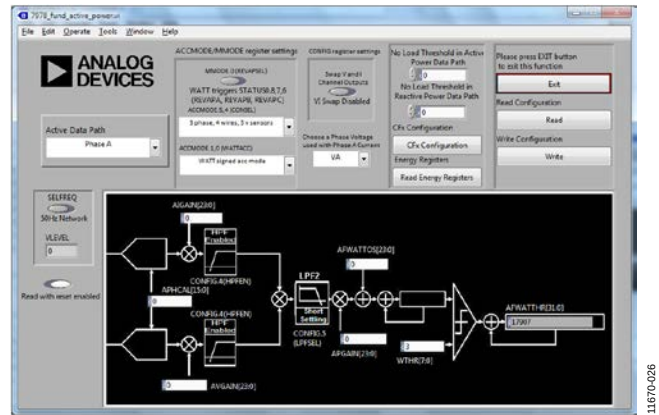


Figure 26. Fundamental Active Power Window

FUNDAMENTAL REACTIVE POWER

The Fundamental Reactive Power window is shown in Figure 27. This window is similar to the Total Reactive Power window. The registers are setup to reflect the fundamental reactive power.

- On the left, **SELFREQ** is used to select the frequency of the power line being used. Setting the correct line frequency can speed up the fundamental calculations.
- **VLEVEL** is the trigger level for the fundamental based on the following equation:

$$VLEVEL = \frac{V_{FS}}{V_n} \times 4 \times 10^6$$

- **Exit** returns to the main menu.
- **Read** reads the current configuration of the part and the energy register values.
- **Write** writes the current configuration to the registers.
- See the Total Reactive Power section for all other settings.

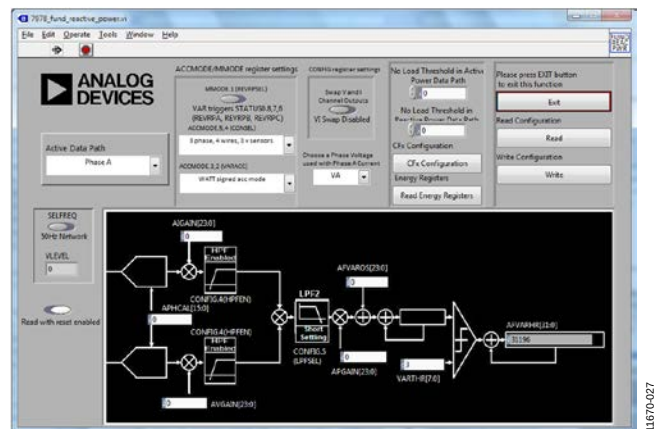


Figure 27. Fundamental Reactive Power Window

POWER QUALITY

The Power Quality windows provide access to all power quality measurements performed inside the [ADE7978](#): zero-crossing detection, zero-crossing timeout and period measurement (see Figure 28), neutral current mismatch (see Figure 29), overvoltage and overcurrent detection (see Figure 30), peak detection (see Figure 31), sag detection (see Figure 32), and time intervals between phases (see Figure 33).

- At the top left, **Active Measurement** is used to select the active window.
- **Read Configuration** reads all configuration registers used inside the windows.
- **Write Configuration** writes all configuration registers with the values introduced inside the windows.
- **Wait For Interrupts** manages the interrupts set in the MASK1 register.

The procedure is as follows:

1. Set the interrupt to be monitored using the corresponding switch placed in the window.
2. Set the other registers linked to the interrupt functionality.
3. Click the **Write Configuration** button to update the [ADE7978](#) registers.
4. Click the **Wait For Interrupts** button.

The program monitors the `IRQ1` pin. When it is low, it cancels the interrupt by writing to the `STATUS1` register with the corresponding interrupt flag set to 1. Then, it reads the `ISUM`, `PHSTATUS`, `IPEAK`, `VPEAK`, `ANGLE0`, `ANGLE1`, and `ANGLE2` registers and displays them. The **Timeout for interrupts** boxes are used to set the amount of time in milliseconds that the part waits for a zero crossing. **Time MCU waits until cancelling interrupts** sets the amount of time the Blackfin processor of the SDP-B board waits before resetting an interrupt.

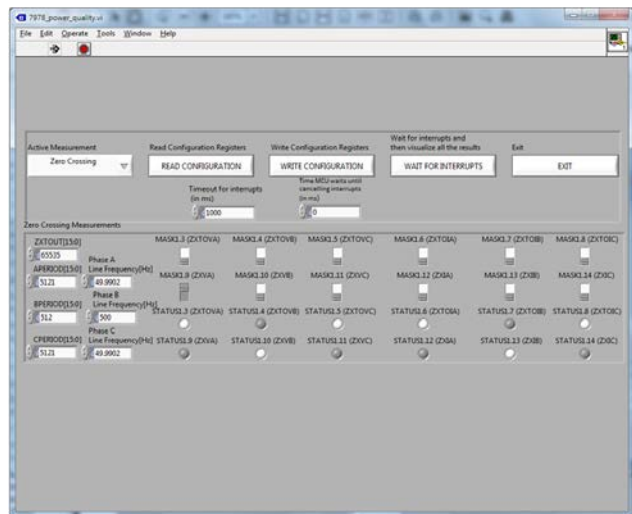


Figure 28. Power Quality Zero-Crossing Measurements

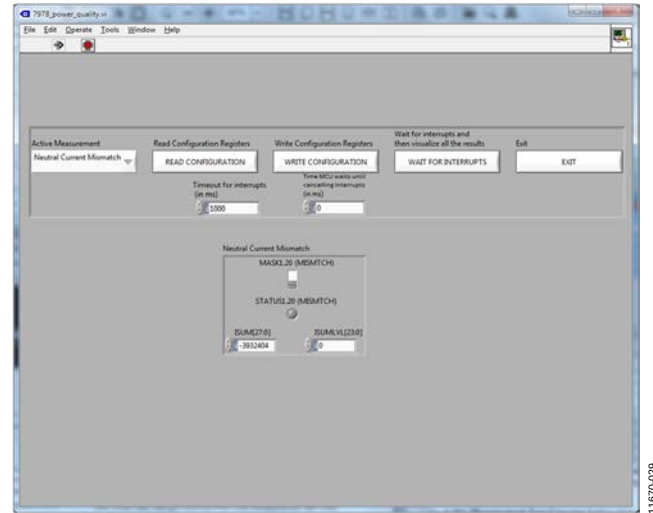


Figure 29. Power Quality Neutral Current Mismatch Window

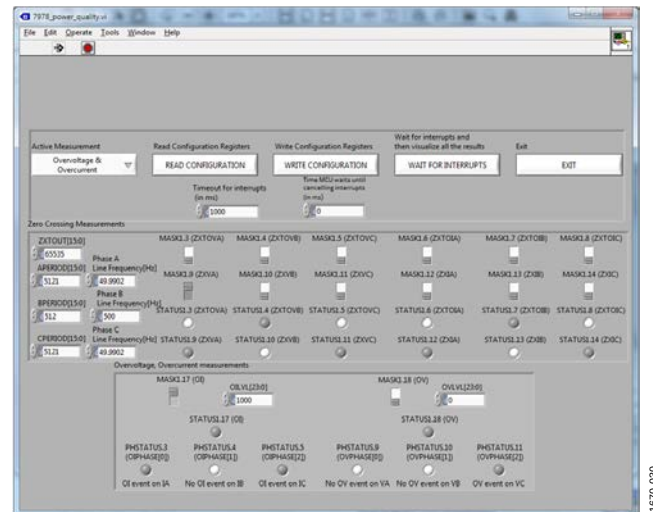


Figure 30. Power Quality Overvoltage and Overcurrent Measurements

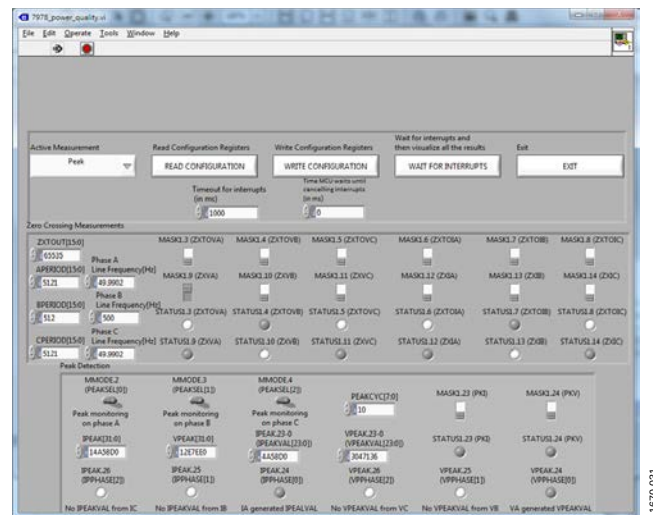


Figure 31. Power Quality Peak Detection

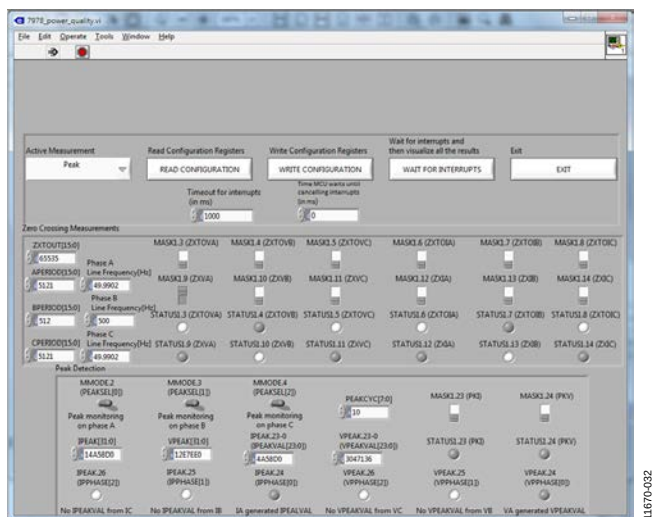


Figure 32. Power Quality Sag Detection

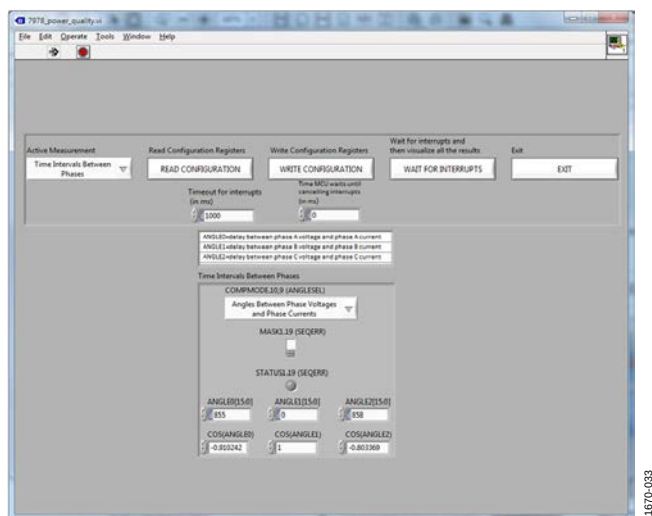


Figure 33. Power Quality Time Interval Between Phases

QUICK SETUP

The Quick Setup window is shown in Figure 34. This window can be used to rapidly initialize a three-phase meter. Set the **Meter Constant** (MC, in impulses/kWh), the **Nominal Voltage** (VN, in V rms units), the **Nominal Current** (IN, in A rms units), and the **Nominal Line Frequency** (f_n , either 50 Hz or 60 Hz) must be set using the window controls.

Begin Computations starts the program that reads rms voltages and currents and calculates the full-scale voltage and currents used to further initialize the meter. This process reads the rms voltages 100 times and the rms currents 100 times and

then averages them (this reduces jitter in the measurement, therefore increasing the accuracy).

The program then computes the full-scale voltages and currents and the constants that are important for setting up the [ADE7978](#): the constant n , CFDEN, WTHR, VARTHR, VATHR, VLEVEL, and VNOM. The expressions used to determine these constants are the ones presented in the [ADE7978/ADE7933/ADE7932](#) data sheet.

The values calculated by the quick start program can be overwritten. **Update Registers** allows you to:

- Initialize the gain, CF1DEN, CF2DEN, CF3DEN, WTHR, VARTHR, VATHR, VLEVEL, and VNOM registers
- Enable the CF1 pin to provide a signal proportional to the total active power, enable the CF2 pin to provide a signal proportional to the fundamental reactive power, and enable the CF3 pin to provide a signal proportional to the apparent power.
- Select the state of Bit 14 (SELFREQ) in the COMPMODE register based on the nominal line frequency, f_n .

At this point, the evaluation board is set up as a three-phase meter, and calibration can be performed. To store the register initializations, click **Save to File** in the All Register Access window (see Figure 15). If the board is reset for any reason, the registers can be loaded into the [ADE7978](#) by loading the contents of the data file. To do this, click **Load from File** in the All Register Access window.

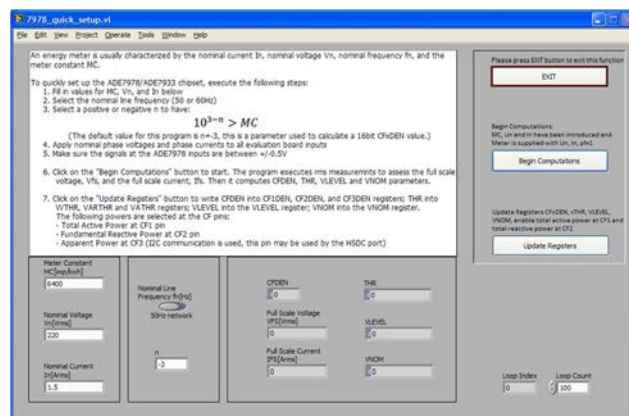


Figure 34. Quick Setup Window

NOTES

NOTES

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

**ESD Caution**

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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