7A, PolyPhase Synchronous Step-Down Regulator

FEATURES

- **High Efficiency: Up to 96%**
- **7A Output Current at V_{IN} = 3V**
- **Adjustable Frequency: 1.5MHz Nominal**
- **PolyPhase Operation (Up to 12 Phases)**
- **Spread Spectrum Frequency Modulation**
- **Output Tracking and Margining**
- **±1% Reference Accuracy**
- 2.5V to 5.5V V_{IN} Range
- Phase Lockable from 0.75MHz to 2.25MHz
- Selectable Burst Mode® Operation
- Low Dropout Operation: 100% Duty Cycle
- Low Quiescent Current: 450µA
- Current Mode Operation for Excellent Line and Load Transient Response
- Shutdown Mode Draws Only 0.2µA Supply Current
- Available in 38-Pin (5mm × 7mm) QFN Package

APPLICATIONS

- Point of Load Power Supply
- Portable Instruments
- Distributed Power Systems
- Battery-Powered Equipment

DESCRIPTION

The LTC®3415 is a high efficiency, monolithic synchronous buck regulator using a phase lockable constant frequency, current mode architecture. PolyPhase® operation allows multiple LTC3415s to run out of phase while using minimal input and output capacitance. The operating supply range is from 5.5V down to 2.5V, making it suitable for single Lithium-Ion battery as well as point of load power supply applications. Burst Mode operation provides high efficiency at low load currents. 100% duty cycle provides low dropout operation that extends operating time in battery-operated systems.

The operating frequency is internally set at 1.5MHz, allowing the use of small surface mount inductors. For switching-noise sensitive applications, it can be externally synchronized from 0.75MHz to 2.25MHz. The PHMODE pin allows user control of the phase of the outgoing clock signal. The current sense comparator is factory trimmed for accurate output current sharing. Burst Mode operation is inhibited during synchronization or when the MODE pin is pulled low to reduce noise and RF interference.

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TYPICAL APPLICATION

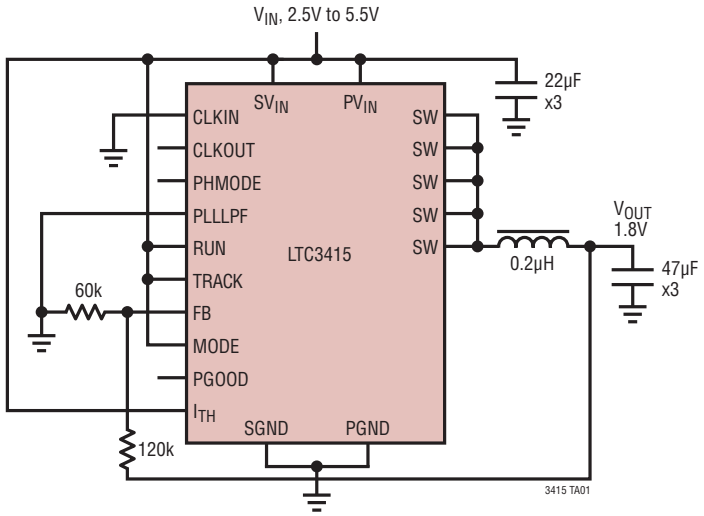
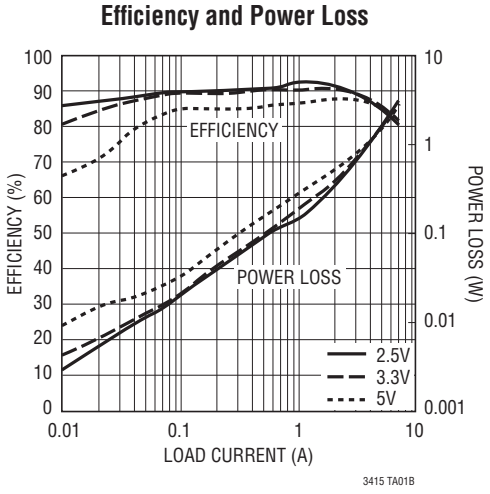


Figure 1. High Efficiency Step-Down Converter

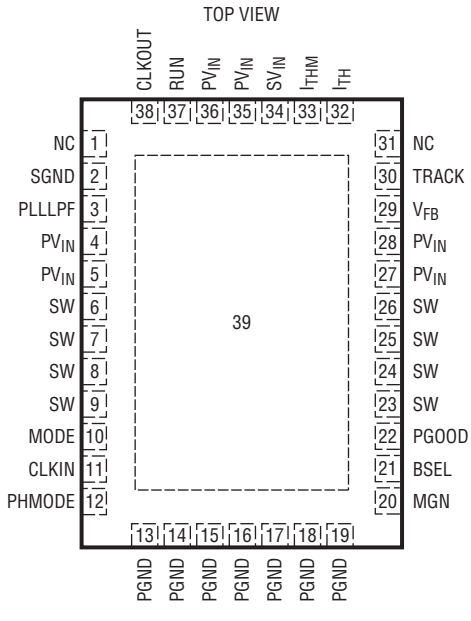


ABSOLUTE MAXIMUM RATINGS

(Note 1)

SV_{IN}, PV_{IN} Voltage ..... –0.3V to 6V
PLLLPF, PGOOD Voltages.....–0.3V to V_{IN}
CLKIN, PHMODE, MODE Voltages .....–0.3V to V_{IN}
CLKOUT Voltage ..... –0.3V to 2V
I_{TH}, I_{THM}, V_{FB}, TRACK Voltages.....–0.3V to V_{IN}
MGN, BSEL, RUN Voltages .....–0.3V to V_{IN}
SW Voltage (DC).....–0.3V to (V_{IN} + 0.3V)
Peak SW Sink and Source Current.....15A
Operating Ambient Temperature
Range (Note 2).....–40°C to 85°C
Junction Temperature (Note 5) .....125°C
Storage Temperature.....–65°C to 125°C

PIN CONFIGURATION



UHF PACKAGE
38-LEAD (7mm × 5mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 34°C/W, θ_{JC} = 1.1°C/W
EXPOSED PAD (PIN 39) IS PGND
MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3415EUHF#PBF	LTC3415EUHF#TRPBF	3415	38-Lead (5mm × 7mm) QFN Package	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 3.3V unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SV_{IN}	Signal Input Voltage Range			2.375		5.5	V
V_{FB}	Regulated Feedback Voltage	(Note 3)	●	0.590	0.596	0.602	V
ΔV_{FB}	Reference Voltage Line Regulation	V_{IN} = 2.5V to 5.5V (Note 3)			0.15	0.3	%/V
$V_{LOADREG}$	Output Voltage Load Regulation	Measured in Servo Loop, V_{ITH} = 0.3V Measured in Servo Loop, V_{ITH} = 0.9V	● ●		0.1 –0.05	0.2 –0.2	% %
ΔV_{PGOOD}	Power Good Range			±7	±10	±13	%
R_{PGOOD}	Power Good Pull-Down Resistance	1mA Load, V_{IN} = 3.3V			25	40	Ω

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 3.3V unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_Q	Input DC Bias Current Active Current Sleep Shutdown	(Note 4) V_{FB} = 0.57V, MODE = 0V V_{FB} = 0.63V, MODE = V_{IN} V_{RUN} = 0V		 1350 450 0.2	 5	 µA µA µA
f_{OSC}	Switching Frequency		1.3	1.5	1.7	MHz
f_{SYNC}	SYNC Capture Range		0.75		2.25	MHz
R_{PFET}	$R_{DS(ON)}$ of P-Channel FET	I_{SW} = 100mA		32	40	mΩ
R_{NFET}	$R_{DS(ON)}$ of N-Channel FET	I_{SW} = 100mA		25	32	mΩ
I_{LIMIT}	Peak Current Limit	V_{ITH} = 1V (Note 6)	11	13	15	A
V_{UVLO}	Undervoltage Lockout Threshold	SV_{IN} Rising SV_{IN} Falling	2.05 1.85	2.2 2.0	2.35 2.15	V V
I_{LSW}	SW Leakage Current	V_{RUN} = 0V, V_{IN} = 5.5V		0.1	5	µA
SS Delay	Internal Soft-Start Delay			140		µs
g_m	Error Amplifier's Transconductance		1.7	2	2.2	mmho
RUN	Run Input Threshold	RUN Rising RUN Falling	1.4 1.2	1.5 1.3	1.6 1.4	V V
PGOOD Delay	PGOOD Falling Edge Delay			35		µs
$\%_{MARGINING}$	Output Voltage Margining Percentage	MGN HI, BSEL LOW MGN HI, BSEL HI MGN HI, BSEL = SV_{IN}/2 MGN LOW, BSEL LOW MGN LOW, BSEL HI MGN LOW, BSEL = SV_{IN}/2	3 8 13 –3 –8 –13	5 10 15 –5 –10 –15	7 12 17 –7 –12 –17	% % % % % %
TRACK	Tracking Threshold (Rising) Tracking Threshold (Falling) Tracking Disable Threshold	RUN = V_{IN} RUN = 0V		0.57 0.18 V_{IN} – 0.5		V V V
V_{FB} Slavemode	V_{FB} Slavemode (EA Disable) Threshold			V_{IN} – 0.5		V
I_{TH} Internal	Switch Over Threshold for Internal Compensation			V_{IN} – 0.5		V
OV	Output Overvoltage Threshold	V_{FB} Rising	7	10	13	%
UV	Output Undervoltage Threshold	V_{FB} Falling	–7	–10	–13	%
V_{HYST}	OV/UV Hysteresis	V_{FB} Returning to Regulation		1	3	%

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3415E is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: The LTC3415 is tested in a feedback loop that adjusts V_{FB} to achieve a specified error amplifier output voltage (I_{TH}).

Note 4: Dynamic supply current is higher due to the internal gate charge being delivered at the switching frequency.

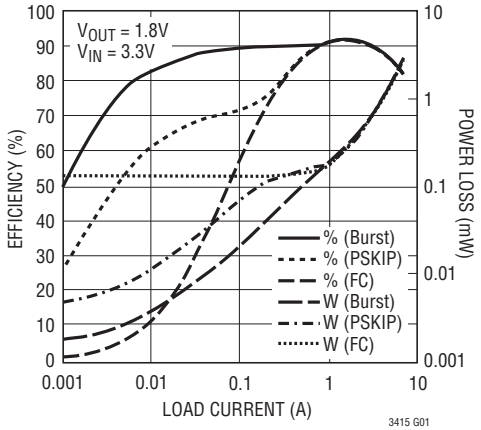
Note 5: T_J is calculated from the ambient temperature T_A and power dissipation as follows: LTC3415: $T_J = T_A + P_D$ (34°C/W).

Note 6: Current Limit is measured with internal servo loop while forcing V_{ITH} = 1V.

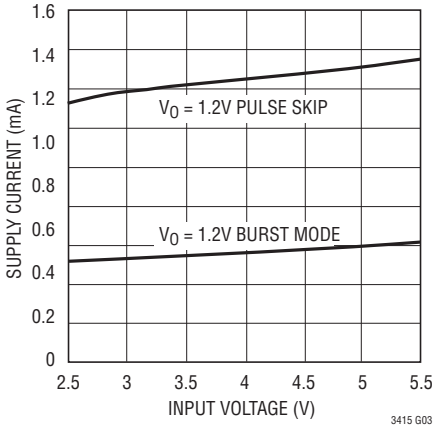
Note 7: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

TYPICAL PERFORMANCE CHARACTERISTICS

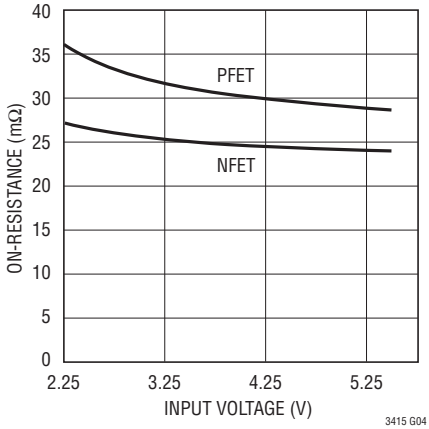
Efficiency and Power Loss vs Load Current (3 Operating Modes) (Reference Figure 13)



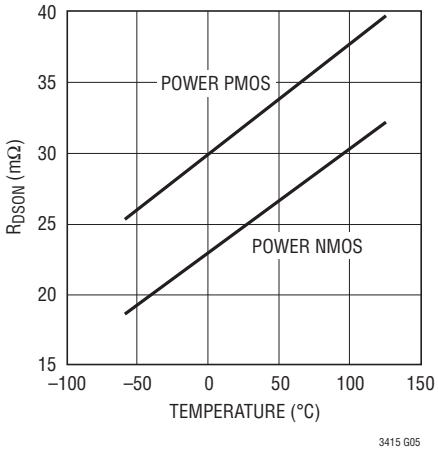
Supply Current vs V_{IN}



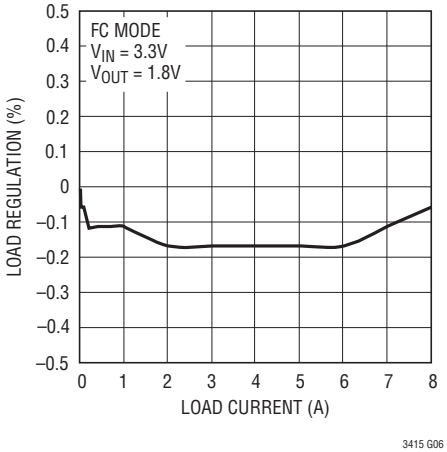
R_{DSON} vs V_{IN}



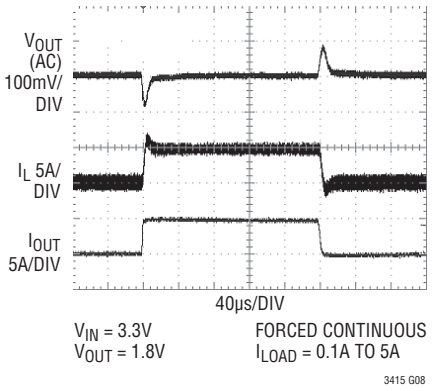
R_{DSON} vs Temperature



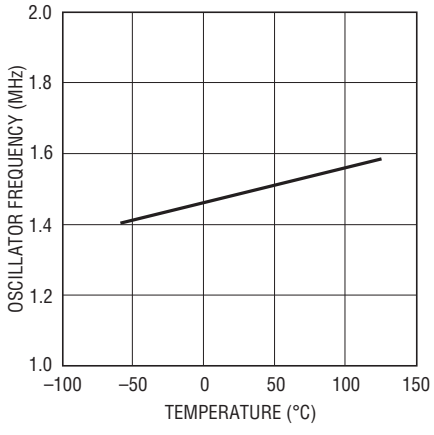
Load Regulation (Reference Figure 13)



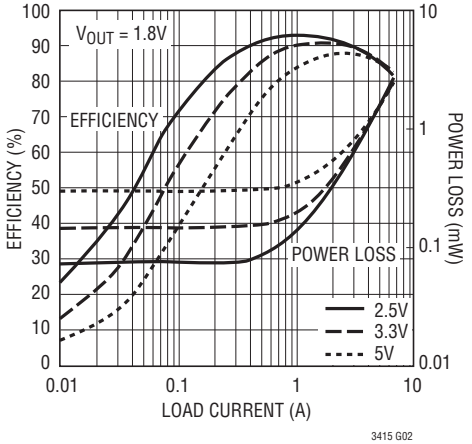
Load Step (Reference Figure 13)



Oscillator Frequency vs Temperature

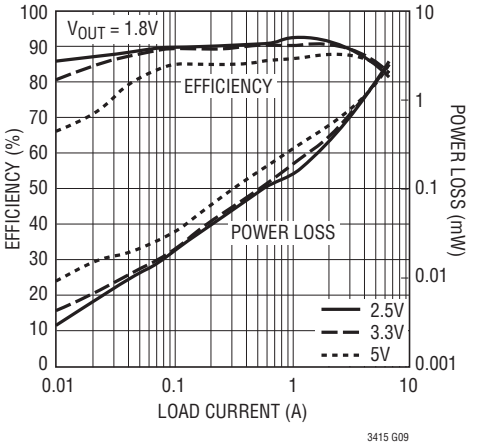


Efficiency and Power Loss vs Load Current Force Continuous Mode

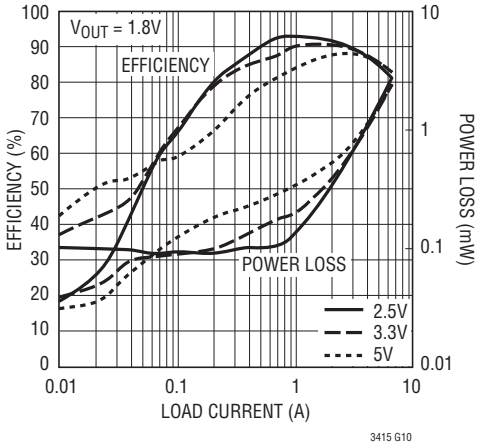


TYPICAL PERFORMANCE CHARACTERISTICS

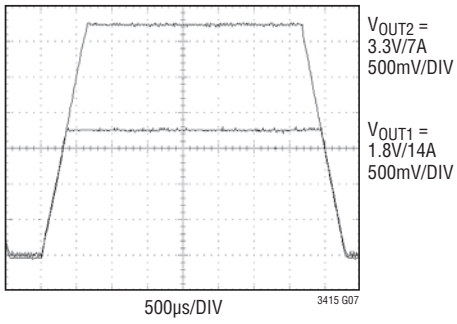
Efficiency and Power Loss
Burst Mode Operation



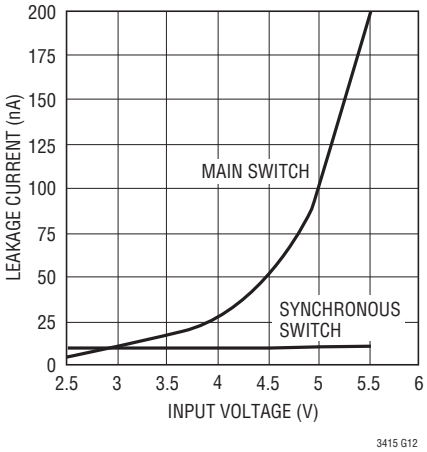
Efficiency and Power Loss
Pulse-Skip Mode Operation



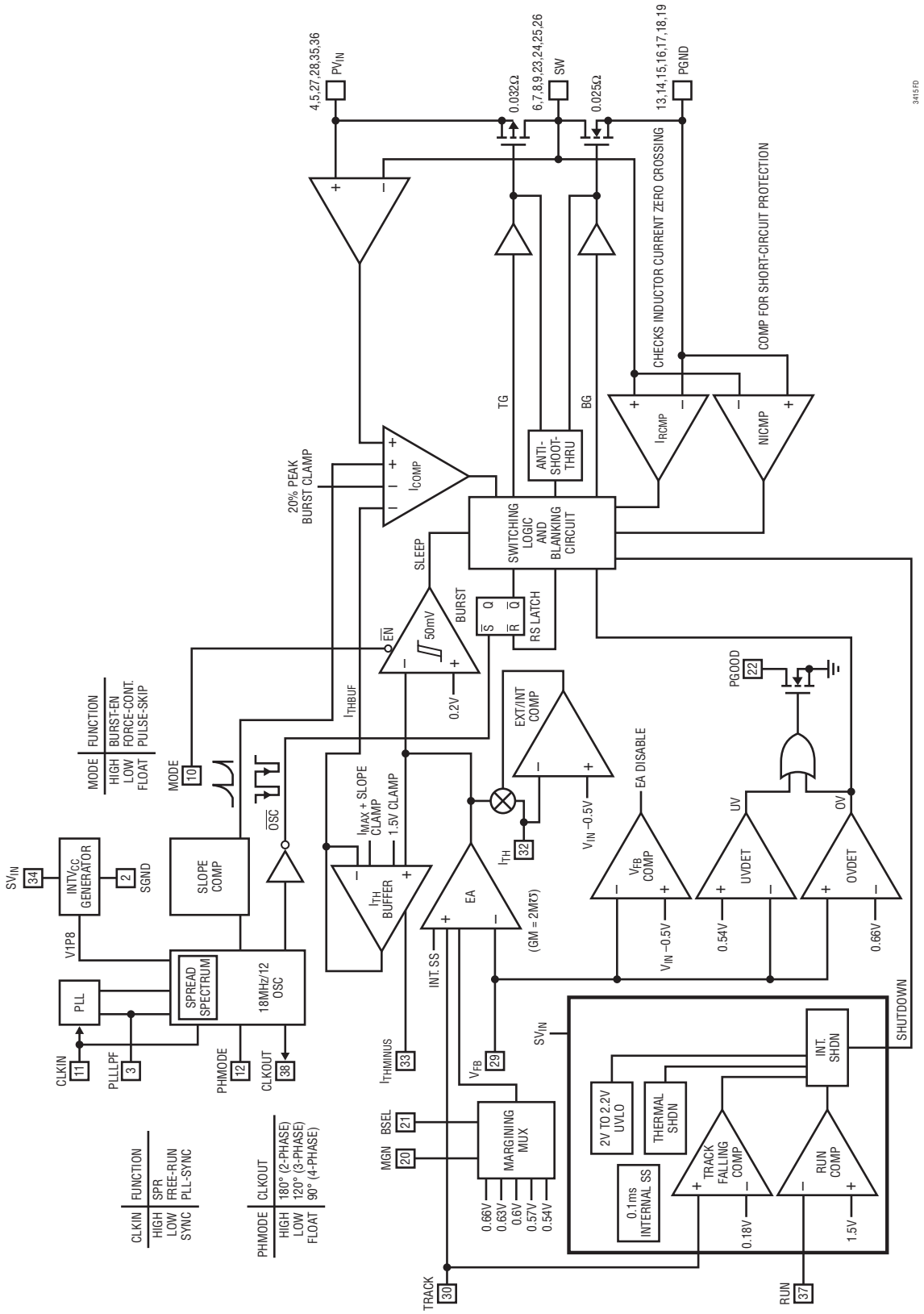
Output Tracking



Switch Leakage Current
vs Input Voltage



FUNCTIONAL DIAGRAM



PIN FUNCTIONS

SGND (Pin 2): Signal Ground. Return ground path for all analog and low power circuitry. Single connection to PGND on system board.

PLLLPF (Pin 3): Phase-Locked-Loop Lowpass Filter. The PLL's lowpass filter is tied to this pin. In spread spectrum mode, placing a capacitor here to SGND controls the slew rate from one frequency to the next. Alternatively, floating this pin allows normal running frequency at 1.5MHz, tying this pin to SV_{IN} forces the part to run at 1.33 times its normal frequency (2MHz), tying it to ground forces the frequency to run at 0.67 times its normal frequency (1MHz).

PV_{IN} (Pins 4, 5, 27, 28, 35, 36): Power V_{IN}. Input voltage to the on chip power MOSFETs. Must be closely decoupled to PGND.

SW (Pins 6, 7, 8, 9, 23, 24, 25, 26): Switch Node Connection to the Inductor. This pin swings from PV_{IN} to PGND.

MODE (Pin 10): Mode Select Input. Tying this pin high enables Burst Mode operation. Tying this pin low enables force continuous operation. Tying it to $V_{IN}/2$ enables pulse-skipping operation.

CLKIN (Pin 11): External Synchronization Input to Phase Detector. This pin is internally terminated to SGND with a 50k resistor. The phase-locked-loop will force the internal top power PMOS turn on to be synchronized with the rising edge of the CLKIN signal. Connect this pin to SV_{IN} to enable spread spectrum modulation. During external synchronization, make sure the PLLLPF pin is not tied to V_{IN} or GND.

PHMODE (Pin 12): Phase Selector Input. This pin determines the phase relationship between the internal oscillator and CLKOUT. Tie it high for 2-phase operation, tie it low for 3-phase operation, and tie it to $V_{IN}/2$ for 4-phase operation.

PGND (Pins 13-19): Power Ground. Return path of internal N-channel power MOSFETs. Connect this pin with the (–) terminals of C_{IN} and C_{OUT}.

MGN (Pin 20): Margining Pin. Tying this pin to a voltage between 0.5V and SV_{IN} – 0.5V disables the margining function and allows normal operation. Tying it high enables positive margining (5, 10, or 15%). Tying it low enables negative margining (–5, –10, or –15%).

BSEL (Pin 21): Margining Bit Select Pin. Tying BSEL low selects ±5%, tying it high selects ±10%. Tying it to $V_{IN}/2$ selects ±15%.

PGOOD (Pin 22): Output Power GOOD with Open-Drain Logic. PGOOD is pulled to ground when the voltage on the V_{FB} pin is not within ±10% of its set point. Disabled during margining and during slave mode operation (V_{FB} tied to V_{IN}).

V_{FB} (Pin 29): Input to the error amplifier that compares the feedback voltage to the internal 0.6V reference voltage. This pin is normally connected to a resistive divider from the output voltage. In PolyPhase operation, tying V_{FB} to SV_{IN} disables its own internal error amplifier and connects the master's I_{TH} voltage to its current comparator.

TRACK (Pin 30): Track Input Pin. This allows the user to control the rise time of the output. Putting a voltage below 0.57V on this pin bypasses the reference input into the error amplifier and servos the V_{FB} pin to the TRACK voltage. Above 0.57V, the tracking function stops and the internal reference again controls the error amplifier. During shutdown, if TRACK is not tied to SV_{IN}, then TRACK's voltage needs to be below 0.18V before the chip shuts down even though RUN is already low. Do not float this pin.

I_{TH} (Pin 32): Error Amplifier Output and Switching Regulator Compensation Point. The current comparator's threshold increases with this control voltage. The normal voltage range of this pin is from 0V to 1.5V. It's also the positive input to the internal I_{TH} differential amplifier. Tying I_{TH} to SV_{IN} enables the internal compensation.

I_{THM} (Pin 33): Negative Input to the Internal I_{TH} Differential Amplifier. Tie this pin to SGND for single phase operation. For PolyPhase, tie the master's I_{THM} to SGND while connecting all of the I_{THM} pins together.

SV_{IN} (Pin 34): Signal Input Voltage. Connect this pin to PV_{IN} through a 1Ω and 0.1µF lowpass filter.

RUN (Pin 37): Run Control Input. Tying this pin above 1.5V turns on the part.

CLKOUT (Pin 38): Output Clock Signal for PolyPhase Operation. The phase of CLKOUT is determined by the state of the PHMODE pin.

Exposed Pad (Pin 39): Power Ground. Must be connected to electrical ground on PCB.

OPERATION

Main Control Loop

The LTC3415 is a constant frequency, current mode, monolithic step down regulator. In normal operation, the internal top P-channel power MOSFET turns on each cycle when the oscillator sets the RS latch, and turns off when the current comparator I_{COMP} resets the RS latch. The peak inductor current at which I_{COMP} resets the RS latch is controlled by the voltage on the I_{TH} pin, which is the output of error amplifier EA. The FB pin allows EA to receive an output feedback voltage from an external resistive divider. When the load current increases, it causes a slight decrease in the feedback voltage relative to the 0.596V reference, which in turn causes I_{TH} voltage to increase until the average inductor current matches the new load current. While the top P-channel power MOSFET is off, the bottom N-Channel power MOSFET is turned on until either the inductor current starts to reverse, as indicated by the current reversal comparator I_{RCMP} or the beginning of the next cycle.

The main control loop is shut down by pulling the RUN pin below 1.5V ($V_{TRACK} = SV_{IN}$ or $V_{TRACK} < 0.18V$). Tying RUN higher than 1.5V allows operation to begin. To control the rise time of the output, a voltage ramp can be applied to the TRACK pin. The FB voltage will servo to the TRACK voltage until TRACK goes above 0.57V, which is when PGOOD is high and the output is in normal regulation. If TRACK is not used (tied high), then an internal 100µs soft-start will ramp up the output.

Burst Mode Operation

The LTC3415 is capable of Burst Mode operation in which the power MOSFETs operate intermittently based on load demand, thus saving quiescent current. For applications where maximizing the efficiency at very light loads is a high priority, Burst Mode operation should be applied. To enable Burst Mode operation, simply tie the MODE pin to V_{IN}. During this operation, the peak current of the inductor is set to approximately 20% of the maximum peak current value in normal operation even though the voltage at the I_{TH} pin indicates a lower value. The voltage at the I_{TH} pin drops when the inductor's average current is greater than the load requirement. As the I_{TH} voltage drops below 0.2V, the BURST comparator trips, causing the internal sleep line to go high and turn off both power MOSFETs.

In sleep mode, the internal circuitry is partially turned off, reducing the quiescent current to about 450µA. The load current is now being supplied from the output capacitor. When the output voltage drops, causing I_{TH} to rise above 0.25V, the internal sleep line goes low, and the LTC3415 resumes normal operation. The next oscillator cycle will turn on the top power MOSFET and the switching cycle repeats.

Pulse-Skipping Mode Operation

In applications where fixed frequency operation, low output ripple and high efficiency at intermediate current is desired, pulse-skipping mode should be used. Pulse-skipping operation allows the LTC3415 to skip cycles at low output loads, thus increasing efficiency by reducing switching current. Tying the MODE pin to $V_{IN}/2$ enables pulse-skipping operation. This allows discontinuous conduction mode (DCM) operation down to near the limit defined by the chip's minimum on-time (about 100ns). Below this output current level, the converter will begin to skip cycles in order to maintain output regulation. Increasing the output load current slightly, above the minimum required for discontinuous conduction mode, allows constant frequency PWM.

Forced Continuous Operation

In applications where fixed frequency operation is more critical than low current efficiency, and where the lowest output ripple is desired, forced continuous operation should be used. Forced continuous operation can be enabled by tying the MODE pin to GND. In this mode, inductor current is allowed to reverse during low output loads, the I_{TH} voltage is in control of the current comparator threshold throughout, and the top MOSFET always turns on with each oscillator pulse. During start-up, forced continuous mode is disabled and inductor current is prevented from reversing until the LTC3415's output voltage is in regulation.

OPERATION

Short-Circuit Protection

When the output is shorted to ground, the LTC3415 will drop cycles to allow the inductor time to decay and prevent the current from running away. Under this fault condition, the top P-channel power MOSFET turns on for a minimum on-time and is held off for as long as it takes for the inductor current to decay to a safe level.

Output Overvoltage

If the LTC3415's output voltage exceeds the regulation point by 10%, which is reflected as a V_{FB} voltage of 0.66V or above, the LTC3415 will attempt to bring back to regulation by shutting off the top P-channel power MOSFET and turning on the bottom N-Channel power MOSFET for as long as needed to lower V_{OUT}. However, if the reverse current flowing from V_{OUT} back through the bottom N-Channel power MOSFET to PGND is greater than 7A, the INEGLIM comparator trips and shuts off the bottom N-Channel power MOSFET to protect it from being destroyed. This scenario can happen when the LTC3415 tries to start into a pre-charged load, which could trigger the overvoltage comparator during the time the LTC3415's internal reference is powering up. As a result, the bottom switch turns on until the amount of reverse current trips the INEGLIM comparator threshold.

Multiphase Operation

For output loads that demand more than 7A of current, multiple LTC3415s can be cascaded to run out of phase to provide more output current without increasing input and output voltage ripple. The CLKIN pin allows the LTC3415 to synchronize to an external clock (between 0.75MHz and 2.25MHz) and the internal phase-locked-loop allows the LTC3415 to lock onto CLKIN's phase as well. The CLKOUT signal can be connected to the CLKIN pin of the following LTC3415 stage to line up both the frequency and the phase of the entire system. Tying the PHMODE pin to SV_{IN}, SGND, or $SV_{IN}/2$ generates a phase difference (between CLKIN and CLKOUT) of 180 degrees, 120 degrees, or 90 degrees respectively, which corresponds to 2-phase, 3-phase, or 4-phase operation. A total of 12 phases can be cascaded to run simultaneously out of phase with respect to each

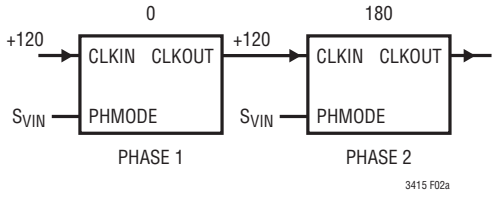


Figure 2a. 2-Phase Operation

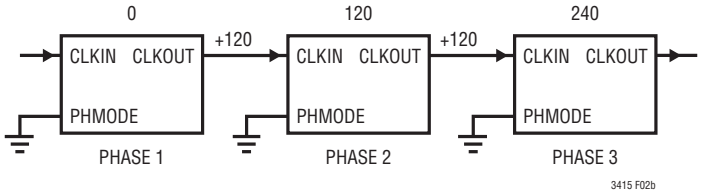


Figure 2b. 3-Phase Operation

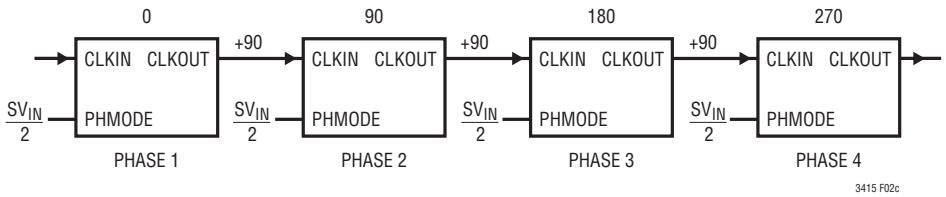


Figure 2c. 4-Phase Operation

OPERATION

other by programming the PHMODE pin of each LTC3415 to different levels. For example, a slave stage that is 180 degrees out of phase from the master can generate a CLKOUT signal that is 300 degrees (PHMODE = 0) away from the master for the next stage, which then can generate a CLKOUT signal that's 420, or 60 degrees (PHMODE = SV_{IN}/2) away from the master for its following stage.

Refer to Figure 2 for configurations of 2-phase, 3-phase, 4-phase, 6-phase and 12-phase operation.

A multiphase power supply significantly reduces the amount of ripple current in both the input and output capacitors. The RMS input ripple current is divided by, and the effective ripple frequency is multiplied by, the number of phases used (assuming that the input voltage is greater than the number

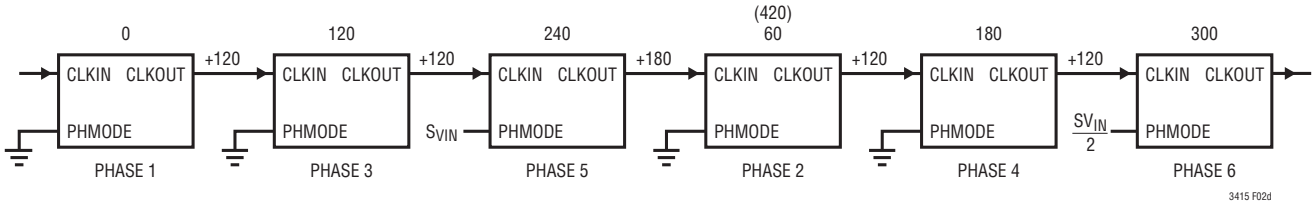


Figure 2d. 6-Phase Operation

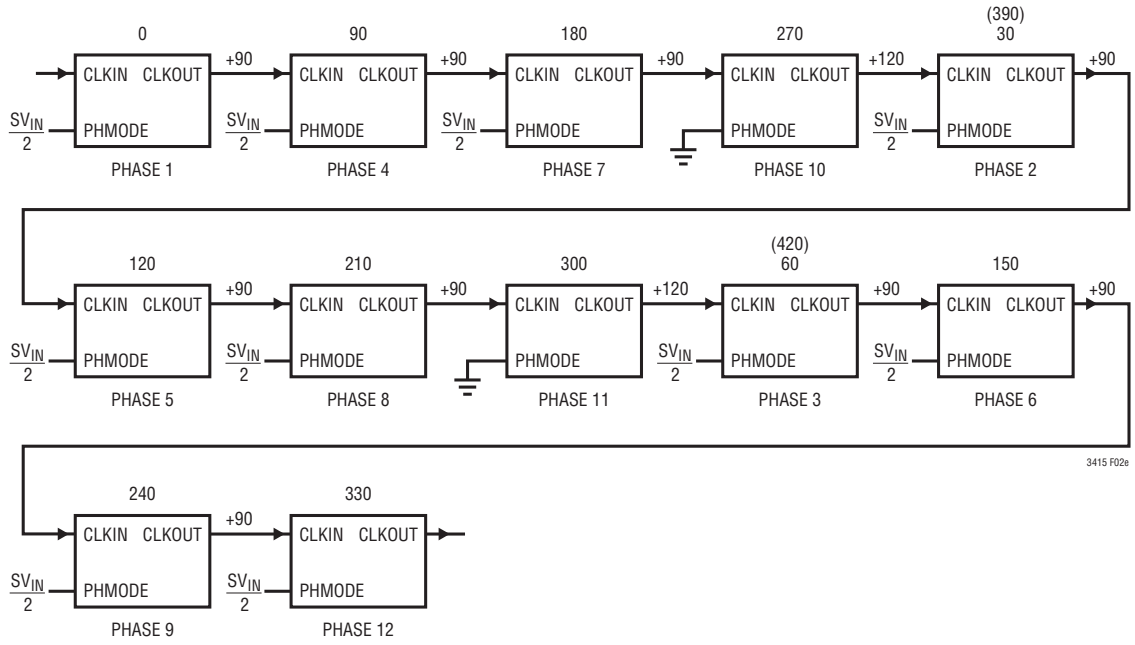


Figure 2e. 12-Phase Operation

OPERATION

of phases used times the output voltage). The output ripple amplitude is also reduced by the number of phases used. Figure 3 graphically illustrates the principle.

The worst-case RMS ripple current for a single stage design peaks at an input voltage of twice the output voltage. The worst case RMS ripple current for a two stage design results in peak outputs of 1/4 and 3/4 of input voltage. When the RMS current is calculated, higher effective duty factor results and the peak current levels are divided as long as the current in each stage is balanced. Refer to Application Note 19 for a detailed description of how to calculate RMS current for the single stage switching regulator. Figures 4 and 5 illustrate how the input and output currents are reduced by using an additional phase. For a 2-phase converter, the input current peaks drop in half and the frequency is doubled. The input capacitor requirement is thus reduced theoretically by a factor of four! Just imagine the possibility of capacitor savings with even higher number of phases!

Output Current Sharing

When multiple LTC3415s are cascaded to drive a common load, accurate output current sharing is essential to achieve optimal performance and efficiency. Otherwise, if one stage is delivering more current than another, then the temperature between the two stages will be different, and that could translate into higher switch $R_{DS(ON)}$, lower efficiency, and higher RMS ripple. Each LTC3415 is trimmed such that when the I_{TH} pins of multiple LTC3415s are tied together, the amount of output current delivered from each LTC3415 is nearly the same.

Different ground potentials among LTC3415 stages, caused by physical distances and ground noises, could cause an offset to the absolute I_{TH} value seen by each stage. To ensure that the ground level doesn't affect the I_{TH} value, the LTC3415 uses a differential driver that takes as input not just the I_{TH} pin, but also the I_{THM} pin. The I_{THM} pins of all the LTC3415 stages should be tied together and then connected to the SGND at only one point.

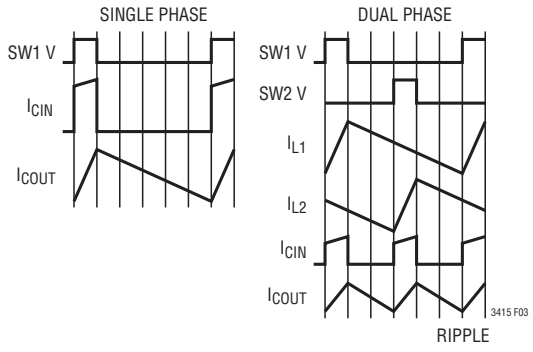


Figure 3. Single and 2-Phase Current Waveforms

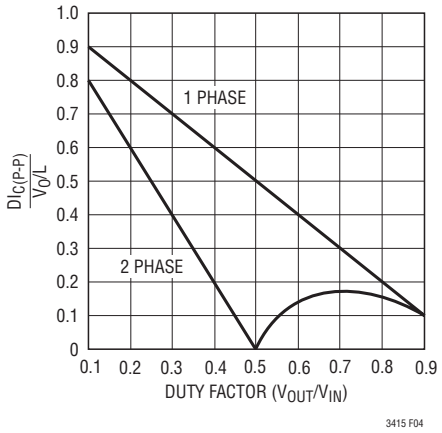


Figure 4. Normalized Output Ripple Current vs Duty Factor [I_{RMS} ≈ 0.3 ($DI_{C(PP)}$)]

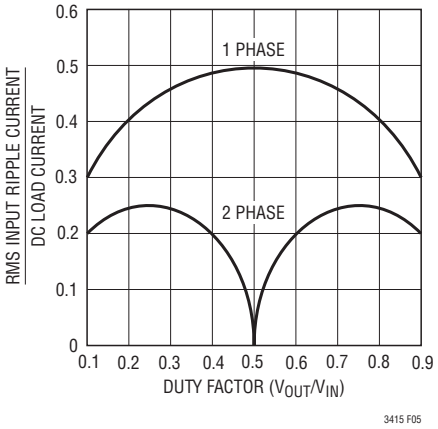


Figure 5. Normalized RMS Input Ripple Current vs Duty Factor for 1 and 2 Output Stages

OPERATION

Phase-Locked-Loop Operation

In order to synchronize to an external signal, the LTC3415 has an internal phase-locked-loop comprised of an internal voltage controlled oscillator and phase detector. This allows the top P-channel power MOSFET turn-on to be locked to the rising edge of an external source. The frequency range of the voltage controlled oscillator is ±50% around the center frequency. Leaving the PLLLPF pin floating corresponds to a free-running frequency of approximately 1.5MHz. Tying PLLLPF directly to SV_{IN} corresponds to 1.33x of center frequency (2MHz) while tying PLLLPF to ground corresponds to 0.67x of center frequency (1MHz).

The phase detector used is an edge sensitive digital type which provides zero degree phase shift between the external and internal oscillators. The output of the phase detector is a complementary pair of current sources charging or discharging the external filter network on the PLLLPF pin. See Figure 6.

If the external frequency, CLKIN, is greater than the oscillator frequency f_{OSC}, current is sourced continuously, pulling up the PLLLPF pin. When the external frequency is less than f_{OSC}, current is sunk continuously, pulling down the PLLLPF pin. If the external and internal frequencies are the same but exhibit a phase difference, the current sources turn on for an amount of time corresponding to the phase difference. Thus the voltage on the PLLLPF pin is adjusted until the phase and frequency of the external and internal oscillators are identical. The CLKIN pin must be driven from a low impedance source such as a logic gate located close to the pin. The loop filter components (C_{LP}, R_{LP}) smooth out the current pulses from the phase detector and provide a stable input to the voltage controlled oscillator. The filter components determine how fast the loop acquires lock. Typically R_{LP} = 10k and C_{LP} is 100pf to 1000pf.

The CLKOUT pin provides a signal to synchronize following stages of LTC3415s. Its amplitude is 0V to 2V and its phase with respect to the internal oscillator (or CLKIN) is controlled by the PHMODE pin.

Internal/External I_{TH} Compensation

During single phase operation, the user can simplify the loop compensation by tying the I_{TH} pin to SV_{IN} to enable internal compensation. This connects an internal 50k resistor in series with a 50pF cap to the output of the error amplifier (internal I_{TH} compensation point). This is a trade-off for simplicity instead of OPTI-LOOP® optimization, where I_{TH} components are external and are selected to optimize the loop transient response with minimum output capacitance. See Checking Transient Response in the Applications Information section.

OPTI-LOOP is a registered trademark of Linear Technology Corporation.

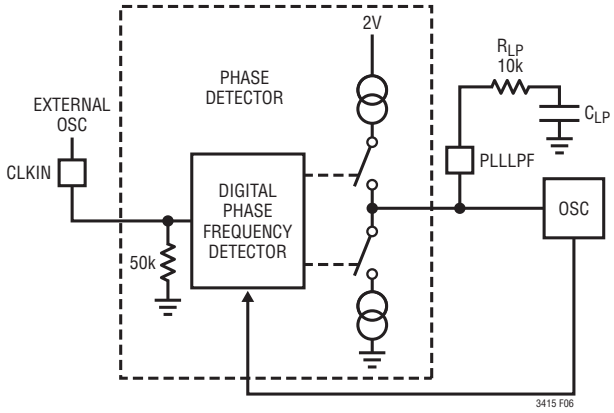


Figure 6. Phase-Locked-Loop Block Diagram

OPERATION

In multiphase operation where all the I_{TH} pins of each LTC3415 are tied together to achieve accurate load sharing, internal compensation is not allowed. External compensation components need to be properly selected for optimal transient response and stable operation.

Master/Slave Operation

In multiphase single-output operation, the user has the option to run in multi-master mode where all the V_{FB}, I_{TH}, and output pins of the stages are tied to each other. All the error amplifiers are effectively operating in parallel and the total g_m of the system is increased by the number of stages. The I_{TH} value, which dictates how much current is delivered to the load from each stage, is averaged and smoothed out by the external I_{TH} compensation components. However, in certain applications, the resulting higher g_m from multiple LTC3415s can make the system loop harder to compensate. In this case, the user can choose an alternative mode of operation.

The second mode of operation is single-master operation where only the error amplifier of the master stage is used while the error amplifiers of the other stages (slaves) are disabled. The slave's error amplifier is disabled by tying its V_{FB} pin to SV_{IN}, which also disables the internal overvoltage comparator and power-good indicator. The master's error amplifier senses the output through its V_{FB} pin and drives the I_{TH} pins of all the stages. To account for ground voltage differences among the stages, the user should tie all I_{THM} pins together and then tie it to the master's signal ground. As a result, not only is it easier to do loop compensation, this single-master operation should also provide for more accurate current sharing among stages because it prevents the error amplifier's output (I_{TH}) of each stage from interfering with that of another stage.

Spread Spectrum Operation

Switching Regulators can be particularly troublesome where electromagnetic interference (EMI) is concerned. Switching regulators operate on a cycle-by-cycle basis to transfer power to an output. In most cases, the frequency of operation is fixed or is a constant based on the output load. This method of conversion creates large components of noise at the frequency of operation (fundamental) and multiples of the operating frequency (harmonics).

To reduce this noise, the LTC3415 can run in spread spectrum operation by tying the CLKIN pin to SV_{IN}. In spread spectrum operation, the LTC3415's internal oscillator is designed to produce a clock pulse whose period is random on a cycle-by-cycle basis but fixed between 70% and 130% of the nominal frequency. This has the benefit of spreading the switching noise over a range of frequencies, thus significantly reducing the peak noise. Figures 7 and 8 show how the spread spectrum feature of the LTC3415 significantly reduces the peak harmonic

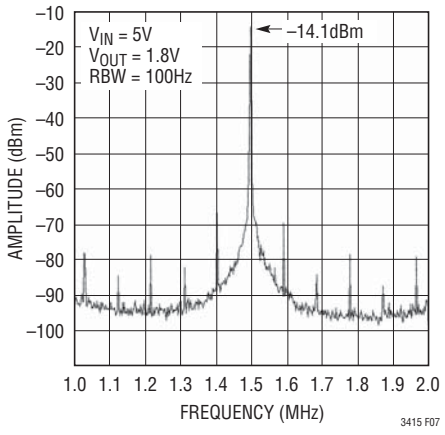


Figure 7. LTC3415's Output Noise Spectrum Analysis in Free-Running Constant Frequency Operation

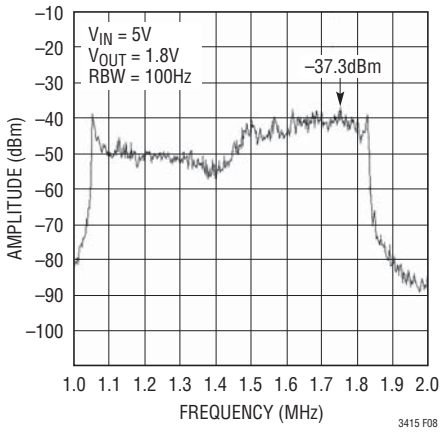


Figure 8. LTC3415's Output Noise Spectrum Analysis in Spread Spectrum Operation

OPERATION

noise vs free-running constant frequency operation. Spread spectrum operation is disabled if CLKIN is tied to ground or if it's driven by an external frequency synchronization signal.

Dropout Operation

When the input supply voltage decreases toward the output voltage, the duty cycle will increase toward the maximum on-time. Further reduction of the supply voltage forces the P-channel power MOSFET to remain on for more than one cycle until it reaches 100% duty cycle. The output voltage will then be determined by the input voltage minus the voltage drop across the P-channel power MOSFET and the inductor.

Slope Compensation and Inductor Peak Current

Slope compensation provides stability by preventing subharmonic oscillations. It works by internally adding a ramp to the inductor current signal at duty cycles in excess of 30%. This causes the internal current comparator to trip earlier. The I_{TH} clamp is also reached earlier than conditions in which the duty cycle is below 30%. As a result, the maximum inductor peak current is lower for higher duty cycle operations.

To compensate for this loss in maximum inductor peak current during high duty cycles, the LTC3415 uses a patented scheme that raises the I_{TH} clamp level (proportional to the amount of slope compensation) when the duty cycle is greater than 30%.

Minimum On-Time Considerations

Minimum on-time, $t_{ON(MIN)}$, is the smallest amount of time that the LTC3415 is capable of turning the top P-channel power MOSFET on and off again. It is determined by the internal timing delays. The minimum on-time for the LTC3415 is about 100ns. Low duty cycle and high frequency applications may approach this minimum on-time limit and care should be taken to ensure that:

$$t_{ON(MIN)} < \frac{V_{OUT}}{(f \bullet V_{IN})}$$

If the duty cycle falls below what can be accommodated by the minimum on-time, the LTC3415 will begin to skip cycles. The output voltage will continue to be regulated, but the ripple current and ripple voltage will increase.

If an application can operate close to the minimum on-time limit, an inductor must be chosen that has low enough inductance to provide sufficient ripple amplitude to meet the minimum on-time requirement. As a general rule, keep the inductor ripple current equal or greater than 30% of the $I_{OUT(MAX)}$ at $V_{IN(MAX)}$.

Output Margining

For a convenient system stress test on the LTC3415's output, the user can program the LTC3415's output to ±5%, ±10% or ±15% of its normal operational voltage.

The MGN pin, when connected to a voltage between 0.5V and SV_{IN} – 0.SV allows normal operation. When the MGN pin is low, it forces negative margining, in which the output voltage is below the regulation point. When MGN is high, the output voltage is forced to above the regulation point. The amount of output voltage margining is determined by the BSEL pin. When BSEL is low, it's 5%. When BSEL is high, it's 10%. When BSEL is V_{IN}/2, it's 15%. When margining is active, the internal output overvoltage and undervoltage comparators are disabled and PGOOD remains high.

Output Power-Good

When the LTC3415's output voltage is within a ±10% window of the regulation point, which is reflected back as a V_{FB} voltage in the range of 0.54V to 0.66V, the output voltage is good and the PGOOD pin is pulled high with the external resistor.

OPERATION

Otherwise, an internal open-drain pull down device (20Ω) will pull the PGOOD pin low. In certain computer systems today, the PGOOD pin is used as a resetting signal while the output voltage is dynamically changed from one level to another. To prevent unwanted power resetting during output voltage changes, the LTC3415's PGOOD falling and rising edges include a blanking delay equivalent to approximately 10µs per every volt of V_{IN}.

Output Voltage Programming

The output voltage is set by an external resistive divider according to the following equation:

$$V_{OUT} = 0.596V \bullet \left(1 + \frac{R2}{R1}\right)$$

The resistive divider allows pin V_{FB} to sense a fraction of the output voltage as shown in Figure 9.

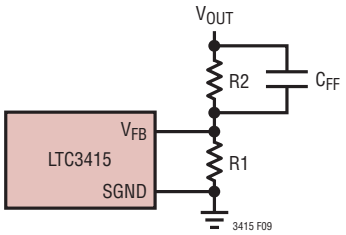


Figure 9. Setting the Output Voltage

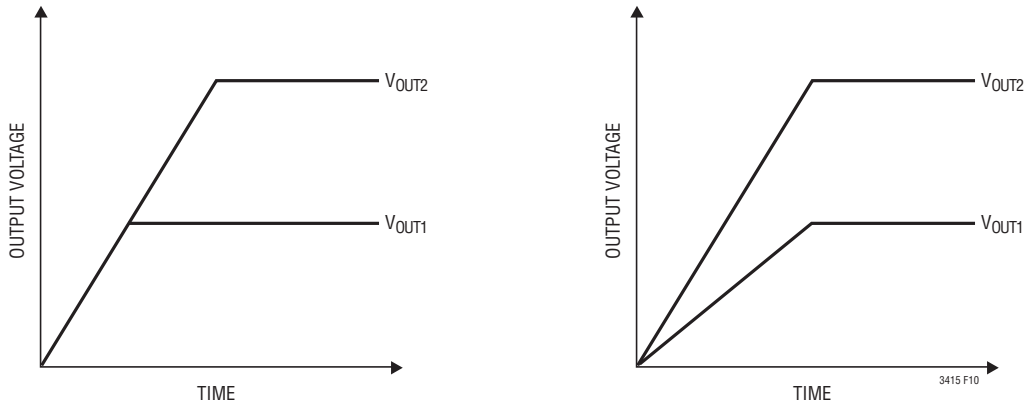
Output Tracking and Sequencing

Some microprocessor, ASIC and DSP chips need two power supplies with different voltage levels. These systems often require voltage sequencing between the core power supply and the I/O power supply. Without proper sequencing, latch-up failure or excessive current draw may occur that could result in damage to the processor's I/O ports or the I/O ports of supporting system devices such as memory, FPGAs or data converters. To ensure that the I/O loads are not driven until the core voltage is properly biased, tracking of the core supply voltage and the I/O supply voltage is necessary.

Voltage tracking is enabled by applying a voltage to the TRACK pin. When the voltage on the TRACK pin is below 0.57V, the feedback voltage will regulate to this tracking voltage. When the tracking voltage exceeds 0.57V, tracking is disabled and the feedback voltage will regulate to the internal reference voltage.

Voltage Tracking

The LTC3415 allows the user to program how its output voltage ramps during start-up by means of the TRACK pin. Through this pin, the output voltage can be set up to either coincidentally or ratiometrically track another output voltage as shown in Figure 10.



(10a) Coincident Tracking **(10b) Ratiometric Sequencing**

Figure 10. Two Different Modes of Output Voltage Sequencing

OPERATION

If the voltage on the TRACK pin is less than 0.57V, voltage tracking is enabled. During voltage tracking, the output voltage is regulated by the tracking voltage through a resistive divider network. The output voltage during tracking can be calculated with the following equation:

$$V_{OUT} = V_{TRACK}\left(1+\frac{R2}{R1}\right), V_{TRACK} < 0.57V$$

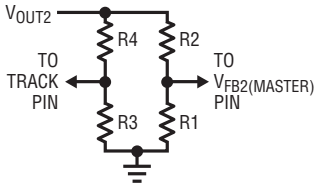
Voltage tracking can be accomplished by sensing a fraction of the output voltage from another regulator. This is typically done by using a resistive divider to attenuate the output voltage that is being tracked. Setting this resistive divider equal to the feedback resistive divider will force the regulator outputs to be equal to each other during tracking. If tracking is not desired, connect the TRACK pin to SV_{IN}. Do not leave the TRACK pin floating. To implement the coincident tracking shown in Figure 10a, connect an extra resistive divider to the output of V_{OUT2} and connect its midpoint to the TRACK pin of the LTC3415 as shown in Figure 11. The ratio of this divider should be selected the same as that of V_{OUT1}'s resistive divider. To implement the ratiometric sequencing in Figure 10b, no extra resistive divider is necessary. Simply connect the TRACK pin to V_{FB} of the master.

An alternative method of tracking is shown in Figure 12. For the circuit of Figure 12, the following equations can be used to determine the resistor values:

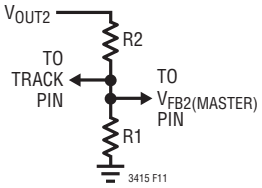
$$V_{OUT1} = 0.596V\left(1+\frac{R2}{R1}\right)$$

$$V_{OUT2} = 0.596V\left(1+\frac{R4+R5}{R3}\right)$$

$$R4 = R3\left(\frac{V_{OUT2}}{V_{OUT1}}-1\right)$$



(11a) Coincident Tracking Setup



(11b) Ratiometric Setup

Figure 11. Setup for Tracking and Ratiometric Sequencing

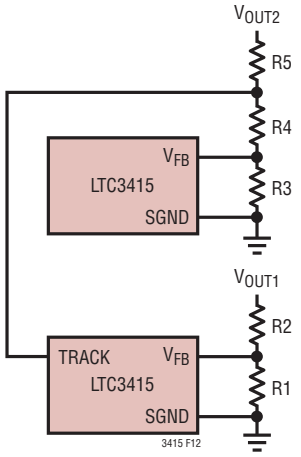


Figure 12. Dual Voltage System with Tracking

OPERATION

During ramp down of the output, if the TRACK pin is not tied to V_{IN}, then the LTC3415 will maintain normal operation even though the RUN pin is programmed low. Only when the TRACK pin is below 0.18V will the RUN signal be gated through internally and shut down the part. This way, coincident tracking and ratiometric sequencing of the two outputs are accomplished during both start-up and shutdown. An output current load, however, needs to be present during this time in order to discharge the output because when TRACK is below 0.57V, forced continuous operation is not allowed and inductor current, therefore, is prevented from going negative.

For applications that do not require tracking or sequencing, simply tie the TRACK pin to SV_{IN} to let RUN control the turn on/off of the LTC3415. Connecting TRACK to SV_{IN} also enables the ~100µs of internal soft-start during start-up.

APPLICATIONS INFORMATION

C_{IN} and C_{OUT} Selection

The input capacitance, C_{IN}, is needed to filter the trapezoidal wave current at the source of the top MOSFET. To prevent large voltage transients from occurring, a low ESR input capacitor sized for the maximum RMS current should be used. The maximum RMS current is given by:

$$I_{RMS} \cong I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required.

Several capacitors may also be paralleled to meet size or height requirements in the design. For low input voltage applications, sufficient bulk input capacitance is needed to minimize transient effects during output load changes.

The selection of C_{OUT} is determined by the effective series resistance (ESR) that is required to minimize voltage ripple and load step transients as well as the amount of bulk capacitance that is necessary to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response. The output ripple, ΔV_{OUT}, is determined by:

$$\Delta V_{OUT} \leq \Delta I_L \left(ESR + \frac{1}{8fC_{OUT}} \right)$$

The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic, and ceramic capacitors are all available in surface mount packages. Special polymer capacitors offer very low ESR but have lower capacitance density than other types. Tantalum capacitors have the highest capacitance density but it is important to only use types that have been surge tested for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR, but can be used in cost-sensitive applications provided that consideration is given to ripple current ratings and long term reliability. Ceramic capacitors have excellent low ESR characteristics and small footprints. Their relatively low value of bulk capacitance may require multiples in parallel.

Using Ceramic Input and Output Capacitors

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at the input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the V_{IN} input. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part.

When choosing the input and output ceramic capacitors, choose the X5R or X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.

APPLICATIONS INFORMATION

Inductor Selection

Given the desired input and output voltages, the inductor value and operating frequency determine the ripple current:

$$\Delta I_L = \left(\frac{V_{OUT}}{fL}\right)\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

Lower ripple current reduces cores losses in the inductor, ESR losses in the output capacitors, and output voltage ripple. Highest efficiency operation is obtained at low frequency with small ripple current. However, achieving this requires a large inductor. There is a tradeoff between component size, efficiency, and operating frequency.

A reasonable starting point is to choose a ripple current that is about 40% of $I_{OUT(MAX)}$. Note that the largest ripple current occurs at the highest V_{IN}. To guarantee that ripple current does not exceed a specified maximum, the inductance should be chosen according to:

$$L = \left(\frac{V_{OUT}}{f\Delta I_{L(MAX)}}\right)\left(1-\frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

Once the value for L is known, the type of inductor must be selected. Actual core loss is independent of core size for a fixed inductor value, but is very dependent on the inductance selected. As the inductance increases, core losses decrease. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core losses and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates “hard,” which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and don’t radiate much energy, but generally cost more than powdered iron core inductors with similar characteristics. The choice of which style inductor to use mainly depends on the price versus size requirements and any radiated field/EMI requirements. New designs for surface mount inductors are available from Coiltronics, Coilcraft, Toko, and Sumida.

Checking Transient Response

The OPTI-LOOP compensation allows the transient response to be optimized for a wide range of loads and output capacitors. The availability of the I_{TH} pin not only allows optimization of the control loop behavior but also provides a DC-coupled and AC filtered closed loop response test point. The DC step, rise time and settling at this test point truly reflects the closed loop response. Assuming a predominantly second order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin. The bandwidth can also be estimated by examining the rise time at the pin.

The I_{TH} external components shown in the Figure 12 circuit will provide an adequate starting point for most applications. The series R-C filter sets the dominant pole-zero loop compensation. The values can be modified slightly (from 0.5 to 2 times their suggested values) to optimize transient response once the final PC layout is done and the particular output capacitor type and value have been determined. The output capacitors need to be selected because their various types and values determine the loop feedback factor gain and phase. An output current pulse of 20% to 100% of full load current having a rise time of 1µs to 10µs will produce output voltage and I_{TH} pin waveforms that will give a sense of the overall loop stability without breaking the feedback loop.

APPLICATIONS INFORMATION

Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to $\Delta I_{LOAD} \bullet ESR$, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem.

The initial output voltage step may not be within the bandwidth of the feedback loop, so the standard second order overshoot/DC ratio cannot be used to determine phase margin. The gain of the loop increases with the R and the bandwidth of the loop increases with decreasing C. If R is increased by the same factor that C is decreased, the zero frequency will be kept the same, thereby keeping the phase the same in the most critical frequency range of the feedback loop. In addition, a feed forward capacitor C_F can be added to improve the high frequency response, as shown in Figure 9. Capacitor C_F provides phase lead by creating a high frequency zero with R2 which improves the phase margin.

The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance. For a detailed explanation of optimizing the compensation components, including a review of control loop theory, refer to Linear Technology Application Note 76.

Although a buck regulator is capable of providing the full output current in dropout, it should be noted that as the input voltage V_{IN} drops toward V_{OUT}, the load step capability does decrease due to the decreasing voltage across the inductor. Applications that require large load step capability near dropout should use a different topology such as SEPIC, Zeta, or single inductor, positive buck/boost.

In some applications, a more severe transient can be caused by switching in loads with large (>10µF) input capacitors. The discharged input capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can deliver enough current to prevent this problem, if the switch connecting the load has low resistance and is driven quickly. The solution is to limit the turn-on speed of the load switch driver. A Hot Swap™ controller is designed specifically for this purpose and usually incorporates current limiting, short-circuit protection, and soft-starting.

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

$$\% \text{ Efficiency} = 100\% - (L1 + L2 + l3 + \ldots)$$

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in LTC3415 circuits: 1) LTC3415 V_{IN} current, 2) switching losses, 3) I^2R losses, 4) other losses.

1) The V_{IN} current is the DC supply current given in the Electrical Characteristics which excludes MOSFET driver and control currents. V_{IN} current results in a small (<1%) loss that increases with V_{IN}, even at no-load.

2) The switching current is the sum of the MOSFET driver and control currents. The MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from V_{IN} to ground. The resulting dQ/dt is a current out of V_{IN} that is typically much larger than the DC bias current. In continuous mode, $I_{GATECHG} = f\ (QT + QB)$, where QT and QB are the gate charges of the internal top and bottom MOSFET switches and f is the operating frequency. The gate charge losses are proportional to V_{IN} and thus their effects will be more pronounced at higher supply voltages and higher switching frequencies.

Hot Swap is a trademark of Linear Technology Corporation.

APPLICATIONS INFORMATION

3) I^2R losses are calculated from the DC resistances of the internal switches, R_{SW}, and external inductor, R_L. In continuous mode, the average output current flows through inductor L but is "chopped" between the internal top and bottom switches. Thus, the series resistance looking into the SW pin is a function of both top and bottom MOSFET $R_{DS(ON)}$ and the duty cycle (DC) as follows:

$$R_{SW} = (R_{DS(ON)}\ TOP)(DC) + (R_{DS(ON)}BOT)(1\text{-}DC)$$

The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. Thus, to obtain I^2R losses:

$$I^2R\ losses = I_{OUT}^2(R_{SW} + R_L)$$

4) Other "hidden" losses such as copper trace and internal battery resistances can account for additional efficiency degradations in portable systems. It is very important to include these "system" level losses in the design of a system. The internal battery and fuse resistance losses can be minimized by ensuring that C_{IN} has adequate charge storage and very low ESR at the switching frequency. Other losses including diode conduction losses during dead-time and inductor core losses generally account for less than 2% total additional loss.

Thermal Considerations

In the majority of applications, the LTC3415 does not dissipate much heat due to its high efficiency. However, in applications where the LTC3415 is running at high ambient temperature with low supply voltage and high duty cycles, such as in dropout, the heat dissipated may exceed the maximum junction temperature of the part. If the junction temperature reaches approximately 150°C, both power switches will be turned off and the SW node will become high impedance.

To avoid the LTC3415 from exceeding the maximum junction temperature, the user will need to do some thermal analysis. The goal of the thermal analysis is to determine whether the power dissipated exceeds the maximum junction temperature of the part. The temperature rise is given by:

$$T_{RISE} = P_D \bullet \theta_{JA}$$

where P_D is the power dissipated by the regulator and θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature.

The junction temperature, T_J, is given by:

$$T_J = T_{RISE} + T_{AMBIENT}$$

As an example, consider the case when the LTC3415 is in dropout at an input voltage of 3.3V with a load current of 5A. From the Typical Performance Characteristics graph of Switch Resistance, the $R_{DS(ON)}$ resistance of the P-channel switch is 0.03. Therefore, power dissipated by the part is:

$$P_D = I^2 \bullet R_{DS(ON)} = 750mW$$

The QFN 5mm × 7mm package junction-to-ambient thermal resistance, θ_{JA}, is around 34°C/W. Therefore, the junction temperature of the regulator operating in a 50°C ambient temperature is approximately:

$$T_J = 0.75 \bullet 34 + 50 = 75.5°C$$

Remembering that the above junction temperature is obtained from an $R_{DS(ON)}$ at 25°C, we might recalculate the junction temperature based on a higher $R_{DS(ON)}$ since it increases with temperature. However, we can safely assume that the actual junction temperature will not exceed the absolute maximum junction temperature of 125°C. Solder the LTC3415's bottom exposed pad to ground for optimal thermal performance.

APPLICATIONS INFORMATION

Board Layout Considerations

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3415. Check the following in your layout:

1) Do the capacitors C_{IN} connect to the power PV_{IN} and power PGND as closely as possible? These capacitors provide the AC current to the internal power MOSFETs and their drivers.

2) Are the C_{OUT} and L1 closely connected? The (–) plate of C_{OUT} returns current to PGND and the (–) plate of C_{IN}.

3) The resistive divider, R1 and R2, must be connected between the (+) plate of C_{OUT} and a ground line terminated near SGND. The feedback signal V_{FB} should be routed away from noisy components and traces, such as the SW line, and its trace should be minimized.

4) Keep sensitive components away from the SW pin. The input capacitor C_{IN}, the compensation capacitor C_C and C_{ITH} and all the resistors R1, R2, R_C should be routed away from the SW trace and the inductor L1.

5) A ground plane is preferred, but if not available, keep the signal and power grounds segregated with small signal components returning to the SGND pin at one point which is then connected to the PGND pin.

Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of power components. These copper areas should be connected to one of the input supplies: PV_{IN}, PGND, SV_{IN}, or SGND.

Design Example

As a design example, consider using the LTC3415 in an application with the following specifications:

V_{IN} = 3.3V, V_{OUT} = 1.8V, $I_{OUT(MAX)}$ = 7A,
$I_{OUT(MIN)}$ = 500mA, f = 1.5MHz

Because efficiency is important at both high and low load current, Burst Mode operation or pulse-skipping operation will be utilized. First calculate the inductor value for about 40% ripple current at maximum V_{IN}:

$$L = \left(\frac{1.8V}{1.5MHz \bullet 2.8A}\right)\left(1-\frac{1.8V}{3.3V}\right) = 0.2\mu H$$

C_{OUT} will be selected based on the ESR that is required to satisfy the output voltage ripple requirement and the bulk capacitance needed for loop stability. For this design, two 100µF ceramic capacitors will be used.

C_{IN} should be sized for a maximum current rating of:

$$I_{RMS} = 7A\left(\frac{2.5V}{4.2V}\right)\sqrt{\frac{4.2V}{2.5V}-1} = 3.43A$$

Decoupling the PV_{IN} pins with three 47µF ceramic capacitors is adequate for most applications.

TYPICAL APPLICATIONS

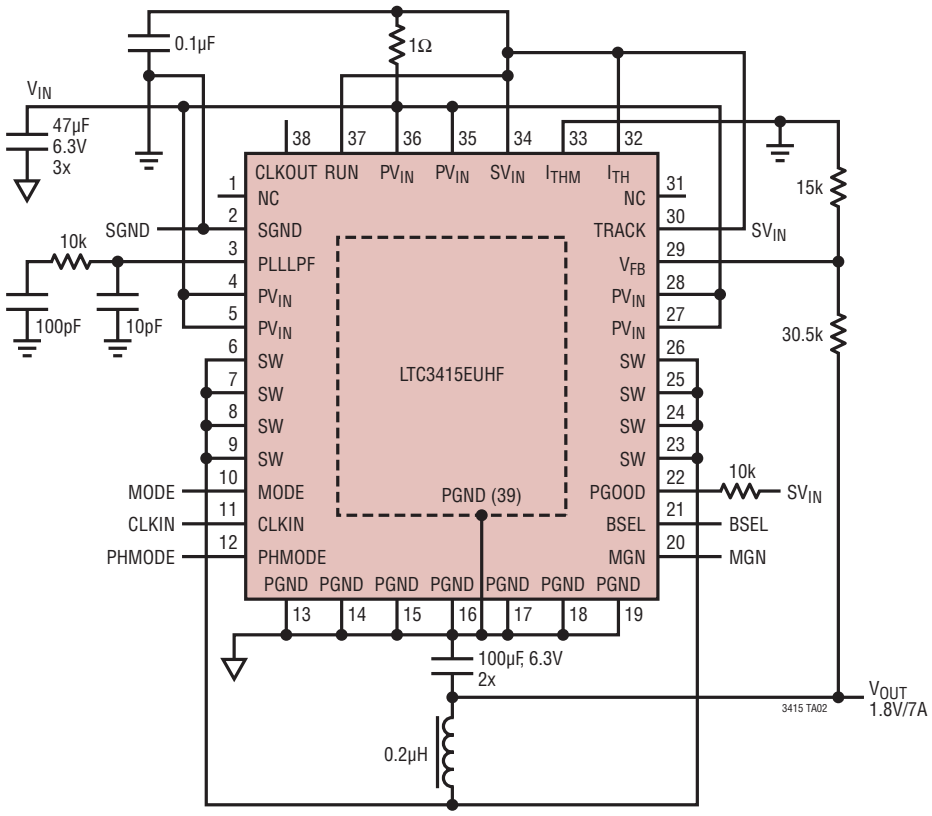
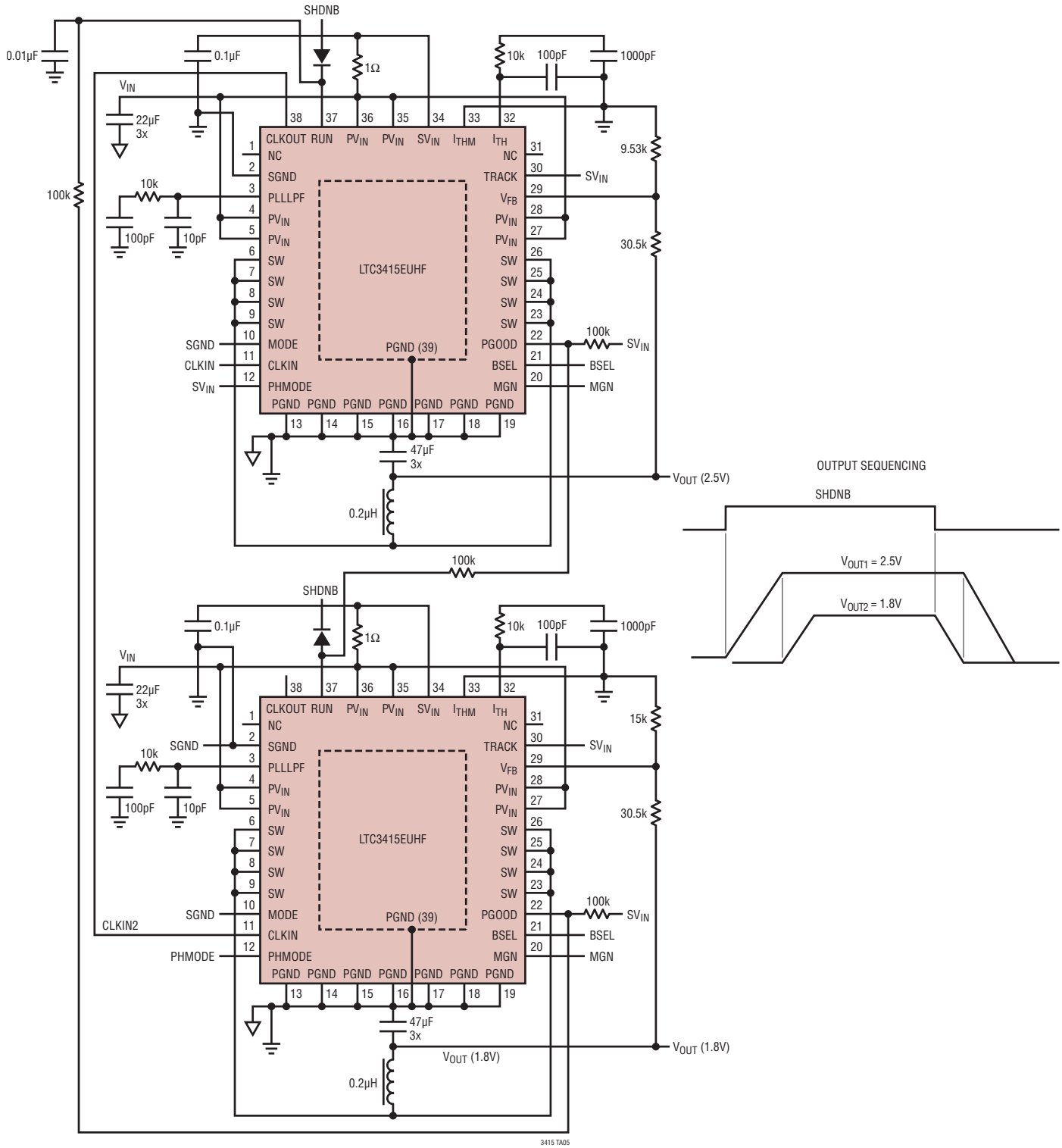


Figure 13. 3.3V to 1.8V/7A Application

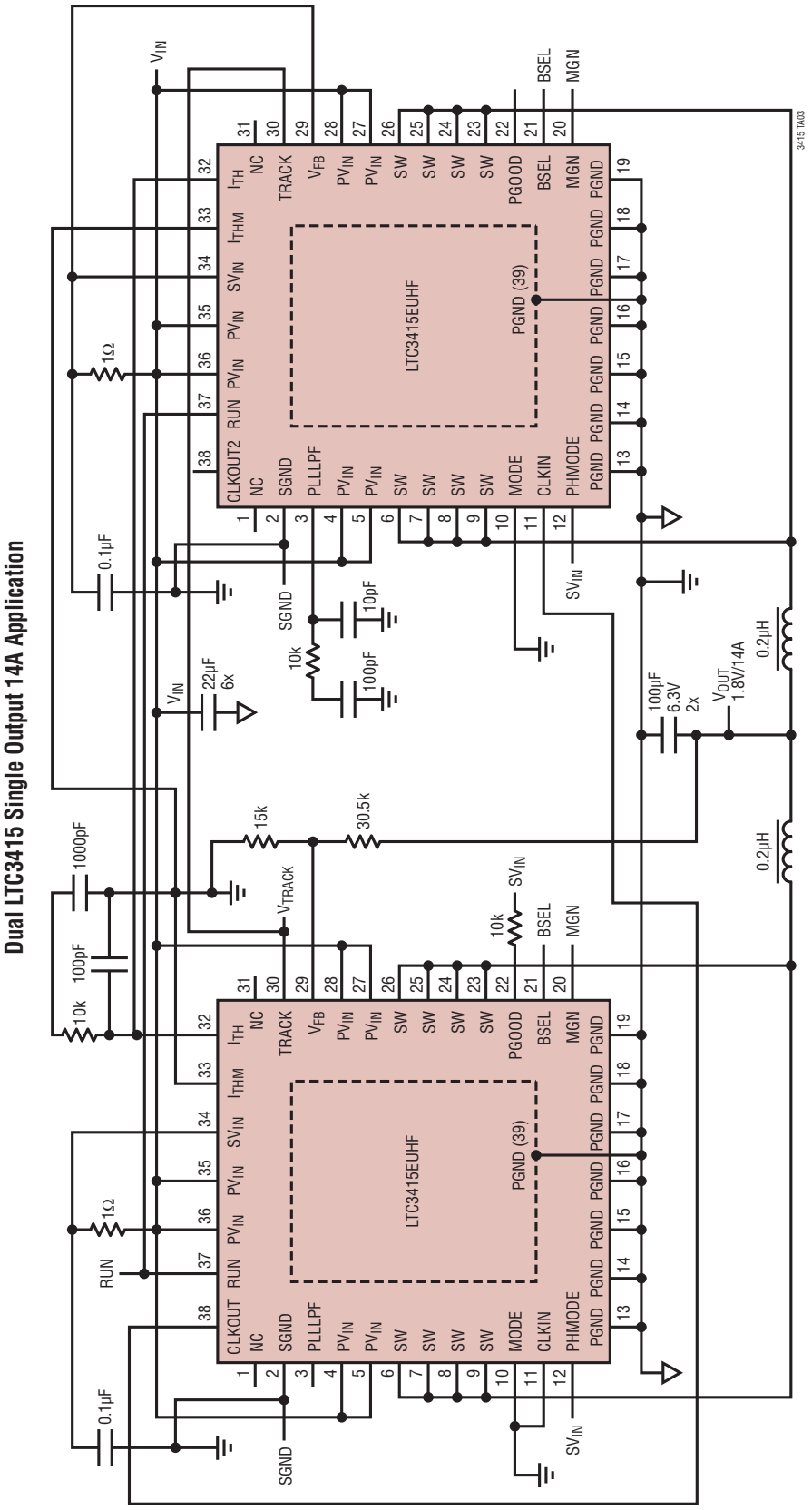
TYPICAL APPLICATIONS

Dual LTC3415 Dual Output Sequencing Application



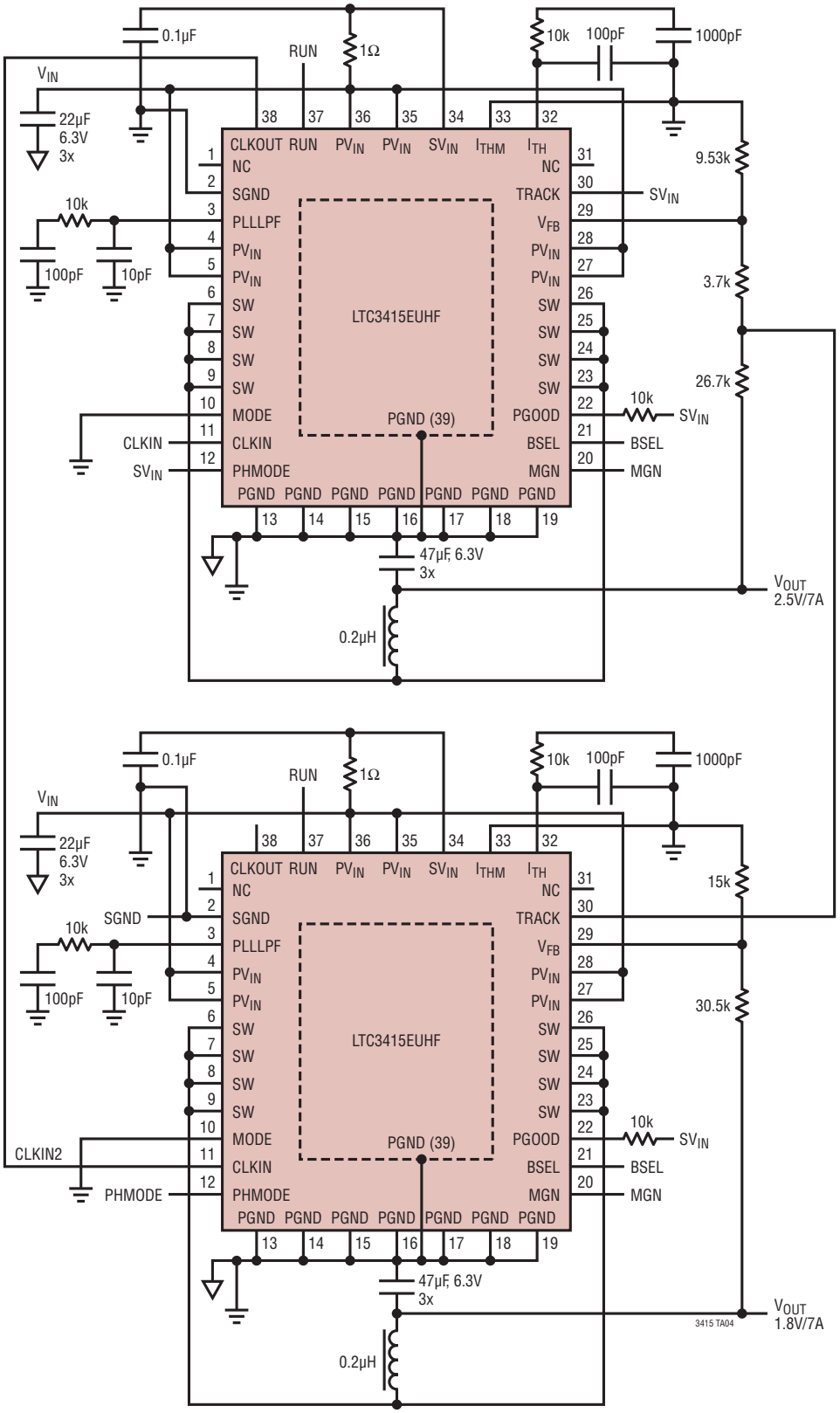
TYPICAL APPLICATIONS

Dual LTC3415 Single Output 14A Application



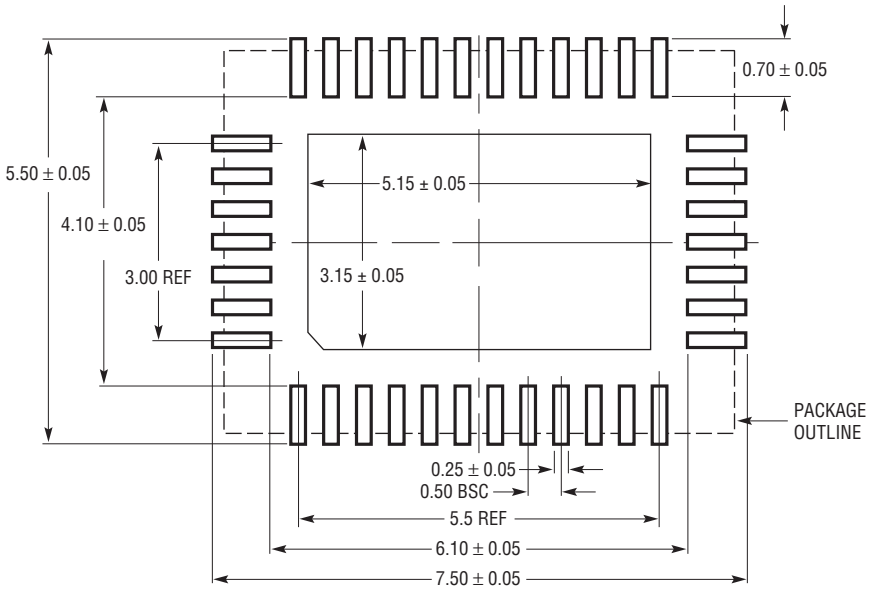
TYPICAL APPLICATIONS

Dual LTC3415 Dual Output Tracking Application

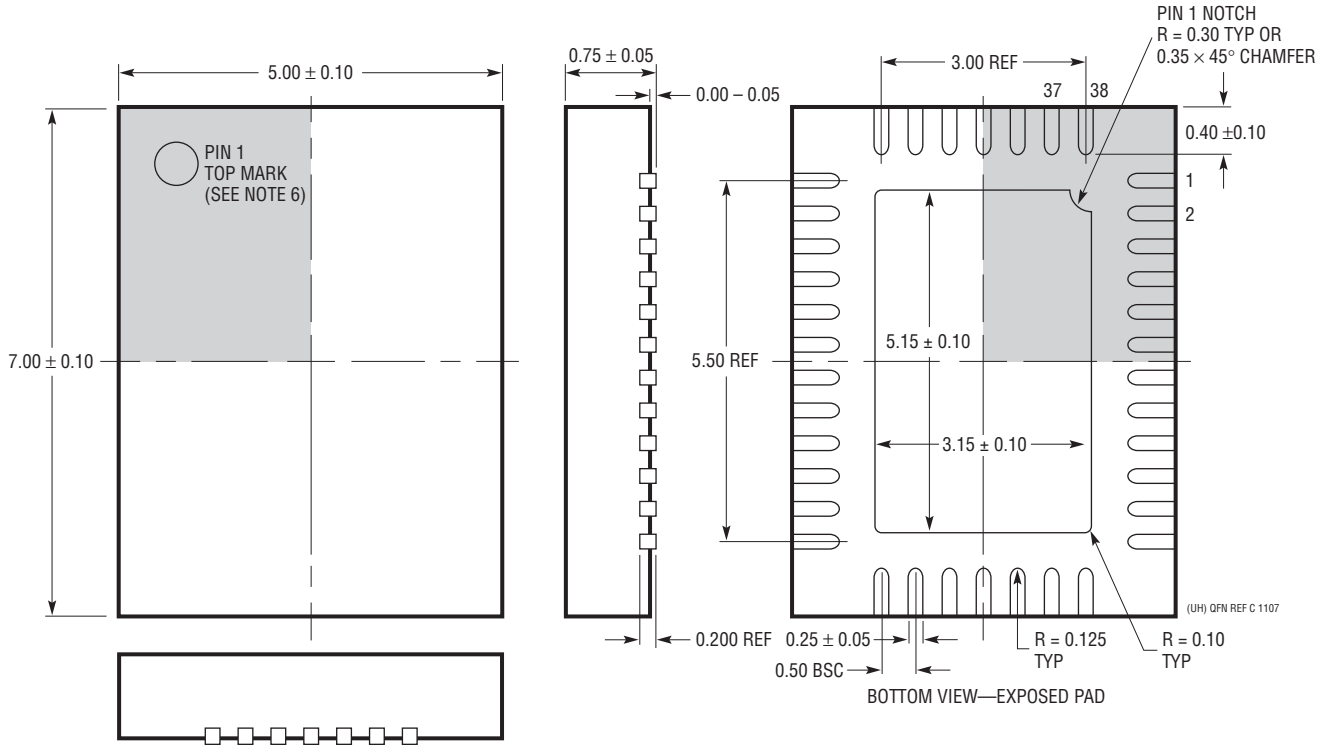


PACKAGE DESCRIPTION

UHF Package
38-Lead Plastic QFN (5mm × 7mm)
(Reference LTC DWG # 05-08-1701)



RECOMMENDED SOLDER PAD LAYOUT
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE M0-220 VARIATION WHKD
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

LINEAR TECHNOLOGY

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3404	600mA I_{OUT}, 1.4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.7V to 6V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 10µA, I_{SD} = <1µA, MS8 Package
LTC3405/ LTC3405A	300mA I_{OUT}, 1.5MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 20µA, I_{SD} = <1µA, ThinSOT Package
LTC3406/ LTC3406B	600mA I_{OUT}, 1.5MHz, Synchronous Step-Down DC/DC Converter	96% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 20µA, I_{SD} = <1µA, ThinSOT Package
LTC3407	Dual 600mA I_{OUT}, 1.5MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 40µA, I_{SD} = <1µA, MS10E Package
LTC3411	1.25A I_{OUT}, 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 60µA, I_{SD} = <1µA, MS10 Package
LTC3412	2.5A I_{OUT}, 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 60µA, I_{SD} = <1µA, TSSOP16E Package
LTC3413	3A I_{OUT} Sink/Source, 2MHz, Monolithic Synchronous Regulator for DDR/QDR Memory Termination	90% Efficiency, V_{IN}: 2.25V to 5.5V, $V_{OUT(MIN)}$ = $V_{REF/2}$, I_Q = 280µA, I_{SD} = <1µA, TSSOP16E Package
LTC3414	4A I_{OUT}, 4MHz, Synchronous Monolithic Step-Down Regulator	95% Efficiency, V_{IN}: 2.25V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 64µA, I_{SD} = <1µA, TSSOP20E Package
LTC3416	4A I_{OUT}, 4MHz, Synchronous Monolithic Step-Down Regulator with Tracking	95% Efficiency, V_{IN}: 2.25V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 64µA, I_{SD} = <1µA, TSSOP20E Package
LTC3418	8A I_{OUT}, 4MHz, Synchronous Monolithic Step-Down Regulator	V_{IN}: 2.25V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, 5mm × 7mm GFN Package
LTC3425	5A I_{OUT}, 8MHz, 4-Phase Synchronous Step-Up DC/DC Converter	5% Efficiency, V_{IN}: 0.5V to 4.5V, $V_{OUT(MAX)}$ = 5.25V, I_Q = 12µA, I_{SD} = <1µA, QFN Package
LTC3428	4A I_{OUT}, 2MHz, Dual Phase Step-Up DC/DC Converter	92% Efficiency, V_{IN}: 1.6V to 4.5V, $V_{OUT(MAX)}$ = 5.25V, I_Q = 1.3mA, I_{SD} = <1µA, DFN Package
LT3430	60V, 2.75A I_{OUT}, 200kHz, High Efficiency Step-Down DC/DC Converter	90% Efficiency, V_{IN}: 5.5V to 60V, $V_{OUT(MIN)}$ = 1.20V, I_Q = 2.5mA, I_{SD} = 25µA, TSSOP16E Package
LT3440	600mA I_{OUT}, 2MHz, Synchronous Buck-Boost DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 2.5V, I_Q = 25µA, I_{SD} = <1µA, MS-10 Package
LTM4600	10A, DC/DC µModule	Complete Synchronous Power Supply in LGA; 4.5V ≤ V_{IN} ≤ 28V; 15mm × 15mm × 2.8mm LGA Package

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