NB638

High Efficiency, Fast Transient, 7A, 28V Synchronous Step-down Converter in a Tiny 3x4mm QFN Package

DESCRIPTION

The NB638 is a fully integrated, high frequency synchronous rectified step-down switch mode converter. It offers a very compact solution to achieve 7A continuous output current over a wide input supply range with excellent load and line regulation. The NB638 operates at high efficiency over a wide output current load range.

Constant-On-Time (COT) control mode provides fast transient response and eases loop stabilization.

Full protection features include SCP, OCP, OVP, UVP and thermal shutdown.

The NB638 requires a minimum number of readily available standard external components and is available in a space-saving QFN20 (3x4mm) package.

FEATURES

- Wide 4.5V to 28V Operating Input Range
- 7A Output Current
- Internal 30mΩ High-Side, 12mΩ Low-Side Power MOSFETs
- Proprietary Switching Loss Reduction Technique
- 1% Reference Voltage
- Programmable Soft Start Time
- Soft Shutdown
- 200kHz to 1MHz Switching Frequency
- SCP, OCP, OVP, UVP Protection and Thermal Shutdown
- Output Adjustable from 0.8V to 14V
- Available in a QFN20 (3x4mm) Package

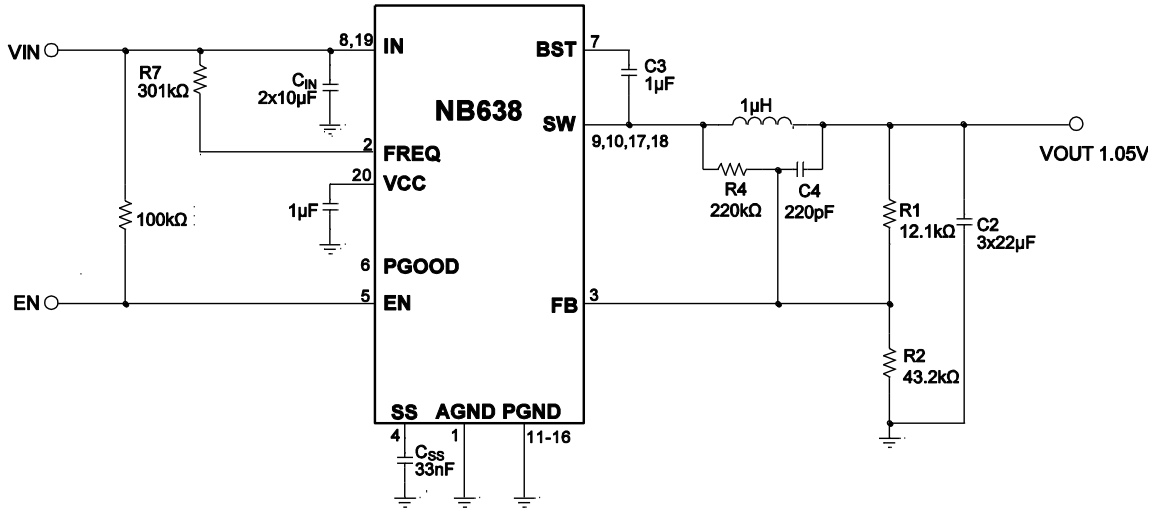
APPLICATIONS

- Notebook Systems and I/O Power
- Networking Systems
- Optical Communication Systems
- Distributed Power and POL Systems

All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance.

"MPS" and "The Future of Analog IC Technology" are registered trademarks of Monolithic Power Systems, Inc.

TYPICAL APPLICATION



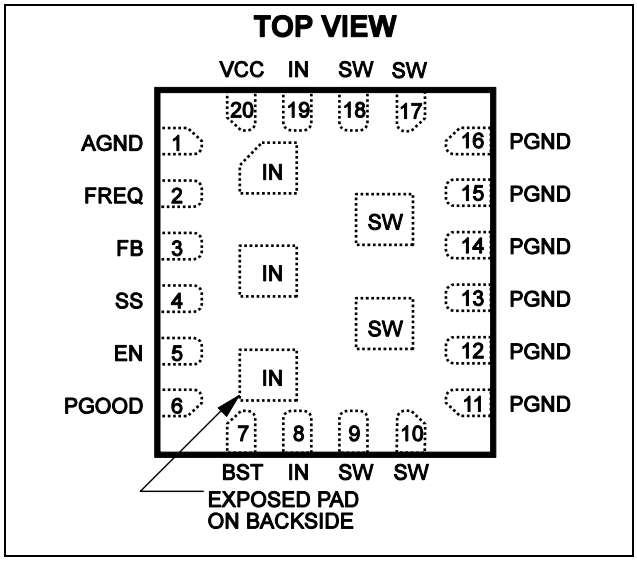
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2017 MPS. All Rights Reserved.

ORDERING INFORMATION

Part Number*	Package	Top Marking
NB638DL	QFN-20 (3mmx4mm)	NB638

***** For Tape & Reel, add suffix –Z (e.g. NB638DL–Z)
For RoHS compliant packaging, add suffix –LF (e.g. NB638DL–LF–Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage V_{IN} 30V
V_{SW} ..... -0.3V to V_{IN} + 0.3V
V_{SW} (30ns) ..... -3V to V_{IN} + 3V
V_{BST} ..... V_{SW} + 6V
$I_{VIN\ (RMS)}$ 3.5A
V_{PGOOD} ..... -0.3V to V_{CC}+0.6V
V_{FREQ} ..... -0.3V to 12V(2)
All Other Pins ..... -0.3V to +6V
Continuous Power Dissipation (T_A = +25°C) (3)
..... 2.6W
Junction Temperature ..... 150°C
Lead Temperature ..... 260°C
Storage Temperature ..... -65°C to +150°C

Recommended Operating Conditions (4)

Supply Voltage V_{IN} ..... 4.5V to 28V
Output Voltage V_{OUT} ..... 0.8V to 14V
Maximum Junct. Temp (T_J) ..... -40°C to +125°C

Thermal Resistance (5)

	θ_{JA}	θ_{JC}
QFN-20 (3mm x4mm)	48	10 ...°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) Guaranteed by design.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D(MAX)=(T_J(MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on JESD51-7, 4-layer PCB.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2017 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_A = +25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Current (Shutdown)	I_{IN}	V_{EN} = 0V		0		μA
Supply Current (Quiescent)	I_{IN}	V_{EN} = 2V V_{FB} = 1V		500		μA
HS Switch On Resistance (5)	HS_{RDS-ON}			30		mΩ
LS Switch On Resistance (5)	LS_{RDS-ON}			12		mΩ
Switch Leakage	SW_{LKG}	V_{EN} = 0V V_{SW} = 0V or 12V		0	10	μA
Current Limit	I_{LIMIT}			12		A
One-Shot On Time	T_{ON}	R7=301kΩ V_{OUT}=1.2V		250		ns
Minimum Off Time(5)	T_{OFF}			100		ns
Fold-back Off Time(5)	T_{FB}	I_{LIM}=1(HIGH)		1.4		μs
OCP hold-off time(5)	T_{OC}	I_{LIM}=1(HIGH)			40	μs
Feedback Voltage	V_{FB}	T_A=25°C	807	815	823	mV
		0°C <T_A<70°C	803	815	827	
Feedback Current	I_{FB}	V_{FB} = 815mV		10	50	nA
Soft Start Charging Current	I_{SS}	V_{SS}=0V		8.5		μA
Soft Stop Charging Current	I_{SS}	V_{SS}=0.815V		8.5		μA
Power Good Rising Threshold	$PGOOD_{Vth-Hi}$			0.9		V_{FB}
Power Good Falling Threshold	$PGOOD_{Vth-Lo}$			0.85		V_{FB}
Power Good Rising delay	T_{PGOOD}	T_{SS}=1ms		1		ms
Power Good Rising delay	T_{PGOOD}	T_{SS} =2ms		1.5		ms
Power Good Rising delay	T_{PGOOD}	T_{SS} =3ms		2		ms
EN Rising Threshold	EN_{Vth-Hi}		1.05	1.35	1.60	V
EN Threshold Hysteresis	$EN_{Vth-Hys}$		250	420	550	mV
EN Input Current	I_{EN}	V_{EN} = 2V		2		μA
V_{IN} Under-Voltage Lockout Threshold Rising	$INUV_{Vth}$		3.8	4.0	4.2	V
V_{IN} Under-Voltage Lockout Threshold Hysteresis	$INUV_{HYS}$			880		mV
V_{CC} Regulator	V_{CC}			5		V
V_{CC} Load Regulation		I_{CC}=5mA		5		%
Vo Over-Voltage Protection Threshold	V_{OVP}			1.25		V_{FB}
Vo Under-Voltage Detection Threshold	V_{UVP}			0.7		V_{FB}
Thermal Shutdown	T_{SD}			150		°C
Thermal Shutdown Hysteresis	T_{SD-HYS}			25		°C

Note:

6) Guaranteed by design.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2017 MPS. All Rights Reserved.

PIN FUNCTIONS

Pin #	Name	Description
1	AGND	Analog Ground.
2	FREQ	Frequency Set during CCM operation. The ON period is determined by the input voltage and the frequency-set resistor connected to FREQ pin. Connect a resistor to IN for line feed-forward. Decouple with a 1nF capacitor.
3	FB	Feedback. An external resistor divider from the output to GND, tapped to the FB pin, sets the output voltage.
4	SS	Soft Start. Connect an external SS capacitor to program the soft start time for the switch mode regulator. When the EN pin becomes high, an internal current source (8.5μA) charges up the SS capacitor and the SS voltage slowly ramps up from 0 to V_{FB} smoothly. When the EN pin becomes low, an internal current source (8.5μA) discharges the SS capacitor and the SS voltage slowly ramps down.
5	EN	EN=1 to enable the NB638. For automatic start-up, connect EN pin to IN with a 100kΩ resistor. It includes an internal 1MΩ pull-down resistor.
6	PGOOD	Power Good Output. The output of this pin is an open drain and is high if the output voltage is higher than 90% of the nominal voltage. There is delay from FB ≥ 90% to PGOOD high, which is 50% of SS time plus 0.5ms.
7	BST	Bootstrap. A 0.1μF-1μF capacitor connected between SW and BS pins is required to form a floating supply across the high-side switch driver.
8, 19	IN	Supply Voltage. The NB638 operates from a +4.5V to +28V input rail. C_{IN} is needed to decouple the input rail. Use wide PCB traces and multiple vias to make the connection.
9, 10, 17, 18	SW	Switch Output. Use wide PCB traces and multiple vias to make the connection.
11-16	PGND	System Ground. This pin is the reference ground of the regulated output voltage. For this reason care must be taken in PCB layout.
20	VCC	Internal Bias Supply. Decouple with a 1μF capacitor as close to the pin as possible.

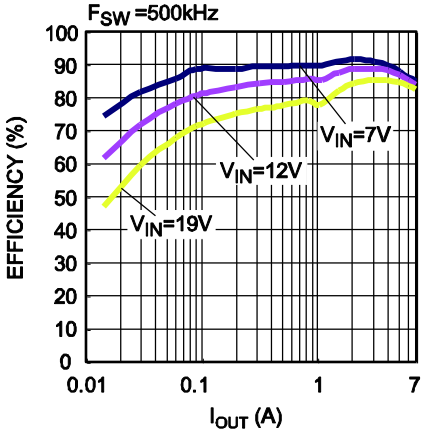
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2017 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN}=12V, V_{OUT} =1.05V, L=1µH, T_A=+25°C, unless otherwise noted.

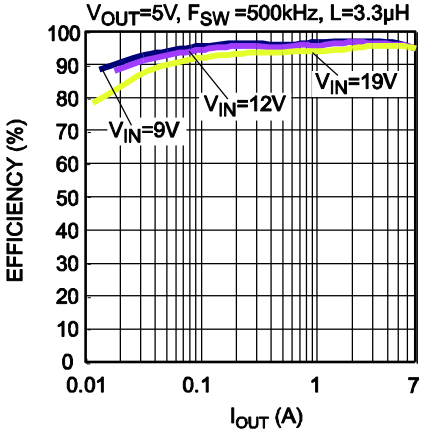
Efficiency vs. Load Current

F_{SW} =500kHz

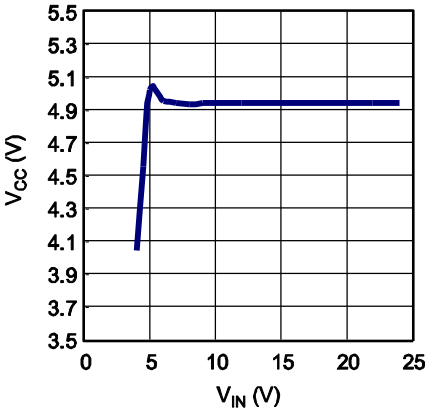


Efficiency vs. Load Current

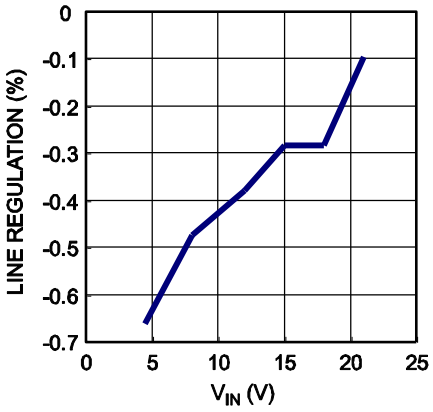
V_{OUT}=5V, F_{SW} =500kHz, L=3.3µH



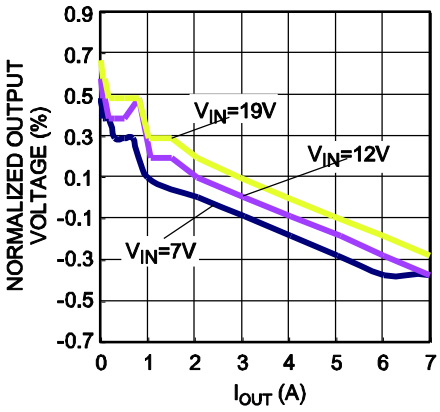
V_{CC} Regulator Line Regulation



Line Regulation

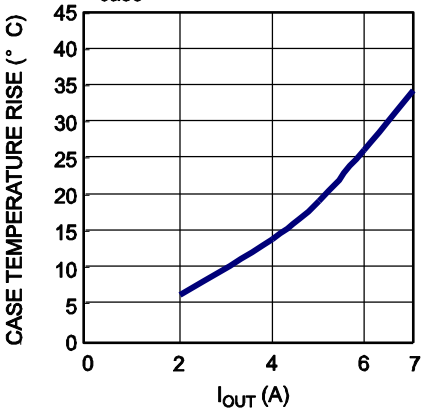


Load Regulation



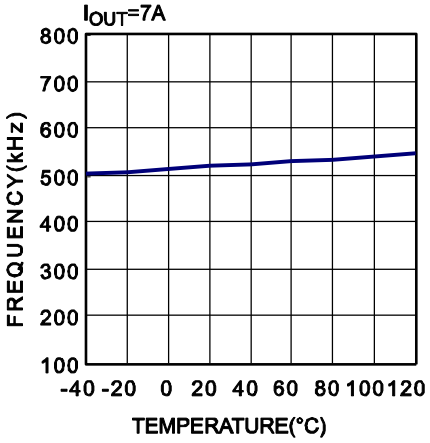
Case Temperature Rise vs. Output Current

T_{case}=22.6°C



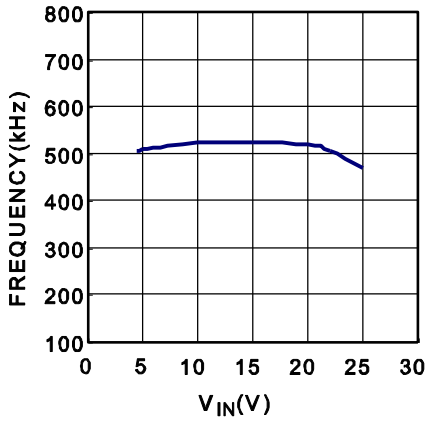
Frequency vs. Temperature

I_{OUT}=7A

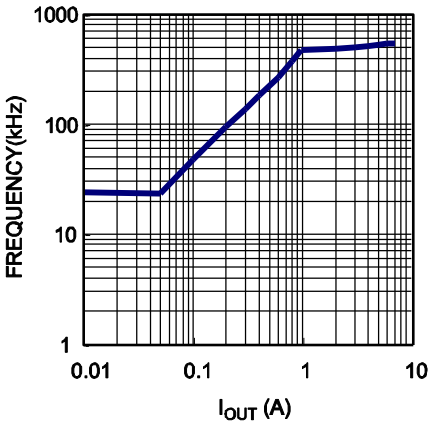


Frequency vs. V_{IN}

R_{FSW}=174kΩ, I_{OUT}=7A



Frequency vs. Load Current

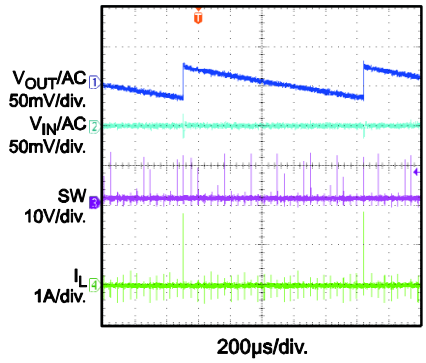


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2017 MPS. All Rights Reserved.

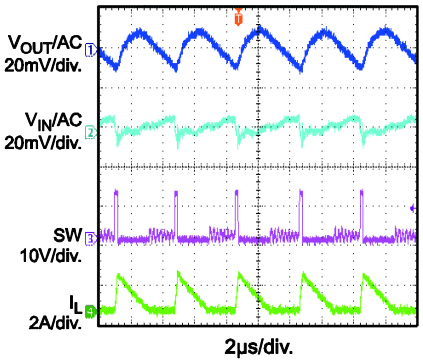
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN}=12V, V_{OUT} =1.05V, L=1µH, T_A=+25°C, unless otherwise noted.

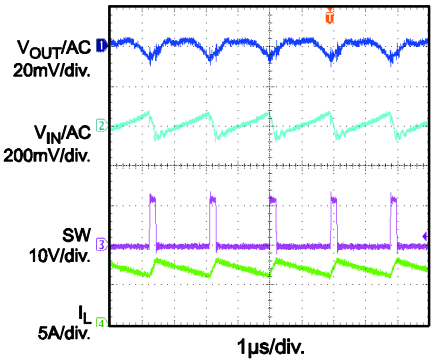
Input/Output Voltage Ripple
I_{OUT} = 0A



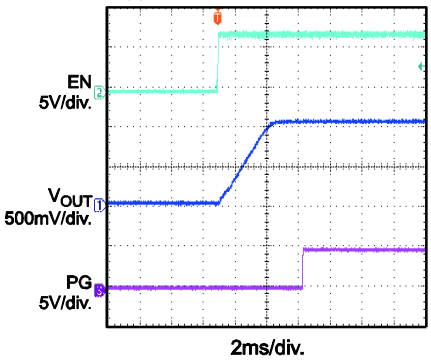
Input/Output Voltage Ripple
I_{OUT} = 0.5A



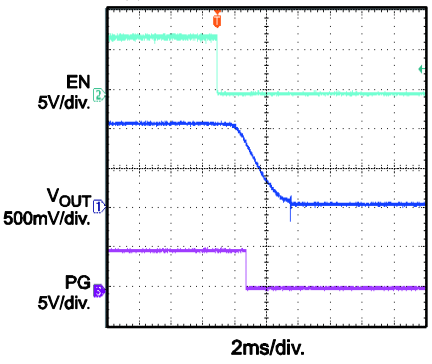
Input/Output Voltage Ripple
I_{OUT} = 7A



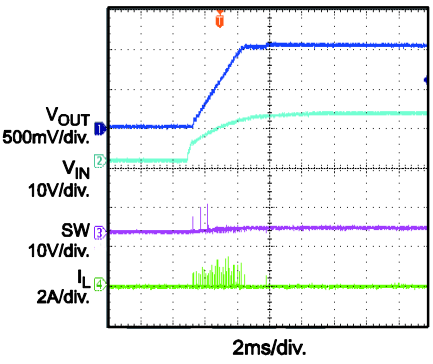
Power Good Through EN Start-Up
C_{SS} = 33nF



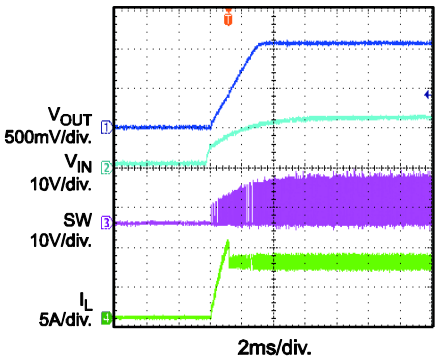
Power Good Through EN Shutdown
C_{SS} = 33nF



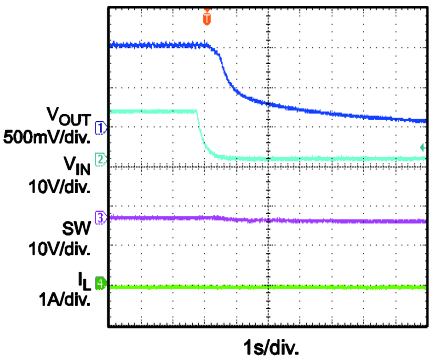
Start-Up Through V_{IN}
I_{OUT} = 0A



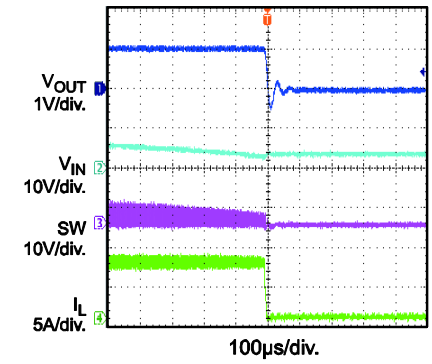
Start-Up Through V_{IN}
I_{OUT} = 7A



Shutdown Through V_{IN}
I_{OUT} = 0A



Shutdown Through V_{IN}
I_{OUT} = 7A

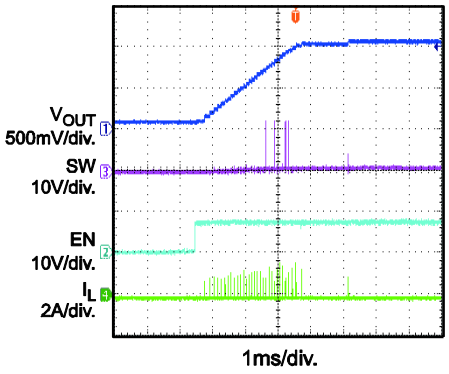


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2017 MPS. All Rights Reserved.

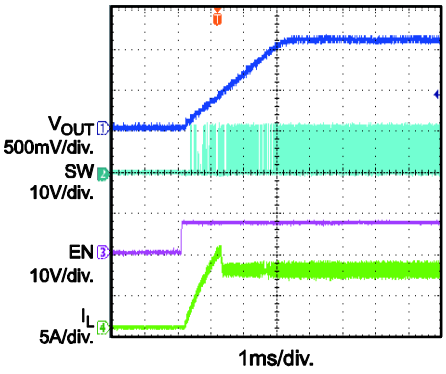
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN}=12V, V_{OUT} =1.05V, L=1µH, T_A=+25°C, unless otherwise noted.

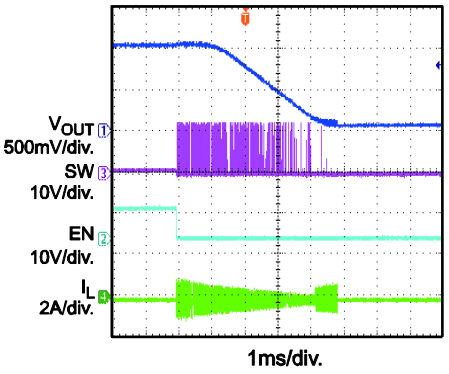
Start-Up Through EN
I_{OUT} = 0A



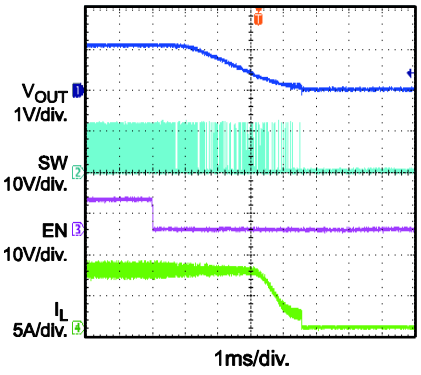
Start-Up Through EN
I_{OUT} = 7A



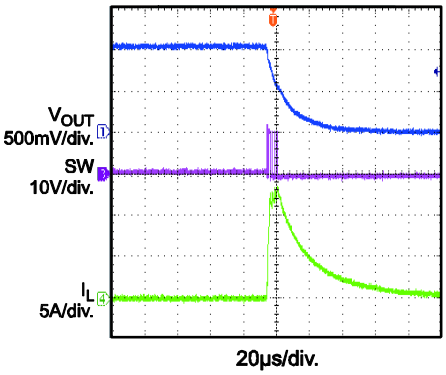
Shutdown Through EN
I_{OUT} = 0A



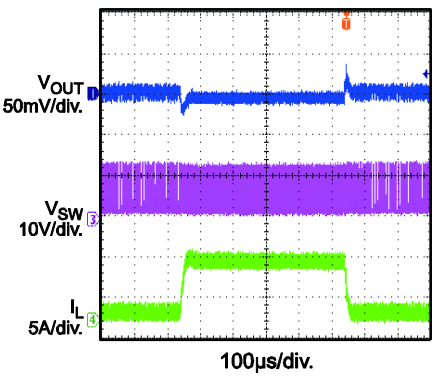
Shutdown Through EN
I_{OUT} = 7A



Short-Circuit Protection



Transient
I_{OUT} =0.8A-7.2A@2.5A/µs,
F_{SW} = 530kHz, C_{OUT} =3x22µF



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2017 MPS. All Rights Reserved.

BLOCK DIAGRAM

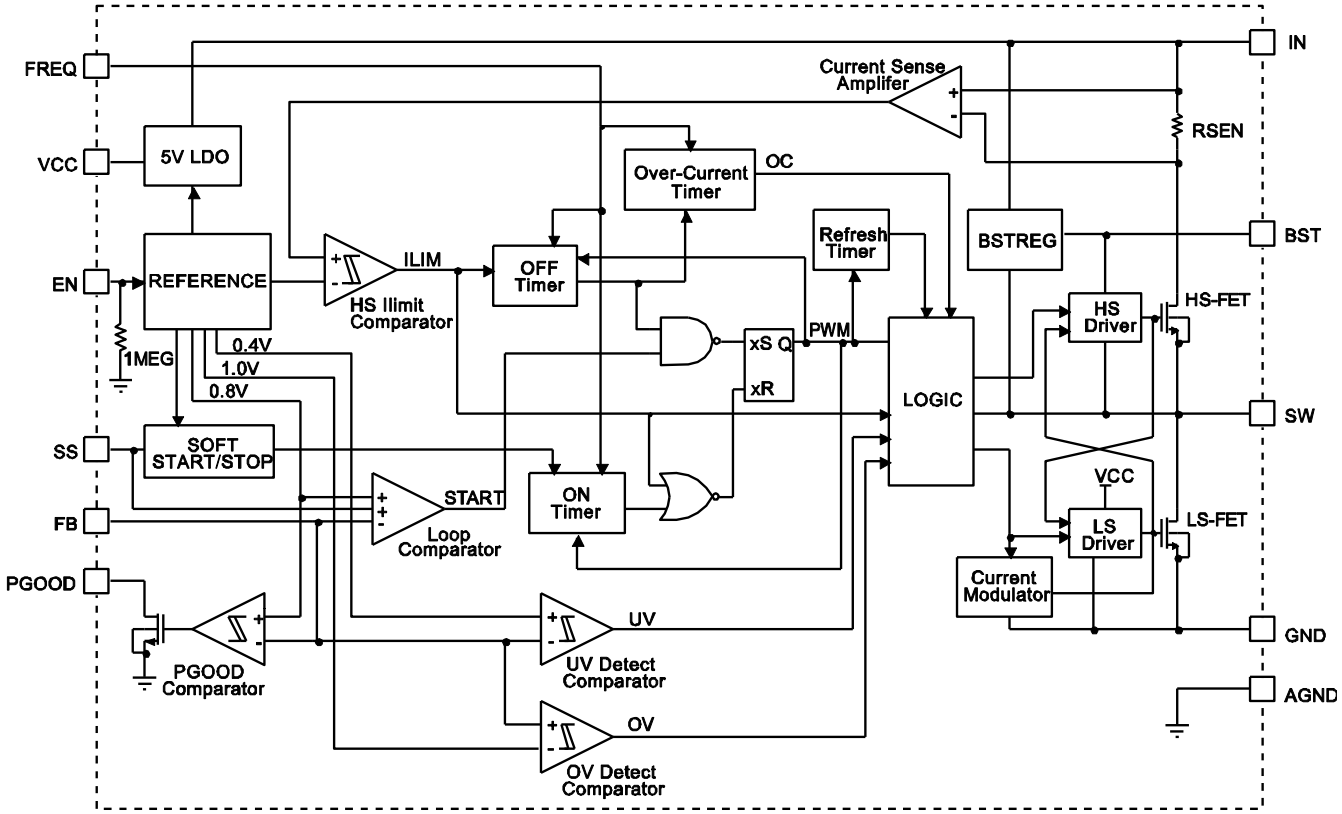


Figure 1—Functional Block Diagram

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2017 MPS. All Rights Reserved.

OPERATION

PWM Operation

The NB638 is a fully integrated synchronous rectified step-down switch mode converter. Constant-on-time (COT) control is employed to provide fast transient response and easy loop stabilization. At the beginning of each cycle, the high-side MOSFET (HS-FET) is turned ON when the feedback voltage (V_{FB}) is below the reference voltage (V_{REF}), which indicates insufficient output voltage. The ON period is determined by the input voltage and the frequency-set resistor as follows:

$$T_{ON}(ns) = \frac{6 \times R7(k\Omega)}{V_{IN}(V) - 0.4} + 40(ns) \quad (1)$$

After the ON period elapses, the HS-FET is turned off, or becomes OFF state. It is turned ON again when V_{FB} drops below V_{REF}. By repeating operation this way, the converter regulates the output voltage. The integrated low-side MOSFET (LS-FET) is turned on when the HS-FET is in its OFF state to minimize the conduction loss. There will be a dead short between input and GND if both HS-FET and LS-FET are turned on at the same time. It's called shoot-through. In order to avoid shoot-through, a dead-time (DT) is internally generated between HS-FET off and LS-FET on, or LS-FET off and HS-FET on.

Heavy-Load Operation

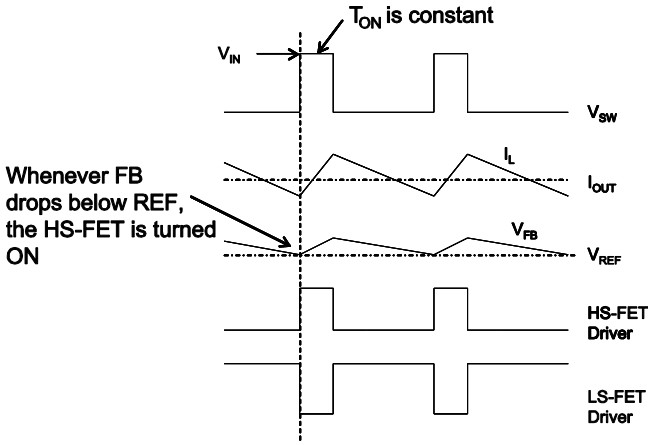


Figure 2—Heavy Load Operation

As Figure 2 shows, when the output current is high, the HS-FET and LS-FET repeat on/off as described above. In this operation, the inductor current will never go to zero. It's called continuous-conduction-mode (CCM) operation. In CCM operation, the switching frequency (F_{SW}) is fairly constant.

Light-Load Operation

At light load or no load condition, the output drops very slowly and the NB638 reduces the switching frequency automatically to maintain high efficiency. The light load operation is shown in Figure 3. The V_{FB} does not reach V_{REF} when the inductor current is approaching zero. The LS-FET driver turns into tri-state (high Z) whenever the inductor current reaches zero. A current modulator takes over the control of LS-FET and limits the inductor current to less than -1mA. Hence, the output capacitors discharge slowly to GND through LS-FET. As a result, the efficiency at light load condition is greatly improved. At light load condition, the HS-FET is not turned ON as frequently as at heavy load condition. This is called skip mode.

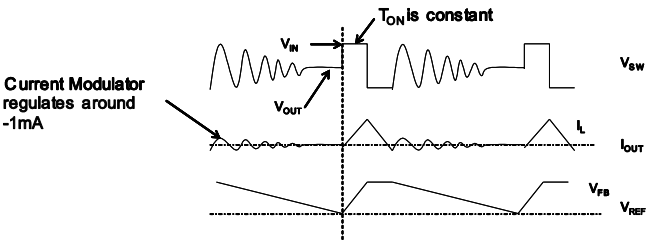


Figure 3—Light Load Operation

As the output current increases from the light load condition, the time period within which the current modulator regulates becomes shorter. The HS-FET is turned ON more frequently. Hence, the switching frequency increases correspondingly. The output current reaches the critical level when the current modulator time is zero. The critical level of the output current is determined as follows:

$$I_{OUT} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times F_{SW} \times V_{IN}} \quad (2)$$

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2017 MPS. All Rights Reserved.

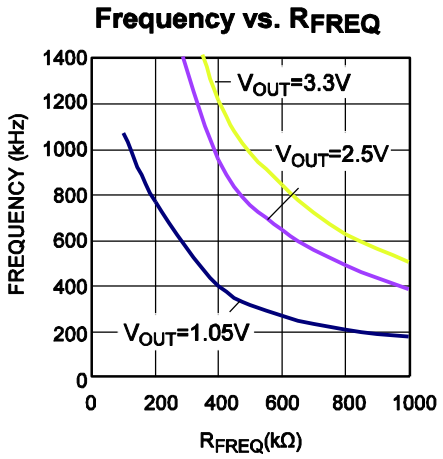
It turns into PWM mode once the output current exceeds the critical level. After that, the switching frequency stays fairly constant over the output current range.

Switching Frequency

Constant on-time (COT) control is used in the NB638 and there is no dedicated oscillator in the IC. The input voltage is feed-forwarded to the on-time one-shot timer through the resistor R7. The duty ratio is kept as V_{OUT}/V_{IN}. Hence, the switching frequency is fairly constant over the input voltage range. The switching frequency can be set as follows:

$$F_{SW}(kHz) = \frac{10^6}{\frac{6 \times R7(k\Omega)}{V_{IN}(V) - 0.4} \times \frac{V_{IN}(V)}{V_{OUT}(V)} + T_{DEALY}(ns)} \quad (3)$$

Where T_{DELAY} is the comparator delay. It's about 40ns.



Generally, the NB638 is set for 200 kHz to 1MHz application. It is optimized to operate at high switching frequency with high efficiency. High switching frequency makes it possible to utilize small sized LC filter components to save system PCB space.

Jitter and FB Ramp Slope

Figure 4 and Figure 5 show jitter occurring in both PWM mode and skip mode. When there is noise in the V_{FB} downward slope, the ON time of HS-FET deviates from its intended location and produces jitter. It is necessary to understand that there is a relationship between a system's stability and the steepness of the V_{FB} ripple's downward slope. The slope steepness of the V_{FB} ripple dominates in noise immunity. The magnitude of the V_{FB} ripple doesn't directly affect the noise immunity directly.

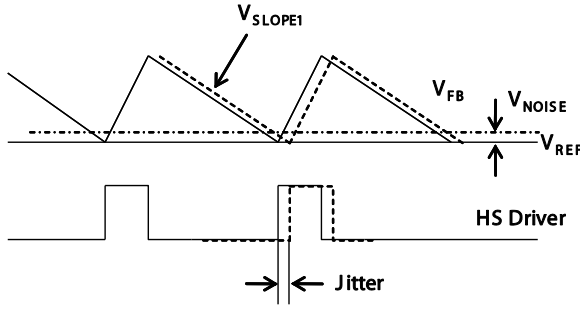


Figure 4—Jitter in PWM Mode

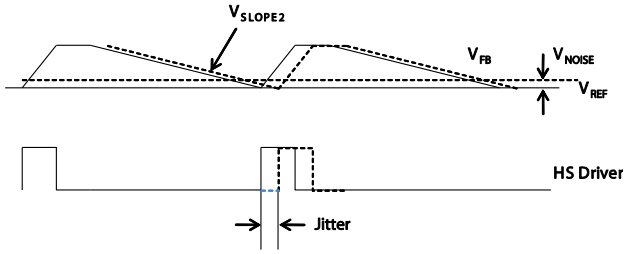


Figure 5—Jitter in Skip Mode

Ramp with Large ESR Cap

In the case of POSCAP or other types of capacitor with larger ESR is applied as output capacitor. The ESR ripple dominates the output ripple, and the slope on the FB is quite ESR related. Figure 6 shows an equivalent circuit in PWM mode with the HS-FET off and without an external ramp circuit. Turn to application information section for design steps with large ESR caps.

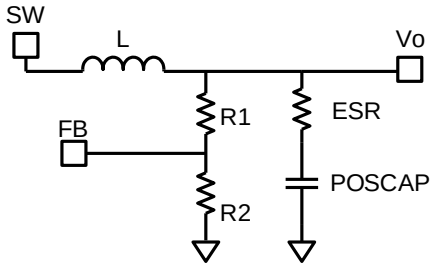


Figure 6—Simplified Circuit in PWM Mode without External Ramp Compensation

To realize the stability when no external ramp is used, usually the ESR value should be chosen as follow:

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2017 MPS. All Rights Reserved.

$$R_{ESR} \geq \frac{\frac{T_{SW}}{0.7\times\pi}+\frac{T_{ON}}{2}}{C_{OUT}} \quad (4)$$

Tsw is the switching period.

Ramp with small ESR Cap

When the output capacitors are ceramic ones, the ESR ripple is not high enough to stabilize the system, and external ramp compensation is needed. Skip to application information section for design steps with small ESR caps.

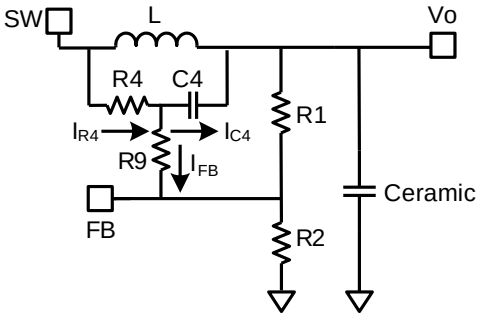


Figure 7—Simplified Circuit in PWM Mode with External Ramp Compensation

In PWM mode, an equivalent circuit with HS-FET off and the use of an external ramp compensation circuit (R4, C4) is simplified in Figure 7. The external ramp is derived from the inductor ripple current. If one chooses C4, R9, R1 and R2 to meet the following condition:

$$\frac{1}{2\pi\times F_{SW}\times C_4} < \frac{1}{5}\times\left(\frac{R_1\times R_2}{R_1+R_2}+R_9\right) \quad (5)$$

Where:

$$I_{R4} = I_{C4} + I_{FB} \approx I_{C4} \quad (6)$$

And the ramp on the V_{FB} can then be estimated as:

$$V_{RAMP} = \frac{V_{IN}-V_O}{R_4\times C_4}\times T_{ON}\times\frac{R_1 // R_2}{R_1 // R_2 + R_9} \quad (7)$$

The downward slope of the V_{FB} ripple then follows

$$V_{SLOPE1} = \frac{-V_{RAMP}}{T_{off}} = \frac{-V_{OUT}}{R_4\times C_4} \quad (8)$$

As can be seen from equation 8, if there is instability in PWM mode, we can reduce either R4 or C4. If C4 can not be reduced further due to limitation from equation 5, then we can only reduce R4. For a stable PWM operation, the V_{slope1} should be design follow equation 9.

$$-V_{slope1} \geq \frac{\frac{T_{SW}}{0.7\times\pi}+\frac{T_{ON}}{2}-R_{ESR}C_{OUT}}{2\times L\times C_{OUT}}V_{OUT}+\frac{Io\times10^{-3}}{T_{SW}-T_{on}} \quad (9)$$

Io is the load current.

In skip mode, the downward slope of the V_{FB} ripple is almost the same whether the external ramp is used or not. Fig.9 shows the simplified circuit of the skip mode when both the HS-FET and LS-FET are off.

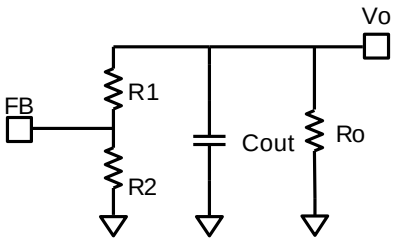


Figure 8—Simplified Circuit in skip Mode

The downward slope of the V_{FB} ripple in skip mode can be determined as follow:

$$V_{SLOPE2} = \frac{-V_{REF}}{((R_1+R_2)//Ro)\times C_{OUT}} \quad (10)$$

Where Ro is the equivalent load resistor.
As described in Fig.5, V_{SLOPE2} in the skip mode is lower than that is in the PWM mode, so it is reasonable that the jitter in the skip mode is larger. If one wants a system with less jitter during ultra light load condition, the values of the V_{FB} resistors should not be too big, however, that will decrease the light load efficiency.

Soft Start/Stop

The NB638 employs soft start/stop (SS) mechanism to ensure smooth output during power-up and power shutdown. When the EN pin becomes high, an internal current source (8.5μA) charges up the SS CAP. The SS CAP voltage takes over the REF voltage to the PWM comparator. The output voltage smoothly ramps

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2017 MPS. All Rights Reserved.

up with the SS voltage. Once the SS voltage reaches the same level as the REF voltage, it keeps ramping up while V_{REF} takes over the PWM comparator. At this point, the soft start finishes and it enters into steady state operation.

When the EN pin becomes low, the SS CAP voltage is discharged through an 8.5μA internal current source. Once the SS voltage reaches REF voltage, it takes over the PWM comparator.

The output voltage will decrease smoothly with SS voltage until zero level. The SS Cap value can be determined as follows:

$$C_{SS}(nF) = \frac{T_{SS}(ms) \times I_{SS}(\mu A)}{V_{REF}(V)} \quad (11)$$

If the output capacitors have large capacitance value, it's not recommended to set the SS time too small. Otherwise, it's easy to hit the current limit during SS. A minimum value of 4.7nF should be used if the output capacitance value is larger than 330μF.

Power Good (PGOOD)

The NB638 has power-good (PGOOD) output. The PGOOD pin is the open drain of a MOSFET. It should be connected to V_{CC} or other voltage source through a resistor (e.g. 100k). After the input voltage is applied, the MOSFET is turned on so that the PGOOD pin is pulled to GND before SS is ready. After FB voltage reaches 90% of REF voltage, the PGOOD pin is pulled high after a delay.

The PGOOD delay time is determined as follows:

$$T_{PGOOD}(ms) = 0.5 \times T_{SS}(ms) + 0.5 \quad (12)$$

When the FB voltage drops to 85% of REF voltage, the PGOOD pin will be pulled low.

Over-Current Protection (OCP) and Short-Circuit Protection (SCP)

The NB638 has cycle-by-cycle over-current limit control. The inductor current is monitored during the ON state. Once it detects that the inductor current is higher than the current limit, the HS-FET is turned off. At the same time, the OCP timer is started. The OCP timer is set as 40μs. If in the following 40μs, the current limit is hit for every cycle, then it'll trigger OCP latch-off. The converter needs power cycle to restart after it triggers OCP.

If short circuit happens, then the current limit will be hit immediately and the FB voltage will become lower than 50% of the REF voltage. When the current limit is hit and the FB voltage is lower than 50% of the REF voltage (0.815V), the device considers this as a dead short on the output and triggers SCP latch-off immediately. This is short circuit protection (SCP).

Over/Under-voltage Protection (OVP/UVP)

The NB638 monitors the output voltage through a resistor divider feedback (FB) voltage to detect overvoltage and undervoltage on the output. When the FB voltage is higher than 125% of the REF voltage (0.8V), it'll trigger OVP latch-off. Once it triggers OVP, the LS-FET is always on while the HS-FET is always off. It needs power cycle to power up again. When the FB voltage is below 50% of the REF voltage (0.815V), it is recognized as UV (under-voltage). Usually, UVP accompanies a hit in current limit and results in SCP.

UVLO protection

The NB638 has under-voltage lock-out protection (UVLO). When the input voltage is higher than the UVLO rising threshold voltage, the NB638 will be powered up. It shuts off when the input voltage is lower than the UVLO falling threshold voltage. This is non-latch protection.

Thermal Shutdown

Thermal shutdown is employed in the NB638. The junction temperature of the IC is internally monitored. If the junction temperature exceeds the threshold value (typically 150ºC), the converter shuts off. This is a non-latch protection. There is about 25ºC hysteresis. Once the junction temperature drops to about 125ºC, it initiates a SS.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2017 MPS. All Rights Reserved.

APPLICATION INFORMATION

Setting the Output Voltage-Large ESR Caps

For applications that electrolytic capacitor or POS capacitor with a controlled output of ESR is set as output capacitors. The output voltage is set by feedback resistors R1 and R2. As figure 9 shows.

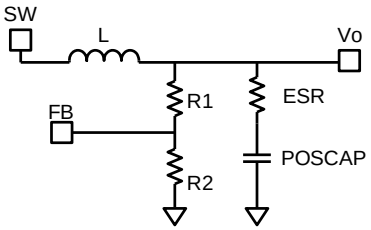


Figure 9—Simplified Circuit of POS Capacitor

First, choose a value for R2. R2 should be chosen reasonably, a small R2 will lead to considerable quiescent current loss while too large R2 makes the FB noise sensitive. It is recommended to choose a value within 5kΩ-50kΩ for R2, using a comparatively larger R2 when Vout is low, etc.,1.05V, and a smaller R2 when Vout is high. Then R1 is determined as follow with the output ripple considered:

$$R_1 = \frac{V_{OUT} - \frac{1}{2}\Delta V_{OUT} - V_{REF}}{V_{REF}} R_2 \quad (13)$$

ΔV_{OUT} is the output ripple determined by equation 21.

Setting the Output Voltage-Small ESR Caps

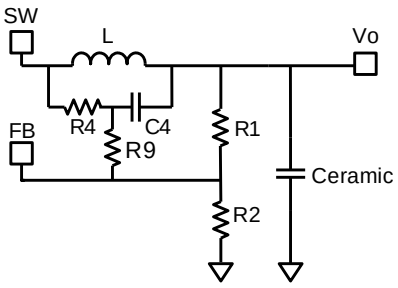


Figure 10—Simplified Circuit of Ceramic Capacitor

When low ESR ceramic capacitor is used in the output, an external voltage ramp should be added to FB through resistor R4 and capacitor C4.The output voltage is influenced by ramp

voltage V_{RAMP} besides R divider as shown in figure 11. The V_{RAMP} can be calculated as shown in equation 7. R2 should be chosen reasonably, a small R2 will lead to considerable quiescent current loss while too large R2 makes the FB noise sensitive. It is recommended to choose a value within 5kΩ-50kΩ for R2, using a comparatively larger R2 when Vo is low, etc.,1.05V, and a smaller R2 when Vo is high. And the value of R1 then is determined as follow:

$$R_1 = \frac{R_2}{\frac{V_{FB(AVG)}}{(V_{OUT} - V_{FB(AVG)})} - \frac{R_2}{R_4 + R_9}} \quad (14)$$

The $V_{FB(AVG)}$ is the average value on the FB, $V_{FB(AVG)}$ varies with the Vin, Vo, and load condition, etc., its value on the skip mode would be lower than that of the PWM mode, which means the load regulation is strictly related to the $V_{FB(AVG)}$. Also the line regulation is related to the $V_{FB(AVG)}$,if one wants to gets a better load or line regulation, a lower Vramp is suggested once it meets equation 9.

For PWM operation, $V_{FB(AVG)}$ value can be deduced from equation 15.

$$V_{FB(AVG)} = V_{REF} + \frac{1}{2} V_{RAMP} \times \frac{R_1 // R_2}{R_1 // R_2 + R_9} \quad (15)$$

Usually, R9 is set to 0Ω, and it can also be set following equation 16 for a better noise immunity. It should also set to be 5 timers smaller than R1//R2 to minimize its influence on Vramp.

$$R_9 \le \frac{1}{2\pi \times C_4 \times 2F_{SW}} \quad (16)$$

Using equation 14 to calculate the output voltage can be complicated. To simplify the calculation of R1 in equation 14, a DC-blocking capacitor Cdc can be added to filter the DC influence from R4 and R9. Figure 12 shows a simplified circuit with external ramp compensation and a DC-blocking capacitor. With this capacitor, R1 can easily be obtained by using equation 17 for PWM mode operation.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2017 MPS. All Rights Reserved.

$$R_1 = \frac{(V_{OUT} - V_{REF} - \frac{1}{2}V_{RAMP})}{V_{REF} + \frac{1}{2}V_{RAMP}} R_2 \quad (17)$$

Cdc is suggested to be at least 10 times larger than C4 for better DC blocking performance, and should also not larger than 0.47μF considering start up performance. In case one wants to use larger Cdc for a better FB noise immunity, combined with reduced R1 and R2 to limit the Cdc in a reasonable value without affecting the system start up. Be noted that even when the Cdc is applied, the load and line regulation are still Vramp related.

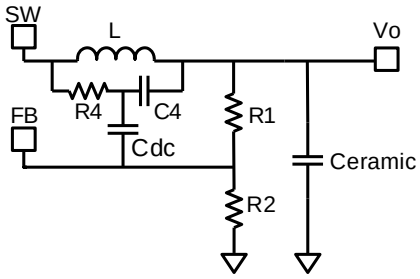


Figure 11—Simplified Circuit of Ceramic Capacitor with DC blocking capacitor

Input Capacitor

The input current to the step-down converter is discontinuous. Therefore, a capacitor is required to supply the AC current to the step-down converter while maintaining the DC input voltage. Ceramic capacitors are recommended for best performance. In the layout, it's recommended to put the input capacitors as close to the IN pin as possible.

The capacitance varies significantly over temperature. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are fairly stable over temperature.

The capacitors must also have a ripple current rating greater than the maximum input ripple current of the converter. The input ripple current can be estimated as follows:

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (18)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (19)$$

For simplification, choose the input capacitor whose RMS current rating is greater than half of the maximum load current.

The input capacitance value determines the input voltage ripple of the converter. If there is input voltage ripple requirement in the system design, choose the input capacitor that meets the specification

The input voltage ripple can be estimated as follows:

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (20)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{F_{SW} \times C_{IN}} \quad (21)$$

Output Capacitor

The output capacitor is required to maintain the DC output voltage. Ceramic or POSCAP capacitors are recommended. The output voltage ripple can be estimated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times F_{SW} \times C_{OUT}}) \quad (22)$$

In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times F_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (23)$$

The output voltage ripple caused by ESR is very small. Therefore, an external ramp is needed to stabilize the system. The external ramp can be generated through resistor R4 and capacitor C4 following equation 5, 8 and 9.

In the case of POSCAP capacitors, the ESR dominates the impedance at the switching frequency. The ramp voltage generated from the ESR is high enough to stabilize the system. Therefore, an external ramp is not needed. A minimum ESR value around 12mΩ is required to ensure stable operation of the converter. For

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2017 MPS. All Rights Reserved.

simplification, the output ripple can be approximated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (24)$$

Inductor

The inductor is required to supply constant current to the output load while being driven by the switching input voltage. A larger value inductor will result in less ripple current that will result in lower output ripple voltage. However, a larger value inductor will have a larger physical size, higher series resistance, and/or lower saturation current. A good rule for determining the inductor value is to allow the peak-to-peak ripple current in the inductor to be approximately 30~40% of the maximum switch current limit. Also, make sure that the peak inductor current is below the maximum switch current limit. The inductance value can be calculated as:

$$L = \frac{V_{OUT}}{F_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (25)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

Choose an inductor that will not saturate under the maximum inductor peak current. The peak inductor current can be calculated as:

$$I_{LP} = I_{OUT} + \frac{V_{OUT}}{2F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (26)$$

The inductors listed in Table 1 are highly recommended for the high efficiency they can provide.

Table 1—Inductor Selection Guide

Part Number	Manufacturer	Inductance (µH)	DCR (mΩ)	Current Rating (A)	Dimensions L x W x H (mm^3)	Switching Frequency (kHz)
PCMC-135T-R68MF	Cyntec	0.68	1.7	34	13.5 x 12.6 x 4.8	600
FDA1254-1R0M	TOKO	1	2	25.2	13.5 x 12.6 x 5.4	300~600
FDA1254-1R2M	TOKO	1.2	2.05	20.2	13.5 x 12.6 x 5.4	300~600

Typical Design Parameter Tables

The following tables include recommended component values for typical output voltages (1.2V, 2.5V, 3.3V) and switching frequencies (300kHz, 500kHz, and 700kHz). Refer to Tables 2-4 for design cases without external ramp compensation and Tables 5-7 for design cases with external ramp compensation. External ramp is not needed when high-ESR capacitors, such as electrolytic or POSCAPs are used. External ramp is needed when low-ESR capacitors, such as ceramic capacitors are used. For cases not listed in this datasheet, a calculator in excel spreadsheet can also be requested through a local sales representative to assist with the calculation.

Table 2—300kHz, $12V_{IN}$

V_{OUT} (V)	L (µH)	R1 (kΩ)	R2 (kΩ)	R7 (kΩ)
1.2	2.2	12.1	26.1	750
2.5	2.2	30	14.3	1500
3.3	1	40.2	13.3	1600

Table 3—500kHz, $12V_{IN}$

V_{OUT} (V)	L (µH)	R1 (kΩ)	R2 (kΩ)	R7 (kΩ)
1.2	1	12.1	26.1	442
2.5	1	30	14.3	845
3.3	1	40.2	13.3	1000

Table 4—700kHz, $12V_{IN}$

V_{OUT} (V)	L (µH)	R1 (kΩ)	R2 (kΩ)	R7 (kΩ)
1.2	1	12.1	26.1	316
2.5	1	30	14.3	590
3.3	1	40.2	13.3	806

Table 5—300kHz, $12V_{IN}$

V_{OUT} (V)	L (µH)	R1 (kΩ)	R2 (kΩ)	R4 (kΩ)	C4 (pF)	R7 (kΩ)
1.2	2.2	12.1	26.1	330	220	750
2.5	2.2	30	14.3	402	220	1500
3.3	2.2	40.2	12.4	422	220	1600

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2017 MPS. All Rights Reserved.

Table 6—500kHz, $12V_{IN}$

V_{OUT} (V)	L (µH)	R1 (kΩ)	R2 (kΩ)	R4 (kΩ)	C4 (pF)	R7 (kΩ)
1.2	1	12.1	26.1	374	220	442
2.5	1	30	14.3	412	220	845
3.3	1	40.2	12.4	422	220	1000

Table 7—700kHz, $12V_{IN}$

V_{OUT} (V)	L (µH)	R1 (kΩ)	R2 (kΩ)	R4 (kΩ)	C4 (pF)	R7 (kΩ)
1.2	1	12.1	26.1	240	220	316
2.5	1	30	14.3	412	220	590
3.3	1	40.2	12.4	422	220	806

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2017 MPS. All Rights Reserved.

TYPICAL APPLICATION

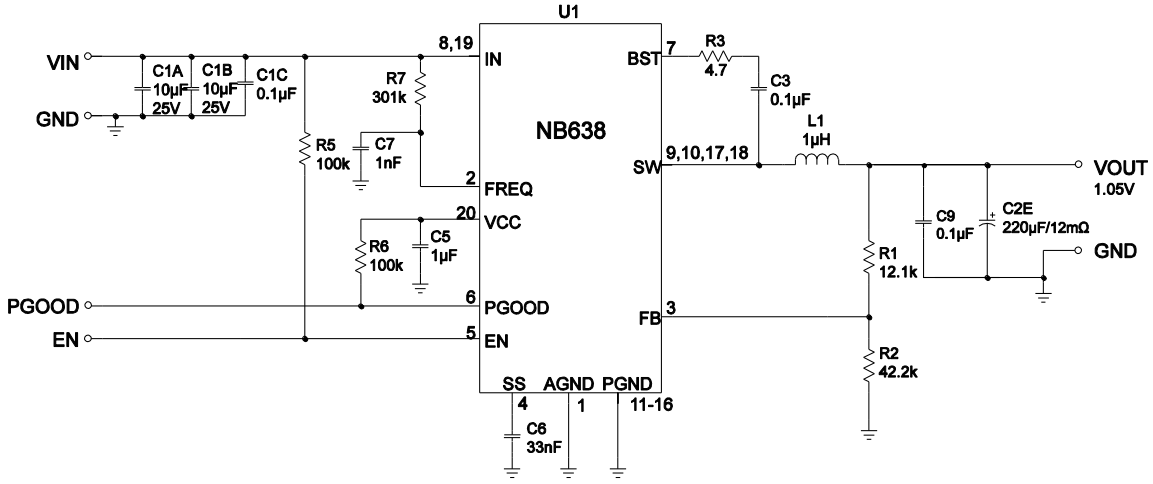


Figure 12 — Typical Application Circuit with No External Ramp

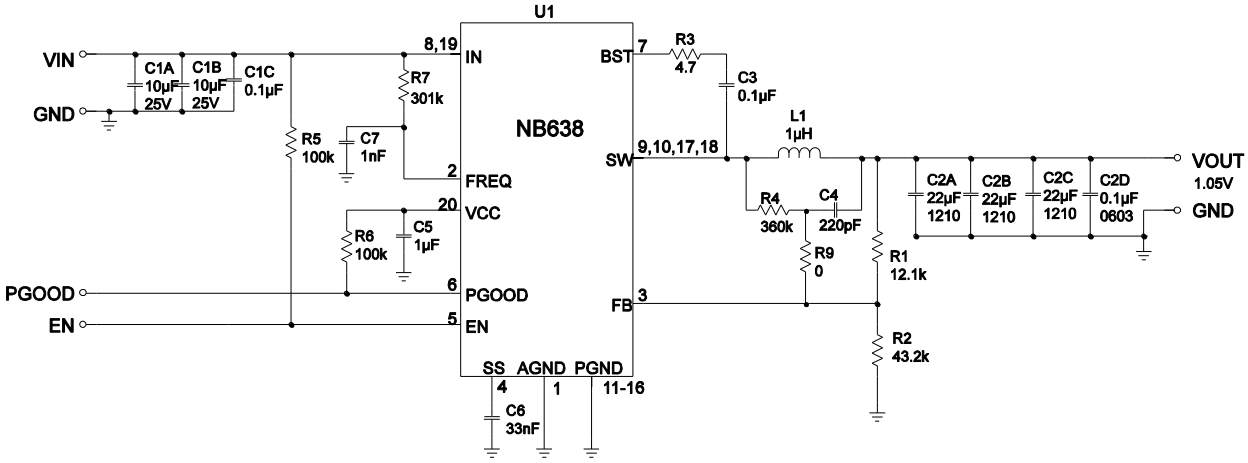


Figure 13 — Typical Application Circuit with Low ESR Ceramic Capacitor

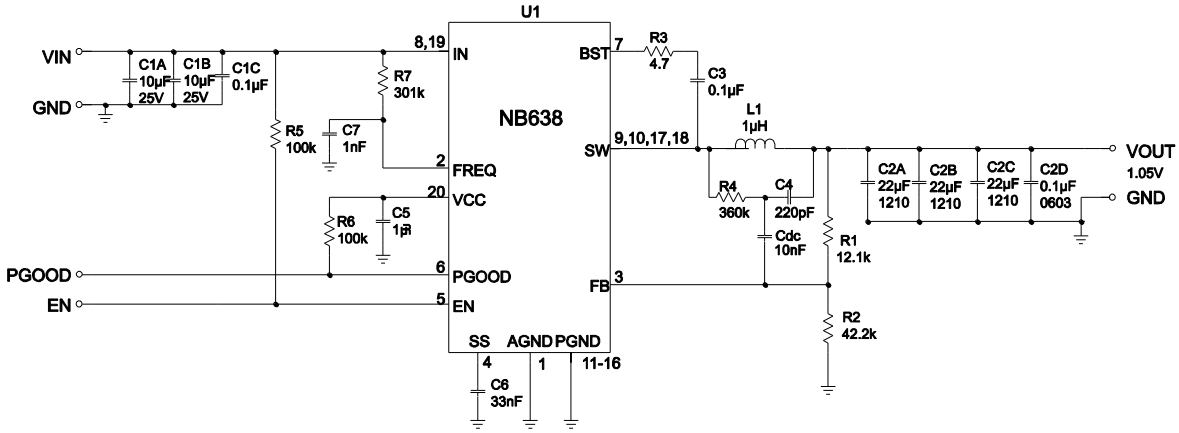
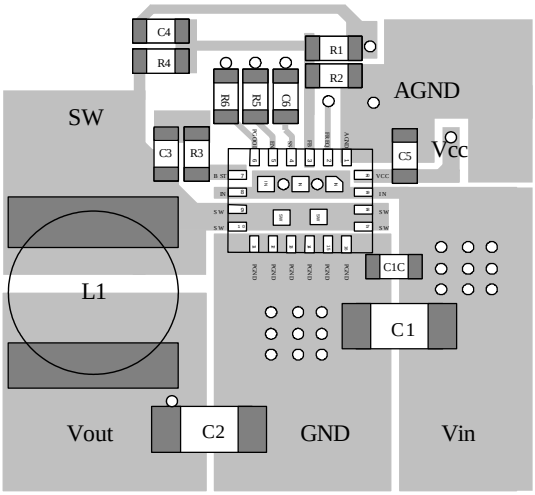


Figure 14 — Typical Application Circuit with Low ESR Ceramic Capacitor and DC-Blocking Capacitor.

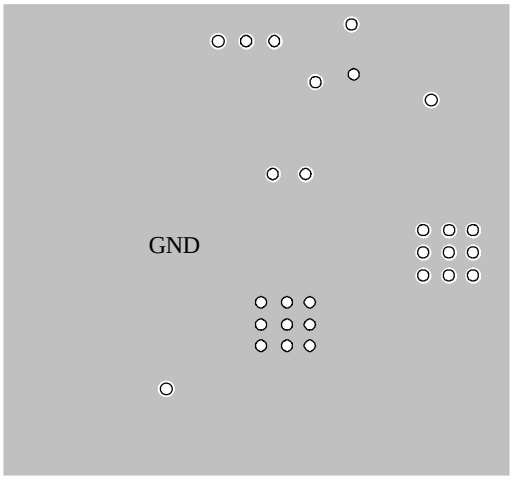
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2017 MPS. All Rights Reserved.

LAYOUT RECOMMENDATION

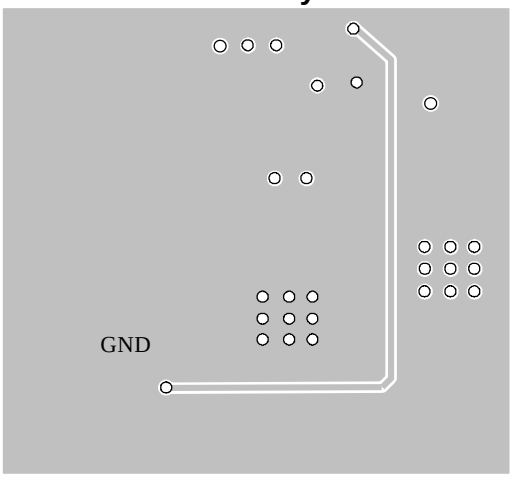
1. The high current paths (GND, IN, and SW) should be placed very close to the device with short, direct and wide traces.
2. Put the input capacitors as close to the IN and GND pins as possible.
3. Put the decoupling capacitor as close to the V_{CC} and GND pins as possible.
4. Keep the switching node SW short and away from the feedback network.
5. The external feedback resistors should be placed next to the FB pin. Make sure that there is no via on the FB trace.
6. Keep the BST voltage path (BST, C3, and SW) as short as possible.
7. Keep the bottom IN and SW pads connected with large copper to achieve better thermal performance.
8. Four-layer layout is strongly recommended to achieve better thermal performance.



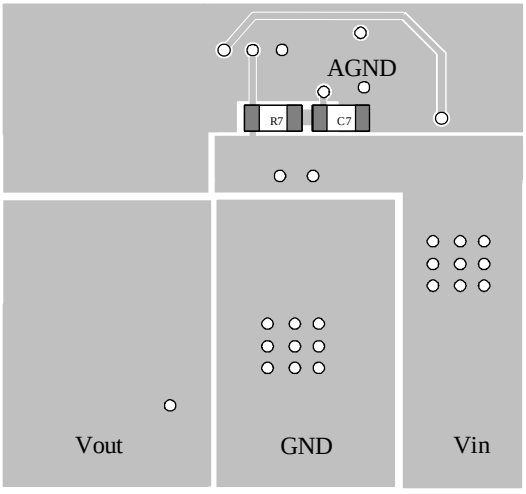
Top Layer



Inner1 Layer



Inner2 Layer



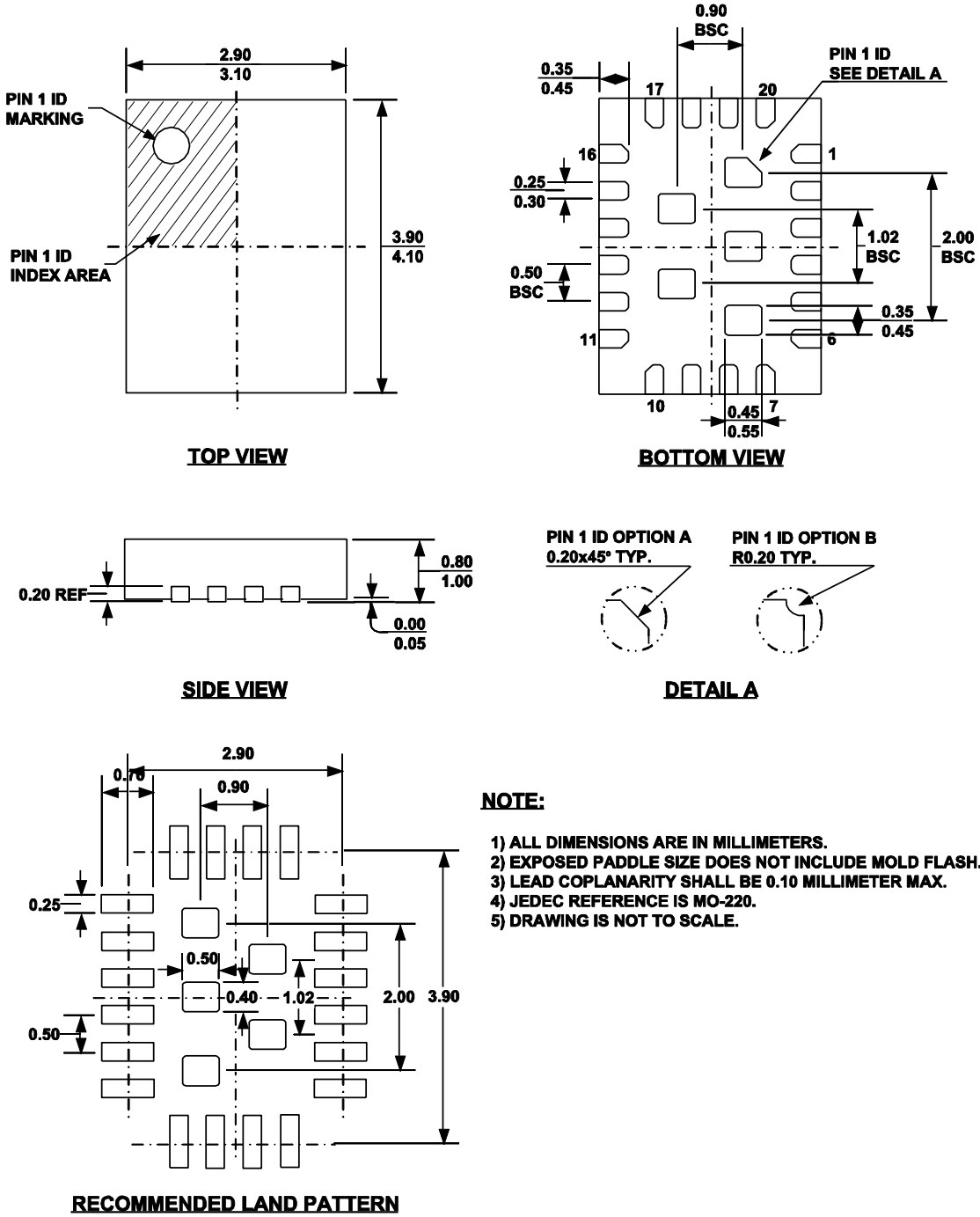
Bottom Layer

Figure 15—PCB Layout

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2017 MPS. All Rights Reserved.

PACKAGE INFORMATION

QFN-20 (3mmx4mm)



NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

NOTICE: The information in this document is subject to change without notice. Users should warrant and guarantee that third party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2017 MPS. All Rights Reserved.