




REVISION CONTROL

Rev 1.0 - Jan 11, 2018, Initial Board Release  
Copied from Si5341 schematic. Updated  
PCB, label, DUT, and ID resistors. tturner

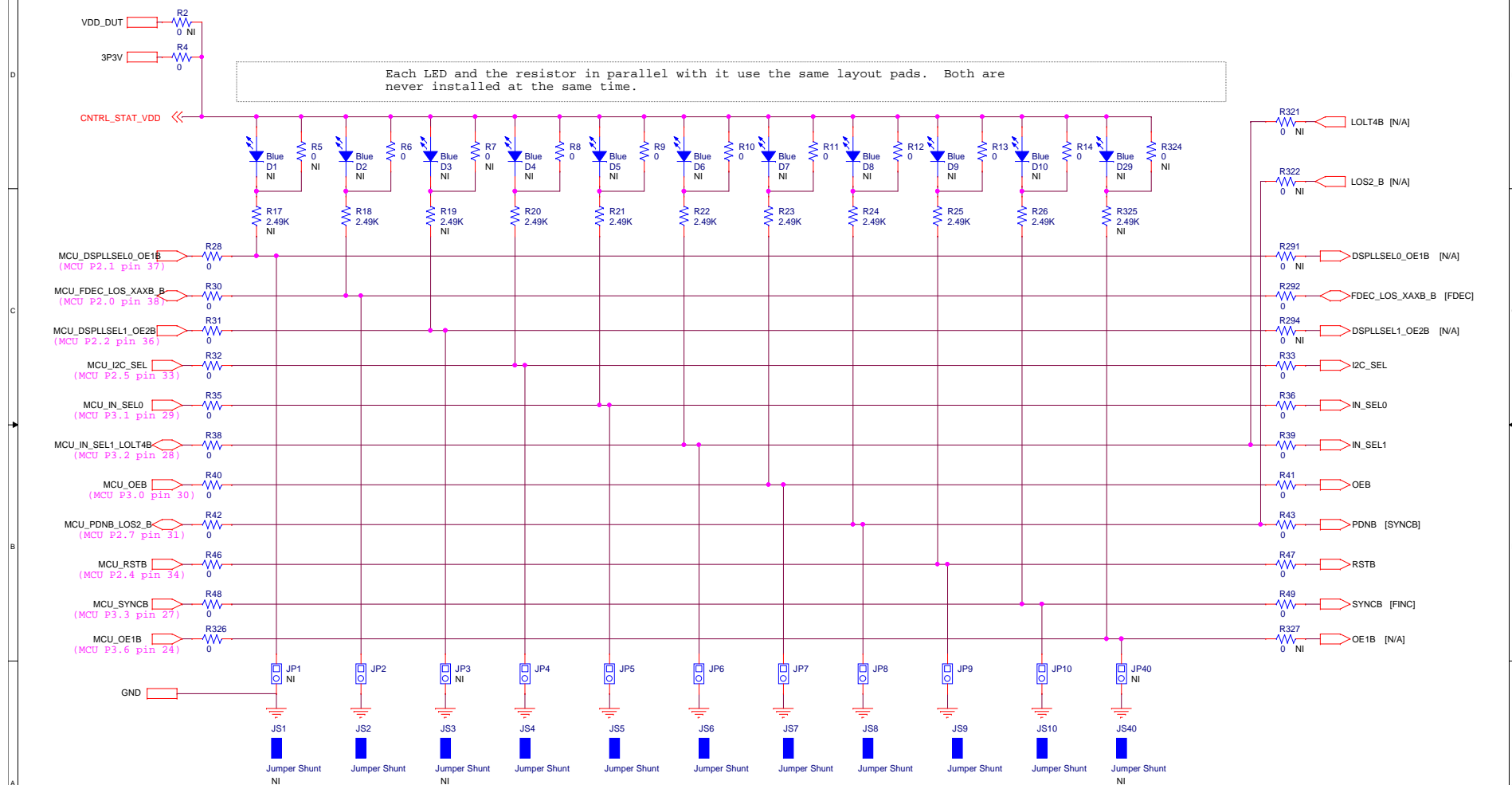
Rev 1.1 - May 24, 2018, Changed U2 from PCA9517D to  
PCA9517AD,118 (this was needed to make sure the NXP  
part is ordered instead of the TI version)

Rev1.2 - May 30, 2018, Changed J39 and J40 to not installed (external reference)

Rev 1.3 - June 6, 2018, Changed J1, J2, J3, J4, J5, J6  
J7 and J8 to not installed

		400 W Cesar Chavez Austin, TX 78701	
SILICON LABS			
Title SI5341-EB_TOP_REVISION			
Size B	Document Number SI5391P-A-EB		Rev 1.3
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# CONTROL PINS CONNECTIONS



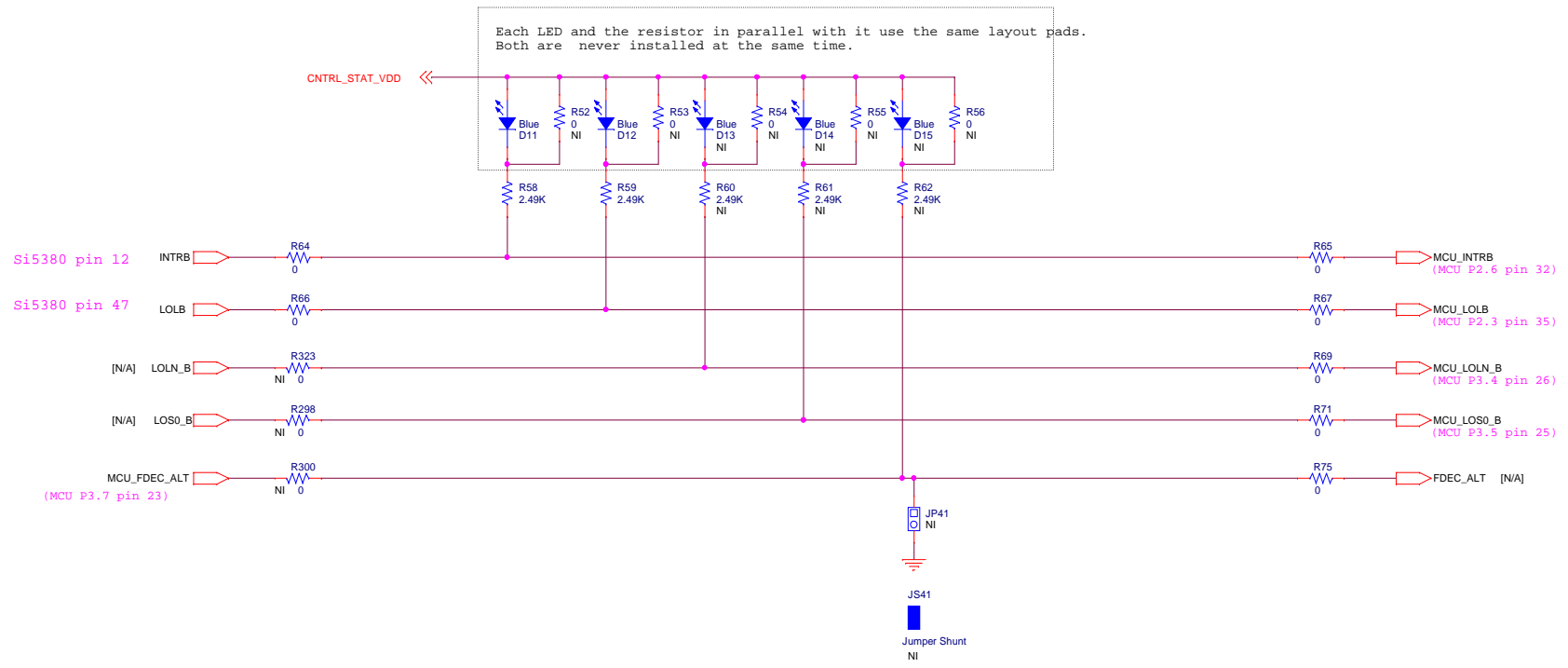
## Note:

1. If the net name differs from the DUT pin name, the corresponding DUT pin name is enclosed in brackets. [DUT Pin Name]

2. "N/A" in brackets indicates that the function is not used for the DUT. [N/A]

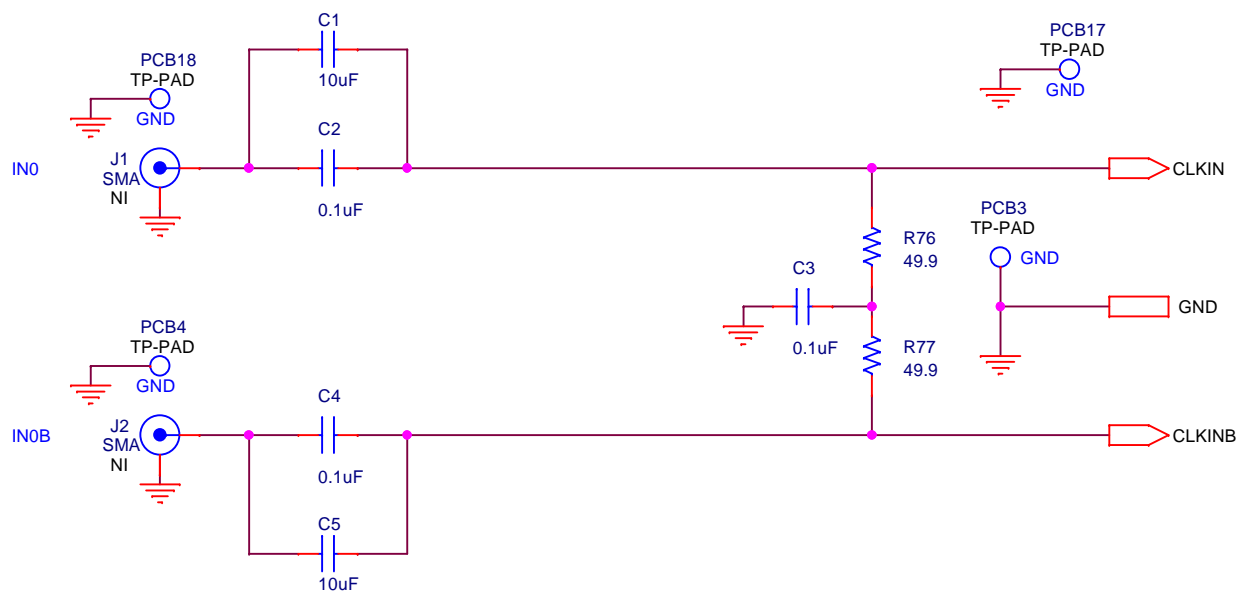
400 W Cesar Chavez Austin, TX 78701		
Title CONTROL PINS_P1		
Size B	Document Number SI5391P-A-EB	Rev 1.3
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# CONTROL PINS CONNECTIONS

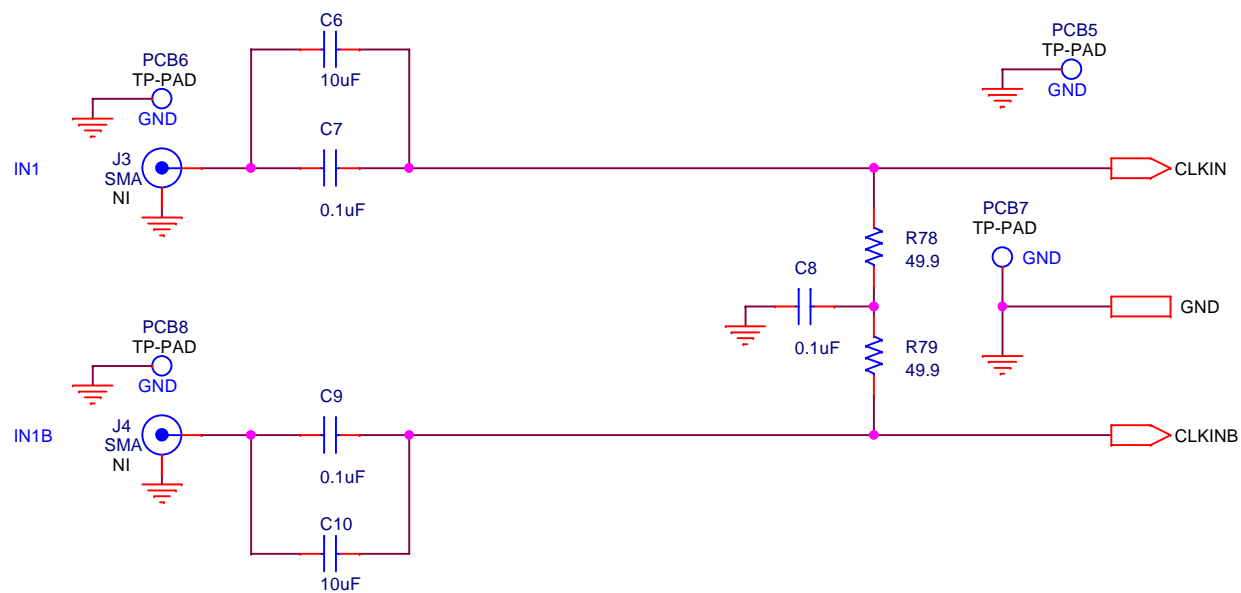



Note:  
1. "N/A" in brackets indicates that the function is not used for the DUT. [N/A]

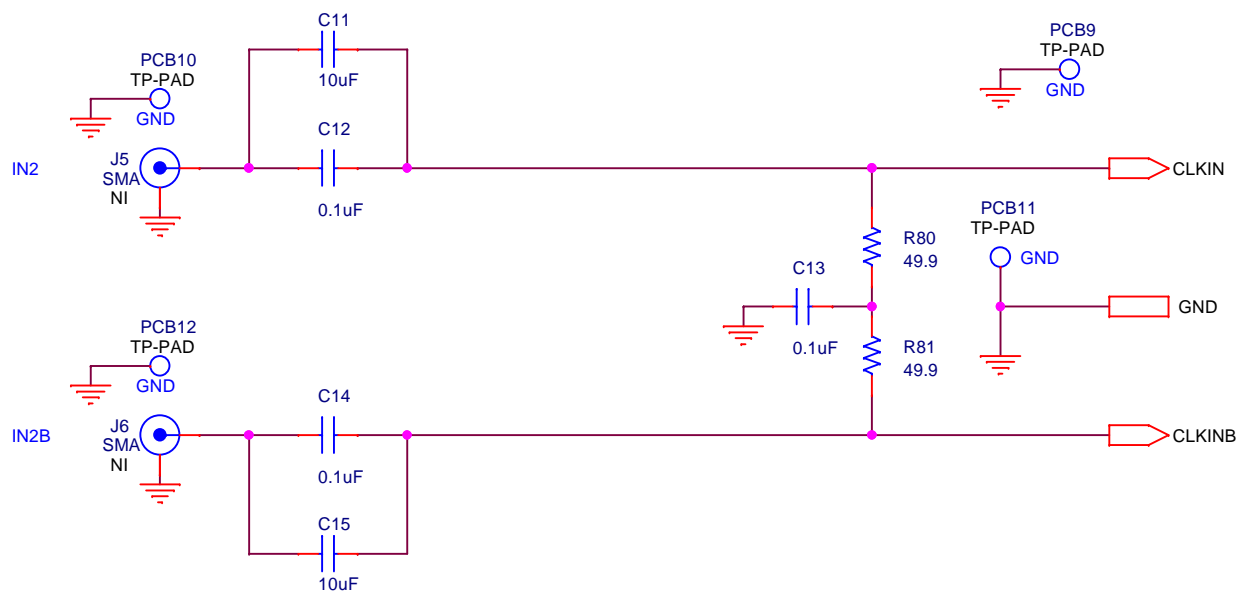
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Title CONTROL_PINS_P2		
Size B	Document Number SI5391P-A-EB	Rev 1.3
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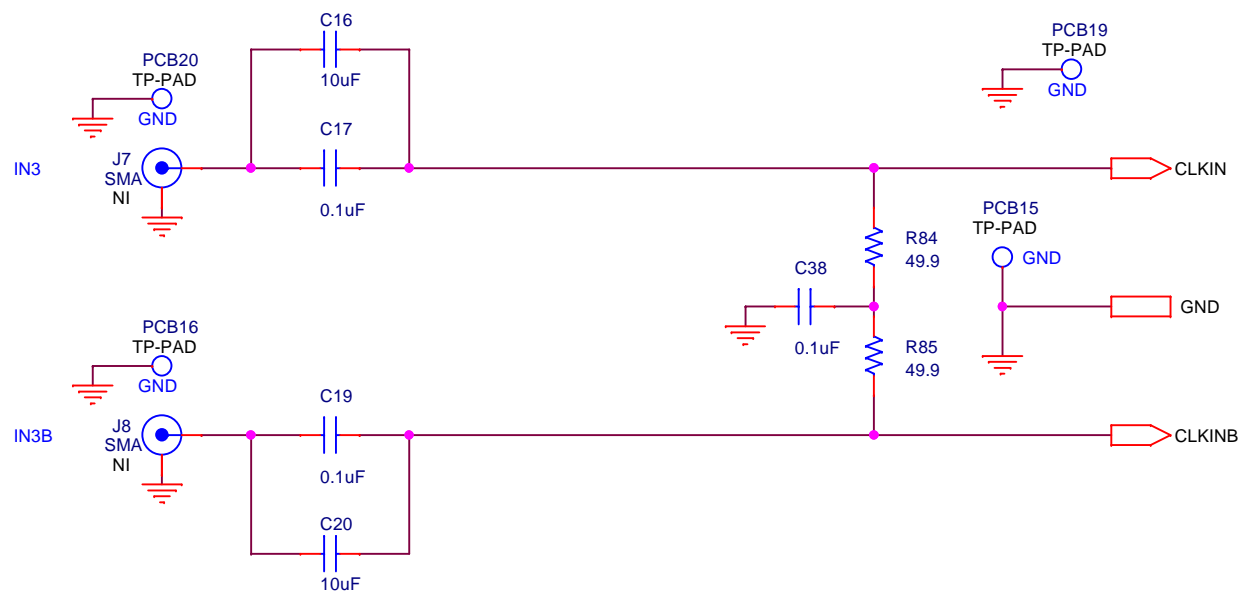
 400 W Cesar Chavez Austin, TX 78701		
Title DIFF_INPUT_CLK		
Size A	Document Number SI5391P-A-EB	Rev 1.3
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 400 W Cesar Chavez Austin, TX 78701		
Title DIFF_INPUT_CLK		
Size A	Document Number SI5391P-A-EB	Rev 1.3
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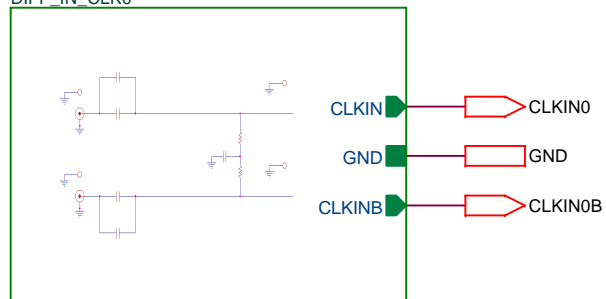
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Title DIFF_INPUT_CLK		
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Title DIFF_INPUT_CLK		
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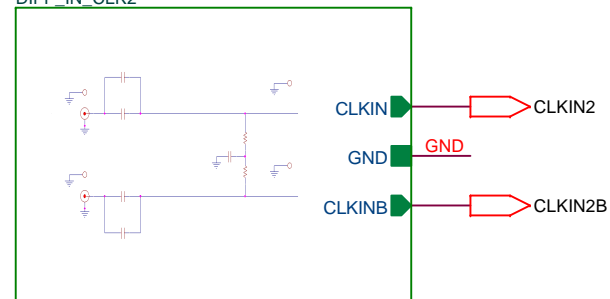


DIFF\_IN\_CLK0



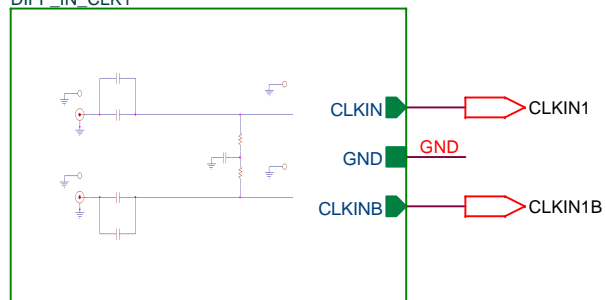
DIFF\_INPUT\_CLK

DIFF\_IN\_CLK2



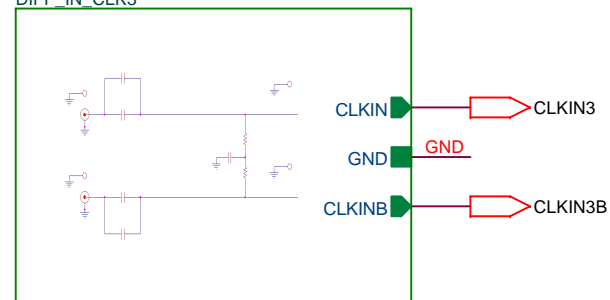
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DIFF\_IN\_CLK1

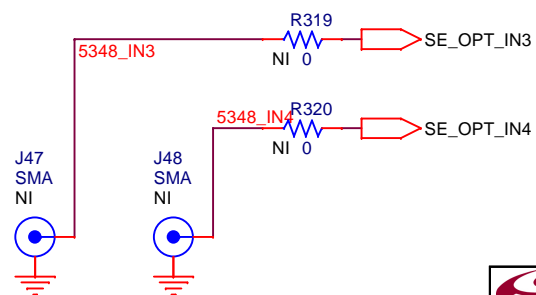


DIFF\_INPUT\_CLK

DIFF\_IN\_CLK3



DIFF\_INPUT\_CLK



Single-ended clocks only.



400 W Cesar Chavez  
Austin, TX 78701

Title

DIFF\_INPUT\_CLOCKS\_4

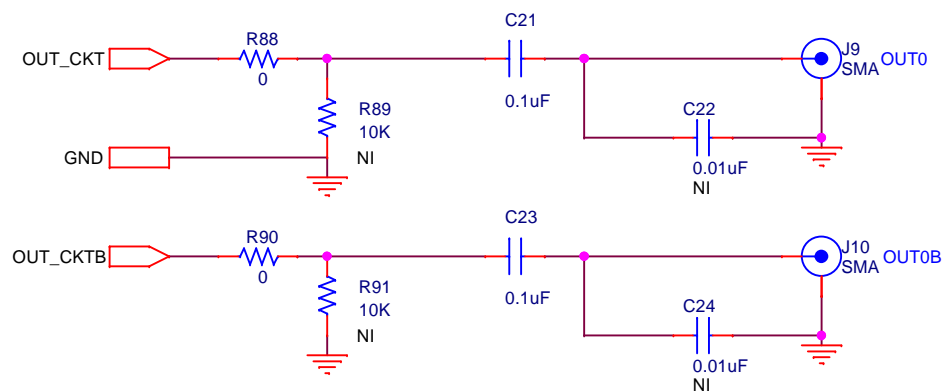
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Document Number  
SI5391P-A-EB

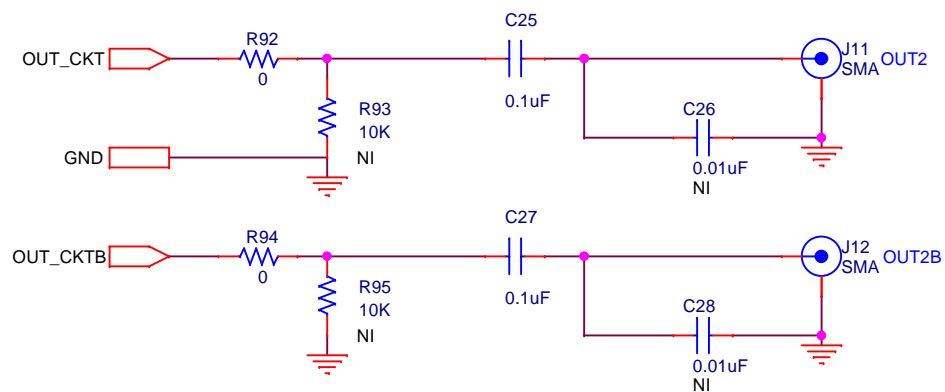
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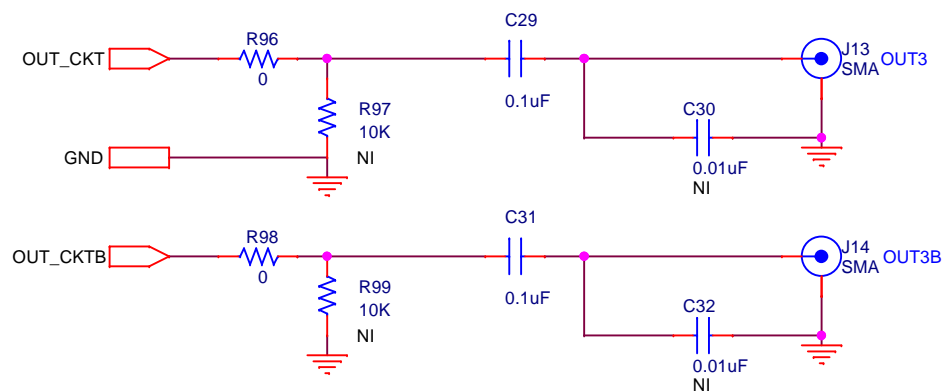
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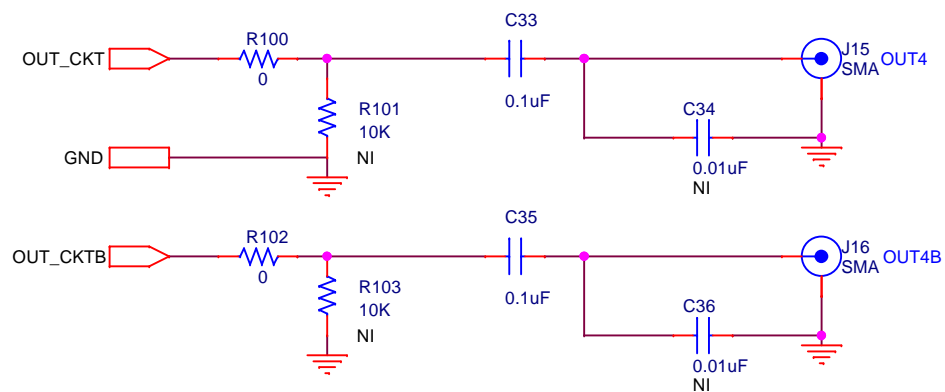
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Title DIFF_OUTPUT_CLK		
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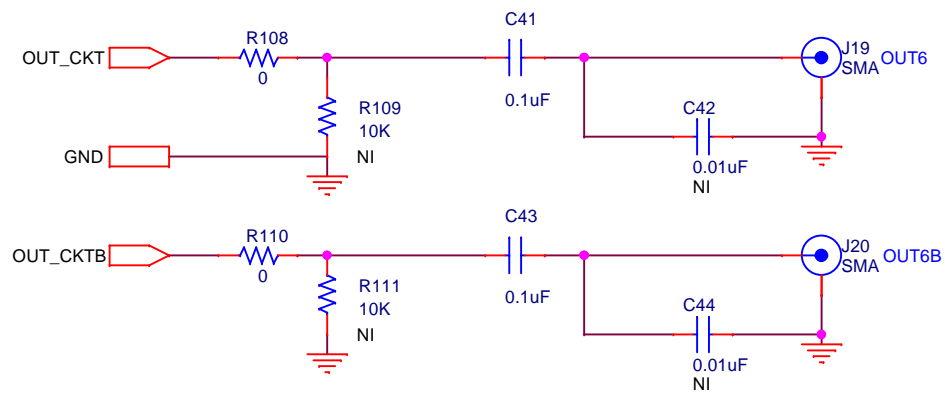
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Title DIFF_OUTPUT_CLK		
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 400 W Cesar Chavez Austin, TX 78701		
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400 W Cesar Chavez  
Austin, TX 78701

Title

DIFF\_OUTPUT\_CLK

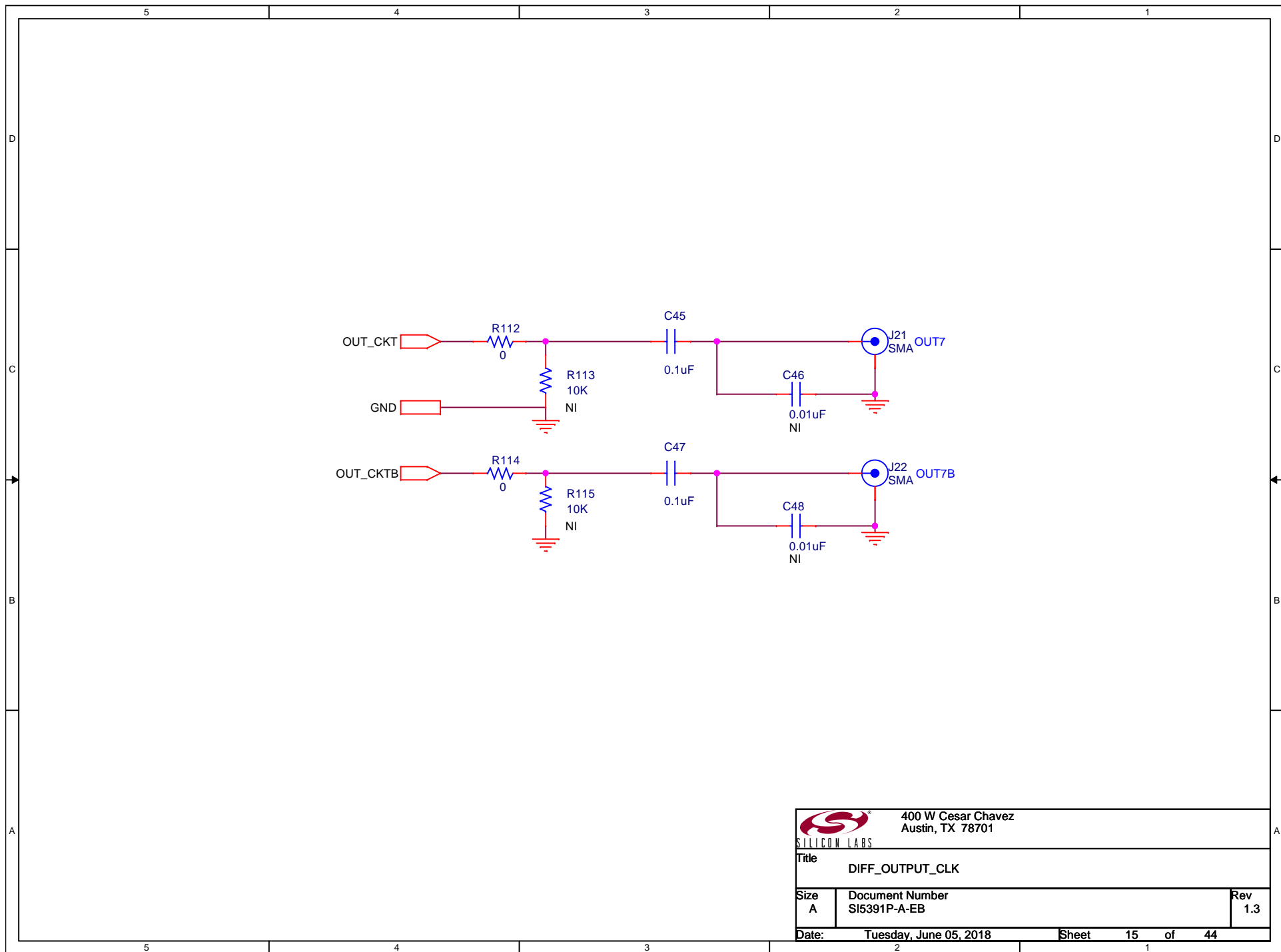
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Document Number  
SI5391P-A-EB

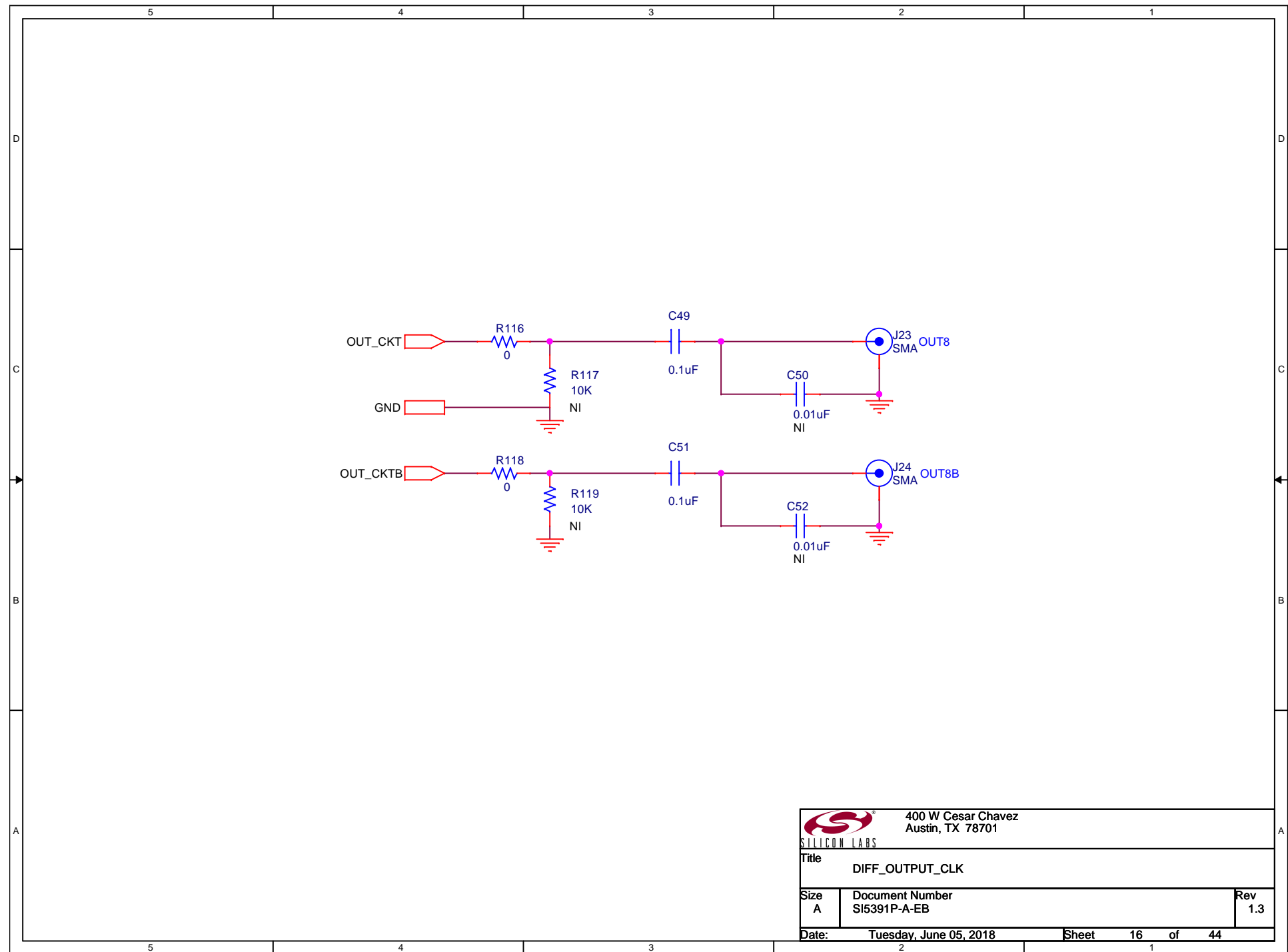
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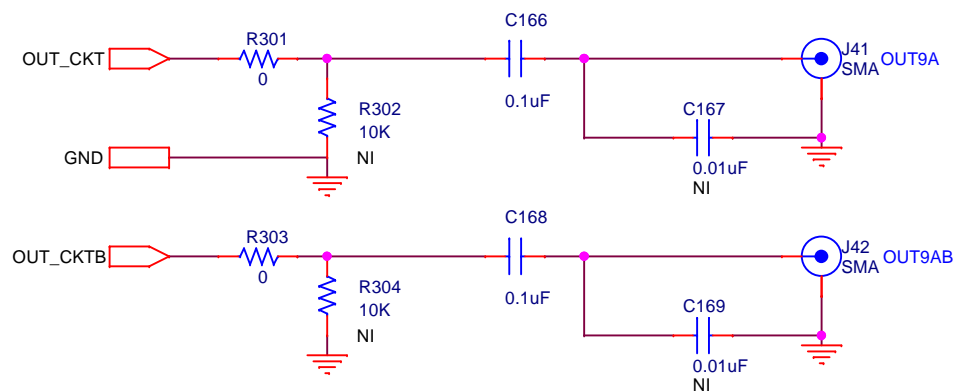



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Title DIFF_OUTPUT_CLK		
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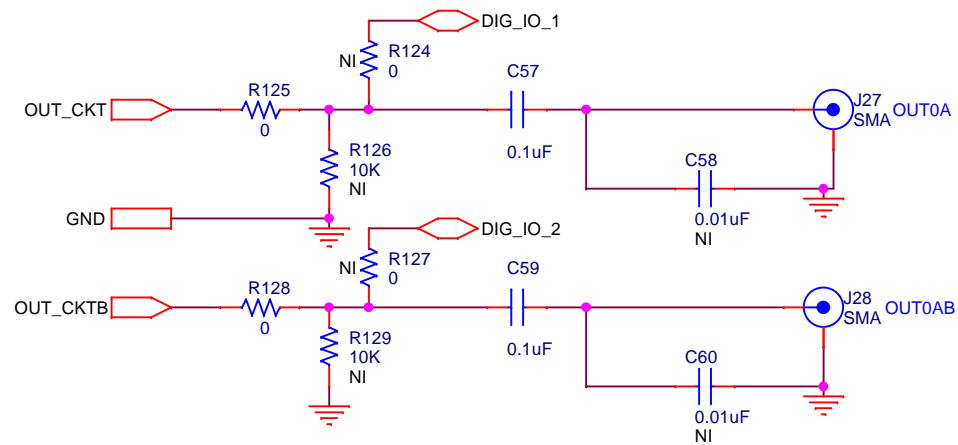
 400 W Cesar Chavez Austin, TX 78701		
Title DIFF_OUTPUT_CLK		
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 400 W Cesar Chavez Austin, TX 78701		
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# DIFF\_OUTPUT\_CLK\_DIG\_IO



400 W Cesar Chavez  
Austin, TX 78701

Title

DIFF\_OUTPUT\_CLK\_DIG\_IO

Size

A

Document Number

SI5391P-A-EB

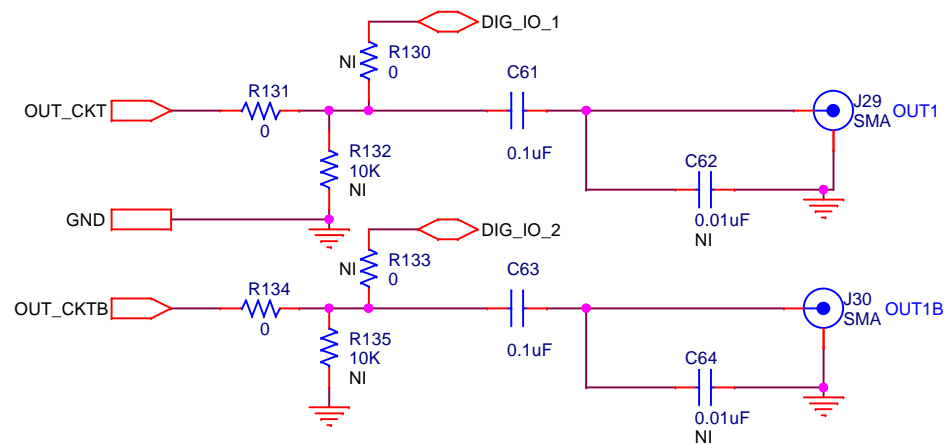
Rev

1.3

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# DIFF\_OUTPUT\_CLK\_DIG\_IO



400 W Cesar Chavez  
Austin, TX 78701

Title

DIFF\_OUTPUT\_CLK\_DIG\_IO

Size

A

Document Number

SI5391P-A-EB

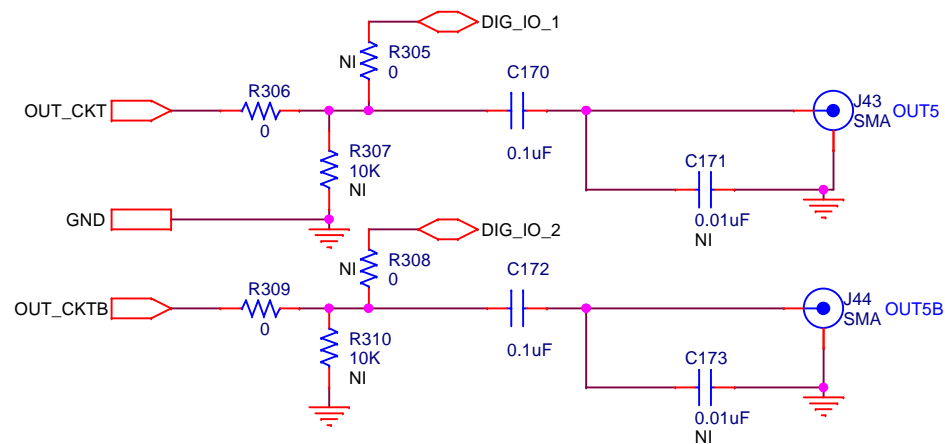
Rev

1.3

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# DIFF\_OUTPUT\_CLK\_DIG\_IO



400 W Cesar Chavez  
Austin, TX 78701

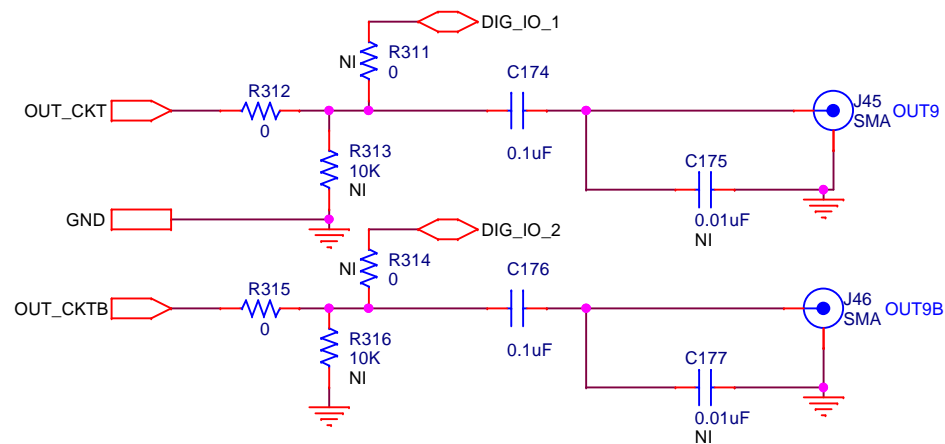
Title  
DIFF\_OUTPUT\_CLK\_DIG\_IO

Size  
A Document Number  
SI5391P-A-EB

Rev  
1.3

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# DIFF\_OUTPUT\_CLK\_DIG\_IO



400 W Cesar Chavez  
Austin, TX 78701

Title

DIFF\_OUTPUT\_CLK\_DIG\_IO

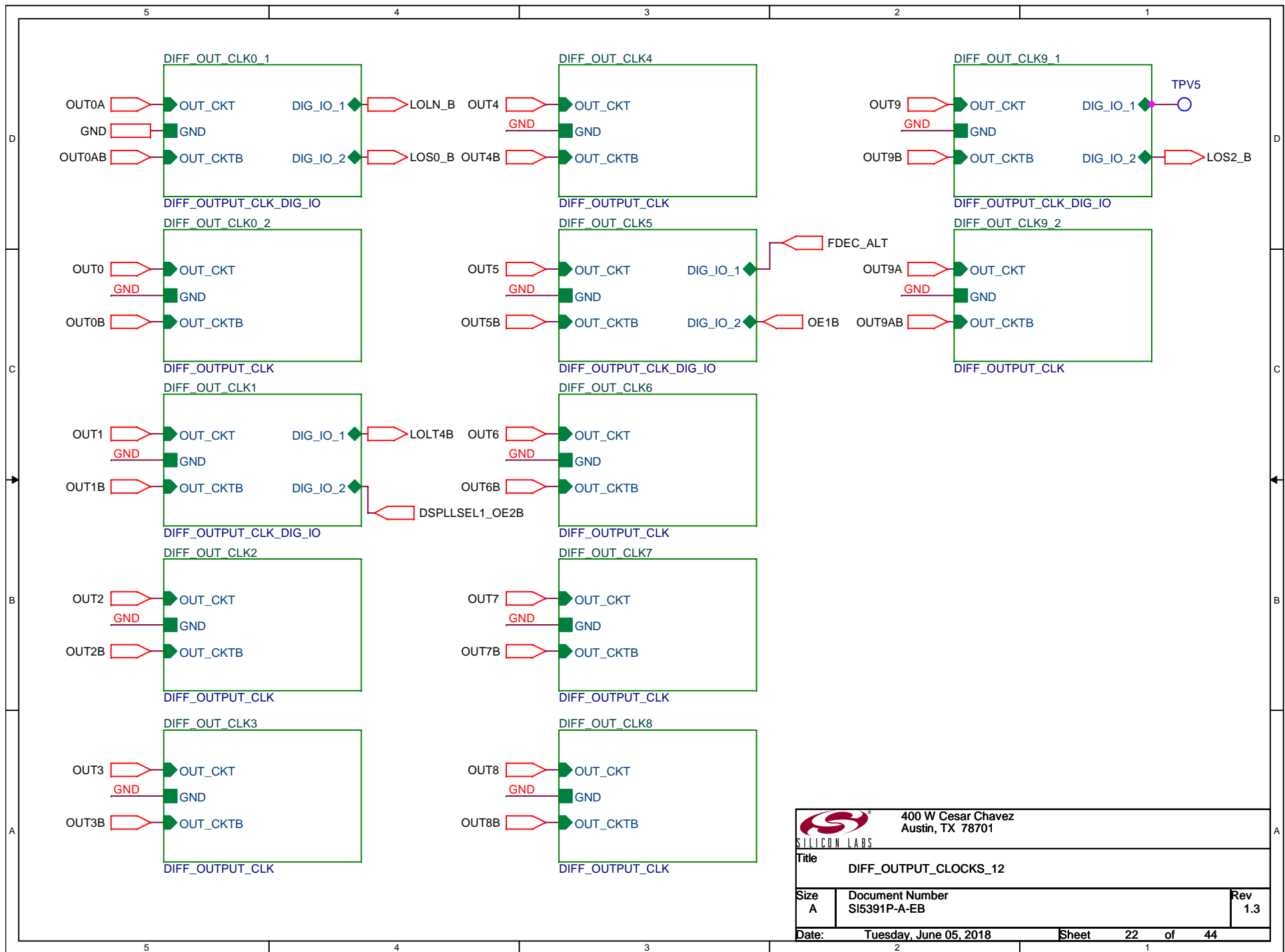
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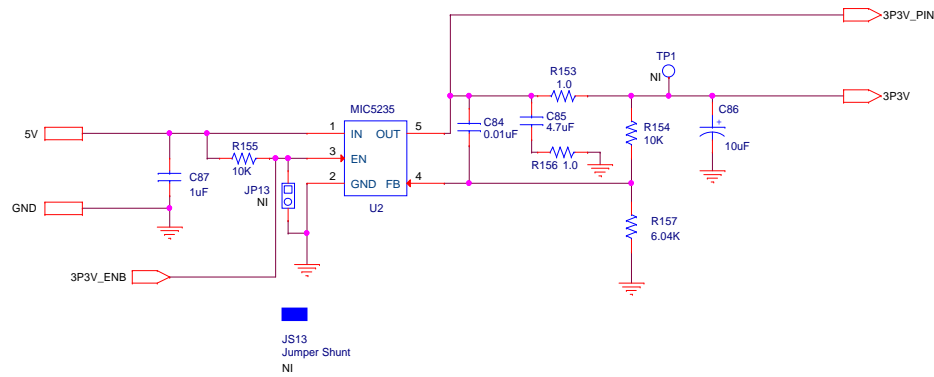
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1.3

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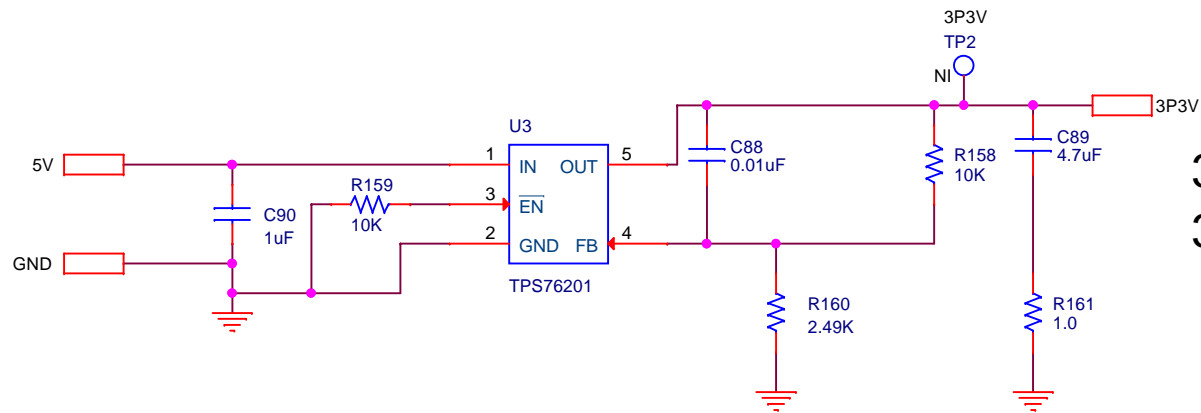
## Fixed 3.3V 150 mA Voltage Regulator




3P3V\_DUT (In Schematic)  
VDDA DUT (Board Silkscreen)

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Title		VDD_REG_MIC5235	
Size	Document Number	Rev	
B	SI5391P-A-EB	1.3	
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# Fixed 3.3V 100 mA Voltage Regulator (Enabled, no current measurement supported.)



3P3V (In Schematic)  
3P3V (Board Silkscreen)

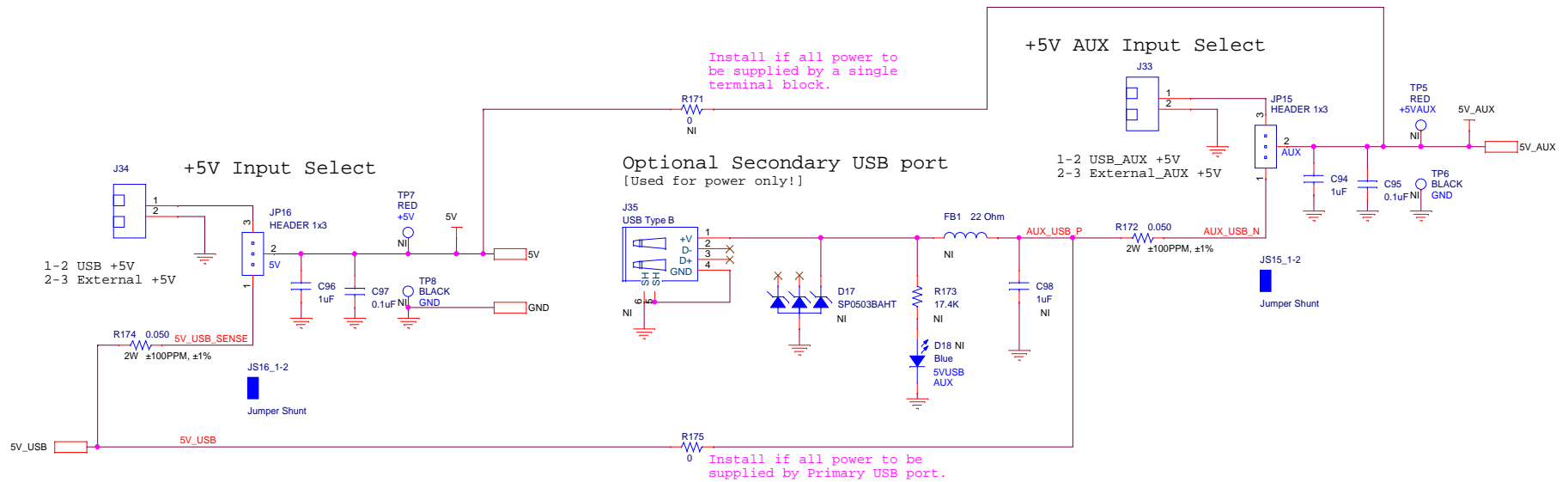
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Title			
FIXED_3V3_REG_TPS76201_EN_NO_IM			
Size A	Document Number SI5391P-A-EB		Rev 1.3
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# MAIN POWER INPUT SELECTS

## EXTERNAL OR USB

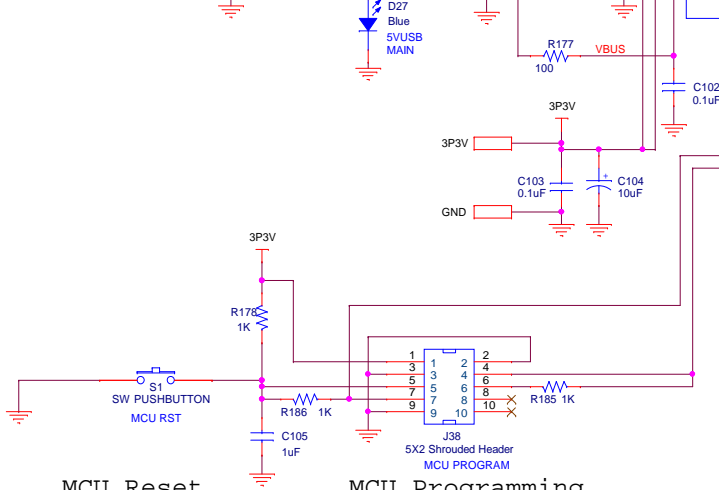
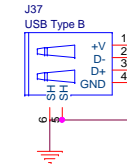
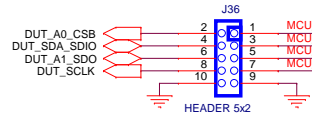


 400 W Cesar Chavez Austin, TX 78701		
Title		
MAIN_POWER_CONNECTIONS		
Size	Document Number	Rev
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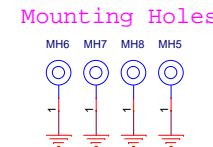
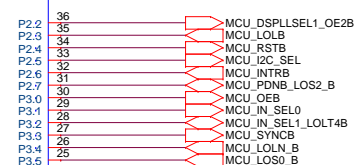
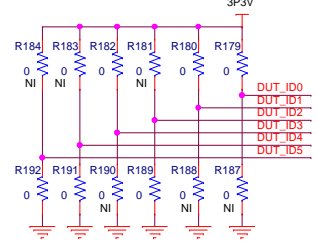
# 8051 MCU

## Jumper Shunts

- JS36\_1-2
- JS36\_3-4
- JS36\_5-6
- JS36\_7-8
- JS36\_9-10

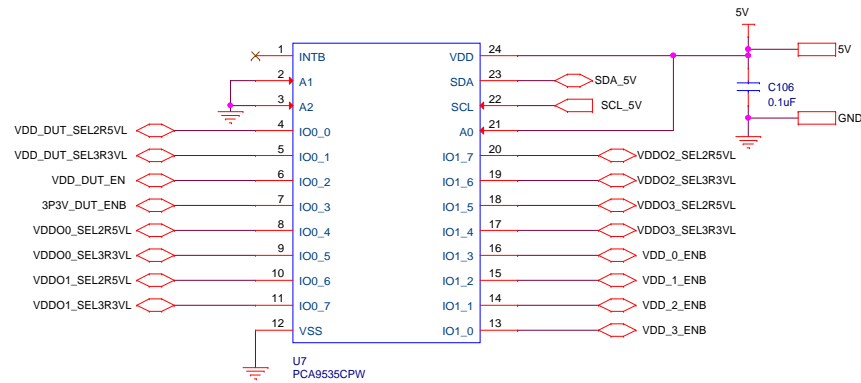


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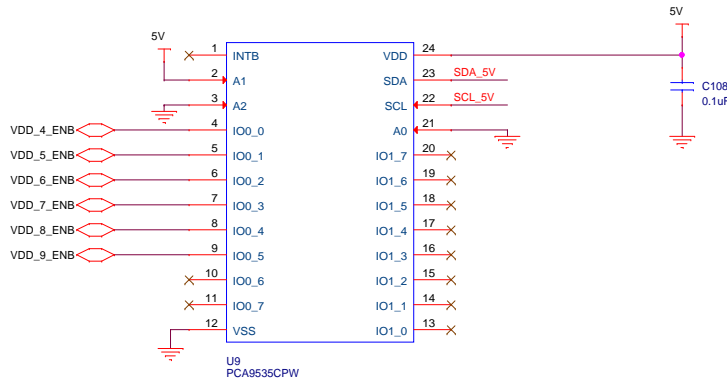


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Title		MCU	
Size	Document Number	Rev	
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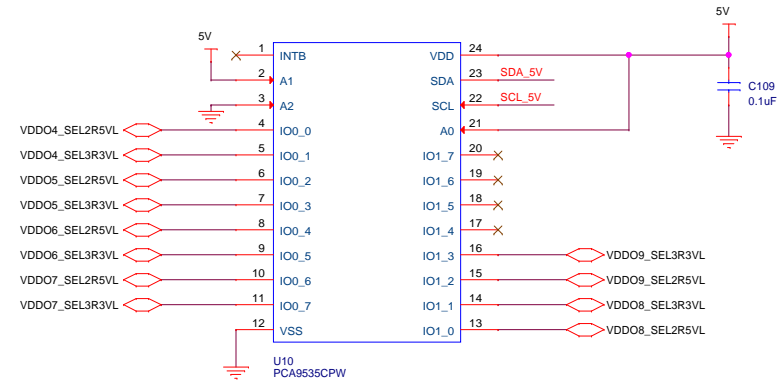
# PERIPHERALS



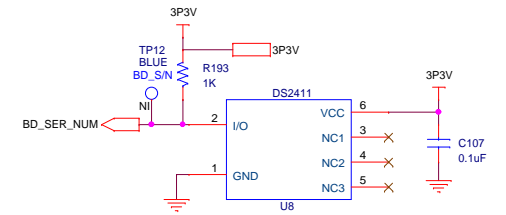
I2C VDD ENABLES/SELECTS FOR REGULATORS  
I2C address: 0100001




I2C VDD ENABLES/SELECTS FOR REGULATORS  
I2C address: 0100010

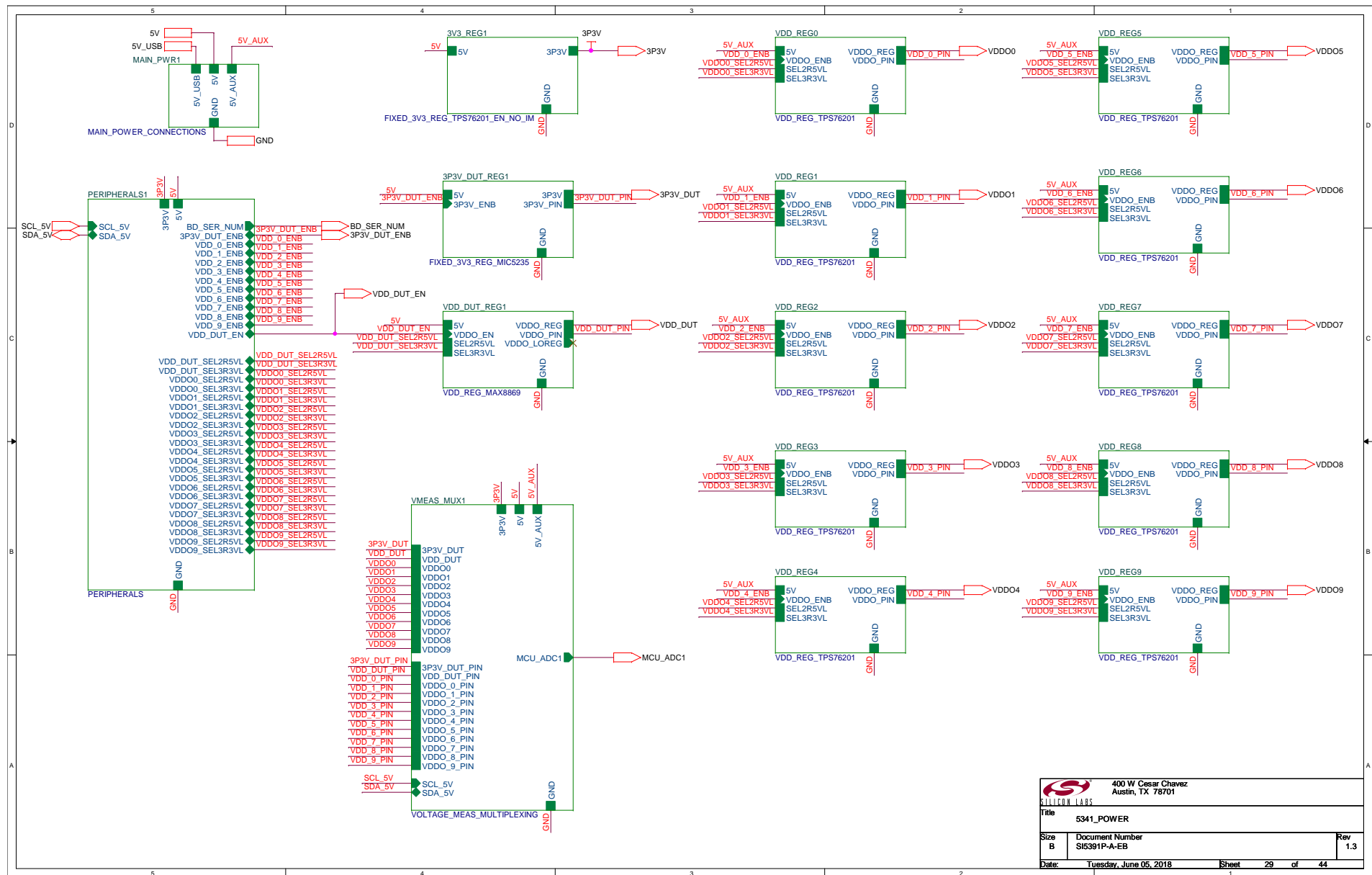


I2C VDD ENABLES/SELECTS FOR REGULATORS  
I2C address: 0100011

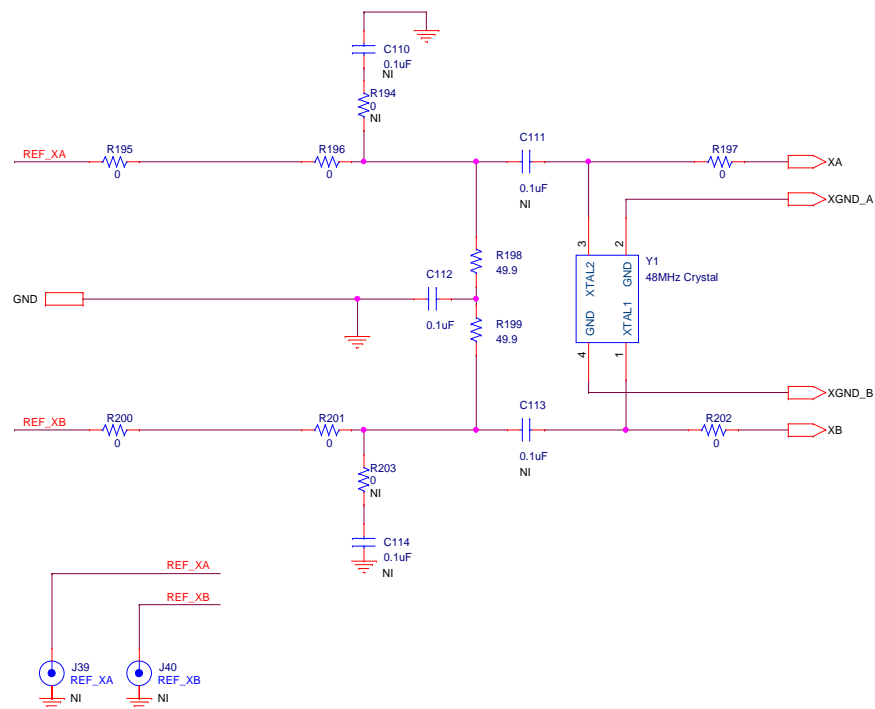



Board Serial Number

		400 W Cesar Chavez Austin, TX 78701	
Title PERIPHERALS			
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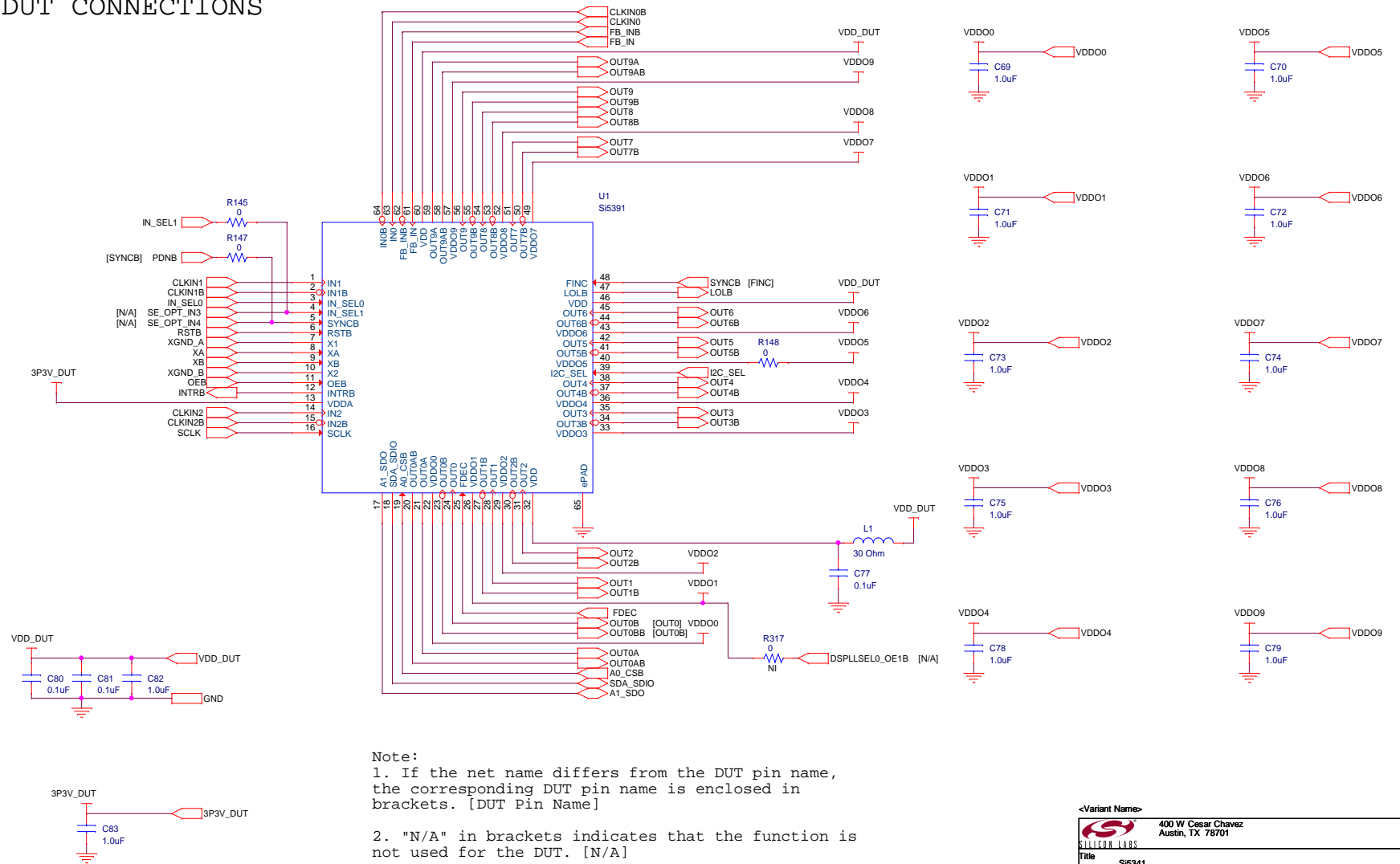


# REFERENCE INPUT CONNECTIONS



 400 W Cesar Chavez Austin, TX 78701		
Title REFERENCE		
Size B	Document Number SI5391P-A-EB	Rev 1.3
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# DUT CONNECTIONS




## Note:

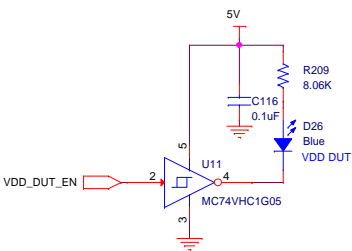
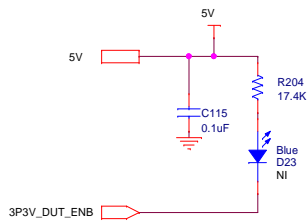
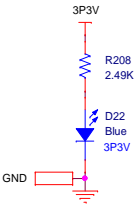
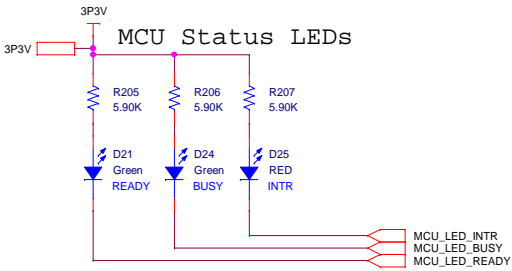
1. If the net name differs from the DUT pin name, the corresponding DUT pin name is enclosed in brackets. [DUT Pin Name]


2. "N/A" in brackets indicates that the function is not used for the DUT. [N/A]

<Variant Name>

 <b>400 W Cesar Chavez</b> <b>Austin, TX 78701</b>		
<b>Title</b> SI5341		
<b>Size</b> B	<b>Document Number</b> SI5391P-A-E8	<b>Rev</b> 1.3
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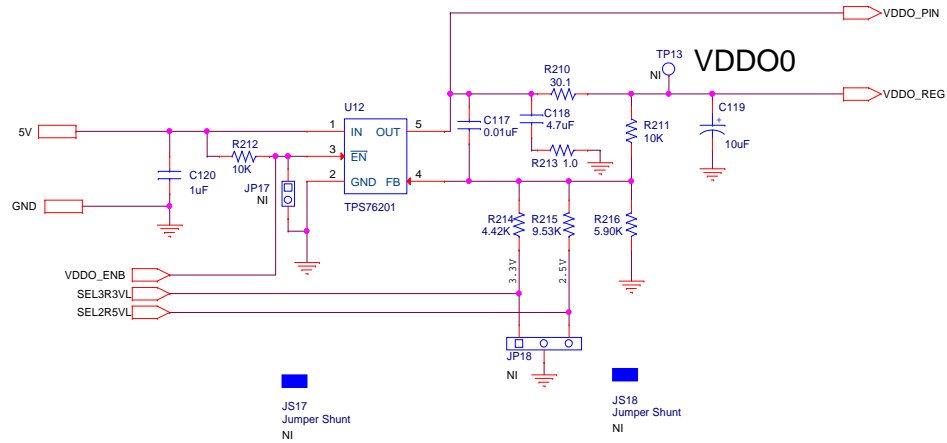
LEDS - SUPPLIES & STATUS




 400 W Cesar Chavez Austin, TX 78701			
Title STATUS_MAIN_SUPPLY_LEDS			
Size B	Document Number SI5391P-A-EB	Rev 1.3	
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# 100 mA Adjustable Voltage Regulator

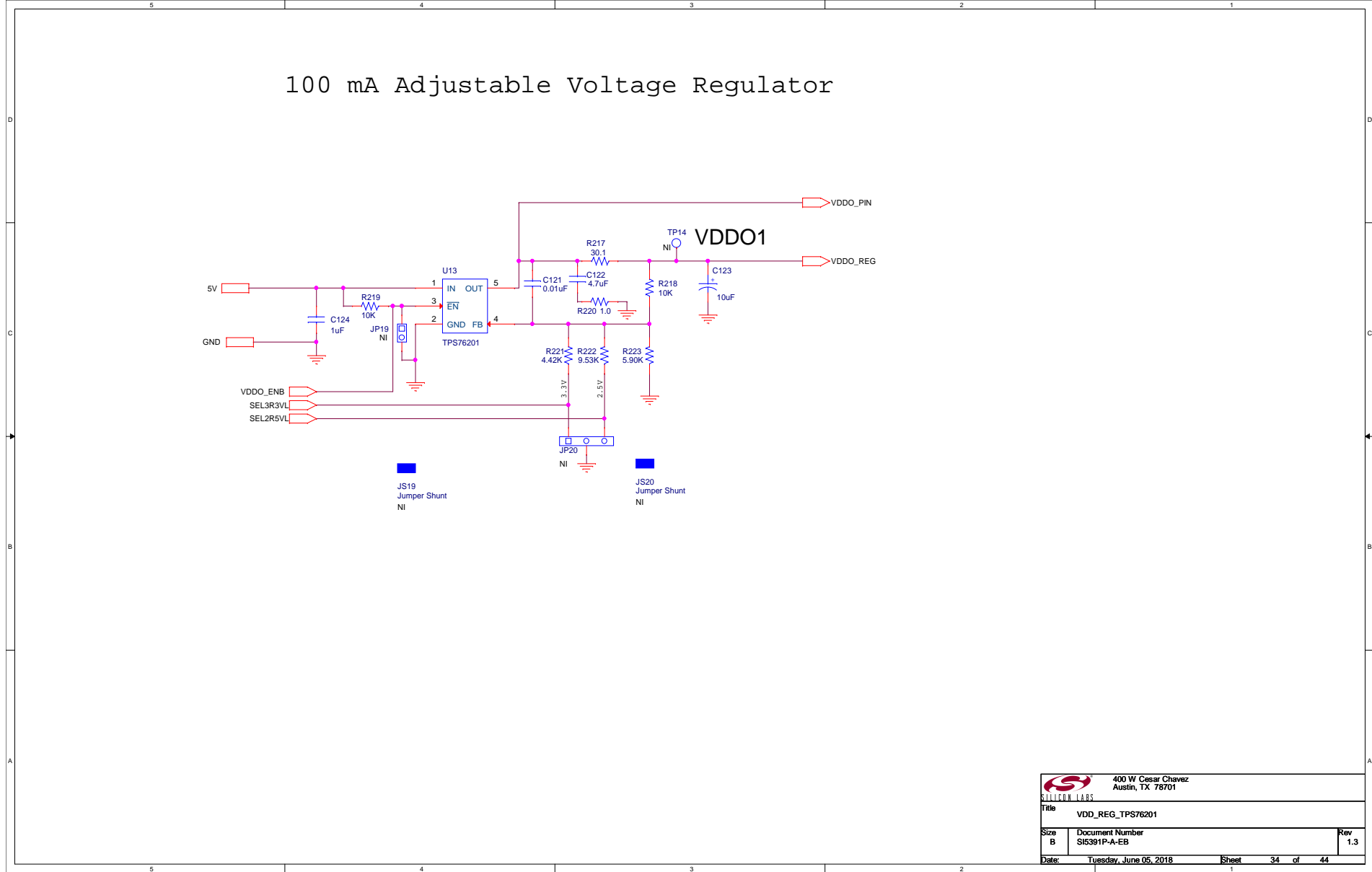


 400 W Cesar Chavez Austin, TX 78701	
Title VDD_REG_TPS76201	
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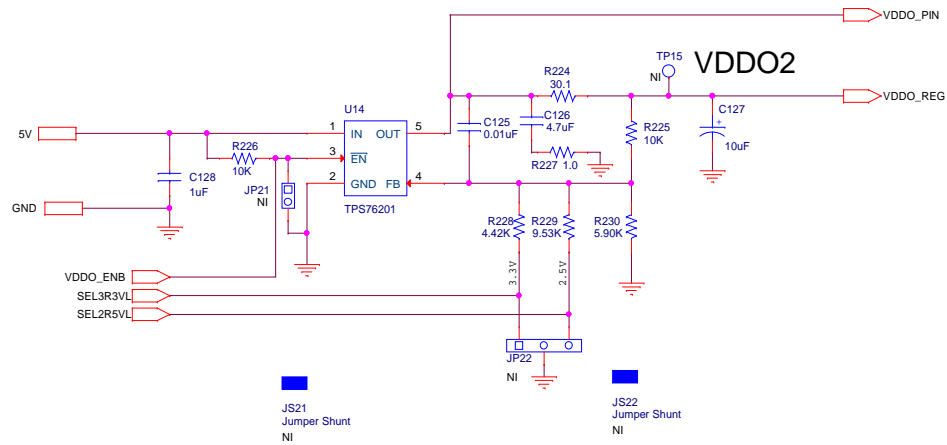
# 100 mA Adjustable Voltage Regulator


The schematic diagram illustrates a 100 mA Adjustable Voltage Regulator circuit. The core component is the TPS76201 integrated circuit (U13), which is configured as a voltage regulator. The input (IN) is connected to a 5V supply through a 10kΩ resistor (R219) and a 1μF capacitor (C124). The enable pin (EN) is connected to the 5V supply through a 10kΩ resistor (R219) and a 1μF capacitor (C124). The feedback pin (FB) is connected to the output (OUT) through a 1.0Ω resistor (R220). The output (OUT) is connected to the load through a 30.1Ω resistor (R217) and a 4.7μF capacitor (C122). The output voltage is adjustable using a potentiometer (R221, R222, R223) with values of 4.42kΩ, 9.53kΩ, and 5.90kΩ, respectively. The output voltage is measured at TP14 (VDDO1) and is labeled VDDO\_REG. The circuit also includes a 10kΩ resistor (R218) and a 10μF capacitor (C123) for output filtering. The input and output pins are labeled VDDO\_PIN and VDDO\_REG. The circuit is powered by a 5V supply and ground (GND). The output voltage is adjustable between 3.3V and 2.5V. The circuit includes two jumpers, JS19 and JS20, which are used to select the output voltage. JS19 is a Jumper Shunt and JS20 is a Jumper Shunt. The circuit is labeled VDDO1.

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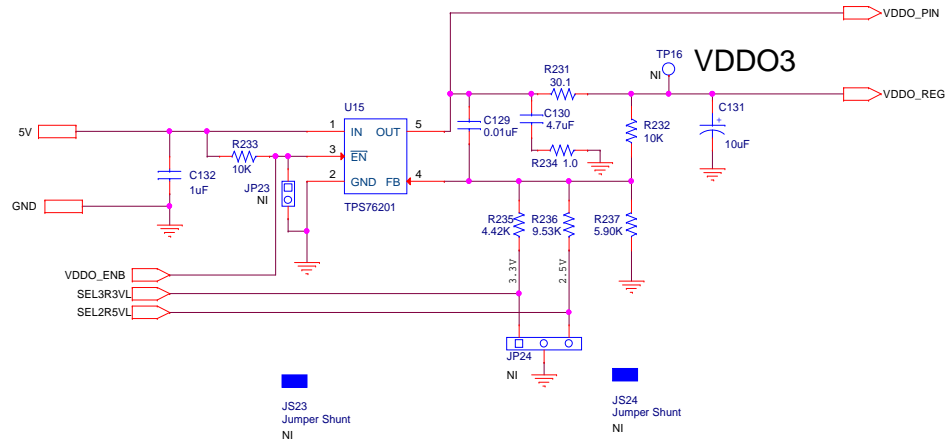



# 100 mA Adjustable Voltage Regulator



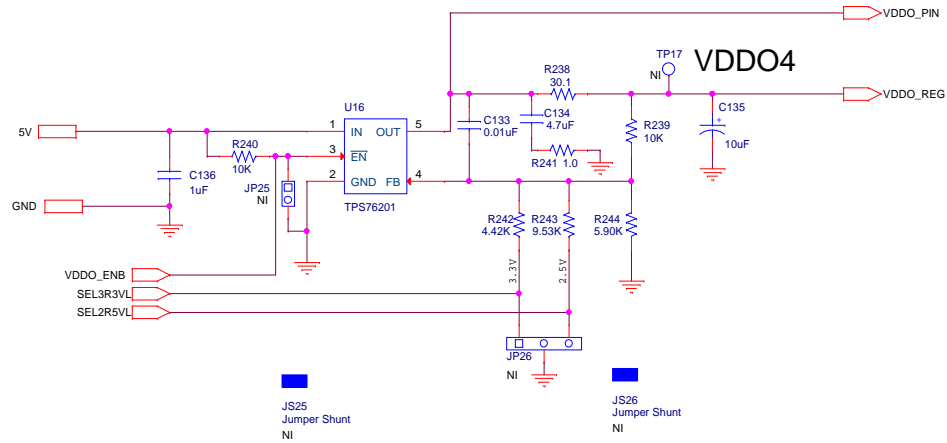
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Title VDD_REG_TPS76201	
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# 100 mA Adjustable Voltage Regulator



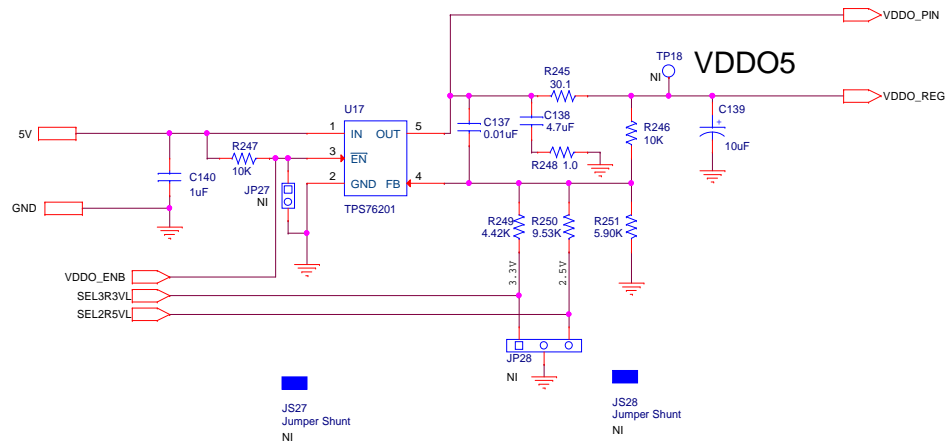
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Title	
VDD_REG_TPS76201	
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# 100 mA Adjustable Voltage Regulator



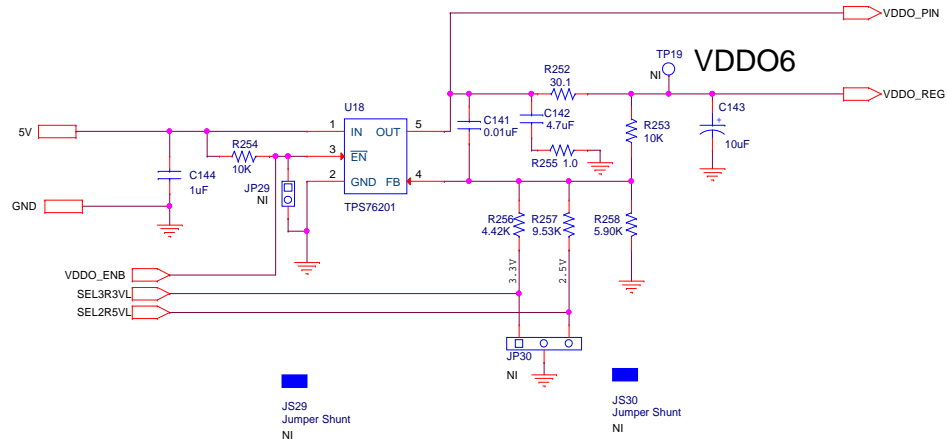
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VDD_REG_TPS76201	
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# 100 mA Adjustable Voltage Regulator



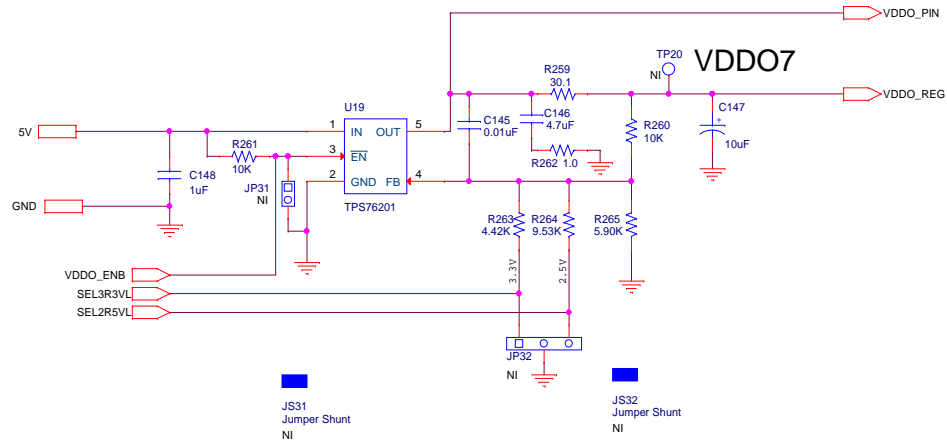
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VDD_REG_TPS76201	
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# 100 mA Adjustable Voltage Regulator



		400 W Cesar Chavez Austin, TX 78701	
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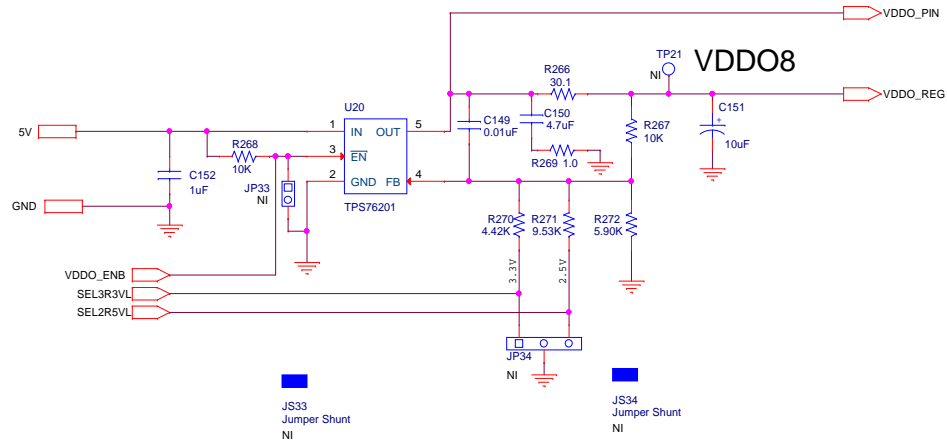
# 100 mA Adjustable Voltage Regulator




 400 W Cesar Chavez Austin, TX 78701	
Title	
VDD_REG_TPS76201	
Size	Document Number
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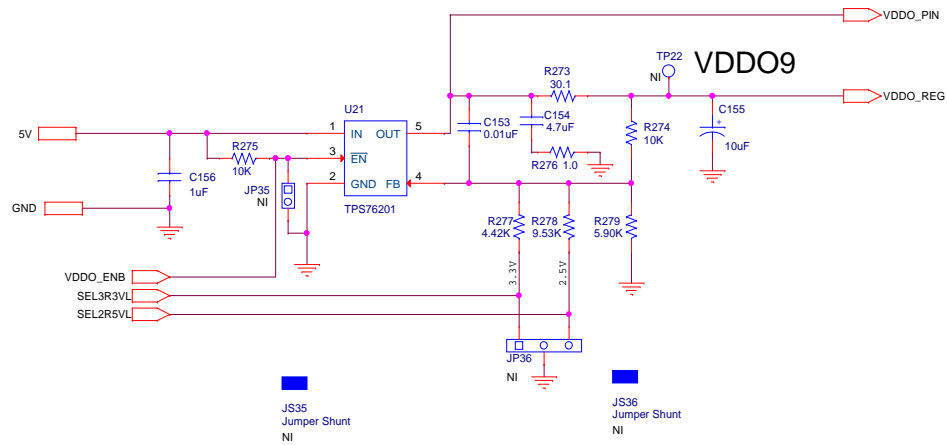



# 100 mA Adjustable Voltage Regulator

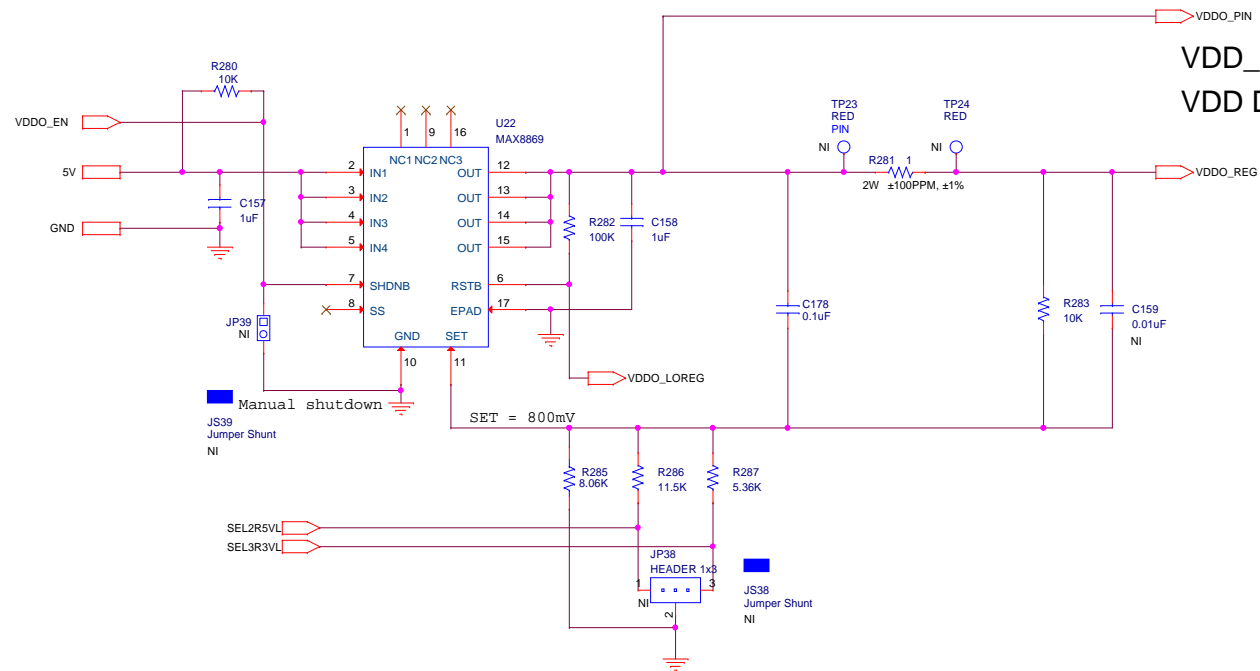


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# 100 mA Adjustable Voltage Regulator



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VDD\_DUT (In Schematic)  
VDD DUT (Board Silkscreen)

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VOLTAGE MEASUREMENT MULTIPLEXING

