MP2005

800mA High PSRR, ULDO Linear Regulator

DESCRIPTION

The MP2005 is a micropower, ultra low-dropout LDO linear regulator. It has a 1.0V to 5.5V input voltage range and can regulate the output voltage from as low as 0.5V. The MP2005 can supply up to 800mA of load current with a typical dropout voltage of 90mV. It requires a bias supply (2.7V to 5.5V) separate from V_{IN} to run the internal reference and LDO drive circuitry. The output current comes directly from the input voltage supply for high efficiency regulation. The 0.5V internal reference voltage allows the output to be programmed to a wide range of voltages (0.5V to 4V).

A low bias current of 100µA makes the MP2005 ideal for use in battery-powered applications. The bias supply V_{BIAS} can be directly applied from the battery while V_{IN} is powered from the high efficiency buck regulator (or other secondary supply). This reduces output noise and the size of the decoupling capacitor.

Other features of MP2005 include thermal overload and current limit protection, stability with ultra low ESR ceramic capacitors as low as 1µF, and fast transient response. The MP2005 is available in a 8-pin QFN (2mm x 3mm) package.

FEATURES

- Wide 1.0V to 5.5V Input Voltage Range
- Stable with 1µF Ceramic Capacitor
- Ultra-Low Dropout (ULDO) voltage: 90mV@800mA
- 2% Accurate Output Voltage
- Adjustable Output Range of 0.5V to 4V
- High PSRR
  - 65dB at 1KHz
  - 48dB at 1MHz
- Better Than 0.0005%/mA Load Regulation
- Stable With Low-ESR Output Capacitors
- Low 100µA Ground Current
- Internal Thermal Protection
- Current Limit Protection
- 1µA Typical Quiescent Current at Shutdown

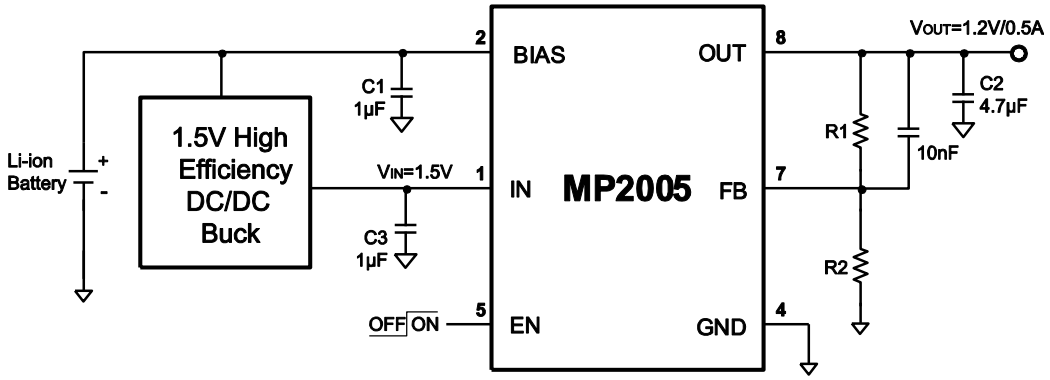
APPLICATIONS

- Low Current Regulators
- Low Power Handheld Devices
- Battery Powered Systems
- Cellular Phones
- Portable Electronic Equipment
- Post Regulation for Switching Power Supplies
- Power Supplies

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TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number*	Package	Top Marking
MP2005DD	QFN-8 (2mm x 3mm)	*See Below*

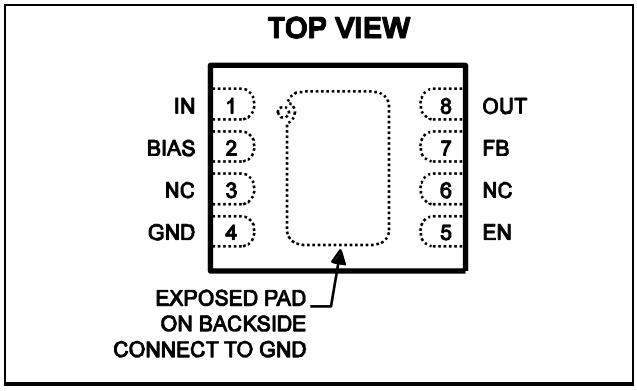
***** For Tape & Reel, add suffix –Z (e.g. MP2005DD–Z)
For RoHS compliant packaging, add suffix –LF (e.g. MP2005DD–LF–Z)

TOP MARKING

N3YW
LLL

N3: product code of MP2005DD;
Y: year code;
W: week code:
LLL: lot number;

PACKAGE REFERENCE



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ABSOLUTE MAXIMUM RATINGS (1)

V_{BIAS}, V_{IN} to GND ..... –0.3V to +6V
FB, EN to GND ..... –0.3V to 6V
OUT ..... –0.3V to 6V
Continuous Power Dissipation (T_A = +25°C) (2) 2.3W
Junction Temperature ..... 150°C
Lead Temperature ..... 260°C
Storage Temperature ..... –65°C to +150°C

Recommended Operating Conditions (3)

Input Voltage V_{IN} ..... 1.0V to 5.5V
Input Voltage V_{BIAS} ..... 2.7V to 5.5V
Output Voltage ..... 0.5V to 4.0V
Load Current ..... 800mA Maximum
Operating Temperature ..... –40°C to +85°C

Thermal Resistance (4) θ_{JA} θ_{JC}

	θ_{JA}	θ_{JC}	
QFN-8 (2mm x 3mm)	55	12	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D(MAX)=(T_J(MAX)-T_A)/\theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 1.5V, V_{BIAS} = 3.6V, V_{OUT} = 1.2V, C2 =4.7µF, C3 = 1µF, T_A = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
V_{IN} Operating Voltage			1.0		5.5	V
V_{BIAS} Operating Voltage			2.7		5.5	V
V_{IN} Operating Current		V_{OUT} = 1.2V		4	10	µA
V_{BIAS} Operating Current		I_{OUT} = 10µA, V_{OUT} = 1.2V		100	150	µA
FB Regulation Voltage		I_{OUT} = 1mA to 800mA	0.490	0.500	0.510	V
		–40°C ≤ T_A ≤ +85°C, V_{OUT} = 0.5 V	0.487	0.500	0.512	
Dropout Voltage		I_{OUT} = 800mA, V_{BIAS} = 3.6V		70	90	mV
V_{IN} Line Regulation		I_{OUT} = 1mA, V_{IN} = 1.0V to 5.5V V_{BIAS} = 3.6V V_{OUT} = 0.5V		0.002		%/V
V_{BIAS} Line Regulation		I_{OUT} = 100mA, V_{BIAS} = 2.7V to 5.5V V_{OUT} = 0.5V V_{IN} = 1.5V		0.04		%/V
Load Regulation		I_{OUT} = 1mA to 800mA		0.0005		%/mA
PSRR		V_{IN} > V_{OUT} + 0.5V, C2 = 10µF, V_{IN}(AC) = 100mV, f = 1MHz		48		dB
EN Input High Voltage			1.3			V
EN Input Low Voltage					0.8	V
EN Input Bias Current		V_{EN} = 1.2V	–1		+1	µA
Thermal Protection				155		°C
Thermal Protection Hysteresis				30		°C
GND Current		I_{LOAD} = 500mA		110	150	µA

PIN FUNCTIONS

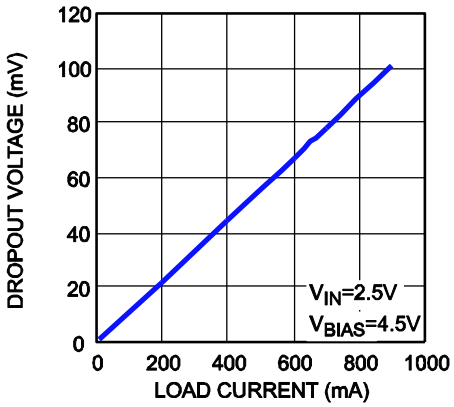
Pin #	Name	Description
1	IN	Power Source Input. Bypass IN to GND with a 1µF or greater capacitor.
2	BIAS	Bias Voltage. Bypass to GND with a 1µF capacitor (or greater)
3, 6	NC	No Connect.
4	GND	Ground.
5	EN	Enable Input. Drive EN high to turn on the MP2005, drive EN low to turn it off. For automatic startup, connect EN to Bias or VIN, and make sure EN voltage ≥1.3V.
7	FB	Feedback Input. Connect a resistive voltage divider from OUT to FB to set the output voltage. OUT feedback threshold is 0.5V.
8	OUT	Regulator Output. OUT is the output of the linear regulator. Bypass OUT to GND with a 1µF or greater capacitor.

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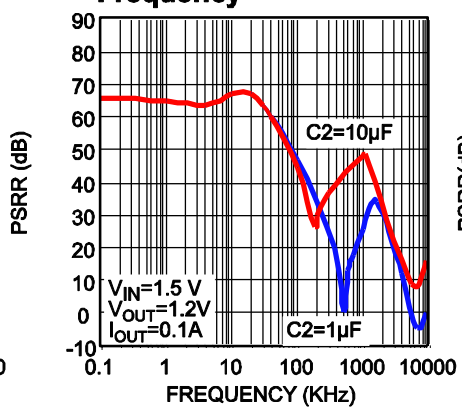
TYPICAL PERFORMANCE CHARACTERISTICS

C1=C3=2.2uF, C2=4.7uF, V_{EN}=V_{BIAS}=3.6V, T_A=25°C, unless otherwise noted

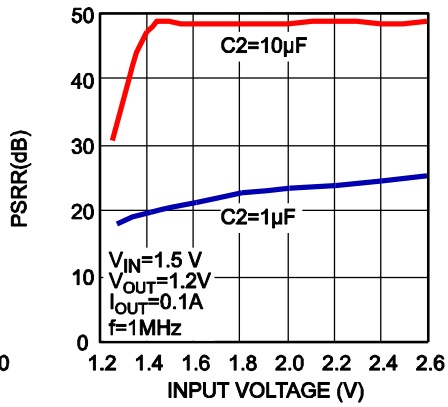
Voltage Dropout



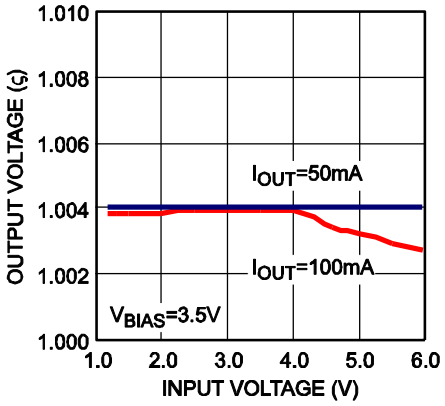
PSRR vs. Frequency



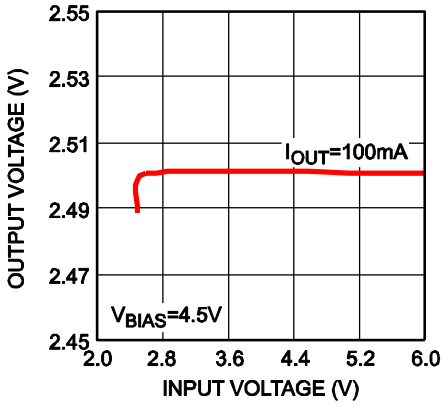
PSRR vs. V_{IN}



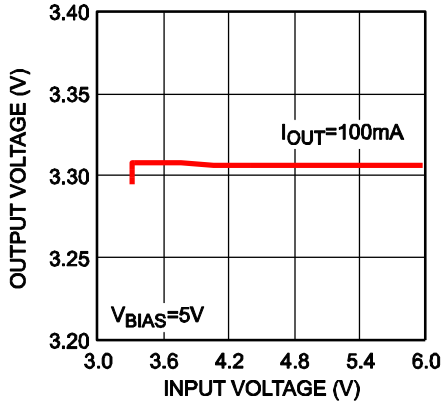
Line Regulation



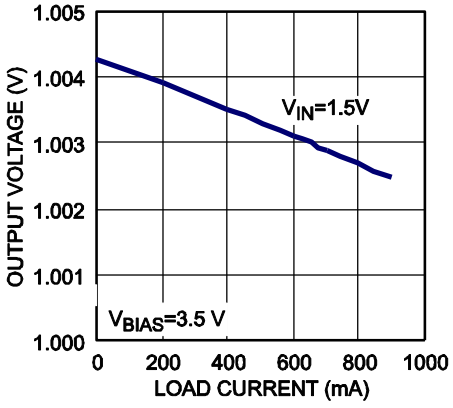
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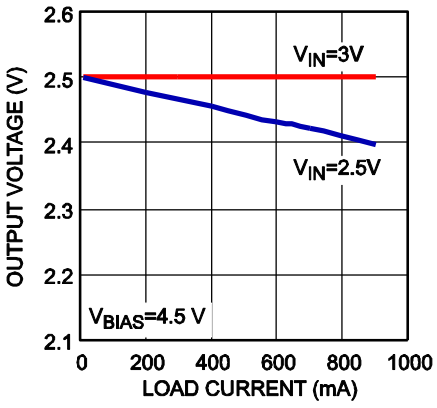
Line Regulation



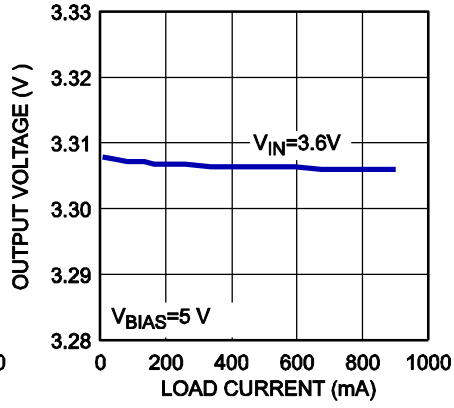
Load Regulation



Load Regulation



Load Regulation

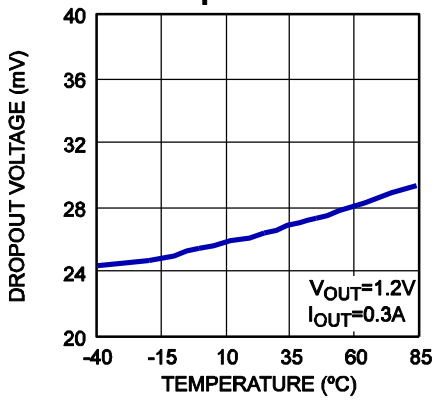


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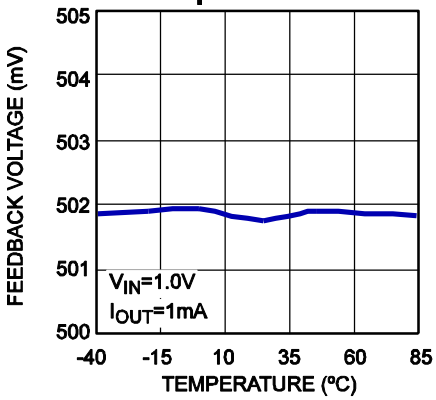
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

C1=C3=2.2uF, C2=4.7uF, V_{EN}=V_{BIAS}=3.6V, T_A=25°C, unless otherwise noted

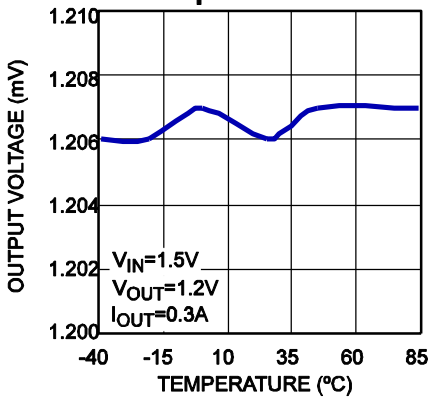
Dropout Voltage vs. Temperature



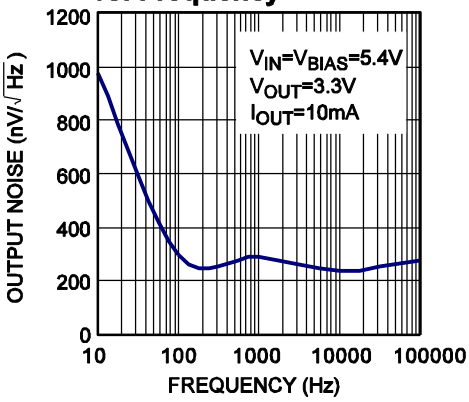
Feedback Voltage vs. Temperature



Output Voltage vs. Temperature



Output Noise vs. Frequency



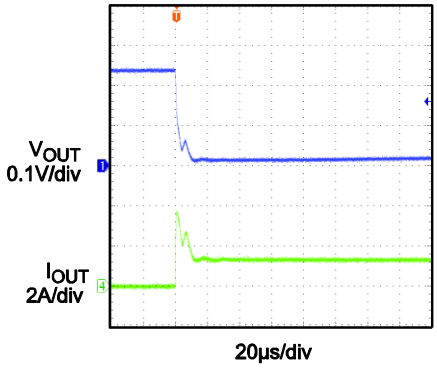
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

C1=C3=2.2uF, C2=4.7uF, V_{EN}=V_{BIAS}=3.6V, V_{IN}=3.6V, T_A=25°C, unless otherwise noted

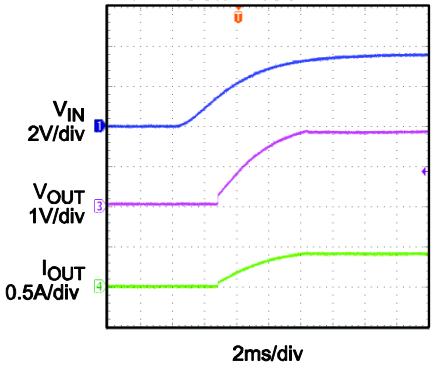
Short Circuit

V_{IN}=2V, V_{OUT}=1.8V



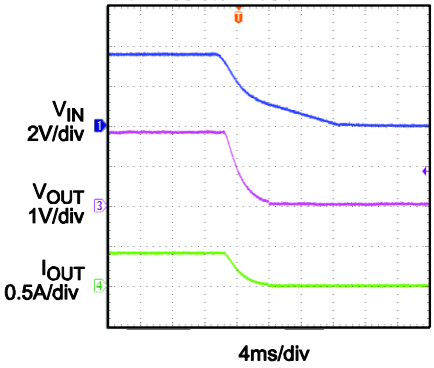
Power Ramp Up

V_{OUT}=1.8V, I_{OUT}=420mA,
with Resistor Load



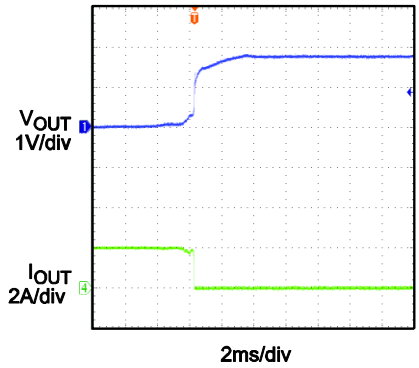
Power Ramp Down

V_{OUT}=1.8V, I_{OUT}=420mA
with Resistor Load



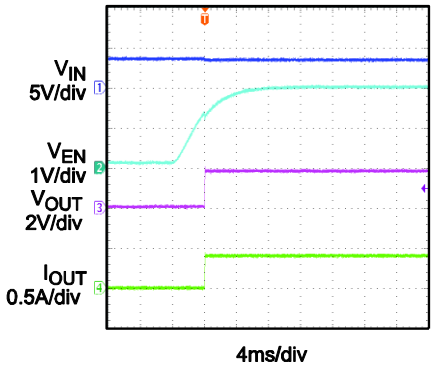
Short Circuit Recovery

V_{IN}=2V, V_{OUT}=1.8V



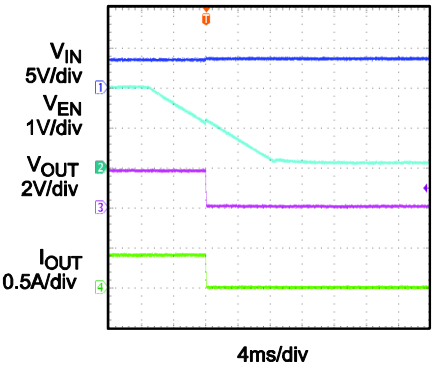
Enable Turn On

V_{OUT}=1.8V, I_{OUT}=400mA
with Resistor Load



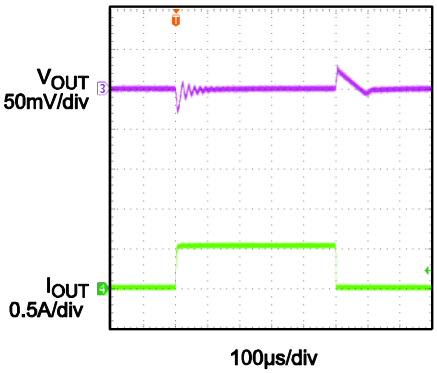
Enable Turn Off

V_{OUT}=1.8V, I_{OUT}=400mA
with Resistor Load



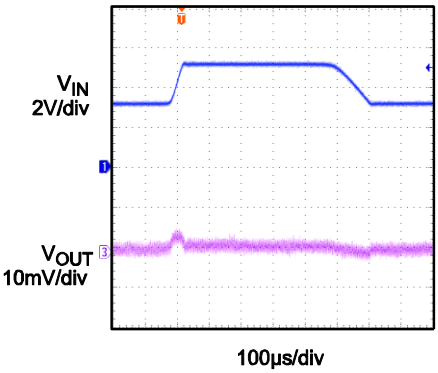
Load Transient

V_{BIAS}=2.9V, V_{OUT}=1.2V, V_{IN}=1.5V,
I_{OUT}=20mA to 600mA,
with Resistor Load



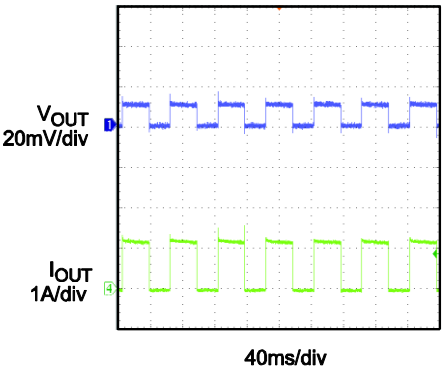
Line Transient

V_{IN}=3.5V to 5.2V, V_{OUT}=1.2V,
I_{OUT}=100mA
with Resistor Load



Thermal Protection

V_{OUT}=1.8V, I_{OUT}=1A
with Resistor Load



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BLOCK DIAGRAM

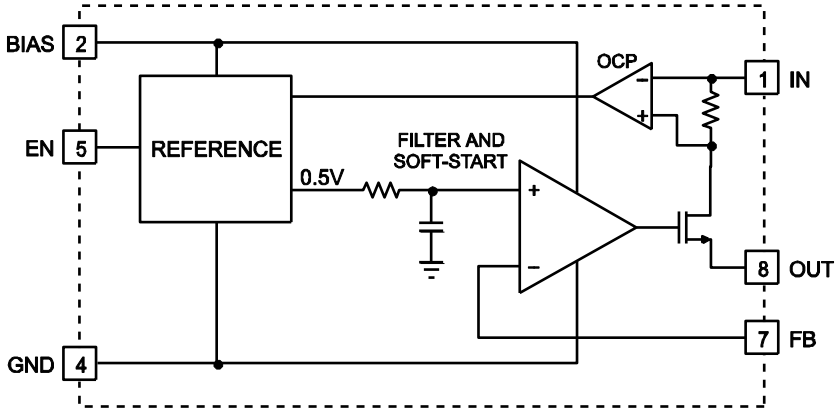


Figure 1—Block Diagram of Super Low Dropout Regulator

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APPLICATION INFORMATION

Setting the Output Voltage

The MP2005 has an adjustable output voltage, set by using a resistive voltage divider from the output voltage to FB pin. The voltage divider divides the output voltage down to the feedback voltage by the ratio:

$$V_{FB} = V_{OUT} \frac{R2}{R1+R2}$$

Where V_{FB} is the feedback threshold voltage (V_{FB} = 0.5V), and V_{OUT} is the output voltage.

Thus the output voltage is:

$$V_{OUT} = 0.5 \times \frac{R1+R2}{R2}$$

R2 can be as high as 100kΩ, but a typical value is 10kΩ. Using that value, R1 is determined by:

$$R1 = R2 \times \left(\frac{V_{OUT} - V_{FB}}{V_{FB}} \right)$$

For example, for a 1.8V output voltage, R2 is 10kΩ, and R1 is 26kΩ. You can select a standard 26kΩ (±1%) resistor for R1.

The following table lists the selected R1 for various output voltages.

Table 1—Adjustable Output Voltages R1 Values

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)
1.25	15	10
1.5	20	
1.8	26	
2	30	
2.5	40	
2.8	46	
3	50	
3.3	56	
4	70	

Bias Input

The bias input is designed for low drop application. The bias pin must be at least 2.7V, and at least 1.5V higher than the output. If V_{IN} supply voltage meets these requirements, the bias pin can be tied to $V_{IN.}$

Feed Forward Capacitor

Feed forward capacitor which a ceramic type capacitor parallels with R1 affects loop stability. According to actual application, MP2005 improves load transient performance by add a suitable feed forward capacitor.

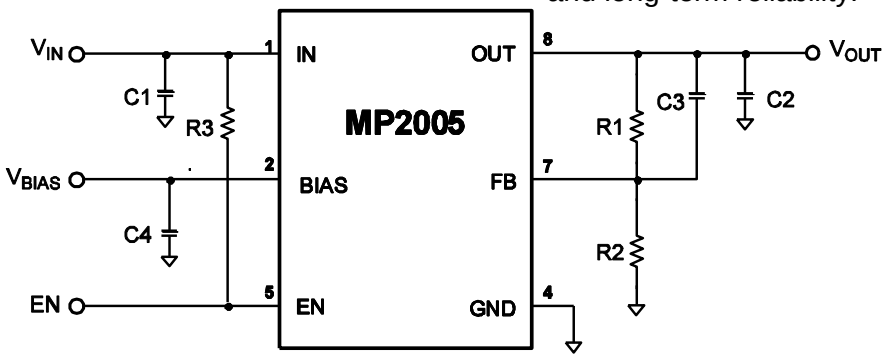
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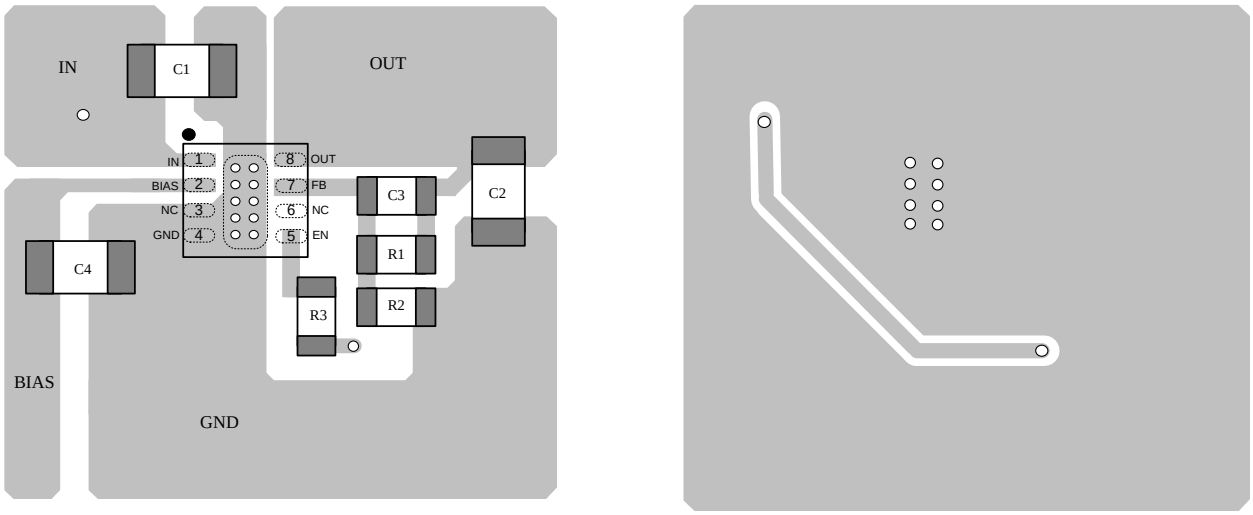
PCB Layout Guide

PCB layout is very important to achieve good regulation, ripple rejection, transient response and thermal performance. It is highly recommended to duplicate EVB layout for optimum performance.

If change is necessary, please follow these guidelines and take Figure 2 for reference.

1) Input and output bypass ceramic capacitors are suggested to be put close to the IN Pin and OUT Pin respectively.
2) Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close to the chip as possible.
3) Connect IN, OUT and especially GND respectively to a large copper area to cool the chip to improve thermal performance and long-term reliability.





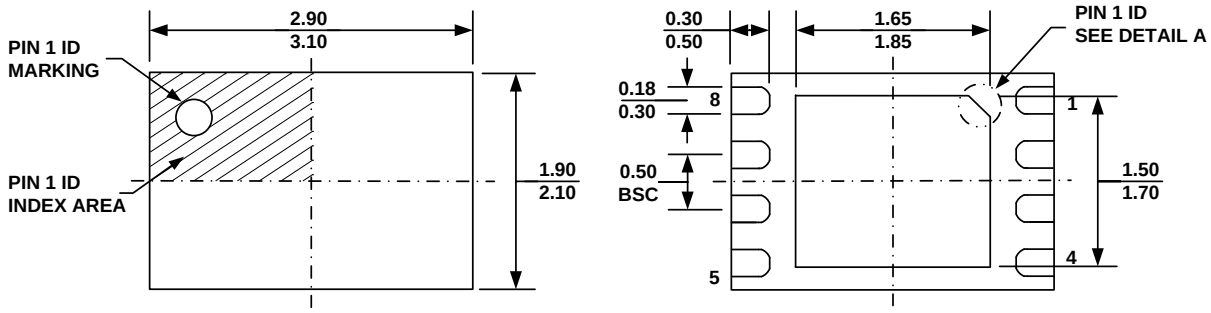
Top Layer **Bottom Layer**

Figure 2—PCB Layout

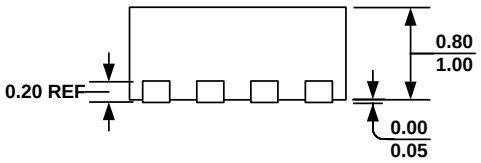
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PACKAGE INFORMATION

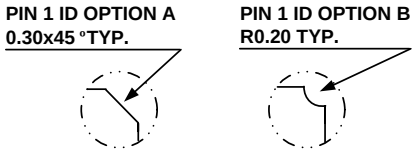
QFN8 (2mm x 3mm)



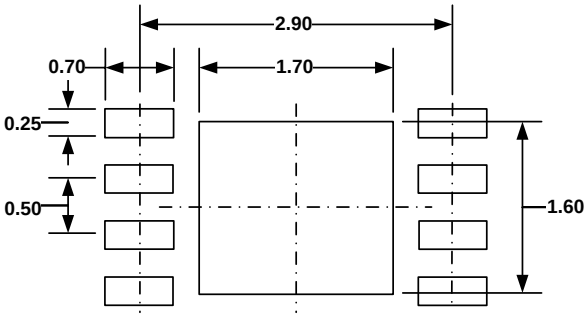
TOP VIEW **BOTTOM VIEW**



SIDE VIEW



DETAIL A



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETER MAX.
4) DRAWING CONFORMS TO JEDEC MO-229, VARIATION VCED-2.
5) DRAWING IS NOT TO SCALE.

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