IXYS

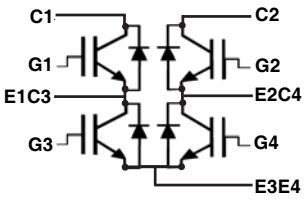
Preliminary Technical Information

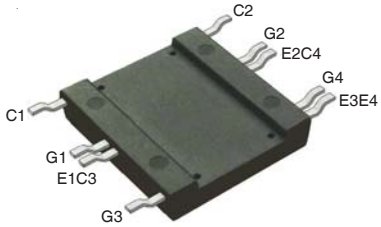
High Voltage, High Gain BIMOSFET™ Monolithic Bipolar MOS Transistor

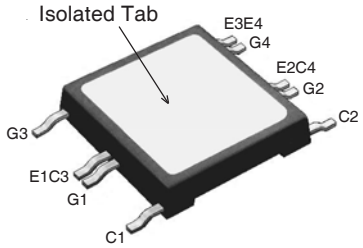
(Electrically Isolated Tab)

MMIX4B20N300

V_{CES} = 3000V
I_{C110} = 14A
$V_{CE(sat)}$ ≤ 3.2V







G = Gate E = Emitter
C = Collector

Symbol	Test Conditions	Maximum Ratings	
V_{CES}	T_C = 25°C to 150°C	3000	V
V_{CGR}	T_J = 25°C to 150°C, R_{GE} = 1MΩ	3000	V
V_{GES}	Continuous	± 20	V
V_{GEM}	Transient	± 30	V
I_{C25}	T_C = 25°C	34	A
I_{C110}	T_C = 110°C	14	A
I_{CM}	T_C = 25°C, V_{GE} = 19V, 1ms	150	A
	10ms	74	A
SSOA (RBSOA)	V_{GE} = 15V, T_{VJ} = 125°C, R_G = 20Ω	I_{CM} = 130	A
	Clamped Inductive Load	1500	V
P_C	T_C = 25°C	150	W
T_J		-55 ... +150	°C
T_{JM}		150	°C
T_{stg}		-55 ... +150	°C
T_L	1.6mm (0.062 in.) from Case for 10s	300	°C
T_{SOLD}	Plastic Body for 10 seconds	260	°C
F_C	Mounting Force	50..200 / 11..45	Nm/lb.in.
V_{ISOL}	50/60Hz, 1 Minute	4000	V~
Weight		8	g

Symbol	Test Conditions (T_J = 25°C Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
BV_{CES}	I_C = 250μA, V_{GE} = 0V	3000			V
$V_{GE(th)}$	I_C = 250μA, V_{CE} = V_{GE}	2.5		5.0	V
I_{CES}	V_{CE} = 0.8 • V_{CES}, V_{GE} = 0V			35	μA
	Note 2, T_J = 125°C			1.5	mA
I_{GES}	V_{CE} = 0V, V_{GE} = ± 20V			±100	nA
$V_{CE(sat)}$	I_C = 20A, V_{GE} = 15V, Note 1		2.7	3.2	V
	T_J = 125°C		3.2		V

Features

- Silicon Chip on Direct-Copper Bond (DCB) Substrate
- Isolated Mounting Surface
- 4000V~ Electrical Isolation
- High Blocking Voltage
- High Peak Current Capability
- Low Saturation Voltage

Advantages

- Low Gate Drive Requirement
- High Power Density

Applications

- Switch-Mode and Resonant-Mode Power Supplies
- Capacitor Discharge Circuits

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Symbol	Test Conditions (T_J = 25°C Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
g_{fs}	I_C = 20A, V_{CE} = 10V, Note 1	11	18		S
C_{ies}	V_{CE} = 25V, V_{GE} = 0V, f = 1MHz		2230		pF
C_{oes}			92		pF
C_{res}			33		pF
Q_g	I_C = 20A, V_{GE} = 15V, V_{CE} = 1000V		105		nC
Q_{ge}			13		nC
Q_{gc}			45		nC
$t_{d(on)}$	**Resistive Switching Times, T_J = 25°C**		64		ns
t_r	I_C = 20A, V_{GE} = 15V		210		ns
$t_{d(off)}$	V_{CE} = 1250V, R_G = 10Ω		300		ns
t_f			504		ns
$t_{d(on)}$	**Resistive Switching Times, T_J = 125°C**		68		ns
t_r	I_C = 20A, V_{GE} = 15V		540		ns
$t_{d(off)}$	V_{CE} = 1250V, R_G = 10Ω		300		ns
t_f			395		ns
R_{thJC}				0.83	°C/W
R_{thCS}			0.05		°C/W
R_{thJA}			30		°C/W

Reverse Diode

Symbol	Test Conditions (T_J = 25°C Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
V_F	I_F = 20A, V_{GE} = 0V			2.1	V
t_{rr}	I_F = 10A, V_{GE} = 0V, $-di_F/dt$ = 100A/µs		1.35		µs
I_{RM}	V_R = 100V, V_{GE} = 0V		30		A

Notes:

1. Pulse test, t ≤ 300µs, duty cycle, d ≤ 2%.
2. Device must be heatsunk for high temperature leakage current measurements to avoid thermal runaway.

PRELIMINARY TECHNICAL INFORMATION

The product presented herein is under development. The Technical Specifications offered are derived from data gathered during objective characterizations of preliminary engineering lots; but also may yet contain some information supplied during a pre-production design evaluation. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

IXYS Reserves the Right to Change Limits, Test Conditions and Dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents: 4,835,592 4,860,072 4,881,106 4,931,844 5,017,508 5,034,796 5,049,961 5,063,307 5,187,117 5,237,481 5,381,025 5,486,715 6,162,665 6,259,123 B1 6,306,728 B1 6,404,065 B1 6,534,343 6,583,505 6,683,344 6,710,405 B2 6,710,463 6,727,585 6,759,692 6,771,478 B2 7,005,734 B2 7,063,975 B2 7,071,537 7,157,338B2

Fig. 1. Output Characteristics @ T_J = 25ºC

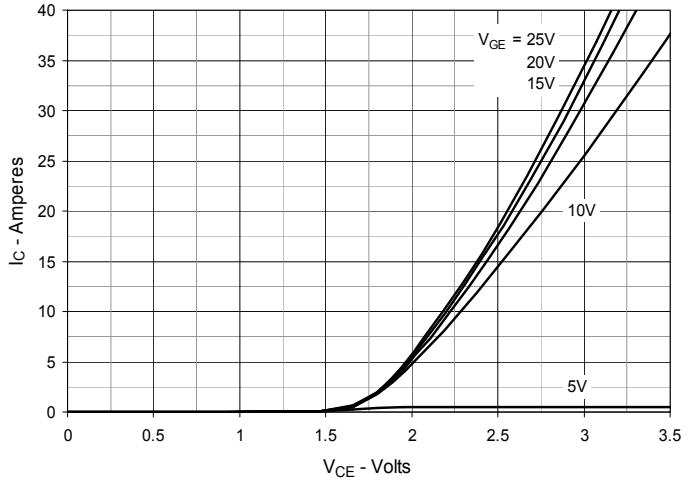


Fig. 2. Extended Output Characteristics @ T_J = 25ºC

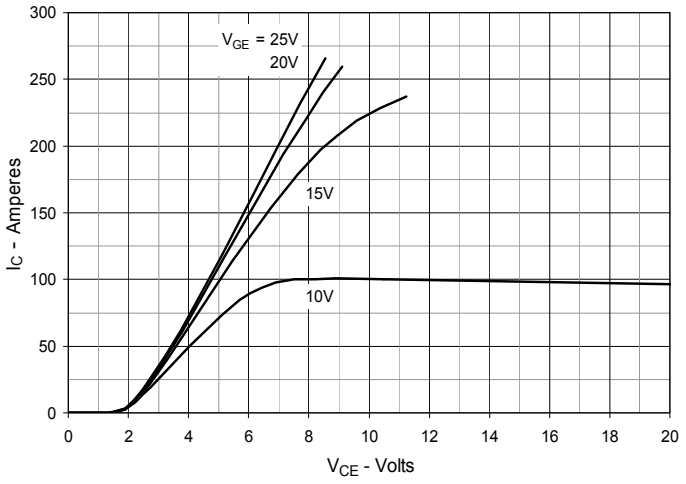


Fig. 3. Output Characteristics @ T_J = 125ºC

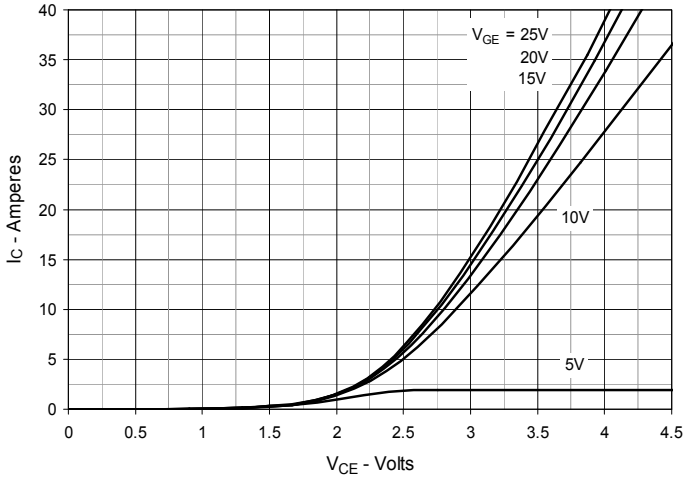


Fig. 4. Dependence of $V_{CE(sat)}$ on Junction Temperature

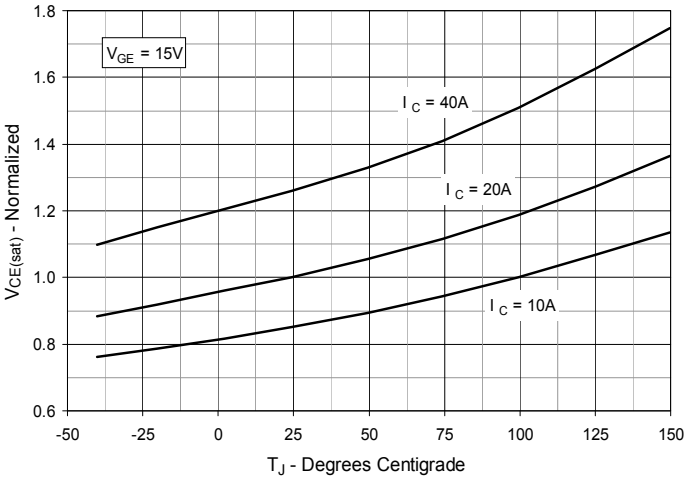


Fig. 5. Collector-to-Emitter Voltage vs. Gate-to-Emitter Voltage

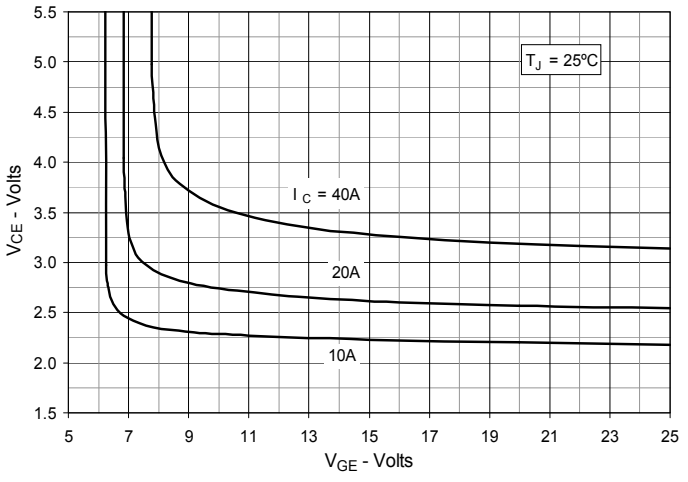
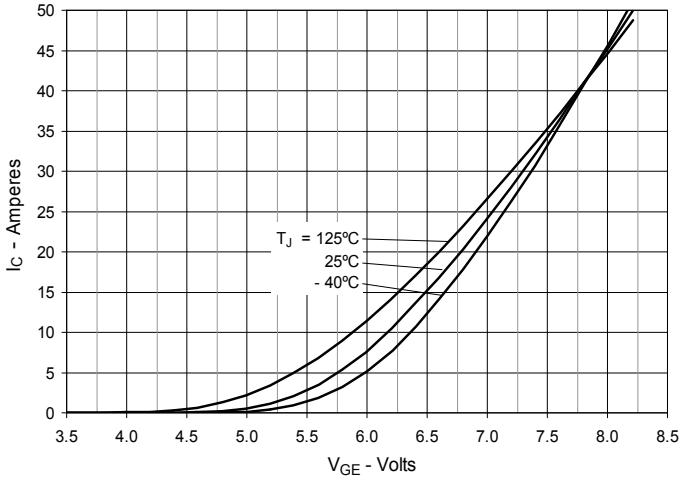


Fig. 6. Input Admittance



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Fig. 7. Transconductance

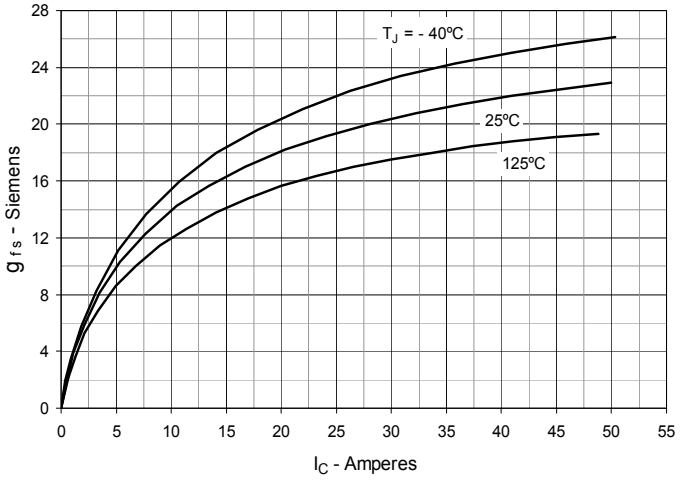


Fig. 8. Forward Voltage Drop of Intrinsic Diode

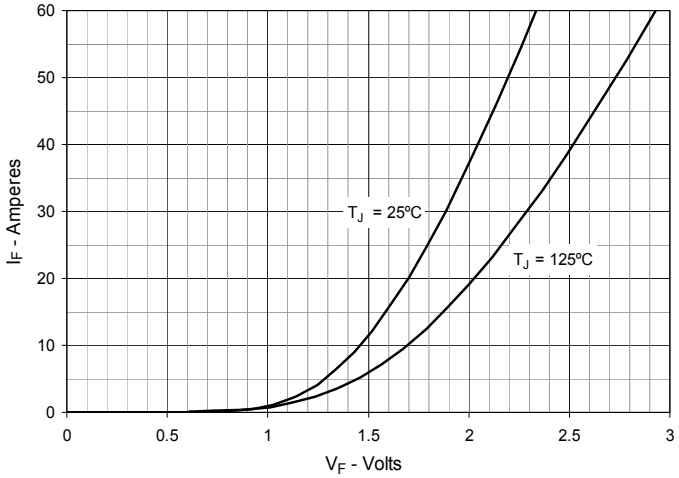


Fig. 9. Gate Charge

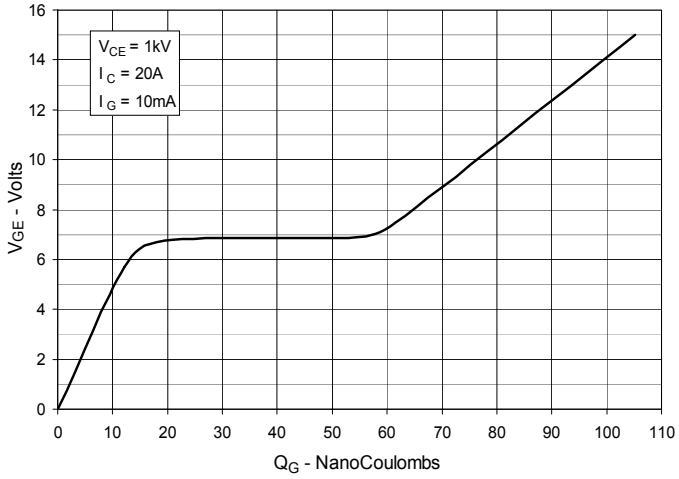


Fig. 10. Capacitance

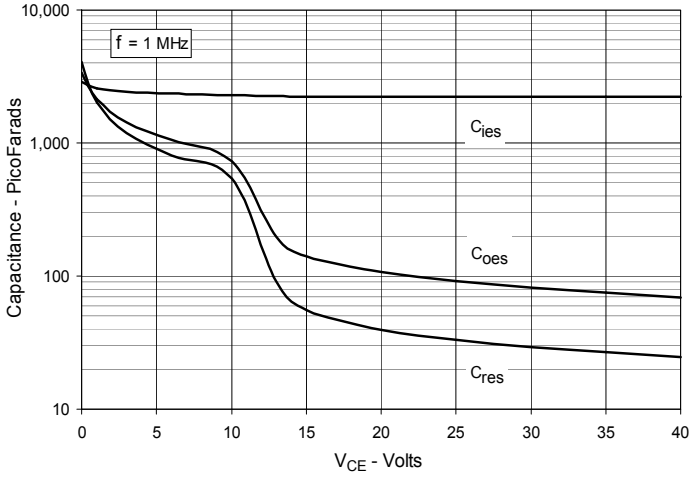


Fig. 11. Reverse-Bias Safe Operating Area

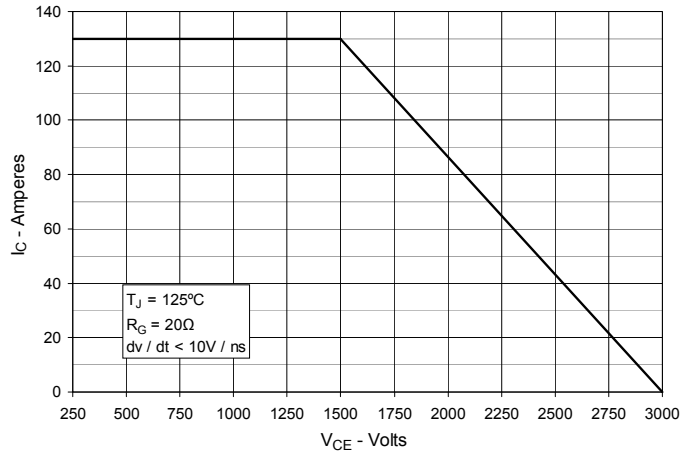
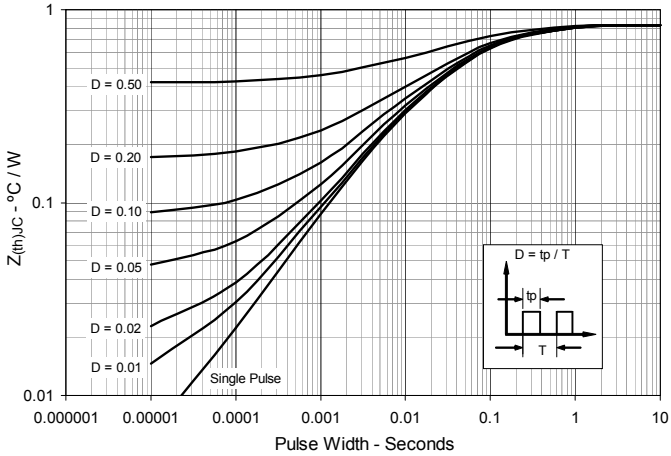


Fig. 12. Maximum Transient Thermal Impedance



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Fig. 13. Resistive Turn-on Rise Time vs. Junction Temperature

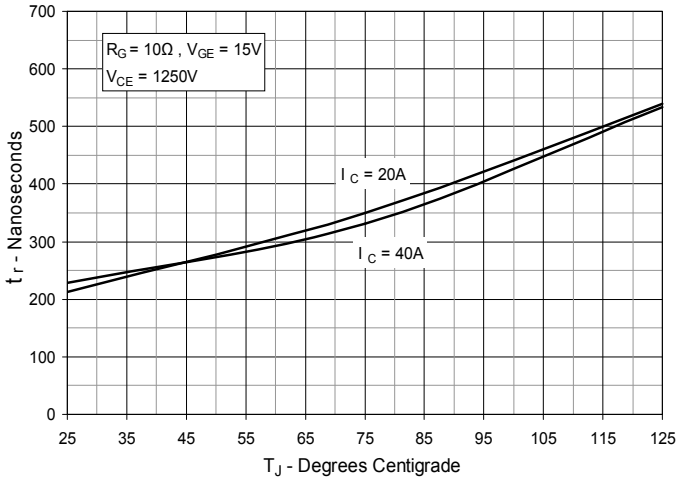


Fig. 14. Resistive Turn-on Rise Time vs. Collector Current

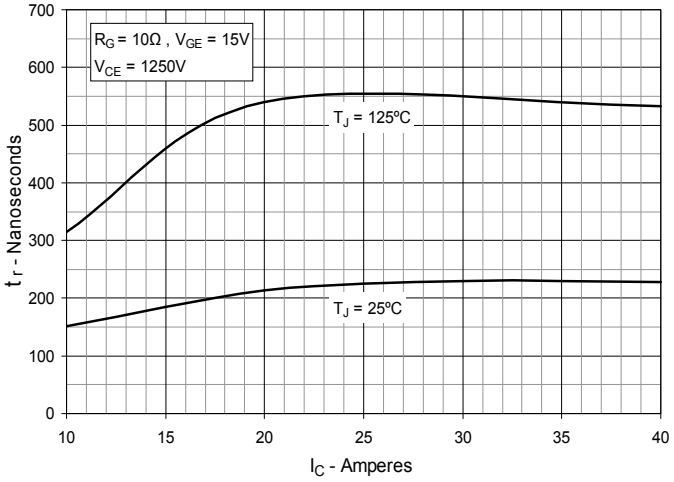


Fig. 15. Resistive Turn-on Switching Times vs. Gate Resistance

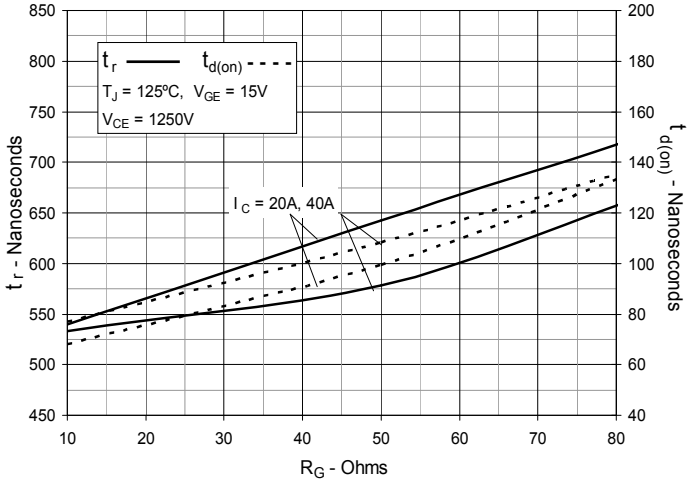


Fig. 16. Resistive Turn-off Switching Times vs. Junction Temperature

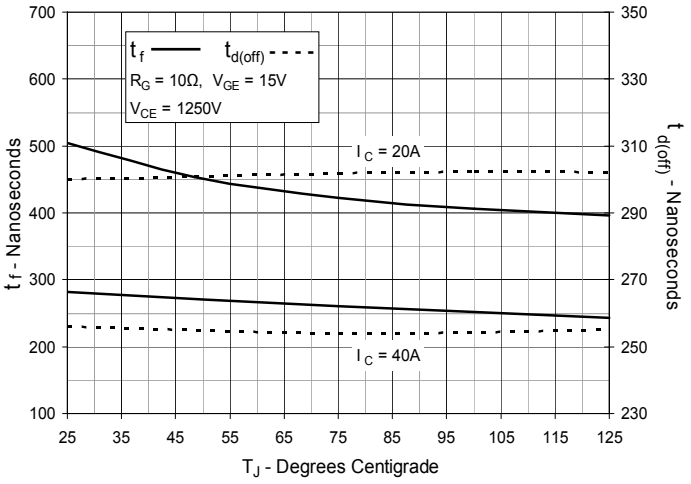


Fig. 17. Resistive Turn-off Switching Times vs. Collector Current

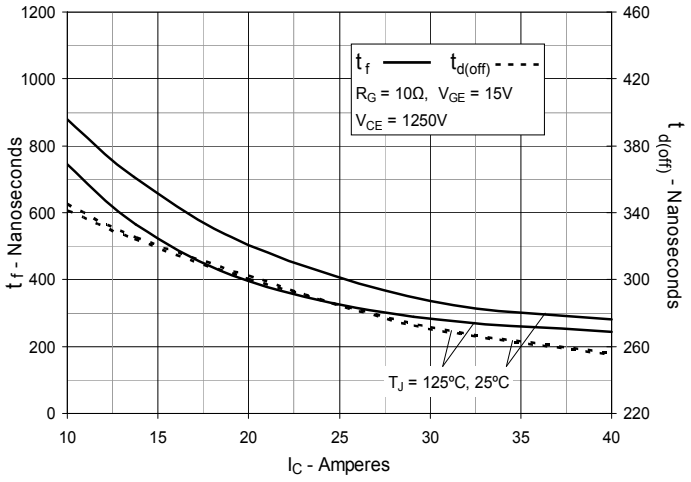
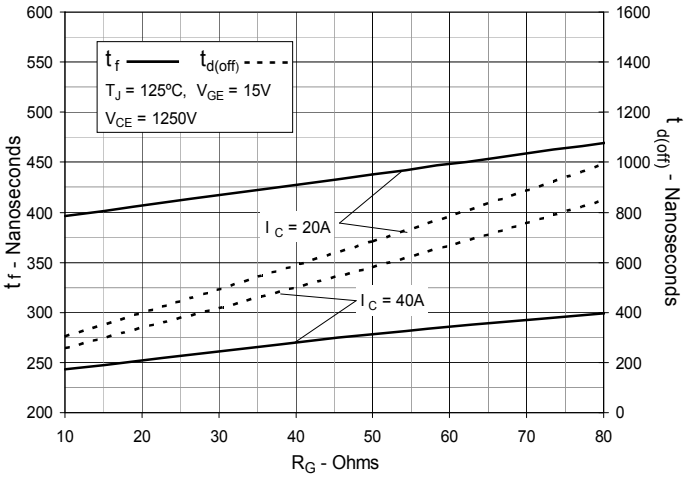
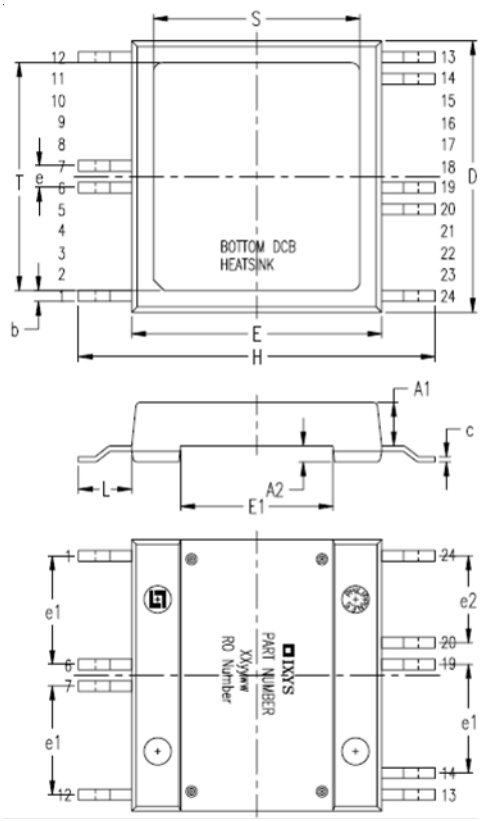


Fig. 18. Resistive Turn-off Switching Times vs. Gate Resistance



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Package Outline



SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.209	.224	5.30	5.70
A1	.154	.161	3.90	4.10
A2	.055	.063	1.40	1.60
b	.035	.045	0.90	1.15
c	.018	.026	0.45	0.65
D	.976	.994	24.80	25.25
E	.898	.915	22.80	23.25
E1	.543	.559	13.80	14.20
e	.079 BSC		2.00 BSC	
e1	.394 BSC		10.00 BSC	
e2	.315 BSC		8.00 BSC	
H	1.272	1.311	32.30	33.30
L	.181	.209	4.60	5.30
L1	.051	.067	1.30	1.70
L2	.000	.006	0.00	0.15
S	.736	.760	18.70	19.30
T	.815	.839	20.70	21.30
∝	0	4°	0	4°

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