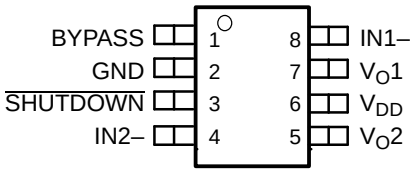
50-mW ULTRALOW VOLTAGE STEREO HEADPHONE AUDIO POWER AMPLIFIER

FEATURES

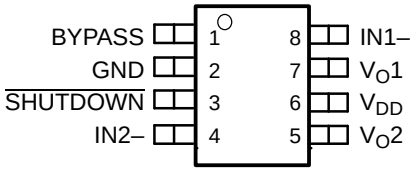
- **50-mW Stereo Output**
- **Low Supply Current . . . 0.75 mA**
- **Low Shutdown Current . . . 50 nA**
- **Pin Compatible With LM4881 and TPA102** (1)
- **Pop Reduction Circuitry**
- **Internal Midrail Generation**
- **Thermal and Short-Circuit Protection**
- **Surface-Mount Packaging**
  – MSOP and SOIC
- **1.6-V to 3.6-V Supply Voltage Range**

(1) The polarity of the $\overline{\text{SHUTDOWN}}$ pin is reversed.

D PACKAGE
(TOP VIEW)



DGK PACKAGE
(TOP VIEW)



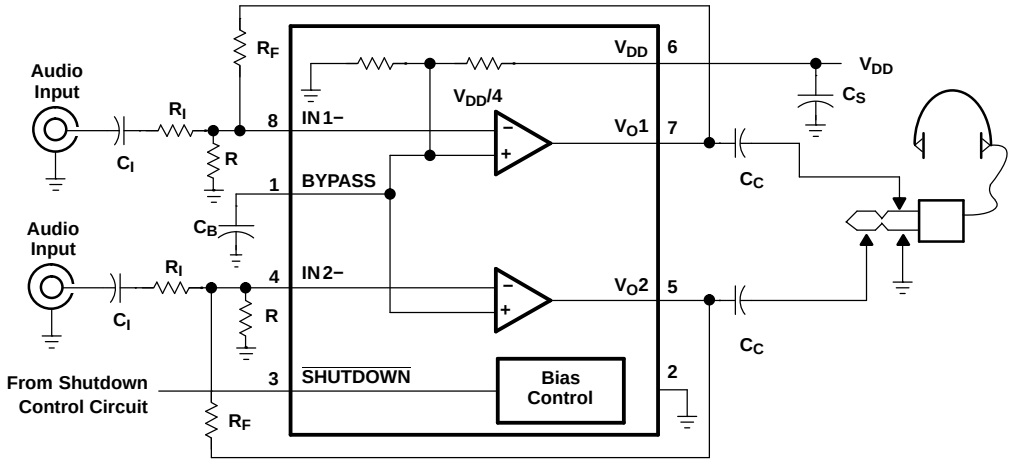
DESCRIPTION

The TPA6100A2D is a stereo audio power amplifier packaged in either an 8-pin SOIC package or an 8-pin MSOP package capable of delivering 50 mW of continuous RMS power per channel into 16-Ω loads. Amplifier gain is externally configured by a means of three resistors per input channel and does not require external compensation for settings of 1 to 10.

The TPA6100A2D is optimized for battery applications because of its low supply current, shutdown current, and THD+N. To obtain the low-supply voltage range, the TPA6100A2D biases BYPASS to $V_{DD}/4$. A resistor with a resistance equal to R_F must be added from the inputs to ground to allow the output to be biased at $V_{DD}/2$.

When driving a 16-Ω load with 45-mW output power from 3.3 V, THD+N is 0.04% at 1 kHz, and less than 0.2% across the audio band of 20 Hz to 20 kHz. For 28 mW into 32-Ω loads, the THD+N is reduced to less than 0.03% at 1 kHz, and is less than 0.2% across the audio band of 20 Hz to 20 kHz.

TYPICAL APPLICATION CIRCUIT



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICE		MSOP SYMBOLIZATION
	SMALL OUTLINE (D)	MSOP(DGK)	
–40°C to 85°C	TPA6100A2D	TPA6100A2DGK	AJL

Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
BYPASS	1	I	Tap to voltage divider for internal mid-supply bias supply. BYPASS is set at V_{DD}/4. Connect to a 0.1-µF to 1-µF low-ESR capacitor for best performance.
GND	2	I	GND is the ground connection.
IN1-	8	I	IN1- is the inverting input for channel 1.
IN2-	4	I	IN2- is the inverting input for channel 2.
$\overline{\text{SHUTDOWN}}$	3	I	Active-low input. When held low, the device is placed in a low supply current mode.
V_{DD}	6	I	V_{DD} is the supply voltage terminal.
V_O1	7	O	V_O1 is the audio output for channel 1.
V_O2	5	O	V_O2 is the audio output for channel 2.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		UNIT
V_{DD}	Supply voltage	4 V
V_I	Input voltage	–0.3 V to V_{DD} + 0.3 V
	Continuous total power dissipation	Internally limited
T_J	Operating junction temperature range	–40°C to 150°C
T_{stg}	Storage temperature range	–65°C to 150°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

(1) Stresses beyond thoselisted under "absolute maximum ratings" may cause permanent damage to thedevice. These are stress ratings only, and functional operation of the deviceat these or any other conditions beyond those indicated under "recommendedoperating conditions" is not implied. Exposure to absolute-maximum-ratedconditions for extended periods may affect devicereliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	710 mW	5.68 mW/°C	454 mW	369 mW
DGK	469 mW	3.75 mW/°C	300 mW	244 mW

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V_{DD}	Supply voltage		1.6	3.6	V
T_A	Operating free-air temperature		–40	85	°C
V_{IH}	High-level input voltage	$\overline{\text{SHUTDOWN}}$	0.6 x V_{DD}		V
V_{IL}	Low-level input voltage	$\overline{\text{SHUTDOWN}}$		0.25 x V_{DD}	

DC ELECTRICAL CHARACTERISTICS

at T_A = 25°C, V_{DD} = 3.6 V (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OO}	Output offset voltage	A_V = 2 V/V		5	40	mV
PSRR	Power supply rejection ratio	V_{DD} = 3.0 V to 3.6 V		72		dB
I_{DD}	Supply current	$\overline{SHUTDOWN}$ = 3.6 V		0.75	2.0	mA
$I_{DD(SD)}$	Supply current in $\overline{SHUTDOWN}$ mode	$\overline{SHUTDOWN}$ = 0 V		50	250	nA
$\|I_{IH}\|$	High-level input current ($\overline{SHUTDOWN}$)	V_{DD} = 3.6 V, $V_I = V_{DD}$			1	µA
$\|I_{IL}\|$	Low-level input current ($\overline{SHUTDOWN}$)	V_{DD} = 3.6 V, V_I = 0 V			1	µA
Z_I	Input impedance (IN1-, IN2-)			> 1		MΩ

AC OPERATING CHARACTERISTICS

V_{DD} = 3.3 V, T_A = 25°C, R_L = 16 Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Output power (each channel)	THD ≤ 0.1%, f = 1 kHz		50		mW
THD+N	Total harmonic distortion + noise	P_O = 45 mW, 20 Hz–20 kHz		0.2%		
B_{OM}	Maximum output power BW	G = 1, THD < 0.5%		> 20		kHz
k_{SVR}	Supply ripple rejection	f = 1 kHz		52		dB
SNR	Signal-to-noise ratio	P_O = 50 mW		90		dB
V_n	Noise output voltage (no noise-weighting filter)			28		µV(rms)

AC OPERATING CHARACTERISTICS

V_{DD} = 3.3 V, T_A = 25°C, R_L = 32 Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Output power (each channel)	THD ≤ 0.1%, f = 1 kHz		35		mW
THD+N	Total harmonic distortion + noise	P_O = 30 mW, 20 Hz–20 kHz		0.2%		
B_{OM}	Maximum output power BW	G = 1, THD < 0.2%		> 20		kHz
k_{SVR}	Supply ripple rejection	f = 1 kHz		52		dB
SNR	Signal-to-noise ratio	P_O = 35 mW		91		dB
V_n	Noise output voltage (no noise-weighting filter)			28		µV(rms)

DC ELECTRICAL CHARACTERISTICS

at T_A = 25°C, V_{DD} = 1.6 V (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OO}	Output offset voltage	A_V = 2 V/V		5	40	mV
PSRR	Power supply rejection ratio	V_{DD} = 1.5 V to 1.7 V		80		dB
I_{DD}	Supply current	$\overline{SHUTDOWN}$ = 1.6 V		1.2	1.5	mA
$I_{DD(SD)}$	Supply current in $\overline{SHUTDOWN}$ mode	$\overline{SHUTDOWN}$ = 0 V		50	250	nA
$\|I_{IH}\|$	High-level input current ($\overline{SHUTDOWN}$)	V_{DD} = 1.6 V, V_I= V_{DD}			1	µA
$\|I_{IL}\|$	Low-level input current ($\overline{SHUTDOWN}$)	V_{DD} = 1.6 V, V_I= 0 V			1	µA
Z_I	Input impedance (IN1-, IN2-)			> 1		MΩ

AC OPERATING CHARACTERISTICS

V_{DD} = 1.6 V, T_A = 25°C, R_L = 16 Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Output power (each channel)	THD≤ 0.1%, f = 1 kHz		9.5		mW
THD+N	Total harmonic distortion + noise	P_O = 9.5 mW, 20 Hz–20 kHz		0.4%		
B_{OM}	Maximum output power BW	G = 0 dB, THD < 0.4%		> 20		kHz
k_{SVR}	Supply ripple rejection	f = 1 kHz		53		dB
SNR	Signal-to-noise ratio	P_O = 9.5 mW		86		dB
V_n	Noise output voltage (no noise-weighting filter)			18		µV(rms)

AC OPERATING CHARACTERISTICS

V_{DD} = 1.6 V, T_A = 25°C, R_L = 32 Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Output power (each channel)	THD≤ 0.1%, f = 1 kHz		7.1		mW
THD+N	Total harmonic distortion + noise	P_O = 6.5 mW, 20 Hz–20 kHz		0.3%		
B_{OM}	Maximum output power BW	G = 0 dB, THD < 0.3%		> 20		kHz
k_{SVR}	Supply ripple rejection	f = 1 kHz		53		dB
SNR	Signal-to-noise ratio	P_O = 7.1 mW		88		dB
V_n	Noise output voltage (no noise-weighting filter)			18		µV(rms)

APPLICATION INFORMATION

GAIN SETTING RESISTORS, R_F, R_I, and R

The voltage gain for the TPA6100A2D is set by resistors R_F and R_I according to Equation 1.

$$\text{Gain} = -\left(\frac{R_F}{R_I}\right) \text{ or Gain (dB)} = 20 \log\left(\frac{R_F}{R_I}\right) \quad (1)$$

Given that the TPA6100A2D is an MOS amplifier, the input impedance is high. Consequently, input leakage currents are not generally a concern, although noise in the circuit increases as the value of R_F increases. In addition, a certain range of R_F values is required for proper start-up operation of the amplifier. Taken together, it is recommended that the effective impedance seen by the inverting node of the amplifier be set between 5 kΩ and 20 kΩ. The effective impedance is calculated in Equation 2.

$$\text{Effective Impedance} = \frac{R_F R_I}{R_F + R_I} \quad (2)$$

As an example, consider an input resistance of 20 kΩ and a feedback resistor of 20 kΩ. The gain of the amplifier would be –1 and the effective impedance at the inverting terminal would be 10 kΩ, which is within the recommended range.

For high-performance applications, metal film resistors are recommended because they tend to have lower noise levels than carbon resistors. For values of R_F above 50 kΩ, the amplifier tends to become unstable due to a pole formed from R_F and the inherent input capacitance of the MOS input structure. For this reason, a small compensation capacitor of approximately 5 pF should be placed in parallel with R_F. In effect, this creates a low-pass filter network with the cutoff frequency defined in Equation 3.

$$f_c = \frac{1}{2\pi R_F C_F} \quad (3)$$

For example, if R_F is 100 kΩ and C_F is 5 pF, then f_c is 318 kHz, which is well outside the audio range.

For maximum signal swing and output power at low supply voltages like 1.6 V to 3.3 V, BYPASS is biased to $V_{DD}/4$. However, to allow the output to be biased at $V_{DD}/2$, a resistor, R, equal to R_F must be placed from the negative input to ground.

INPUT CAPACITOR, C_I

In the typical application, an input capacitor, C_I, is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_I and R_I form a high-pass filter with the corner frequency determined in Equation 4.

$$f_c = \frac{1}{2\pi R_I C_I} \quad (4)$$

The value of C_I is important to consider, as it directly affects the bass (low-frequency) performance of the circuit. Consider the example where R_I is 20 kΩ and the specification calls for a flat bass response down to 20 Hz. Equation 4 is reconfigured as Equation 5.

$$C_I = \frac{1}{2\pi R_I f_c} \quad (5)$$

In this example, C_I is 0.4 µF, so one would likely choose a value in the range of 0.47 µF to 1 µF. A further consideration for this capacitor is the leakage path from the input source through the input network (R_I, C_I) and the feedback resistor (R_F) to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high-gain applications (>10). For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications, as the dc level there is held at $V_{DD}/4$, which is likely higher than the source dc level. It is important to confirm the capacitor polarity in the application.

APPLICATION INFORMATION (continued)

POWER SUPPLY DECOUPLING, C_S

The TPA6100A2D is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure that the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 µF, placed as close as possible to the device V_{DD} lead, works best. For filtering lower frequency noise signals, a larger aluminum electrolytic capacitor of 10 µF or greater placed near the power amplifier is recommended.

MIDRAIL BYPASS CAPACITOR, C_B

The midrail bypass capacitor (C_B) serves several important functions. During start-up, C_B determines the rate at which the amplifier starts up. This helps to push the start-up pop noise into the subaudible range (so low it can not be heard). The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier. The capacitor is fed from a 55-kΩ source inside the amplifier. To keep the start-up pop as low as possible, the relationship shown in Equation 6 should be maintained.

$$\frac{1}{\left(C_B \times 55\ k\Omega\right)} \leq \frac{1}{\left(C_I R_I\right)} \tag{6}$$

As an example, consider a circuit where C_B is 1 µF, C_I is 1 µF, and R_I is 20 kΩ. Inserting these values into Equation 6 results in: 18.18 ≤ 50 which satisfies the rule. Bypass capacitor (C_B) values of 0.47-µF to 1-µF ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

OUTPUT COUPLING CAPACITOR, C_C

In the typical single-supply, single-ended (SE) configuration, an output coupling capacitor (C_C) is required to block the dc bias at the output of the amplifier, thus preventing dc currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by Equation 7.

$$f_c = \frac{1}{2\pi R_L C_C} \tag{7}$$

The main disadvantage, from a performance standpoint, is that the typically small load impedances drive the low-frequency corner higher. Large values of C_C are required to pass low frequencies into the load. Consider the example where a C_C of 68 µF is chosen and loads vary from 32 Ω to 47 kΩ. Table 1 summarizes the frequency response characteristics of each configuration.

Table 1. Common Load Impedances vs Low Frequency Output Characteristics in SE Mode

R_L	C_C	LOWEST FREQUENCY
32 Ω	68 µF	73 Hz
10,000 Ω	68 µF	0.23 Hz
47,000 Ω	68 µF	0.05 Hz

As Table 1 indicates, headphone response is adequate and drive into line level inputs (a home stereo for example) is good.

The output coupling capacitor required in single-supply, SE mode also places additional constraints on the selection of other components in the amplifier circuit. With the rules described earlier still valid, add the following relationship:

$$\frac{1}{\left(C_B \times 55\ k\Omega\right)} \leq \frac{1}{\left(C_I R_I\right)} \ll \frac{1}{R_L C_C} \quad (8)$$

USING LOW-ESR CAPACITORS

Low-ESR capacitors are recommended throughout this application. A real capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance, the more the real capacitor behaves like an ideal capacitor.

3.3-V VERSUS 1.6-V OPERATION

The TPA6100A2D was designed for operation over a supply range of 1.6 V to 3.6 V. There are no special considerations for 1.6-V versus 3.3-V operation as far as supply bypassing, gain setting, or stability. The most important consideration is that of output power. Each amplifier can produce a maxium output voltage swing within a few hundred millivolts of the rails with a 10-kΩ load. However, this voltage swing decreases as the load resistance decreases and the $r_{DS(on)}$ as the output stage transistors becomes more significant. For example, for a 32-Ω load, the maximum peak output voltage with V_{DD} = 1.6 V is approximately 0.7 V with no clipping distortion. This reduced voltage swing effectively reduces the maximum undistorted output power.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPA6100A2D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	6100A2	Samples
TPA6100A2DGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AJL	Samples
TPA6100A2DGKG4	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AJL	Samples
TPA6100A2DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AJL	Samples
TPA6100A2DGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AJL	Samples
TPA6100A2DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	6100A2	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

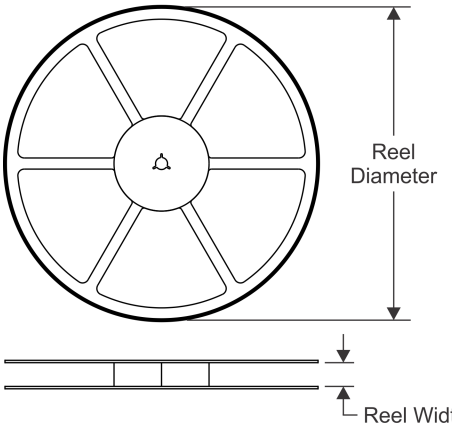
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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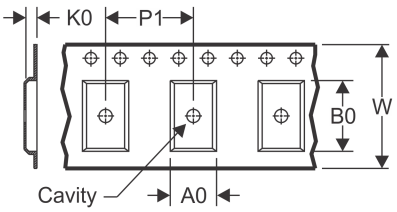
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

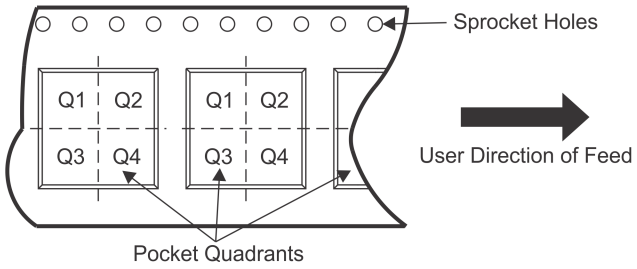


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

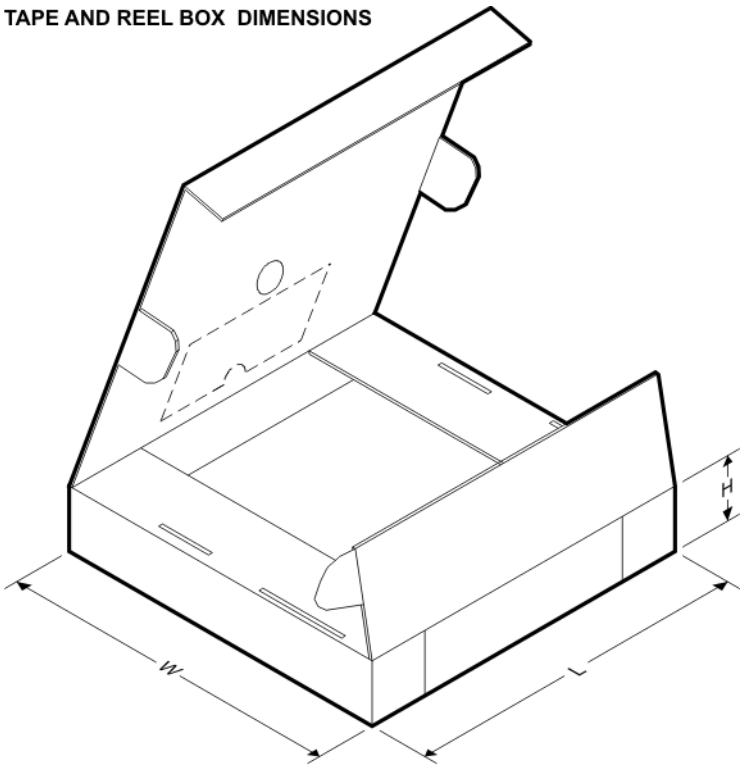
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

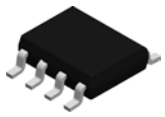
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA6100A2DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPA6100A2DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA6100A2DGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
TPA6100A2DR	SOIC	D	8	2500	350.0	350.0	43.0

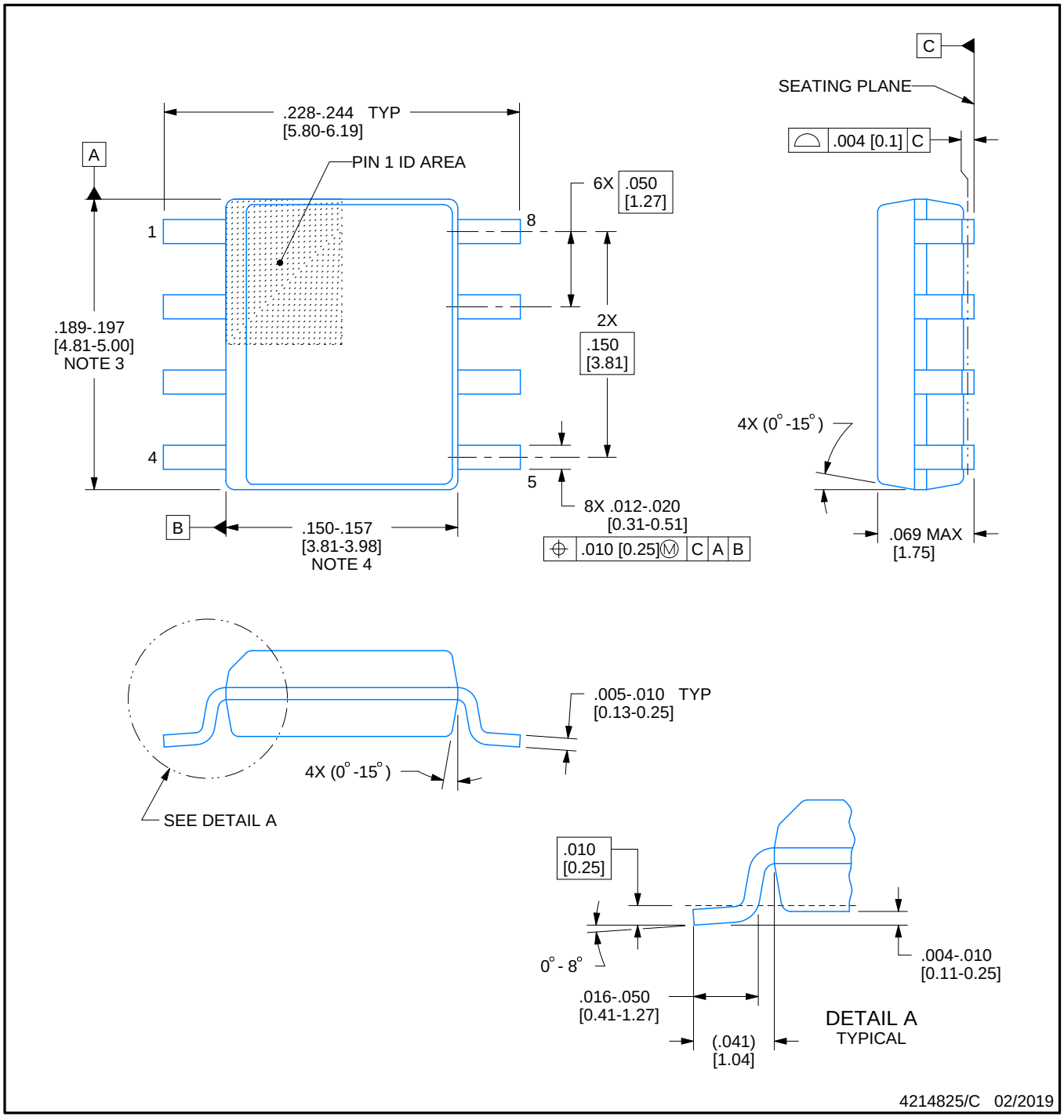


PACKAGE OUTLINE

D0008A

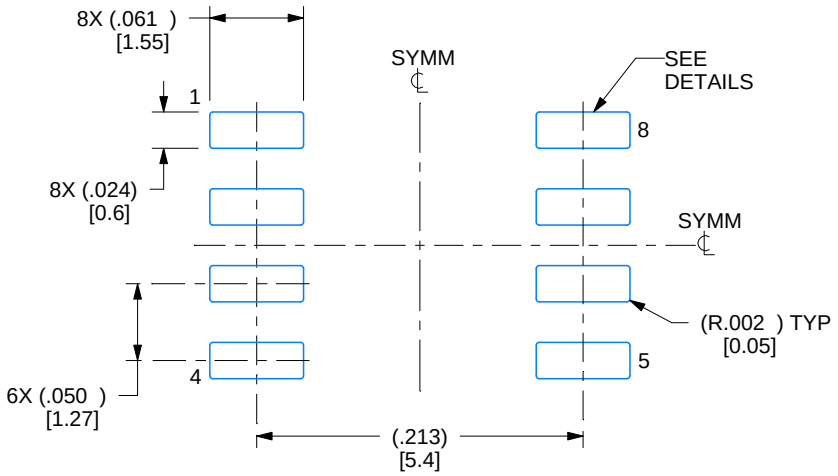
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

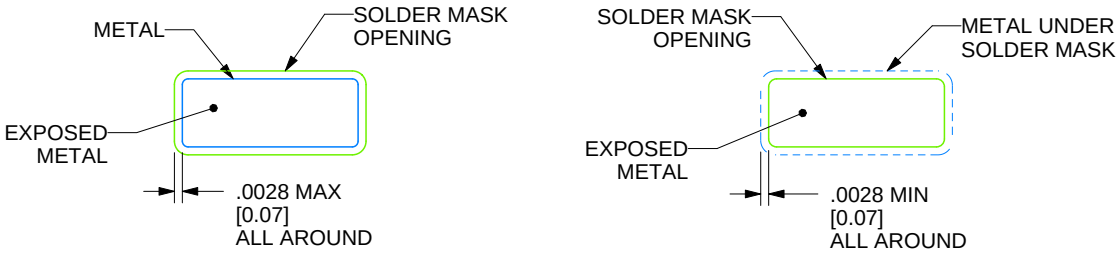


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

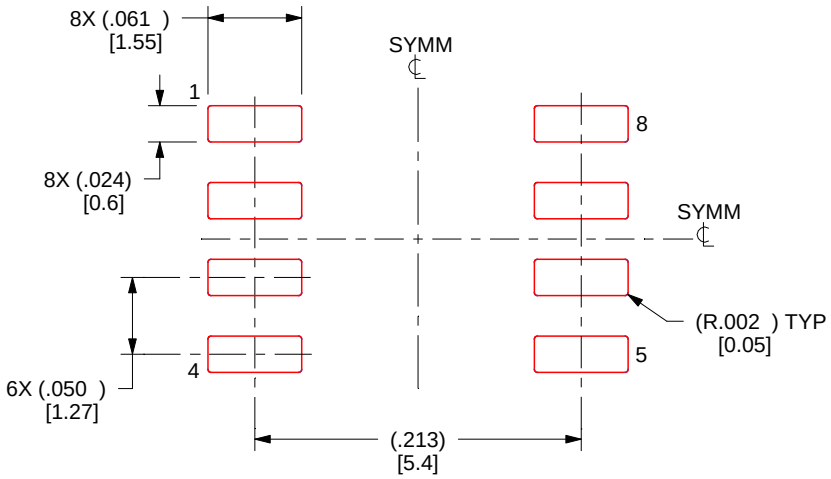
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



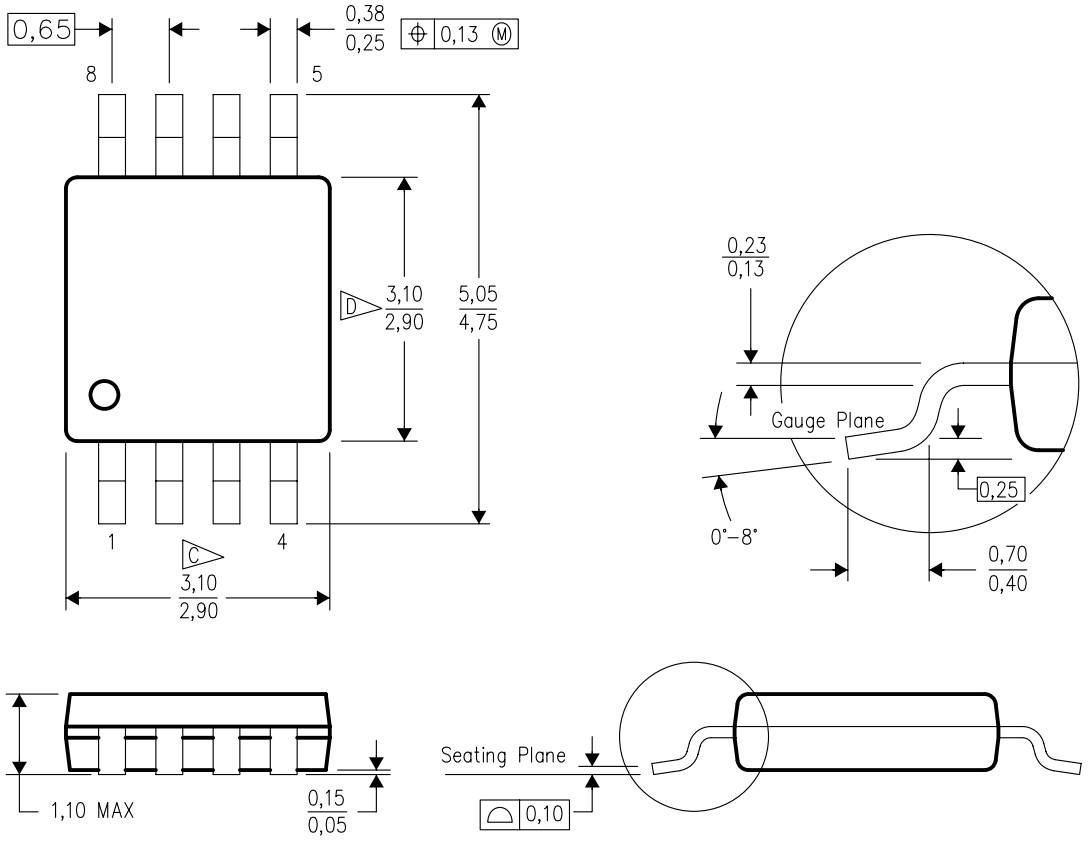
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

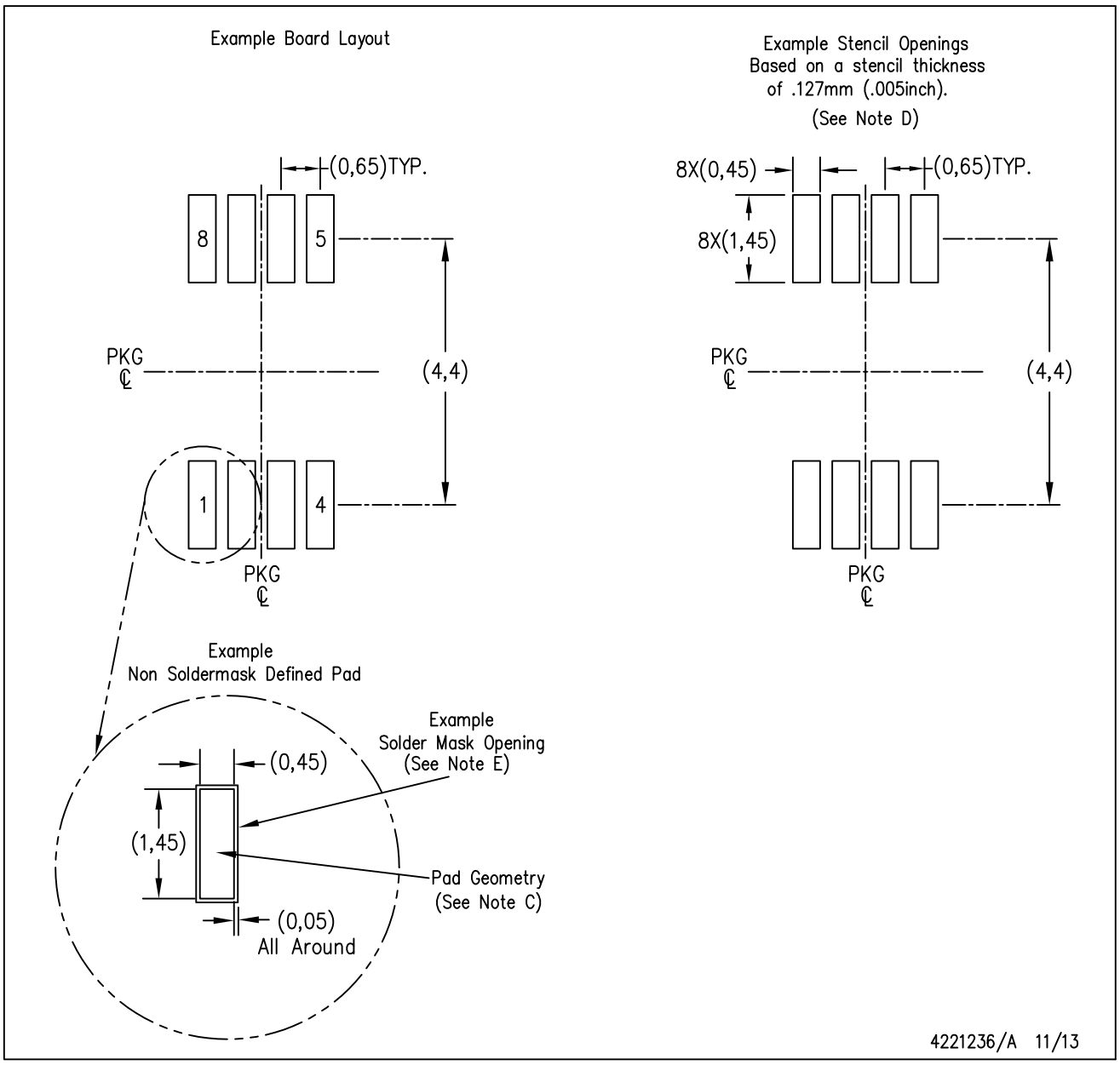
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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