MIC5388/9

Dual 200mA Peak LDO in Wafer Level Chip Scale Package

General Description

The MIC5388/9 is an advanced dual LDO ideal for powering general purpose portable devices. The MIC5388/9 provides two independently-controlled, high-performance, 200mA peak (150mA continuous) LDOs in a miniature 6-bump, 0.5mm pitch, 1.5mm × 1.0mm wafer level chip scale package (WLCSP).

Ideal for battery-powered applications, the MIC5388/9 offers 2% accuracy, low dropout voltage (175mV @ 150mA) and low ground current (typically 32µA per LDO). The MIC5388/9 can also be put into a zero off mode current state, drawing virtually no current when disabled.

When the MIC5389 is disabled an internal resistive load is automatically applied to the output to discharge the output capacitor. This LDO offers fast transient response and high PSRR while consuming a minimum operating current.

Data sheets and support documentation can be found on Micrel's web site at www.micrel.com.

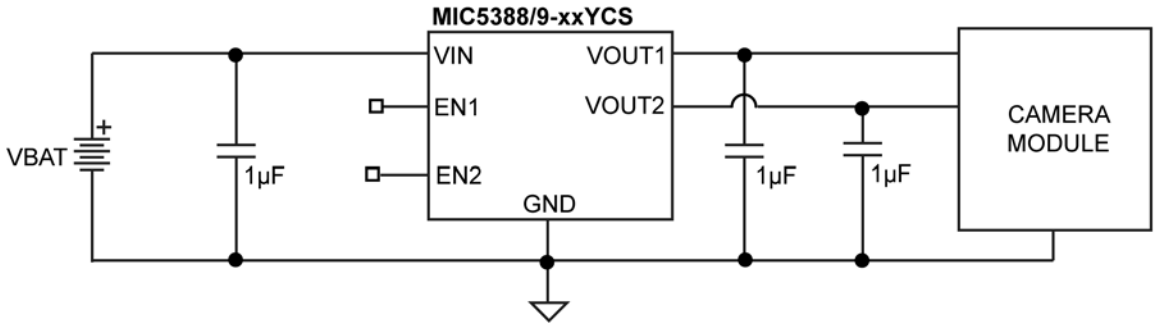
Features

- 2.5V to 5.5V input voltage range
- Two 200mA peak output current LDOs
- High output accuracy (±2%)
- Low quiescent current (32µA per LDO)
- Stable with 1µF ceramic output capacitors
- Low dropout voltage (175mV at 150mA)
- Independent enable pins
- Output discharge circuit (MIC5389)
- Thermal-shutdown protection
- Current-limit protection
- 6-bump 1.5mm × 1.0mm WLCSP package

Applications

- Camera phones
- Mobile phones
- DSC, GPS, PMP, and PDAs
- Portable medical devices
- Portable electronics

Typical Application



Camera Module Power Supply

Ordering Information

Manufacturing Part Number[1, 2]	Marking Code	Voltage V_{OUT1}/V_{OUT2}	Junction Temperature Range	Package
MIC5388-SGYCS*	8A8	3.3V/1.8V	–40° to +125°C	6-Bump Wafer Level Chip Scale Package
MIC5388-MMYCS*	8B8	2.8V/2.8V	–40° to +125°C	6-Bump Wafer Level Chip Scale Package
MIC5388-MLYCS*	8C8	2.8V/2.7V	–40° to +125°C	6-Bump Wafer Level Chip Scale Package
MIC5388-MGYCS	8D8	2.8V/1.8V	–40° to +125°C	6-Bump Wafer Level Chip Scale Package
MIC5388-M4YCS*	8E8	2.8V/1.2V	–40° to +125°C	6-Bump Wafer Level Chip Scale Package
MIC5388-G4YCS*	8F8	1.8V/1.2V	–40° to +125°C	6-Bump Wafer Level Chip Scale Package
MIC5389-SGYCS*	8A9	3.3V/2.8V	–40° to +125°C	6-Bump Wafer Level Chip Scale Package
MIC5389-MMYCS*	8B9	2.8V/2.8V	–40° to +125°C	6-Bump Wafer Level Chip Scale Package
MIC5389-MLYCS*	8C9	2.8V/2.7V	–40° to +125°C	6-Bump Wafer Level Chip Scale Package
MIC5389-MGYCS	8D9	2.8V/1.8V	–40° to +125°C	6-Bump Wafer Level Chip Scale Package
MIC5389-M4YCS*	8E9	2.8V/1.2V	–40° to +125°C	6-Bump Wafer Level Chip Scale Package
MIC5389-G4YCS*	8F9	1.8V/1.2V	–40° to +125°C	6-Bump Wafer Level Chip Scale Package

Notes:

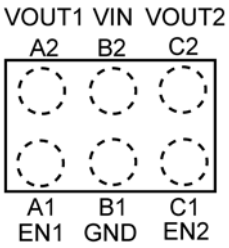
1. Other voltages available. Contact Micrel Marketing for details.
2. MIC5389 offers auto-discharge function.

* Contact Micrel Marketing for availability.

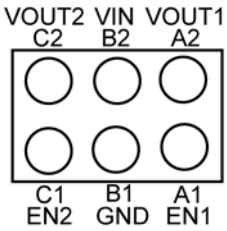
Pin Configuration



Ball A1 Identifier



TOP VIEW



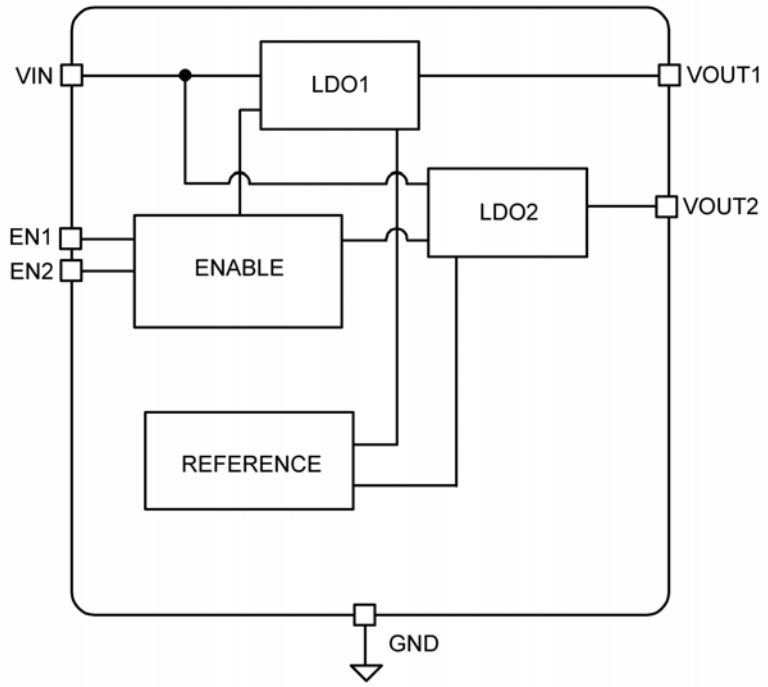
BOTTOM VIEW

6-Bump, 0.5mm Pitch WLCSP (CS)

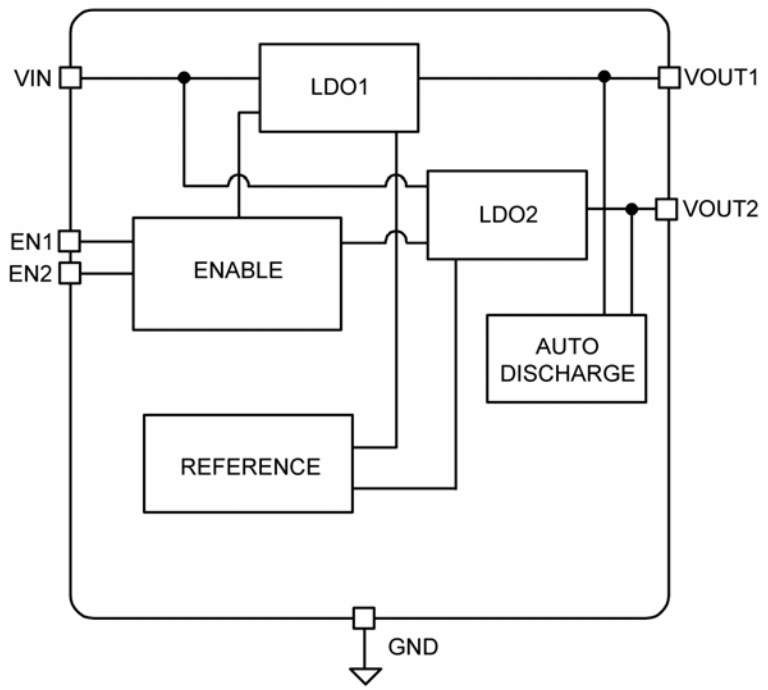
Pin Description

Pin Number	Pin Name	Pin Function
A1	EN1	Enable Regulator 1. Active High Input. Logic High = On; Logic Low = Off. Do not leave floating.
B1	GND	Ground.
C1	EN2	Enable Regulator 2. Active High Input. Logic High = On; Logic Low = Off. Do not leave floating.
C2	VOUT2	Regulator Output – LDO2
B2	VIN	Voltage Supply Input.
A2	VOUT1	Regulator Output – LDO1

Functional Block Diagrams



MIC5388 Block Diagram



MIC5389 Block Diagram

Absolute Maximum Ratings[1]

Supply Voltage (V_{IN}) ..... –0.3V to +6V
Enable Voltage (V_{EN1}, V_{EN2}) ..... –0.3V to V_{IN}
Power Dissipation (P_D) ..... Internally Limited[3]
Lead Temperature (soldering, 10sec.) ..... 260°C
Junction Temperature (T_J) ..... –40°C to +125°C
Storage Temperature (T_S) ..... –65°C to +150°C
ESD Rating[4] 2kV

Operating Ratings[2]

Supply Voltage (V_{IN}) ..... +2.5V to +5.5V
Enable Voltage (V_{EN1}, V_{EN2}) ..... –0.3V to V_{IN}
Junction Temperature (T_A) ..... –40°C to +125°C
Junction Thermal Resistance
6-Bump, 0.5mm Pitch WLCSP (θ_{JA}) ..... 108°C/W

Electrical Characteristics[5]

V_{IN} = V_{EN1} = V_{EN2} = V_{OUT} + 1V; higher of the two regulator outputs; $I_{OUTLDO1}$ = $I_{OUTLDO2}$ = 100µA; C_{OUT1} = C_{OUT2} = 1µF; T_J = 25°C, **bold** values indicate –40°C to +125°C, unless noted.

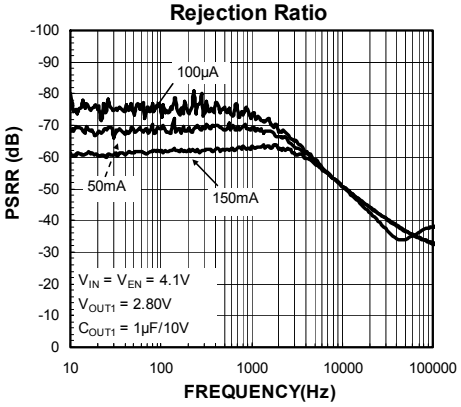
Parameter	Condition	Min.	Typ.	Max.	Units
Output Voltage Accuracy	Variation from nominal V_{OUT}	–2.0		+2.0	%
	Variation from nominal V_{OUT}; –40°C to +125°C	**–3.0**		**+3.0**	
Line Regulation	V_{IN} = V_{OUT} +1V to 5.5V, I_{OUT} = 100µA		0.02	**0.3**	%/V
Load Regulation	I_{OUT} = 100µA to 150mA		0.3	1.2	%
Dropout Voltage	I_{OUT} = 50mA		55	**110**	mV
	I_{OUT} = 150mA		175	**310**	
Ground Pin Current	V_{EN1} = High; V_{EN2} = Low; I_{OUT} = 0mA		32	**45**	µA
	V_{EN1} = Low; V_{EN2} = High; I_{OUT} = 0mA		32	**45**	
	V_{EN1} = V_{EN2} = High; I_{OUT1} = I_{OUT2} = 0mA		60	**85**	
Ground Pin Current in Shutdown	V_{EN1} = V_{EN2} = 0V		0.05	1	µA
Ripple Rejection	f = 1kHz; C_{OUT} = 1µF		73		dB
Current Limit	V_{OUT} = 0V	200	325	550	mA
Output Voltage Noise	C_{OUT} = 1µF, 10Hz to 100kHz		175		μV_{RMS}
Auto-Discharge NFET Resistance	MIC5389 Only; V_{EN1} = V_{EN2} = 0V; V_{IN} = 3.6V		30		Ω
Enable Inputs (EN1/EN2)					
Enable Input Voltage	Logic Low			**0.2**	V
	Logic High	**1.2**			
Enable Input Current	V_{IL} ≤ 0.2V		0.01	**1**	µA
	V_{IH} ≥ 1.2V		0.01	**1**	
Turn-On Time	C_{OUT} = 1µF		50	**125**	µs

Notes:

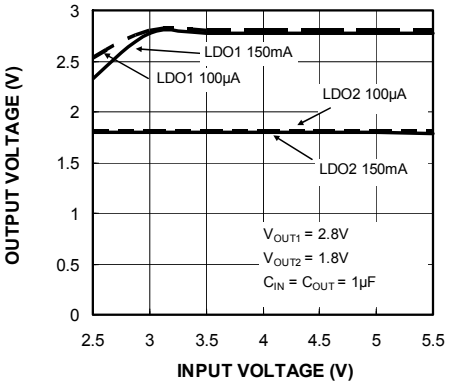
1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside its operating rating.
3. The maximum allowable power dissipation of any T_A (ambient temperature) is $P_{D(max)} = (T_{J(max)} – T_A) / \theta_{JA}$. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the regulator will go into thermal shutdown.
4. Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5kΩ in series with 100pF.
5. Specification for packaged product only.

Typical Characteristics

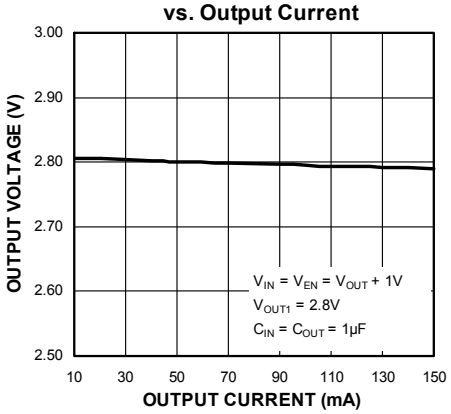
Power Supply Rejection Ratio



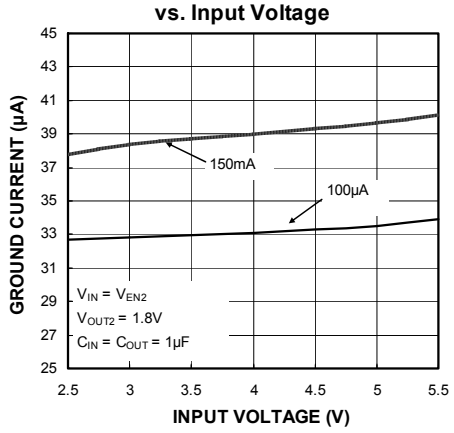
Output Voltage vs. Input Voltage



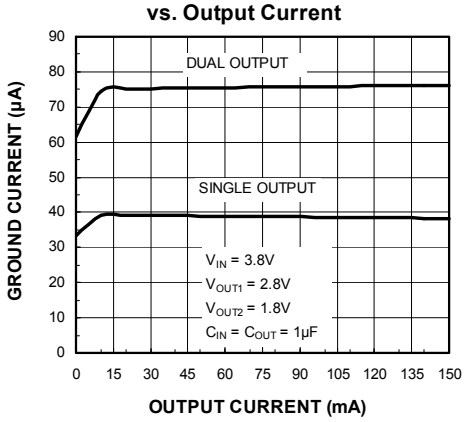
Output Voltage vs. Output Current



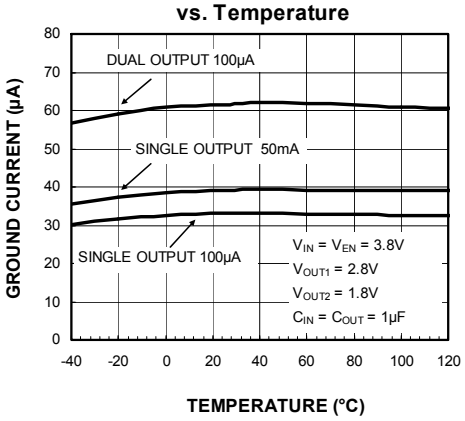
Ground Current vs. Input Voltage



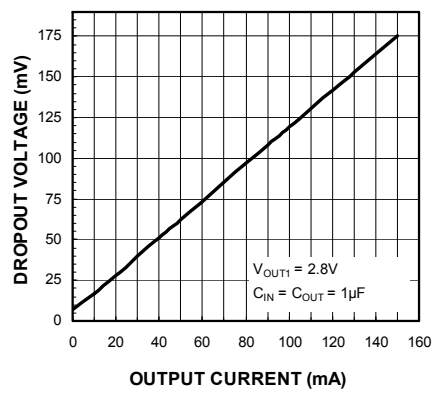
Ground Current vs. Output Current



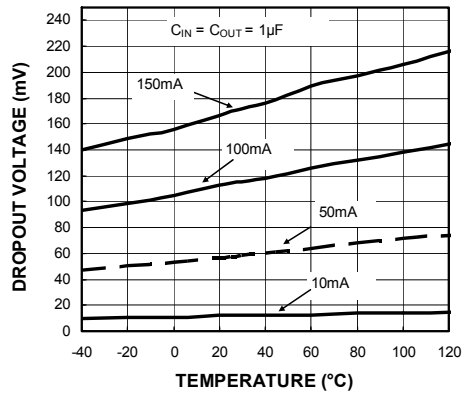
Ground Current vs. Temperature



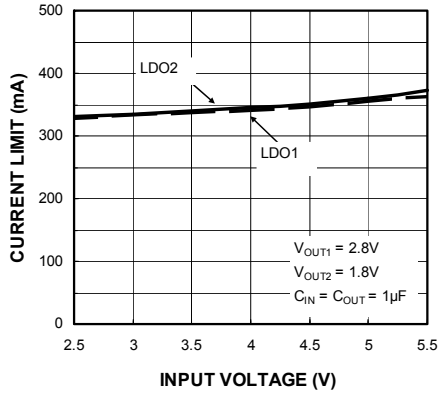
Dropout Voltage vs. Output Current



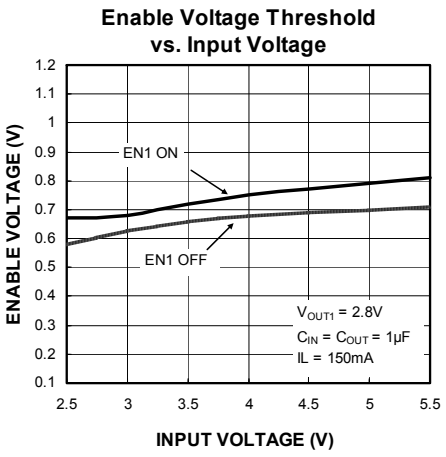
Dropout Voltage vs. Temperature

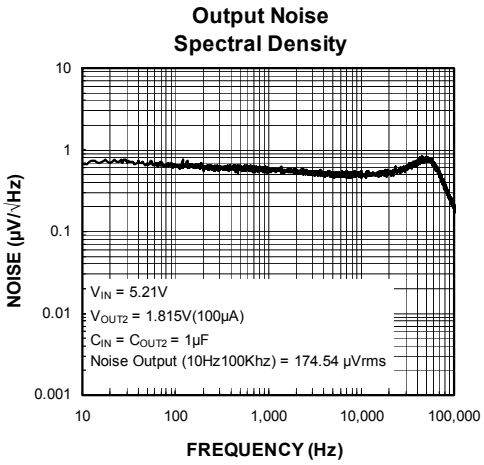


Current Limit vs. Input Voltage



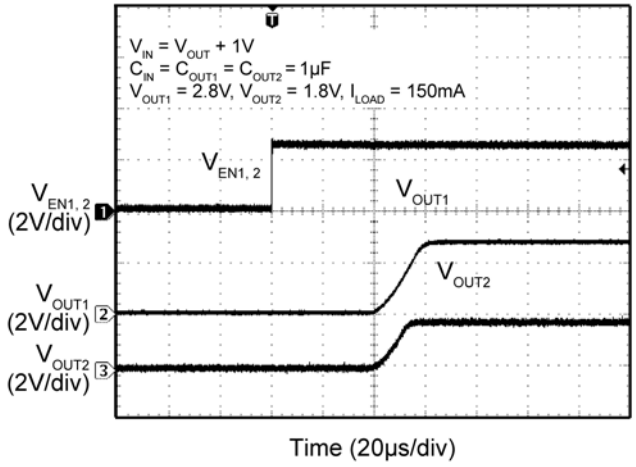
Typical Characteristics (Continued)





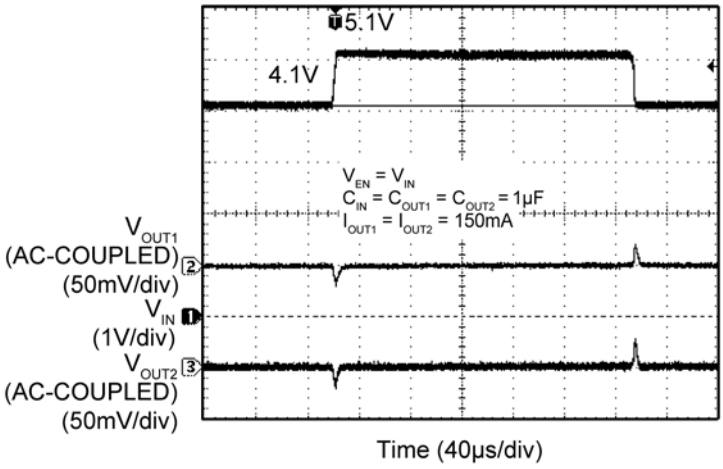
Functional Characteristics

Turn-On Time



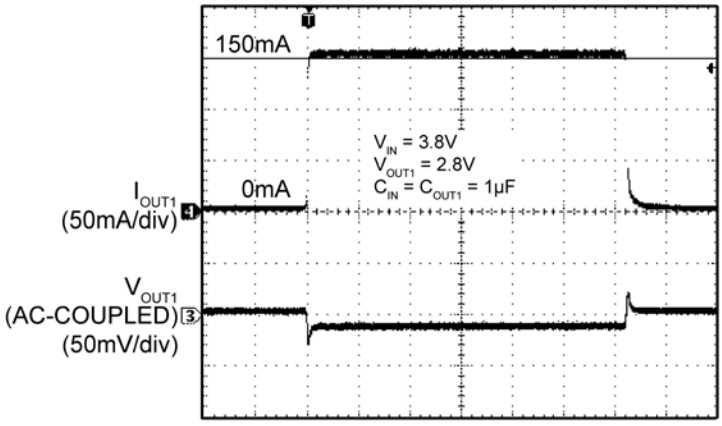
Time (20µs/div)

Line Transient



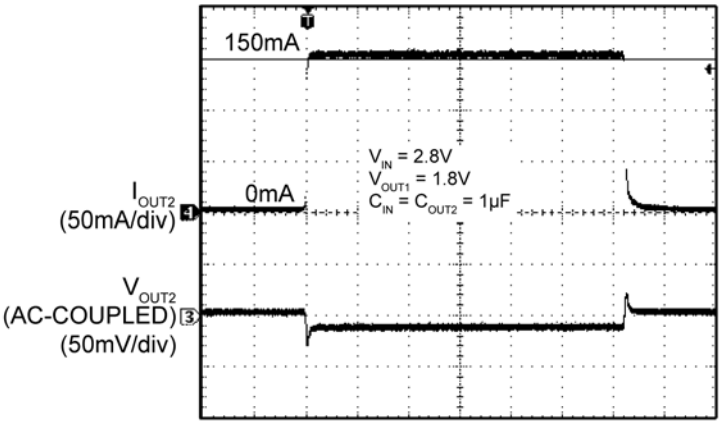
Time (40µs/div)

Load Transient V_{OUT1}



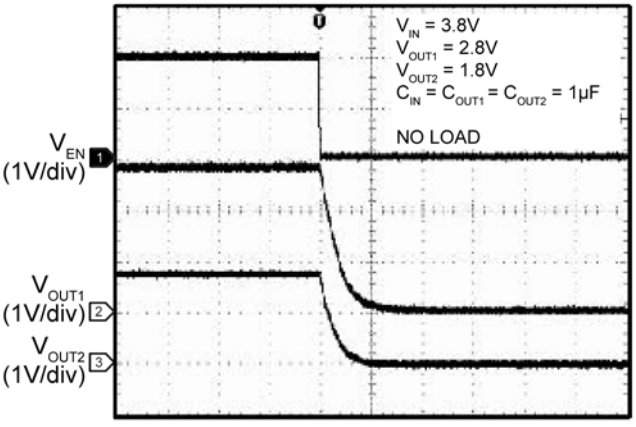
Time (40µs/div)

Load Transient V_{OUT2}



Time (40µs/div)

Turn-Off Time (MIC5389 – Auto Discharge)



Time (100µs/div)

Application Information

MIC5388/9 is a dual 150mA LDO in a miniature 6-bump WLCSP package. The MIC5389 includes an auto-discharge circuit for each of the LDO outputs that are activated when the output is disabled. The MIC5388/9 regulator is fully protected from damage due to fault conditions through linear current limiting and thermal shutdown.

Input Capacitor

The MIC5388/9 is a high-performance, high-bandwidth device. An input capacitor of 1µF capacitor is required from the input to ground to provide stability. Low-ESR ceramic capacitors provide optimal performance at a minimum of space. Additional high-frequency capacitors, such as small-valued NPO dielectric type capacitors, help filter out high-frequency noise and are good practice in any RF-based circuit. X5R or X7R dielectrics are recommended for the input capacitor. Y5V dielectrics lose most of their capacitance over temperature and are therefore, not recommended.

Output Capacitor

The MIC5388/9 requires an output capacitor of 1µF or greater to maintain stability. The design is optimized for use with low-ESR ceramic chip capacitors. High-ESR capacitors may cause high-frequency oscillation. The output capacitor can be increased, but performance has been optimized for a 1µF ceramic output capacitor and does not improve significantly with larger capacitance.

X7R/X5R dielectric type ceramic capacitors are recommended because of their temperature performance. X7R type capacitors change capacitance by 15% over their operating temperature range and are the most stable type of ceramic capacitors. Z5U and Y5V dielectric capacitors change value by as much as 50% and 60%, respectively, over their operating temperature ranges. To use a ceramic chip capacitor with Y5V dielectric, the value must be much higher than an X7R ceramic capacitor to ensure the same minimum capacitance over the equivalent operating temperature range.

No-Load Stability

Unlike many other voltage regulators, the MIC5388/9 will remain stable and in regulation with no load. This is especially important in CMOS RAM keep-alive applications.

Enable/Shutdown

The MIC5388/9 comes with two active high enable pins that allow each regulator to be disabled independently. Forcing the enable pin low disables the regulator and sends it into a “zero” off mode current state. In this state, current consumed by the regulator goes nearly to zero. When disabled the MIC5389 switches a 30Ω (typical) load on the regulator output to discharge the external capacitor.

Forcing the enable pin high enables the output voltage. The active high enable pin uses CMOS technology and the enable pin cannot be left floating; a floating enable pin may cause an indeterminate state on the output.

Thermal Considerations

The MIC5388/9 is designed to provide 150mA of continuous current for both outputs in a very small package. Maximum ambient operating temperature can be calculated based on the output current and the voltage drop across the part. For example if the input voltage is 3.6V, the output voltage is 2.8V for V_{OUT1}, 1.8V for V_{OUT2} and the output current = 150mA. The actual power dissipation of the regulator circuit can be determined using the equation:

$$P_D = (V_{IN} – V_{OUT1})\ I_{OUT1} + (V_{IN} – V_{OUT2})\ I_{OUT2} + V_{IN}\ I_{GND}$$

Because this device is CMOS and the ground current is typically <100µA over the load range, the power dissipation contributed by the ground current is < 1% and can be ignored for this calculation.

$$P_D = (3.6V – 2.8V) \times 150mA + (3.6V - 1.8) \times 150mA$$

$$P_D = 0.39W$$

To determine the maximum ambient operating temperature of the package, use the junction to ambient thermal resistance of the device and the following basic equation:

$$P_{D(MAX)} = \left(\frac{T_{J(MAX)} - T_A}{\theta_{JA}} \right)$$

$T_{J(max)}$ = 125°C, and the maximum junction temperature of the die, θ_{JA}, thermal resistance = 108°C/W.

Substituting P_D for $P_{D(max)}$ and solving for the ambient operating temperature will give the maximum operating conditions for the regulator circuit. The junction-to-ambient thermal resistance for the minimum footprint is 108°C/W.

The maximum power dissipation must not be exceeded for proper operation.

For example, when operating the MIC5388-MGYCS at an input voltage of 3.6V and 150mA loads at each output with a minimum footprint layout, the maximum ambient operating temperature T_A can be determined as follows:

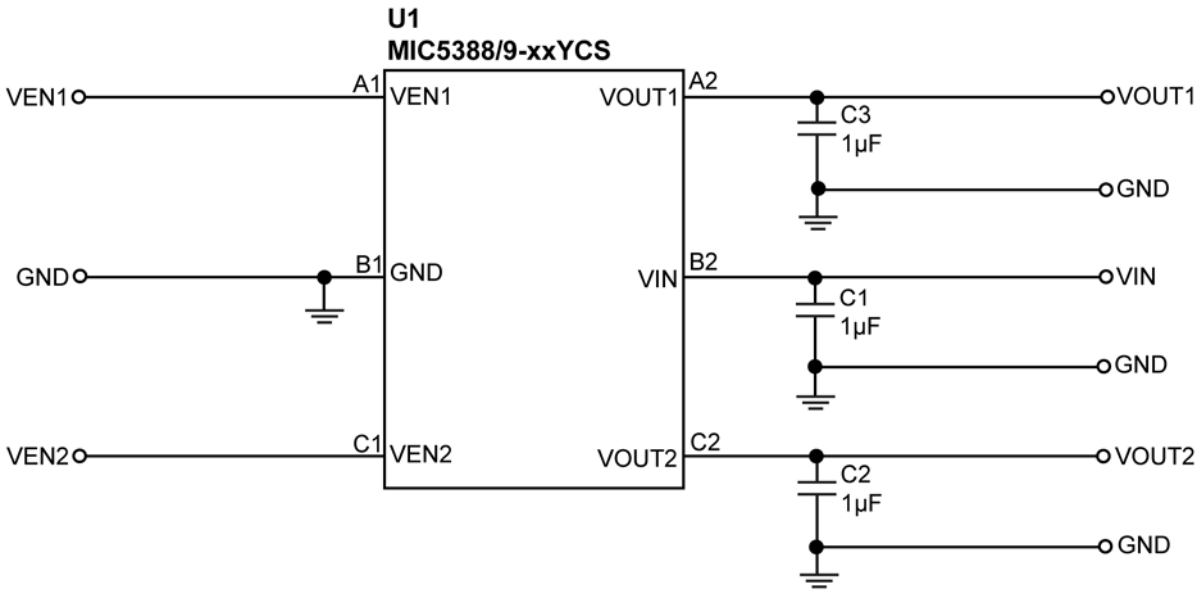
$$0.39W = (125°C – T_A)/(108°C/W)$$

$$T_A = 82.88°C$$

Therefore, a 2.8V/1.8V application with 150mA at each output current can accept an ambient operating temperature of 82.88°C in a miniature 6-bump 0.5mm pitch 1.5mm × 1.0mm WLCSP package. For a full discussion of heat sinking and thermal effects on voltage regulators, refer to the "Regulator Thermals" section of *Micrel's Designing with Low-Dropout Voltage Regulators* handbook. This information can be found on Micrel's website at:

http://www.micrel.com/_PDF/other/LDOBk_ds.pdf

MIC5388/9 Schematic



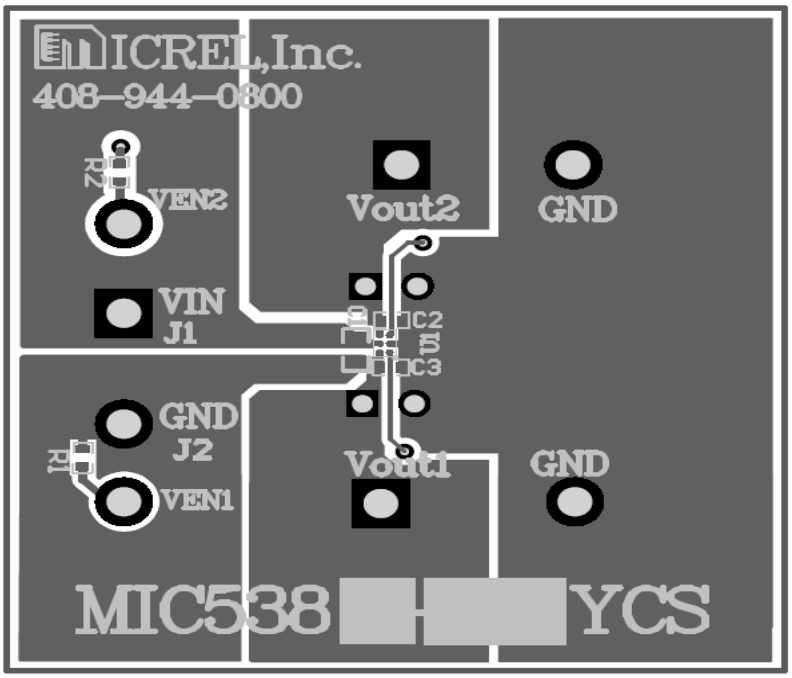
Bill of Materials

Item	Part Number	Manufacturer	Description	Qty.
C1, C2, C3	C1005X5R1A105K	TDK[1]	1µF,10V Ceramic Capacitor, X5R, 0402	**3**
U1	**MIC5388/9-XXYCS**	**Micrel, Inc.[2]**	**Dual, 200mA Peak LDO in Wafer Level Chip Scale Package**	**1**

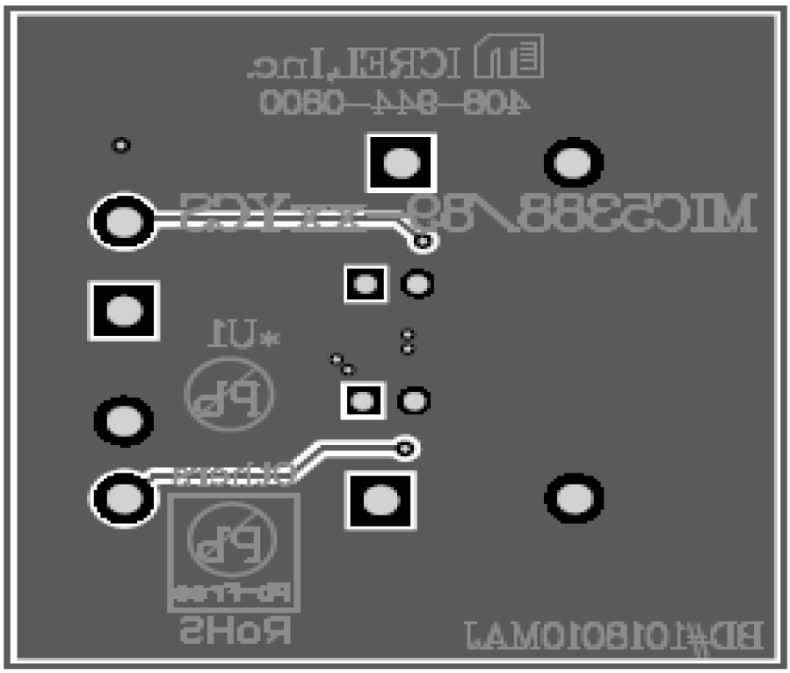
Notes:

1. TDK: www.tdk.com.
2. **Micrel, Inc.: www.micrel.com.**

PCB Layout Recommendations

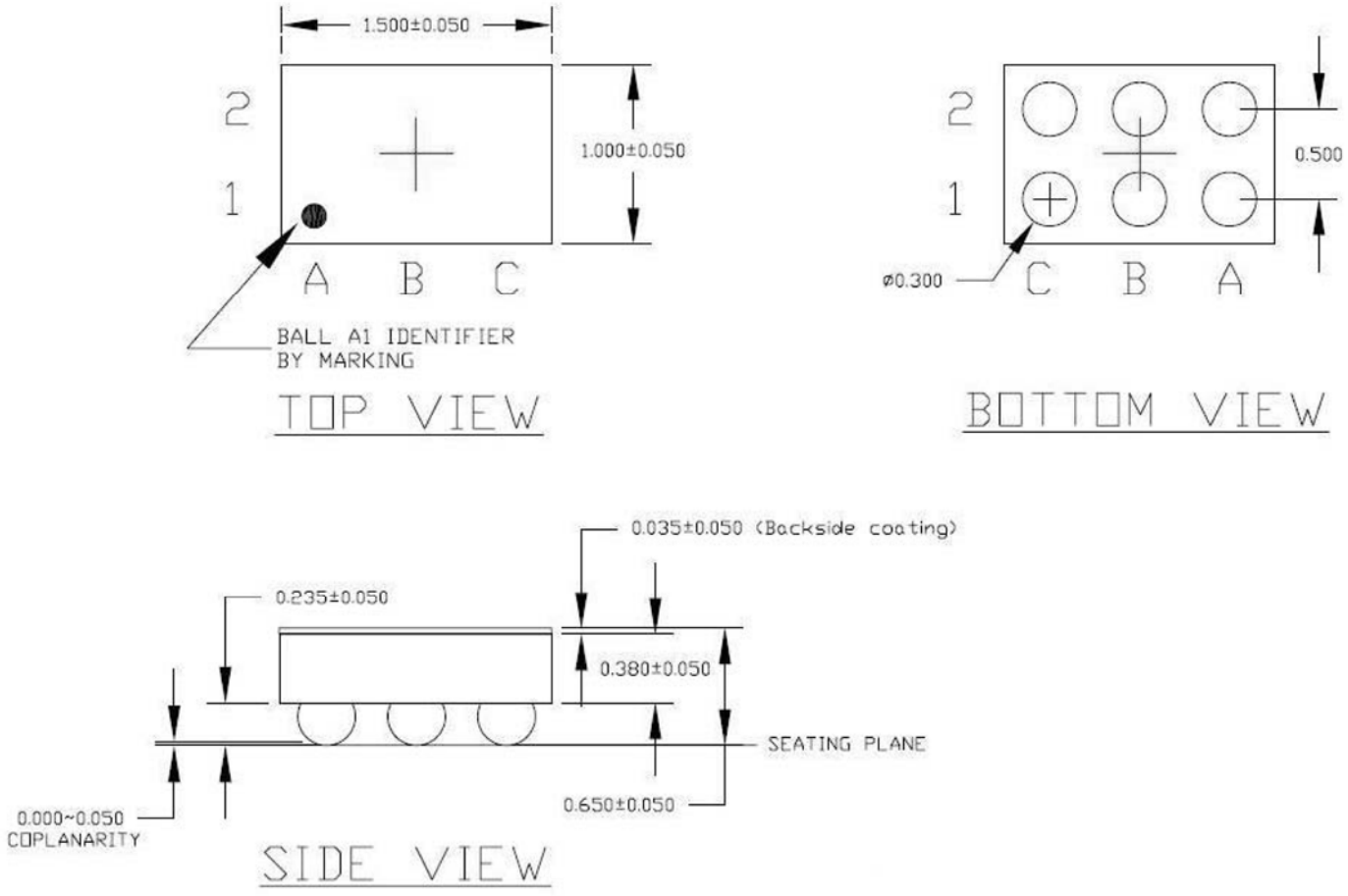


Top Layer



Bottom Layer

Package Information



6-Bump, 0.5mm Pitch 1.5mm × 1.0mm Wafer Level Chip-Scale Package (CS)

MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA
TEL +1 (408) 944-0800 FAX +1 (408) 474-1000 WEB http://www.micrel.com

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