L6920DB

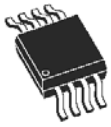
Synchronous rectifier step up converter

General features

- 0.8V start up input voltage
- Up to 5.5V operating input voltage
- Internal synchronous rectifier
- Adjustable output voltage from 1.8V
- 3.3V and 5V fixed output voltages
- Low battery voltage detection
- Reverse battery protection
- 750mA input current limit
- Switching frequency up to 1MHz
- 1.23V reference voltage available

Applications

- Conversion from 1 to 3 alkaline,
- NiMH, NiCd battery cells or 1 lithium ION
- PDA and handheld instruments
- Digital cameras
- Cellular phones
- GPS
- Distributed power



MSOP8

Description

The L6920DB is a high efficiency monolithic step up switching converter IC especially designed for battery powered application.

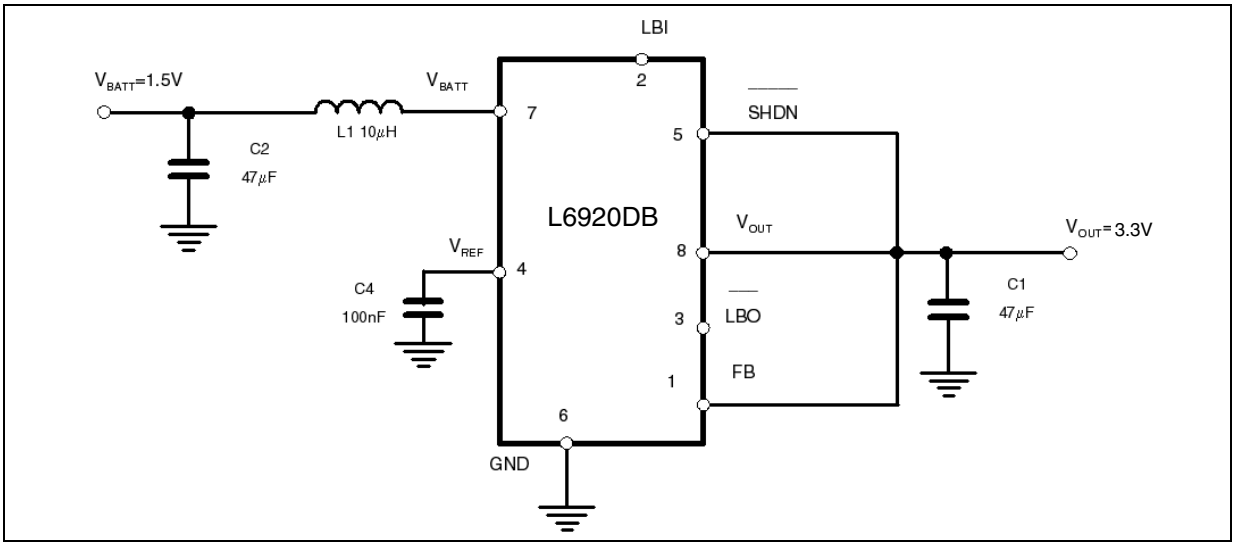
Package is MSOP8 in order to minimize PCB space. It requires only three external components to realize the conversion from the battery voltage to the selected output voltage.

The minimum output voltage is 1.8V: suitable to supply the most advanced ASIC and µP.

High switching frequency allows for a low profile, small sized inductor and output capacitor to be used.

Reference voltage, low battery detection and Shutdown are provided together with over current.

Application circuit



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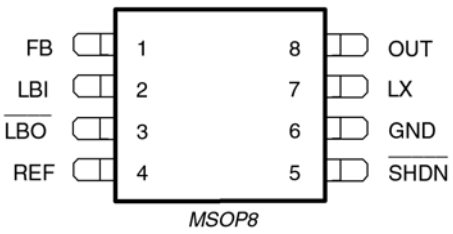
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1 Pin settings

1.1 Pin connection

Figure 1. Pin connection (top view)



1.2 Pin description

Table 1. Pin description

N°	Type	Description
1	FB	Output voltage selector. Connect FB to GND for Vout=5V or to OUT for Vout=3.3V. Connect FB to an external resistor divider for adjustable output voltage
2	LBI	Battery low voltage detector input. The internal threshold is set to 1.23V. A resistor divider is needed to adjust the desired low battery threshold.
3	$\overline{\text{LBO}}$	Battery low voltage detector output. If the voltage at the LBI pin drops below the internal threshold typ. 1.23V, $\overline{\text{LBO}}$ goes low. The $\overline{\text{LBO}}$ is an open drain output and so a pull-up resistor (about 200KΩ) has to be added for correct output setting .
4	REF	1.23V reference voltage. Bypass this output to GND with a 100nF capacitor for filtering high frequency noise. No capacitor is required for stability
5	$\overline{\text{SHDN}}$	Shutdown pin. When pin 5 is below 0.2V the device is in shutdown, when pin 5 is above 0.6V the device is operating.
6	GND	Ground pin
7	LX	Step-up inductor connection
8	OUT	Power OUTPUT pin

2 Electrical data

2.1 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{ccmax}	V_{cc} to GND	6	V
	LBI, $\overline{SHDN}$, FB to GND	6	V
$V_{out\ max}$	Vout to GND	6	V

2.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Maximum thermal resistance junction-ambient	180	°C/W
T_J	Maximum junction temperature	150	°C

3 Electrical characteristics

Table 4. Electrical characteristcs

(V_{IN} = 2V, FB = GND, T_J = 25°C unless otherwise specified)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
V_{CC} Section						
V_{IN}	Minimum Start Up Input Voltage	V_{out} = 3.3V		0.8		V
I_q	Quiescent Current	I_l = 0 mA, FB = 1.4V, V_{out} = 3.3V LBI = SHDN = 2V		9	12	µA
		I_l = 0 mA, FB = 1.4V, V_{out} = 5V LBI = SHDN = 2V		11	15	µA
I_{sd}	Shut Down Current	V_{in} = 5V, I_l = 0 mA		0.1	1	µA
Irev	Reverse battery current	V_{in} = -4V		0.1	1	µA
Power section						
R_{on-N}	Active switch ON resistance			300		mΩ
R_{on-P}	Synchronous switch ON resistance			300		mΩ
Control section						
V_{out}	Output voltage	FB = OUT, I_l = 0 mA	3.2	3.3	3.4	V
		FB = GND, I_l = 0 mA	4.9	5	5.1	V
	Output voltage range	External divider	1.8		5.2	V
V_{LBI}	LBI threshold			1.23		V
V_{LBO}	LBO logic LOW	I_{sink} = 1mA		0.2	0.4	V
I_{lim}	LX switch current limit		0.7	0.8	0.9	A
T_{onmax}	Maximum on time	V_{out} = 3.3V	3.75	5	6.25	µs
T_{offmin}	Minimum off time	V_{out} = 3.3V	0.75	1	1.25	µs
$\overline{SHDN}$	$\overline{SHDN}$ logic LOW				0.2	V
	$\overline{SHDN}$ logic HIGH		0.6			V
V_{ref}	Reference Voltage		1.18	1.23	1.27	V

4 Typical performance

Figure 2. Efficiency vs output current @ V_{OUT} = 3.3V

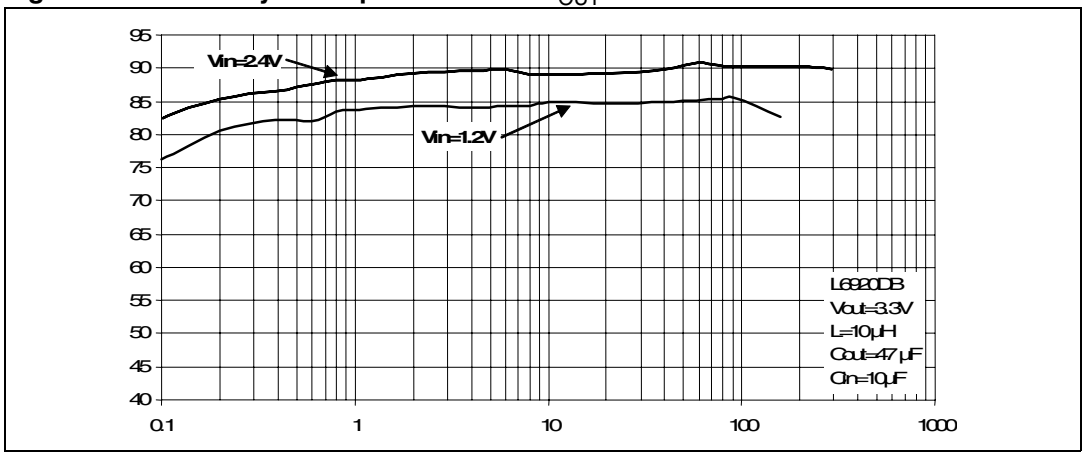


Figure 3. Efficiency vs output current @ V_{OUT} = 5V

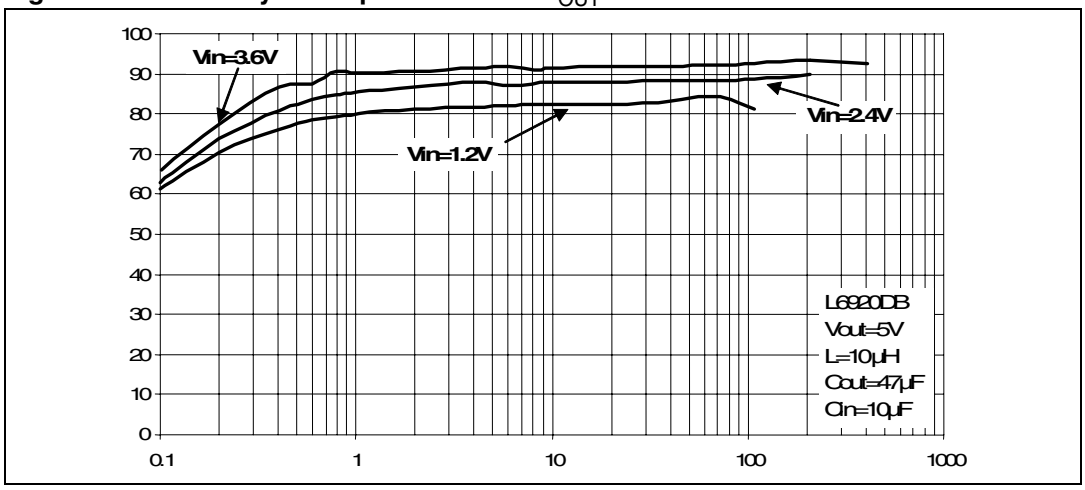
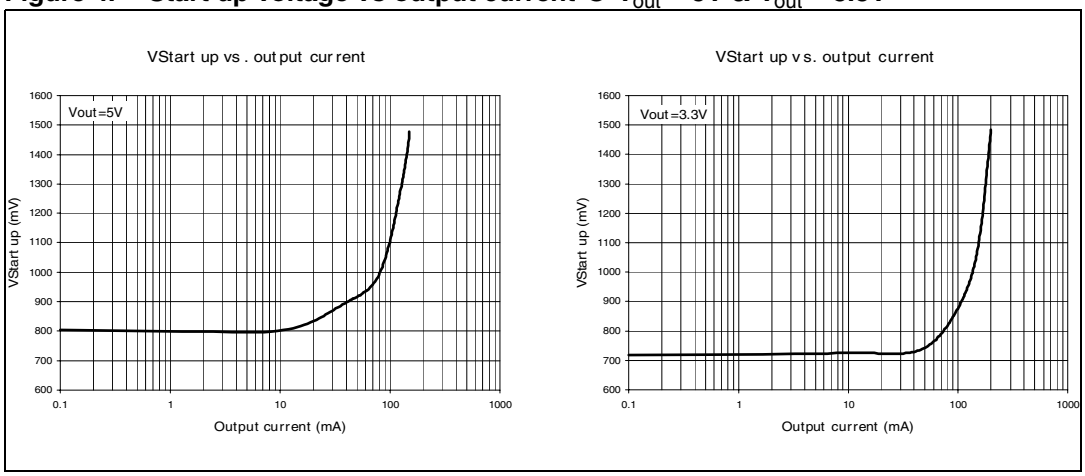


Figure 4. Start up voltage vs output current @ V_{out} = 5V & V_{out} = 3.3V



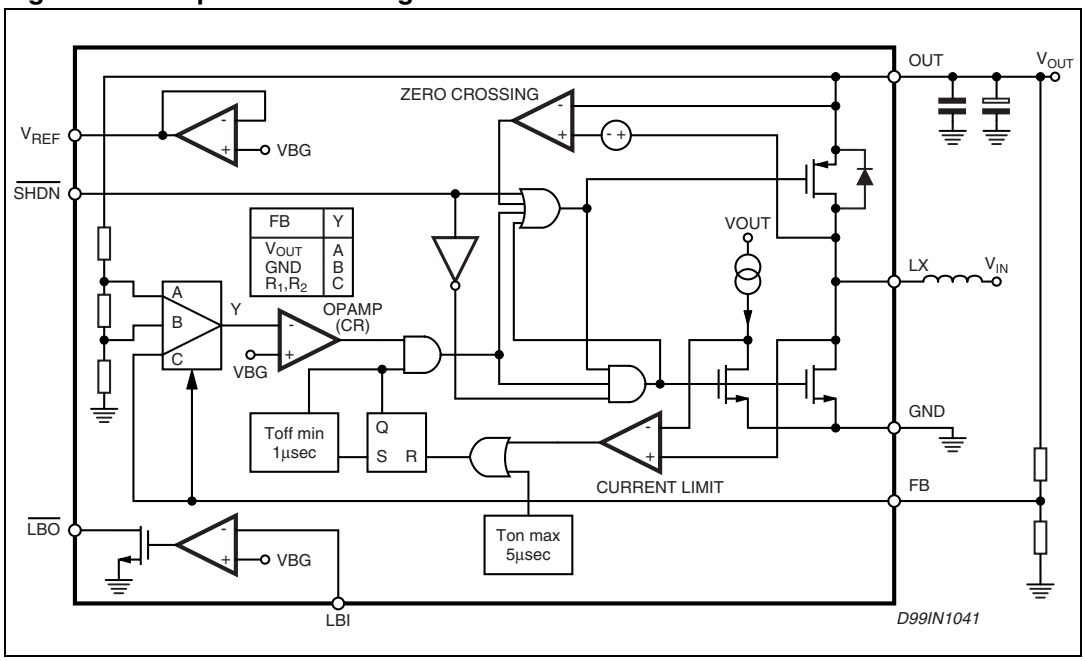
5 Detailed description

The L6920DB is a high efficiency, low voltage step-up DC/DC converter particularly suitable for 1 to 3 cells (Li-Ion/ polymer, NiMH respectively) battery up conversion.

These performances are achieved via a strong reduction of quiescent current (10µA only) and adopting a synchronous rectification that implies also a reduced cost in the application (no external diode required).

Operation is based on maximum ON time - minimum OFF time control, tailored by a current limit set to 800mA. A simplified block diagram is shown here below.

Figure 5. Simplified block diagram



5.1 Principle of operation

In L6920DB the control is based on a comparator that continuously checks the status of output voltage.

If the output voltage is lower than the expected value, the control function of the L6920DB directs the energy stored in the inductor to be transferred to the load. This is accomplished by alternating between two basic steps:

- T_{ON} phase: the energy is transferred from the battery to the inductor by shorting LX node to ground via the N-channel power switch. The switch is turned off if the current flowing in the inductor reaches 750mA or after a maximum on time set to 5µs.
- T_{OFF} phase: the energy stored in the inductor is transferred to the load through the synchronous switch for at least a minimum off time equal to 1µs. After this, the synchronous switch is turned off as soon as the output voltage goes lower than the regulated voltage or the current flowing in the inductor goes down to zero.

So, in case of light load, the device works in PFM mode, as shown in *Figure 8*:

Figure 6. PFM mode condition: V_{out} = 5V; V_{batt} =1.5V ; C2 = V_{out} ; C3 = Inductor Current

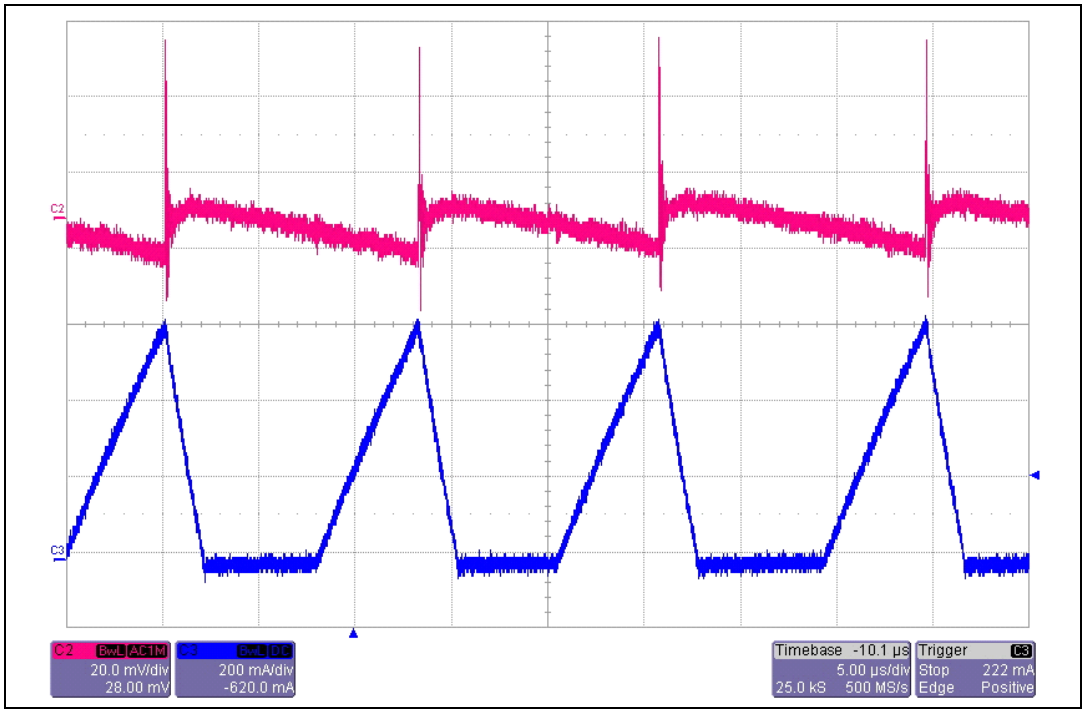
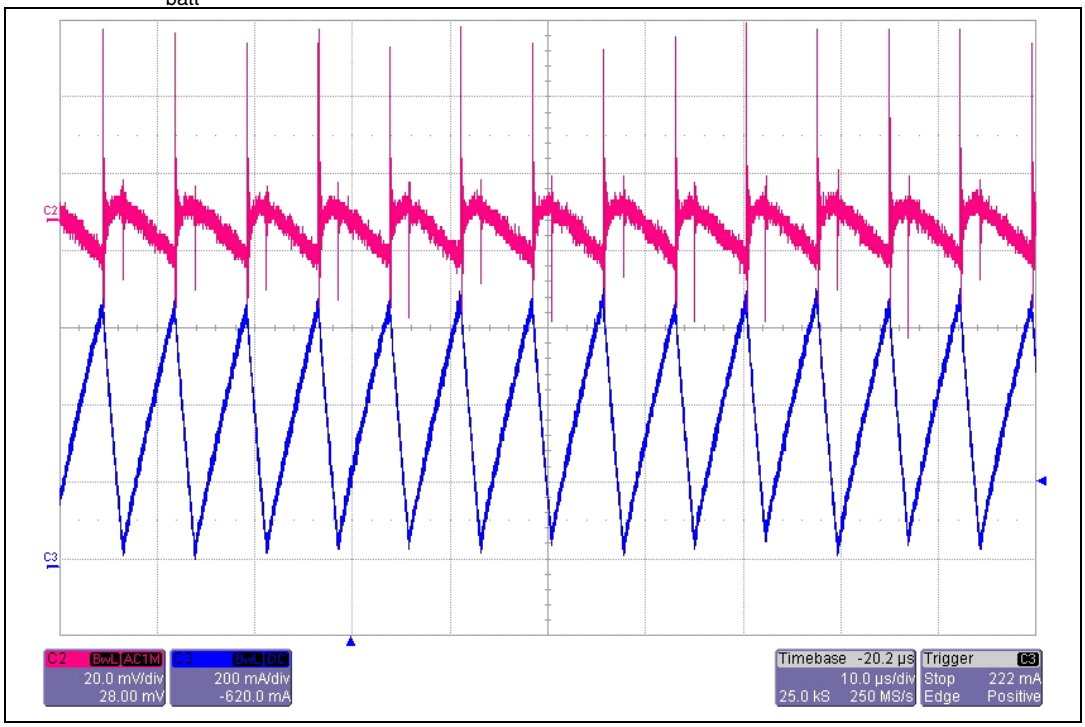


Figure 7 shows how the device works in case of heavy load.

Figure 7. Heavy load conditions C2 = V_{out}; C3 = Inductor Current; V_{out} = 5V; V_{batt}=1.5V



Considering that current in the inductor is limited to 800mA, the maximum load current is defined by the following relationship:

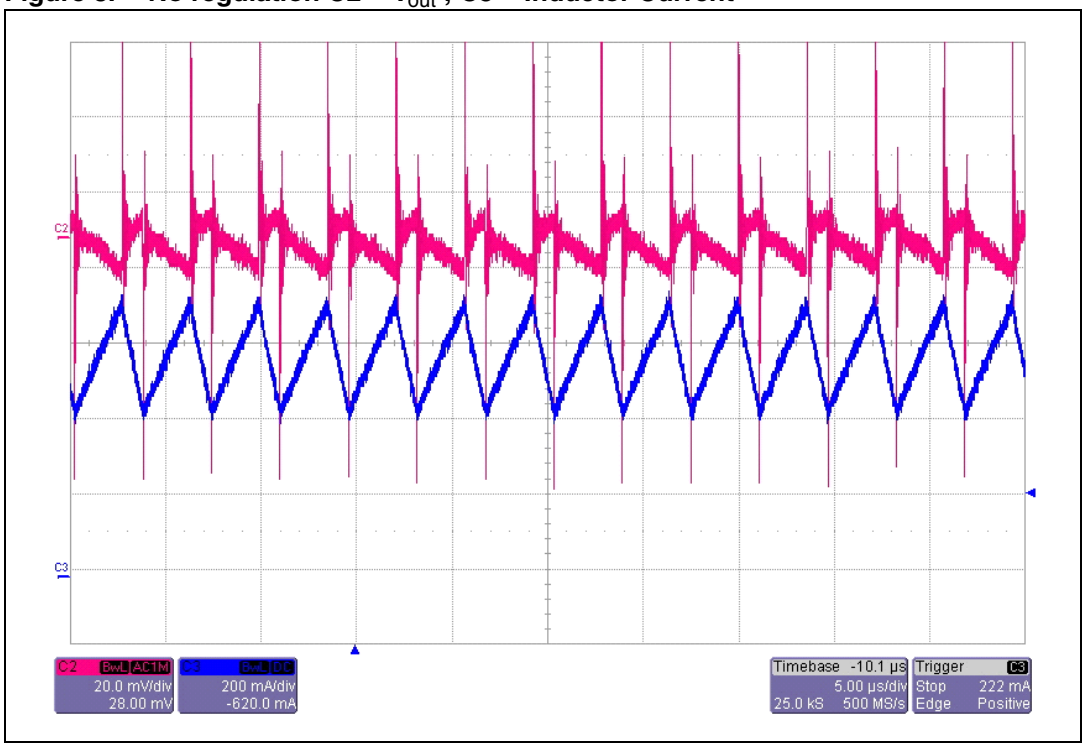
Equation 1

$$I_{LOAD_LIM} = \frac{V_{in}}{V_{out}} \cdot \left(I_{LIM} - T_{OFF_MIN} \cdot \frac{V_{out} - V_{in}}{2 \cdot L} \right) \cdot \eta$$

Where η is the efficiency and I_{LIM} = 750mA

Of course, if I_{LOAD} is greater than I_{LOAD_LIM} the regulation is lost (*Figure 8*).

Figure 8. No regulation C2 = V_{out} ; C3 = Inductor Current



5.2 Start-up

One of the key features of L6920DB is the startup at supply voltage down to 0.8V (please see the diagram in *Figure 4*).

The device leaves the startup mode of operation as soon as Vout goes over 1.4V. During startup, the synchronous switch is off and the energy is transferred to the load through its intrinsic body diode.

The N-channel switches with a very low $R_{DS(on)}$ thanks to an internal charge pump used to bias the power MOS gate. Because of this modified behavior, T_{ON}/T_{OFF} times are lengthened. Current limit and zero crossing detection are still available.

5.3 Shutdown

In shutdown mode ($\overline{SHDN}$ pulled low) all internal circuitries are turned off, minimizing the current provided by the battery (I_{SHDN} < 100 nA, in typical case).

Both switches are turned off, and the low battery comparator output is forced in high impedance state.

The synchronous switch body diode causes a parasitic path between power supply and output that can't be avoided also in shutdown.

5.4 Low battery detection

The L6920DB includes a low battery detector comparator.

Threshold is V_{REF} voltage and a hysteresis is added to avoid oscillations when input crosses the threshold slowly. The $\overline{LBO}$ is an open drain output so a pull up resistor is required for a proper use.

5.5 Low battery input

It is possible to fix, using an external resistor divider, the $\overline{LBO}$ threshold, in order to adapt the $\overline{LBO}$ detection at the correct input source, by the following equation:

Equation 2

$$V_{batt\text{-}th} = 1.23V \cdot \left(1 + \frac{R1}{R2}\right)$$

Where $V_{batt\text{-}th}$ is the battery voltage at which the internal comparetor is triggered.

5.6 Reverse polarity

A protection circuit has been implemented to avoid that L6920DB and the battery are destroyed in case of wrong battery insertion.

In addition, this circuit has been designed so that the current required by the battery is zero also in reverse polarity.

If a battery can be inserted in reverse direction, a non polarized capacitor should be installed in location of C2.

5.7 Output voltage selection

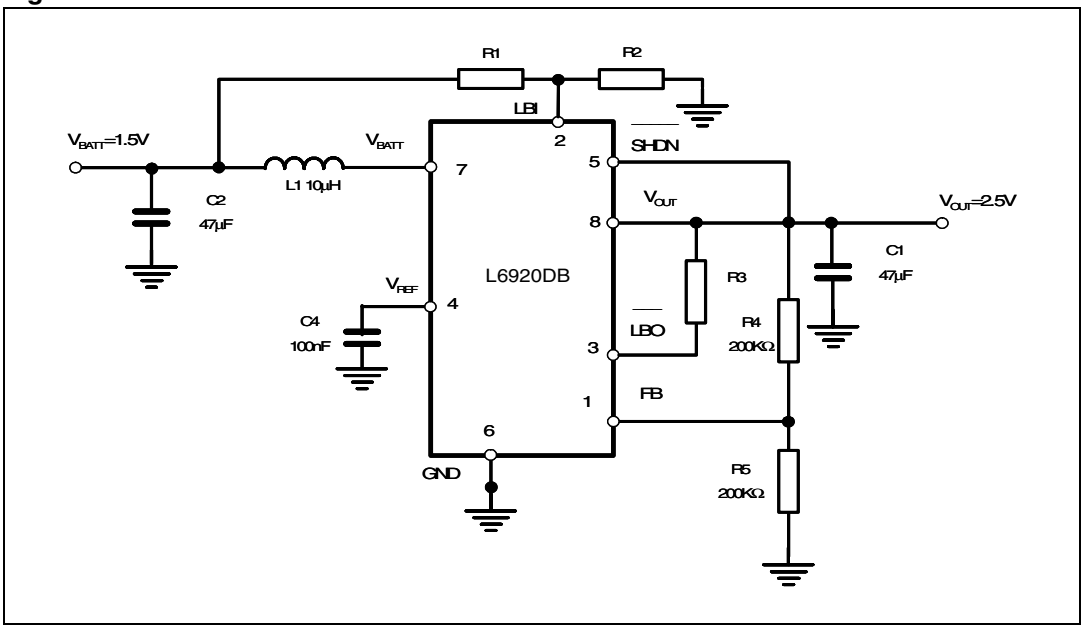
Output voltage must be selected acting on FB pin.

Three choices are available: fixed 3.3V, 5V or adjustable output set via an external resistor divider.

Table 5. Output voltage connection

V_{out} = 3.3V	FB pin connected to OUT (see application circuit)
V_{out} = 5V	FB pin connected to GND
1.8V < V_{out} < 5.5V	FB pin connected to a resistive divider $V_{out} = 1.23V \cdot \left(1 + \frac{R4}{R5}\right)$

Figure 9. Test circuit



6 Package mechanical data

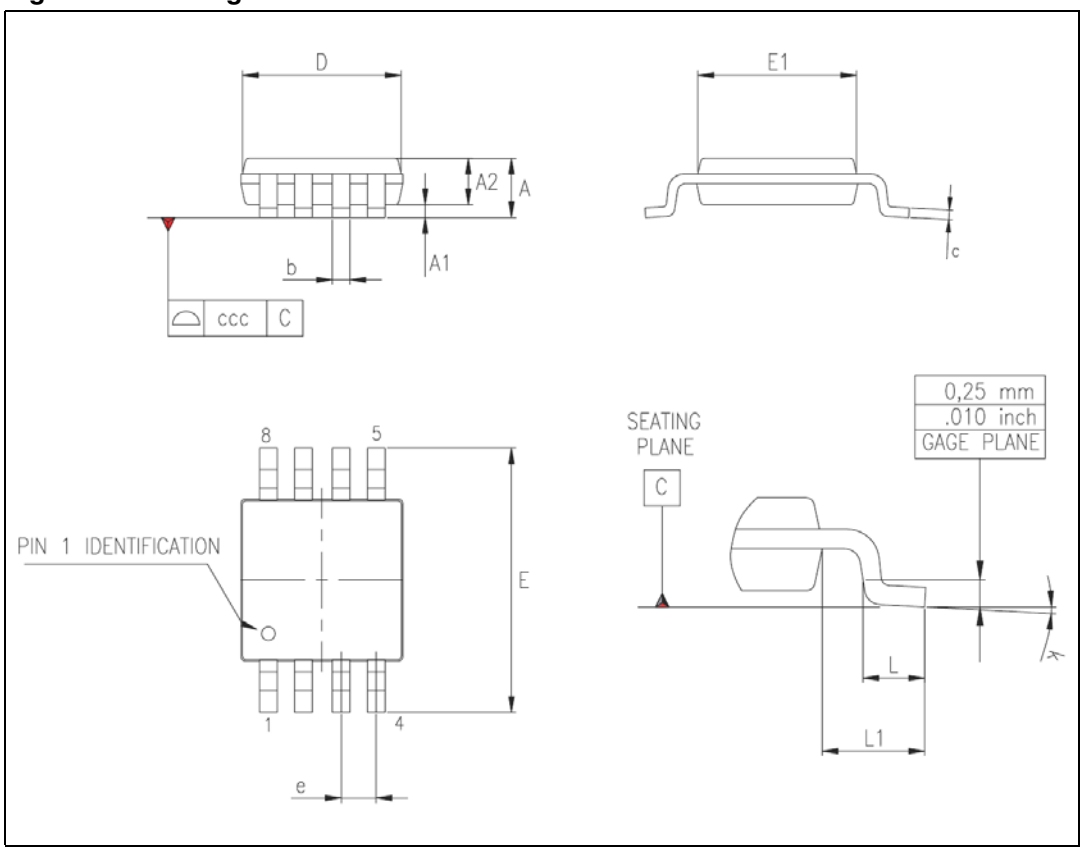
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Table 6. MSOP8 Mechanical data

Dim.	mm.			inch		
	Min	Typ	Max	Min	Typ	Max
A			1.10			0.043
A1	0.050		0.150	0.002		0.006
A2	0.750	0.850	0.950	0.03	0.033	0.037
b	0.250		0.400	0.010		0.016
c	0.130		0.230	0.005		0.009
D (1)	2.900	3.000	3.100	0.114	0.118	0.122
E	4.650	4.900	5.150	0.183	0.193	0.20
E1 (1)	2.900	3.000	3.100	0.114	0.118	0.122
e		0.650			0.026	
L	0.400	0.550	0.700	0.016	0.022	0.028
L1		0.950			0.037	
k	0° (min.) 6° (max.)					
aaa			0.100			0.004

1. D and F does not include mold flash or protrusions. Mold flash or potrusions shall not exceed 0.15mm (.006inch) per side.

Figure 10. Package dimensions



7 Order code

Table 7. Order code

Part number	Package	Packaging
L6920DB	MSOP8	Tube
L6920DBTR	MSOP8	Tape and reel

8 Revision history

Table 8. Revision history

Date	Revision	Changes
18-Mar-2005	1	First issue
03-Aug-2005	2	Changed from “Preliminary Data” to “Datasheet”. Modified Section 1 and Table 5. Added Figg. 3, 6 and new Section 3.
01-Jun-2006	3	New template, modified application circuit and *Figure 9.*
13-Oct-2006	4	Cover page description updated.
30-Oct-2006	5	Typo in *Figure 7 on page 8*

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