

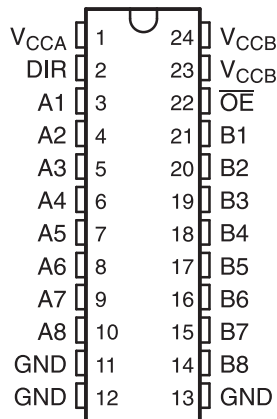
## 8-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

Check for Samples: [SN74LVC8T245-Q1](#)

### FEATURES

- **Qualified for Automotive Applications**
- **Control Inputs  $V_{IH}/V_{IL}$  Levels Are Referenced to  $V_{CCA}$  Voltage**
- **$V_{CC}$  Isolation Feature – If Either  $V_{CC}$  Input Is at GND, All Are in the High-Impedance State**
- **Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.65-V to 5.5-V Power-Supply Range**

**PW PACKAGE  
(TOP VIEW)**



### DESCRIPTION

This 8-bit non-inverting bus transceiver uses two separate configurable power-supply rails. The SN74LVC8T245-Q1 is optimized to operate with  $V_{CCA}$  and  $V_{CCB}$  set at 1.65 V to 5.5 V. The A port is designed to track  $V_{CCA}$ .  $V_{CCA}$  accepts any supply voltage from 1.65 V to 5.5 V. The B port is designed to track  $V_{CCB}$ .  $V_{CCB}$  accepts any supply voltage from 1.65 V to 5.5 V. This allows for universal low-voltage bidirectional translation between any of the 1.8-V, 2.5-V, 3.3-V, and 5.5-V voltage nodes.

The SN74LVC8T245-Q1 is designed for asynchronous communication between two data buses. The logic levels of the direction-control (DIR) input and the output-enable ( $\overline{OE}$ ) input activate either the B-port outputs or the A-port outputs or place both output ports into the high-impedance mode. The device transmits data from the A bus to the B bus when the B-port outputs are activated, and from the B bus to the A bus when the A-port outputs are activated. The input circuitry on both A and B ports is always active and must have a logic HIGH or LOW level applied to prevent excess  $I_{CC}$  and  $I_{CCZ}$ .

The SN74LVC8T245-Q1 is designed so that the control pins (DIR and  $\overline{OE}$ ) are supplied by  $V_{CCA}$ .

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The  $V_{CC}$  isolation feature ensures that if either  $V_{CC}$  input is at GND, all outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

### ORDERING INFORMATION<sup>(1)</sup>

$T_A$	PACKAGE <sup>(2)</sup>	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	TSSOP – PW Reel of 2000	SN74LVC8T245QPWRQ1	NH245Q

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).
- (2) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).



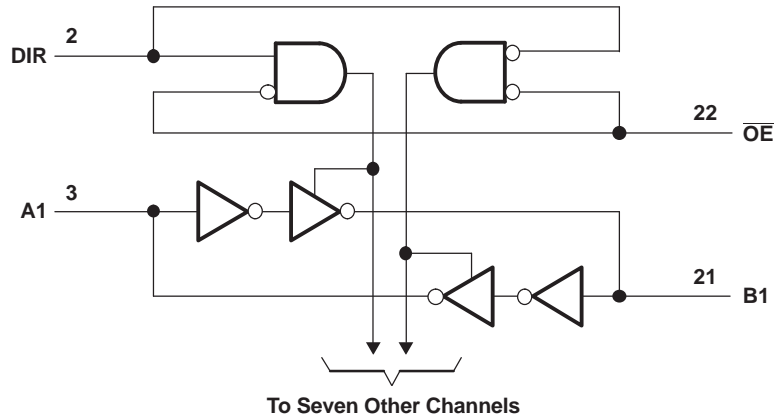
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

**FUNCTION TABLE<sup>(1)</sup>  
(EACH 8-BIT SECTION)**

CONTROL INPUTS		OUTPUT CIRCUITS		OPERATION
$\overline{OE}$	DIR	A PORT	B PORT	
L	L	Enabled	Hi-Z	B data to A bus
L	H	Hi-Z	Enabled	A data to B bus
H	X	Hi-Z	Hi-Z	Isolation

(1) Input circuits of the data I/Os are always active.

**LOGIC DIAGRAM (POSITIVE LOGIC)**



**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT	
$V_{CCA}$ $V_{CCB}$	Supply voltage range	-0.5	6.5	V	
$V_I$	Input voltage range <sup>(2)</sup>	I/O ports (A port)	-0.5	6.5	V
		I/O ports (B port)	-0.5	6.5	
		Control inputs	-0.5	6.5	
$V_O$	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>	A port	-0.5	6.5	V
		B port	-0.5	6.5	
$V_O$	Voltage range applied to any output in the high or low state <sup>(2) (3)</sup>	A port	-0.5	$V_{CCA} + 0.5$	V
		B port	-0.5	$V_{CCB} + 0.5$	
$I_{IK}$	Input clamp current		-50	mA	
$I_{OK}$	Output clamp current		-50	mA	
$I_O$	Continuous output current		±50	mA	
	Continuous current through each $V_{CCA}$ , $V_{CCB}$ , and GND		±100	mA	
$\theta_{JA}$	Package thermal impedance <sup>(4)</sup>		88	°C/W	
$T_{stg}$	Storage temperature range	-65	150	°C	

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The output positive-voltage rating may be exceeded up to 6.5 V maximum if the output current rating is observed.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

**RECOMMENDED OPERATING CONDITIONS** (1) (2) (3) (4)

			$V_{CCI}$	$V_{CCO}$	MIN	MAX	UNIT
$V_{CCA}$	Supply voltage				1.65	5.5	V
$V_{CCB}$					1.65	5.5	
$V_{IH}$	High-level input voltage	Data inputs <sup>(5)</sup>	1.65 V to 1.95 V		$V_{CCI} \times 0.65$		V
			2.3 V to 2.7 V		1.7		
			3 V to 3.6 V		2		
			4.5 V to 5.5 V		$V_{CCI} \times 0.7$		
$V_{IL}$	Low-level input voltage	Data inputs <sup>(5)</sup>	1.65 V to 1.95 V		$V_{CCI} \times 0.35$		V
			2.3 V to 2.7 V		0.7		
			3 V to 3.6 V		0.8		
			4.5 V to 5.5 V		$V_{CCI} \times 0.3$		
$V_{IH}$	High-level input voltage	Control inputs (referenced to $V_{CCA}$ ) <sup>(6)</sup>	1.65 V to 1.95 V		$V_{CCA} \times 0.65$		V
			2.3 V to 2.7 V		1.7		
			3 V to 3.6 V		2		
			4.5 V to 5.5 V		$V_{CCA} \times 0.7$		
$V_{IL}$	Low-level input voltage	Control inputs (referenced to $V_{CCA}$ ) <sup>(6)</sup>	1.65 V to 1.95 V		$V_{CCA} \times 0.35$		V
			2.3 V to 2.7 V		0.7		
			3 V to 3.6 V		0.8		
			4.5 V to 5.5 V		$V_{CCA} \times 0.3$		
$V_I$	Input voltage	Control inputs			0	5.5	V
$V_{IO}$	Input/output voltage	Active state			0	$V_{CCO}$	V
		3-State			0	5.5	V
$I_{OH}$	High-level output current		1.65 V to 1.95 V		-4		mA
			2.3 V to 2.7 V		-8		
			3 V to 3.6 V		-24		
			4.5 V to 5.5 V		-32		
$I_{OL}$	Low-level output current		1.65 V to 1.95 V		4		mA
			2.3 V to 2.7 V		8		
			3 V to 3.6 V		24		
			4.5 V to 5.5 V		32		
$\Delta t/\Delta v$	Input transition rise or fall rate	Data inputs	1.65 V to 1.95 V		20		ns/V
			2.3 V to 2.7 V		20		
			3 V to 3.6 V		10		
			4.5 V to 5.5 V		5		
$T_A$	Operating free-air temperature				-40	125	°C

(1)  $V_{CCI}$  is the  $V_{CC}$  associated with the data input port.

(2)  $V_{CCO}$  is the  $V_{CC}$  associated with the output port.

(3) All unused or driven (floating) data inputs (I/Os) of the device must be held at logic HIGH or LOW (preferably  $V_{CCI}$  or GND) to ensure proper device operation and minimize power. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

(4) All unused control inputs must be held at  $V_{CCA}$  or GND to ensure proper device operation and minimize power consumption.

(5) For  $V_{CCI}$  values not specified in the data sheet,  $V_{IH}$  min =  $V_{CCI} \times 0.7$  V,  $V_{IL}$  max =  $V_{CCI} \times 0.3$  V.

(6) For  $V_{CCA}$  values not specified in the data sheet,  $V_{IH}$  min =  $V_{CCA} \times 0.7$  V,  $V_{IL}$  max =  $V_{CCA} \times 0.3$  V.

**ELECTRICAL CHARACTERISTICS**<sup>(1) (2) (3)</sup>

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CCA</sub>	V <sub>CCB</sub>	T <sub>A</sub> = 25°C			T <sub>A</sub> = -40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -100 μA, V <sub>I</sub> = V <sub>IH</sub>	1.65 V to 4.5 V	1.65 V to 4.5 V				V <sub>CCO</sub> - 0.1		V
	I <sub>OH</sub> = -4 mA, V <sub>I</sub> = V <sub>IH</sub>	1.65 V	1.65 V				1.2		
	I <sub>OH</sub> = -8 mA, V <sub>I</sub> = V <sub>IH</sub>	2.3 V	2.3 V				1.9		
	I <sub>OH</sub> = -24 mA, V <sub>I</sub> = V <sub>IH</sub>	3 V	3 V				2.4		
	I <sub>OH</sub> = -32 mA, V <sub>I</sub> = V <sub>IH</sub>	4.5 V	4.5 V				3.8		
V <sub>OL</sub>	I <sub>OL</sub> = 100 μA, V <sub>I</sub> = V <sub>IL</sub>	1.65 V to 4.5 V	1.65 V to 4.5 V				0.1		V
	I <sub>OL</sub> = 4 mA, V <sub>I</sub> = V <sub>IL</sub>	1.65 V	1.65 V				0.45		
	I <sub>OL</sub> = 8 mA, V <sub>I</sub> = V <sub>IL</sub>	2.3 V	2.3 V				0.3		
	I <sub>OL</sub> = 24 mA, V <sub>I</sub> = V <sub>IL</sub>	3 V	3 V				0.55		
	I <sub>OL</sub> = 32 mA, V <sub>I</sub> = V <sub>IL</sub>	4.5 V	4.5 V				0.55		
I <sub>I</sub>	DIR	V <sub>I</sub> = V <sub>CCA</sub> or GND	1.65 V to 5.5 V	1.65 V to 5.5 V			±1	±2	μA
I <sub>off</sub>	A or B port	V <sub>I</sub> or V <sub>O</sub> = 0 to 5.5 V	0 V	0 to 5.5 V			±2	±11	μA
			0 to 5.5 V	0 V			±2	±11	
I <sub>OZ</sub>	A or B port	V <sub>O</sub> = V <sub>CCO</sub> or GND, OE = V <sub>IH</sub>	1.65 V to 5.5 V	1.65 V to 5.5 V			±1	±6	μA
I <sub>CCA</sub>	V <sub>I</sub> = V <sub>CCI</sub> or GND, I <sub>O</sub> = 0	1.65 V to 5.5 V	1.65 V to 5.5 V				20		μA
		5 V	0 V				20		
		0 V	5 V				-10		
I <sub>CCB</sub>	V <sub>I</sub> = V <sub>CCI</sub> or GND, I <sub>O</sub> = 0	1.65 V to 5.5 V	1.65 V to 5.5 V				20		μA
		5 V	0 V				-10		
		0 V	5 V				20		
I <sub>CCA</sub> + I <sub>CCB</sub>	V <sub>I</sub> = V <sub>CCI</sub> or GND, I <sub>O</sub> = 0	1.65 V to 5.5 V	1.65 V to 5.5 V				40		μA
ΔI <sub>CCA</sub>	A port	One A port at V <sub>CCA</sub> - 0.6 V, DIR at V <sub>CCA</sub> , B port = open	3 V to 5.5 V	3 V to 5.5 V			50		μA
	DIR	DIR at V <sub>CCA</sub> - 0.6 V, B port = open, A port at V <sub>CCA</sub> or GND					50		
ΔI <sub>CCB</sub>	B port	One B port at V <sub>CCB</sub> - 0.6 V, DIR at GND, A port = open	3 V to 5.5 V	3 V to 5.5 V			50		μA
C <sub>i</sub>	Control inputs	V <sub>I</sub> = V <sub>CCA</sub> or GND	3.3 V	3.3 V		4		5	pF
C <sub>io</sub>	A or B port	V <sub>O</sub> = V <sub>CCA/B</sub> or GND	3.3 V	3.3 V		8.5		10	pF

(1) V<sub>CCO</sub> is the V<sub>CC</sub> associated with the output port.(2) V<sub>CCI</sub> is the V<sub>CC</sub> associated with the input port.(3) All unused control inputs must be held at V<sub>CCA</sub> or GND to ensure proper device operation and minimize power consumption.

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range,  $V_{CCA} = 1.8\text{ V} \pm 0.15\text{ V}$  (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$		$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A	B	1.7	25.9	1.3	13.2	1	11.4	0.8	11.1	ns
$t_{PHL}$											
$t_{PLH}$	B	A	0.9	28.8	0.8	27.6	0.7	27.4	0.7	27.4	ns
$t_{PHL}$											
$t_{PHZ}$	$\overline{OE}$	A	1.5	33.6	1.5	33.4	1.5	33.3	1.4	33.2	ns
$t_{PLZ}$											
$t_{PHZ}$	$\overline{OE}$	B	2.4	36.2	1.9	17.1	1.7	16	1.3	14.3	ns
$t_{PLZ}$											
$t_{PZH}$	$\overline{OE}$	A	0.4	28	0.4	27.8	0.4	27.7	0.4	27.7	ns
$t_{PZL}$											
$t_{PZH}$	$\overline{OE}$	B	1.8	40	1.5	20	1.2	16.6	0.9	14.8	ns
$t_{PZL}$											

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range,  $V_{CCA} = 2.5\text{ V} \pm 0.2\text{ V}$  (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$		$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A	B	1.5	25.4	1.2	13	0.8	10.2	0.6	8.8	ns
$t_{PHL}$											
$t_{PLH}$	B	A	1.2	13.3	1	13.1	1	12.9	0.9	12.8	ns
$t_{PHL}$											
$t_{PHZ}$	$\overline{OE}$	A	1.4	13	1.4	13	1.4	13	1.4	13	ns
$t_{PLZ}$											
$t_{PHZ}$	$\overline{OE}$	B	2.3	33.6	1.8	15	1.7	14.3	0.9	10.9	ns
$t_{PLZ}$											
$t_{PZH}$	$\overline{OE}$	A	1	17.2	1	17.3	1	17.2	1	17.3	ns
$t_{PZL}$											
$t_{PZH}$	$\overline{OE}$	B	1.7	32.2	1.5	18.1	1.2	14.1	1	11.2	ns
$t_{PZL}$											

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range,  $V_{CCA} = 3.3 \text{ V} \pm 0.3 \text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$		$V_{CCB} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		$V_{CCB} = 5 \text{ V} \pm 0.5 \text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A	B	1.5	25.2	1.1	12.8	0.8	10.3	0.5	10.4	ns
$t_{PHL}$											
$t_{PLH}$	B	A	0.8	11.2	0.8	10.2	0.7	10.1	0.6	10	ns
$t_{PHL}$											
$t_{PHZ}$	$\overline{OE}$	A	1.6	12.2	1.6	12.2	1.6	12.2	1.6	12.2	ns
$t_{PLZ}$											
$t_{PHZ}$	$\overline{OE}$	B	2.1	33	1.7	14.3	1.5	12.6	0.8	10.3	ns
$t_{PLZ}$											
$t_{PZH}$	$\overline{OE}$	A	0.8	14.1	0.8	13.6	0.8	13.2	0.8	13.6	ns
$t_{PZL}$											
$t_{PZH}$	$\overline{OE}$	B	1.8	31.7	1.4	18.4	1.1	12.9	0.9	10.9	ns
$t_{PZL}$											

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range,  $V_{CCA} = 5 \text{ V} \pm 0.5 \text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$		$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A	B	1.5	25.4	1	12.8	0.7	10	0.4	8.2	ns
$t_{PHL}$											
$t_{PLH}$	B	A	0.7	11	0.4	8.8	0.3	8.5	0.3	8.3	ns
$t_{PHL}$											
$t_{PHZ}$	$\overline{OE}$	A	0.3	9.4	0.3	9.4	0.3	9.4	0.3	9.4	ns
$t_{PLZ}$											
$t_{PHZ}$	$\overline{OE}$	B	2	32.7	1.6	13.7	1.4	12	0.7	9.7	ns
$t_{PLZ}$											
$t_{PZH}$	$\overline{OE}$	A	0.7	10.9	0.7	10.9	0.7	10.9	0.7	10.9	ns
$t_{PZL}$											
$t_{PZH}$	$\overline{OE}$	B	1.5	31.6	1.3	18.4	1	13.7	0.9	10.7	ns
$t_{PZL}$											

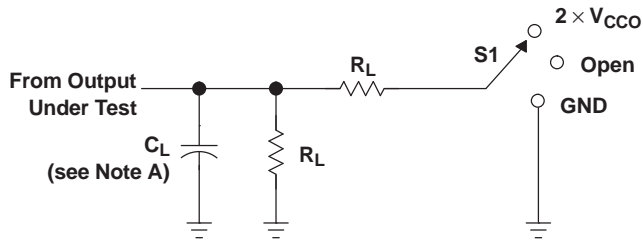
## OPERATING CHARACTERISTICS

$T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	$V_{CCA} =$ $V_{CCB} = 1.8 \text{ V}$	$V_{CCA} =$ $V_{CCB} = 2.5 \text{ V}$	$V_{CCA} =$ $V_{CCB} = 3.3 \text{ V}$	$V_{CCA} =$ $V_{CCB} = 5 \text{ V}$	UNIT
			TYP	TYP	TYP	TYP	
$C_{pdA}$ (1)	A-port input, B-port output	$C_L = 0,$ $f = 10 \text{ MHz},$ $t_r = t_f = 1 \text{ ns}$	2	2	2	3	pF
	B-port input, A-port output		12	13	13	16	
$C_{pdB}$ (1)	A-port input, B-port output		13	13	14	16	
	B-port input, A-port output		2	2	2	3	

(1) Power dissipation capacitance per transceiver

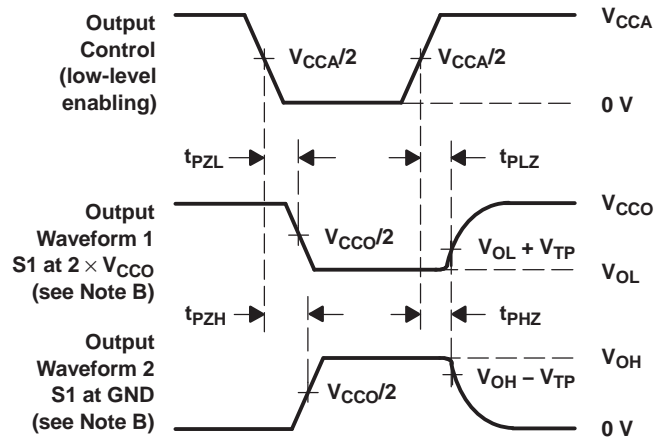
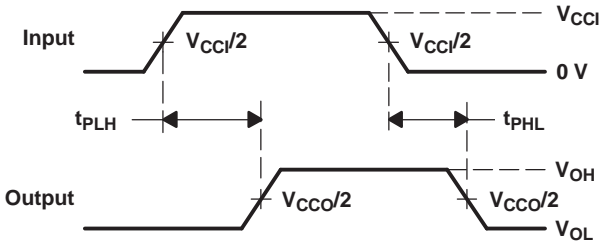
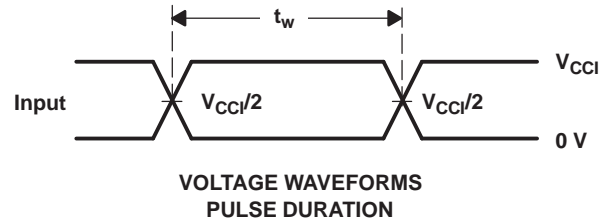
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CCO}$
$t_{PHZ}/t_{PZH}$	GND

$V_{CCO}$	$C_L$	$R_L$	$V_{TP}$
$1.8\text{ V} \pm 0.15\text{ V}$	15 pF	2 k $\Omega$	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	15 pF	2 k $\Omega$	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	15 pF	2 k $\Omega$	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	15 pF	2 k $\Omega$	0.3 V



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50\ \Omega$ ,  $dv/dt \geq 1\text{ V/ns}$ .  
 D. The outputs are measured one at a time, with one transition per measurement.  
 E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
 G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .  
 H.  $V_{CCI}$  is the  $V_{CC}$  associated with the input port.  
 I.  $V_{CCO}$  is the  $V_{CC}$  associated with the output port.  
 J. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC8T245QPWRQ1	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	NH245Q	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN74LVC8T245-Q1 :**



- Catalog: [SN74LVC8T245](#)
- Enhanced Product: [SN74LVC8T245-EP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC8T245QPWRQ1	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC8T245QPWRQ1	TSSOP	PW	24	2000	367.0	367.0	38.0

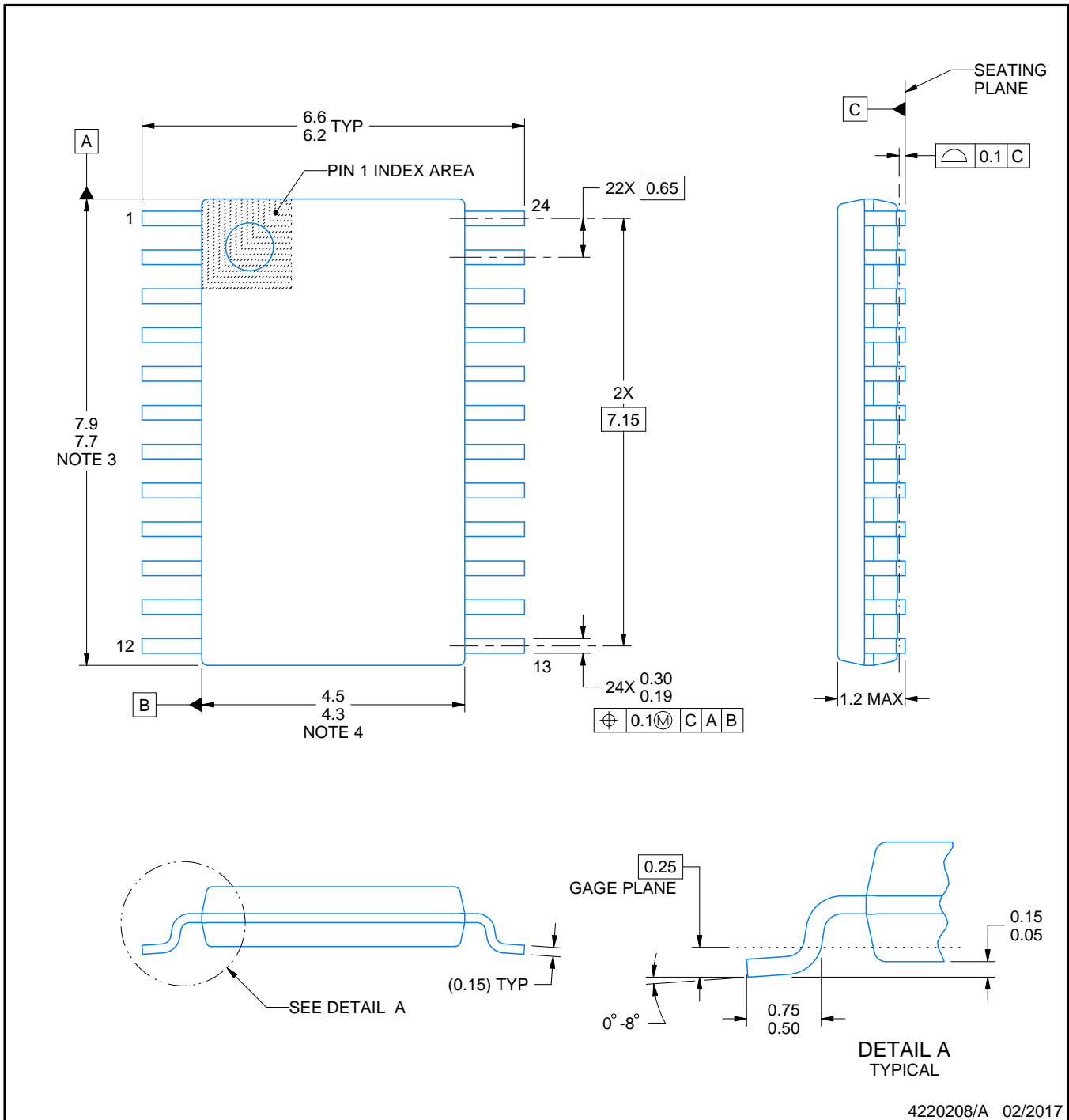
# PW0024A



# PACKAGE OUTLINE

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220208/A 02/2017

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## IMPORTANT NOTICE AND DISCLAIMER

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