DEMO CIRCUIT 1569A
QUICK START GUIDE

LT3958
High Voltage Monolithic Boost Converter

DESCRIPTION

Demonstration circuit 1569A is a High Voltage Monolithic Boost Converter featuring the LT3958. The LT3958 can be configured as a boost, flyback, SEPIC, and inverting converter, but the demonstration circuit is assembled as a boost. The input voltage range is 11V to 40V and the output voltage is 48V with 500mA over the entire input voltage range.

The LT3958 has an internal n-channel 3.3A, 84V power switch for high voltage, power, and efficiency. The dual paddle package provides excellent heat dissipation for the internal power switch. The LT3958 current-mode dc/dc converter features adjustable switching frequency, soft-start, compensation, shutdown and undervoltage lockout with hysteresis, and a feedback pin (FBX) that can be used in both positive and negative applications. A SYNC input can be used to synchronize the switching at a frequency higher than the IC is programmed.

For flyback converters, SENSE1 and SENSE2 pins are available to filter the internal flyback current sense signal.

The demonstration circuit features small 1210 case size ceramic input and output capacitors. The internal n-channel power switch provides efficiency as high as 94% in typical boost applications with 24W output.

The LT3958 datasheet gives a complete description of the part, operation and applications information. The datasheet must be read in conjunction with this Quick Start Guide for demonstration circuit 1569A. The LT3958 is assembled in a 36-lead plastic UHE package with two thermally enhanced pads for SW and GND. Proper board layout is essential for both proper operation and maximum thermal performance. See the datasheet section 'Layout Considerations'.

Design files for this circuit board are available. Call the LTC factory.

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PERFORMANCE SUMMARY **Specifications are at TA = 25°C**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply Range		11		40	V
Output Voltage Programmed	V_{IN} = 11V-40V, $I_{LOAD} \leq$ 500mA		48		V
Switching Frequency	R_T = 41.2k		300		kHz
Maximum Output current	V_{IN} = 11V-40V		500		mA
Input Undervoltage Lockout (falling)	R1=392k, R2=53.6k		10.3		V
Input Turn-on Voltage (rising)	R1=392k, R2=53.6k		10.9		v
Efficiency	V_{IN} = 12V, I_{LOAD} = 500mA		94.6		%

QUICK START PROCEDURE

Demonstration circuit 1569A is easy to set up to evaluate the performance of the LT3958. Refer to Figure 1 for proper measurement equipment setup and follow the procedure below:

NOTE. When measuring the input or output voltage ripple, care must be taken to avoid a long ground lead on the oscilloscope probe. Measure the input or output voltage ripple by touching the probe tip directly across the Vin or Vout and GND terminals.

1. Place jumpers in the following positions:

   JP1 NO SYNC

2. With power off, connect the input power supply to VIN and GND.

   NOTE. Connect power to GND, not SGND.

3. Connect a load of 500mA or less to VOUT and GND terminals (not SGND).

4. Turn on the power at the input.

   NOTE. Make sure that the input voltage does not exceed 40V.

5. Check for the proper output voltage (48V).

   NOTE. If there is no output, temporarily disconnect the load to make sure that the load is not set too high.

6. Once the proper output voltage is established, adjust the load and input within the operating ranges and observe the output voltage regulation, ripple voltage, efficiency and other parameters.

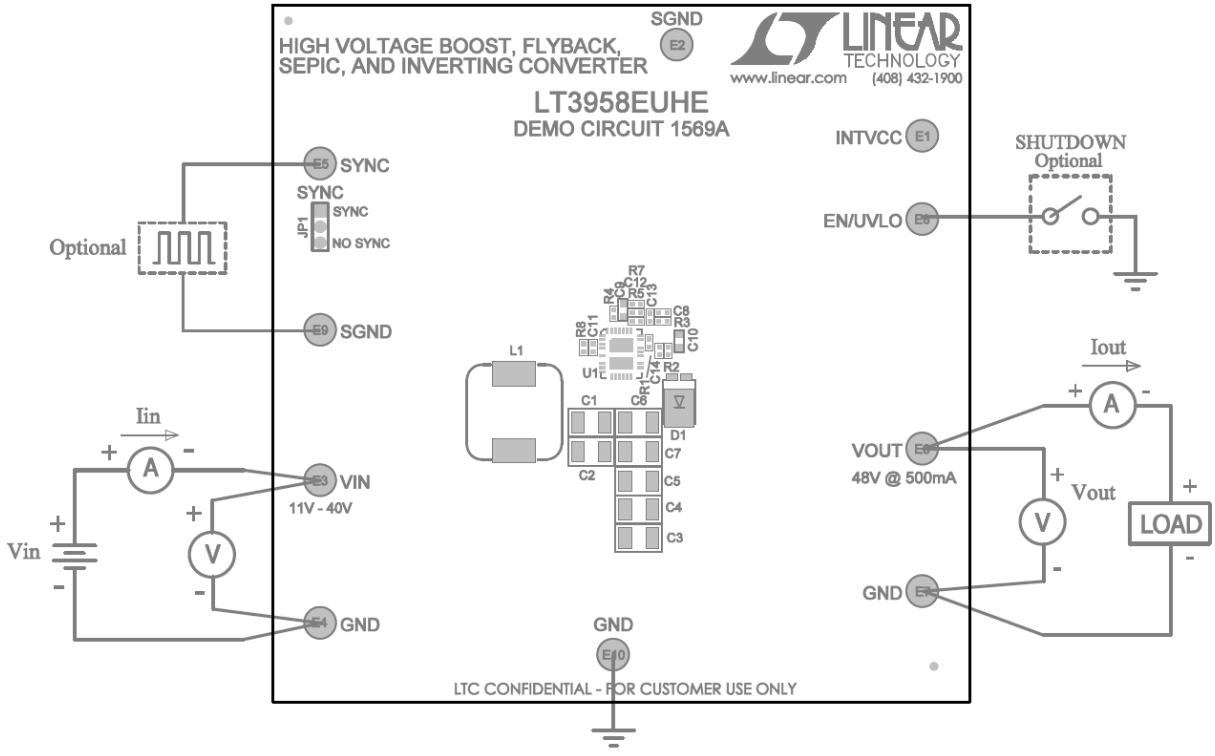


Figure 1. Proper Measurement Equipment Setup

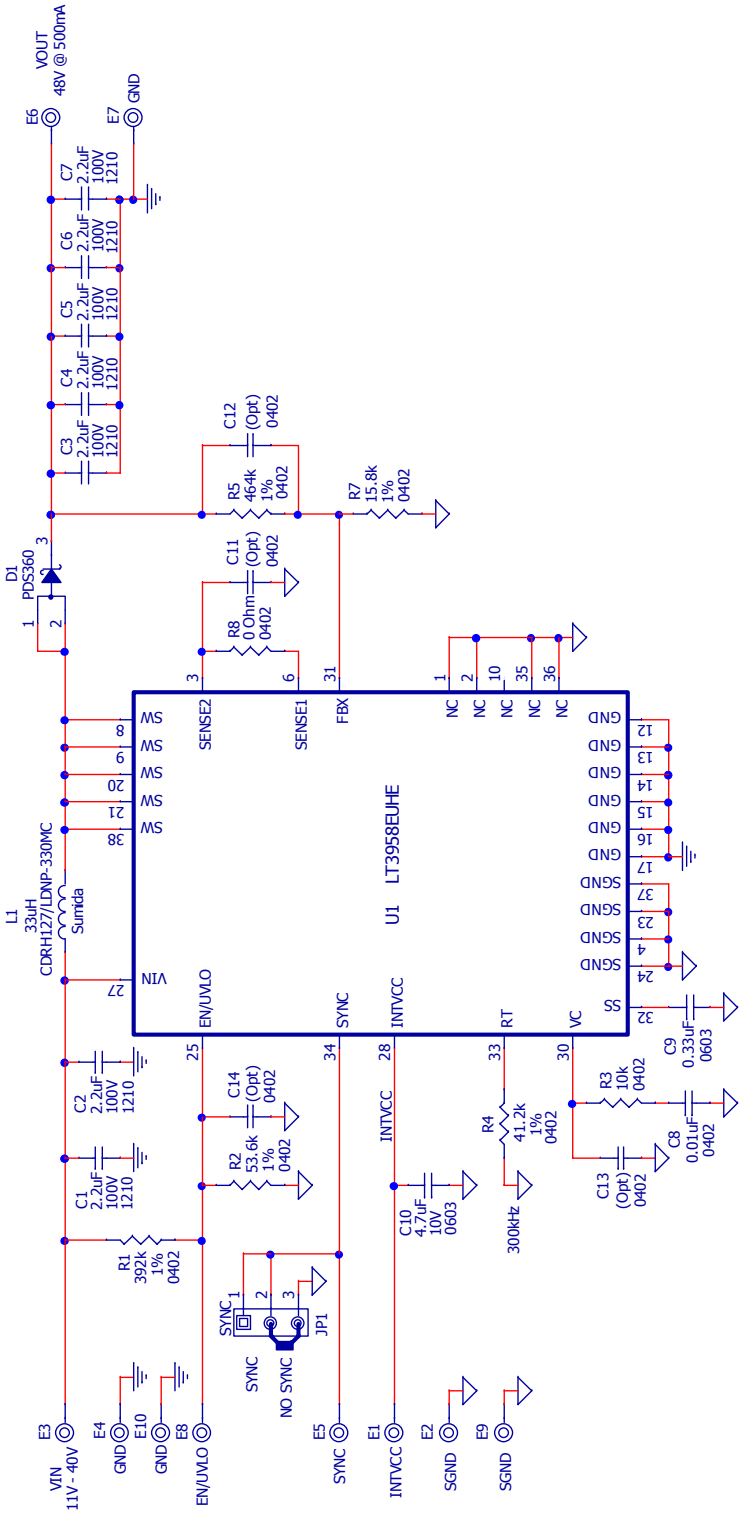
TERMINAL OPTIONS

DC1569A has both **GND** and **SGND** terminals. The schematic shows that the GND and SGND pins of the IC are not tied together outside the IC. They are internally connected. It is important that power ground currents do not run on the SGND components. SGND is used to terminate the signal ground components such as compensation and feedback. Input and output power as well as input and output caps, catch diodes, etc. should all connect to the GND plane. The SGND terminals are provided in case the customer would like to make signal ground measurements, but they do not need to be used. Improperly connecting input power to the SGND terminal results in noisy behavior of the IC.

EN/UVLO (enable / undervoltage lockout) is provided as a terminal so that the part can quickly be placed in shutdown by tying EN/UVLO to GND. The EN/UVLO pin is already being used as an undervoltage lockout threshold for the VIN with resistors R1 and R2. Undervoltage lockout stops the IC from switching when VIN is too low, but shutdown further reduces the VIN pin q current when EN/UVLO is tied directly to GND. It is okay to leave the EN/UVLO terminal floating.

INTVCC is provided as a terminal to be able to power INTVCC externally or to tie INTVCC directly to VIN when VIN remains below 13V. It is okay to leave the INTVCC terminal floating.

SYNC is provided as a terminal to be able to externally synchronize the internal power switching frequency. If SYNC is not used, the terminal should be left floating and the JP1 position should be set at 'NO SYNC'. If SYNC is used, the switching frequency of SYNC should be slightly higher than the programmed switching frequency of the IC and the JP1 position must be set at 'SYNC'. Please see the datasheet for details regarding the use of SYNC and the switching frequency range.


VOUT
48V @ 500mA
E6
E7
GND
C7 2.2uF 100V 1210
C6 2.2uF 100V 1210
C5 2.2uF 100V 1210
C4 2.2uF 100V 1210
C3 2.2uF 100V 1210
C12 (Opt) 0402
R5 464k 1% 0402
R7 15.8k 1% 0402
D1 PDS360
C11 (Opt) 0402
R8 0 Ohm 0402
L1 33uH CDRH127/LDNP-330MC Sumida
U1 LT3958EUHE
SW
SENSE2
SENSE1
FBX
NC
GND
SGND
VIN
EN/UVLO
SYNC
INTVCC
RT
VC
SS
C2 2.2uF 100V 1210
C1 2.2uF 100V 1210
C14 (Opt) 0402
R2 53.6k 1% 0402
R1 392k 1% 0402
C10 4.7uF 10V 0603
R4 41.2k 1% 0402
300kHz
R3 10k 0402
C13 (Opt) 0402
C8 0.01uF 0402
C9 0.33uF 0603
SYNC
NO SYNC
JP1
E3
VIN
11V - 40V
E4
GND
E10
GND
E8
EN/UVLO
E5
SYNC
E1
INTVCC
E2
SGND
E9
SGND