LM3263 High-Current Step-Down DC-DC Converter With MIPI® RF Front-End Control Interface for RF Power Amplifiers

1 Features

- MIPI® RFFE Digital Control Interface
- Operates from a Single Li-Ion Cell: 2.7 V to 5.5 V
- Dynamically Adjustable Output Voltage: 0.4 V to 3.6 V (Typical) in PFM and PWM Modes
- High-Efficiency PFM and PWM Modes With Internal Seamless Transition
- 2.5-A Maximum Load Current in PWM Mode
- 2.7 MHz (Typical) Switching Frequency
- ACB (Reduces Inductor Requirements and Size)
- Internal Compensation
- Current and Thermal Overload Protection
- Very Small Solution Size: Approximately 9.1 mm^2

2 Applications

- Smartphones
- RF PC Cards
- Tablets, eBook Readers
- Handheld Radios
- Battery-Powered RF Devices

3 Description

The LM3263 is a DC-DC converter optimized for powering multi-mode multi-band RF power amplifiers (PAs) from a single lithium-ion cell. The LM3263 steps down an input voltage from 2.7 V to 5.5 V to a dynamically adjustable output voltage of 0.4 V to 3.6 V. The output voltage is externally programmed through the RFFE Digital Control Interface and is set to ensure efficient operation at all power levels of the RF PA.

When operating in pulse width modulated (PWM) mode, the LM3263 produces a small and predictable amount of output voltage ripple thus meeting the power and stringent spectral-compliance needs of RF PAs with minimal filtering and minimal excess headroom. When operating in PFM mode, the LM3263 enables the lowest current consumption across PA output power level settings and therefore maximizes system efficiency.

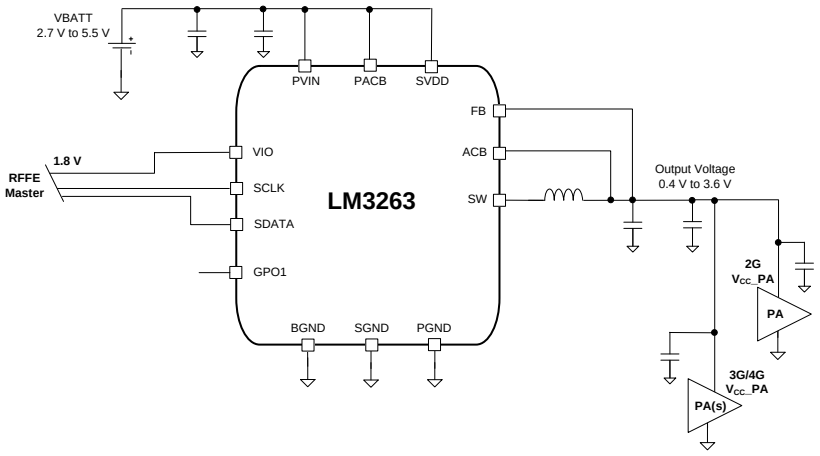
The LM3263 has a unique *A*ctive *C*urrent assist and analog *B*ypass (ACB) feature to minimize inductor size without any loss of output regulation for the entire battery voltage and RF output power range, until dropout. ACB provides a parallel current path, when needed, to limit the maximum inductor current to 1.45 A (typical) while still driving a 2.5-A load. The ACB feature also enables operation with minimal dropout voltage.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (MAX)
LM3263	DSBGA (16)	2.049 mm × 2.049 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application



Copyright © 2016, Texas Instruments Incorporated

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Pin Configuration and Functions ... 3
6 Specifications ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 ESD Ratings ... 4
6.3 Recommended Operating Conditions ... 4
6.4 Thermal Information ... 4
6.5 Electrical Characteristics ... 5
6.6 System Characteristics ... 6
6.7 Typical Characteristics ... 9
7 Detailed Description ... 12
7.1 Overview ... 12
7.2 Functional Block Diagram ... 13
7.3 Feature Description ... 13
7.4 Device Functional Modes ... 17
7.5 Programming ... 19
7.6 Register Map ... 22
8 Application Information ... 24
8.1 Application Information ... 24
8.2 Typical Application ... 24
9 Power Supply Recommendations ... 26
10 Layout Considerations ... 27
10.1 Layout Guidelines ... 27
10.2 4. Layout Examples ... 28
10.3 DSBGA Package Assembly and Use ... 36
11 Device and Documentation Support ... 37
11.1 Device Support ... 37
11.2 Documentation Support ... 37
11.3 Community Resources ... 37
11.4 Trademarks ... 37
11.5 Electrostatic Discharge Caution ... 37
11.6 Glossary ... 37
12 Mechanical, Packaging, and Orderable Information ... 37

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (August 2013) to Revision B — **Page**

- Added *Device Information* and *Pin Configuration and Functions* sections, *ESD Ratings* and *Feature Description*, *Device Functional Modes*, *Application and Implementation*, *Power Supply Recommendations*, *Layout*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections ... 1
- Added *Thermal Information* table with revised $R_{\theta JA}$ value (from 50°C/W to 77.1°C/W) and additional thermal values. ... 4

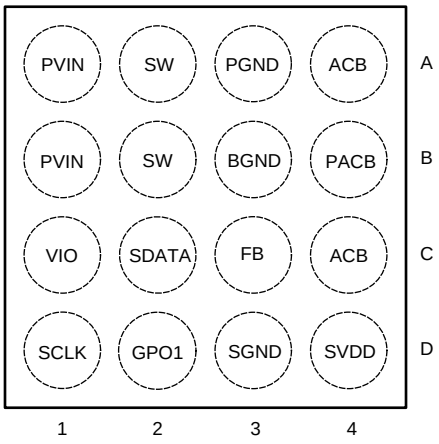
Changes from Original (June 2013) to Revision A — **Page**

- Added new inductor to recommended table ... 36

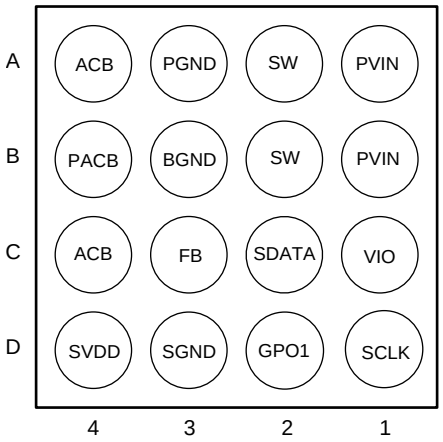
Copyright © 2013–2016, Texas Instruments Incorporated

5 Pin Configuration and Functions

YFQ Package
16-Pin DSBGA
Top View



YFQ Package
16-Pin DSBGA
Bottom View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NUMBER		
ACB	A4	Output	ACB and analog bypass output. Connect to the output at the output filter capacitor.
	C4		
BGND	B3	Ground	ACB, analog bypass ground, and digital ground.
FB	C3	Input	Feedback analog input. Connect to the output at the output filter capacitor.
GPO1	D2	Output	General purpose output. Also used to reconfigure USID.
PACB	B4	Power	ACB power supply input
PGND	A3	Ground	Power ground to the internal NFET switch
PVIN	A1	Power	Power supply voltage input to the internal PFET switch
	B1		
SCLK	D1	Digital/Input	Digital control interface RFFE Bus clock input. Typically connected to RFFE master on RF or baseband IC. SCLK must be held low when VIO is not applied.
SDATA	C2	Digital Input/Output	Digital control interface RFFE bus data input/output. Typically connected to RFFE master on RF or baseband IC. SDATA must be held low when VIO is not applied.
SGND	D3	Ground	Signal analog ground (low current)
SVDD	D4	Power	Analog power supply voltage
SW	A2	Analog	Switching node connection to the internal PFET switch and NFET synchronous rectifier.
	B2		
VIO	C1	Input	VIO functions as the RFFE interface reference voltage. VIO also functions as reset and enable input to the LM3263. Typically connected to voltage regulator controlled by RF or baseband IC.

Copyright © 2013–2016, Texas Instruments Incorporated

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	UNIT
VBATT pins to GND (PVIN, SVDD, PACB to PGND, SGND, BGND)	–0.2	6	V
FB, SW, GPO1, ACB, VIO, SDATA, SCLK	GND – 0.2 V	See(3)	V
Continuous power dissipation(4)	Internally limited		
Maximum operating junction temperature, $T_{J\text{-}MAX}$		150	°C
Maximum lead temperature (soldering 10 seconds)		260	°C
Storage temperature, T_{stg}	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the potential at the GND pins.
(3) Abs Max for FB, SW, GPO1, ACB, VIO, SDATA, SCLK is the lessor of V_{IN} + 0.2 V, or 6 V.
(4) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 150°C (typical) and disengages at T_J = 125°C (typical).

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Input voltage range PVIN, SVDD, PACB	2.7	5.5	V
Input voltage range VIO	1.65	1.95	V
Recommended current load	0	2.5	A
Junction temperature, T_J	–30	125	°C
Ambient temperature, T_A(1)	–30	90	°C

(1) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be de-rated. Maximum ambient temperature ($T_{A\text{-}MAX}$) is dependent on the maximum operating junction temperature ($T_{J\text{-}MAX\text{-}OP}$ = 125°C), the maximum power dissipation of the device in the application ($P_{D\text{-}MAX}$), and the junction-to ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by the following equation: $T_{A\text{-}MAX} = T_{J\text{-}MAX\text{-}OP} – (R_{\theta JA} \times P_{D\text{-}MAX})$. At higher power levels duty cycle usage is assumed to drop (that is, maximum power 12.5% usage is assumed) for GSM/GPRS mode.

6.4 Thermal Information

THERMAL METRIC(1)		LM3263 YFQ (DSBGA) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	77.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	15.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	15.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

Copyright © 2013–2016, Texas Instruments Incorporated

6.5 Electrical Characteristics

Unless otherwise noted, all limits apply to the *Typical Application* with V_{BATT} = 3.8 V (= PVIN = SVDD = PACB), VIO = 1.8 V, T_J = 25°C.(1)(2)(3)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{FB,MIN}$	Feedback voltage at minimum setting	VSET[7:0] = 1Bh, SMPS_CFG[5] = 1b		0.4		V
		VSET[7:0] = 1Bh, SMPS_CFG[5] = 1b −30°C ≤ T_J = T_A ≤ 90°C	0.35		0.45	
$V_{FB,MAX}$	Feedback voltage at maximum setting	VSET[7:0] = F0h, V_{BATT} = 3.9 V, SMPS_CFG[5] = 0b		3.6		V
		VSET[7:0] = F0h, V_{BATT} = 3.9 V, SMPS_CFG[5] = 0b −30°C ≤ T_J = T_A ≤ 90°C	3.492		3.708	
I_{SHDN}	Shutdown supply current	SW = 0 V, VIO = 0 V(4)		0.02		µA
		SW = 0 V, VIO = 0 V(4) −30°C ≤ T_J = T_A ≤ 90°C			4	
I_{L-PWR}	Low-power mode supply current	VSET[7:0] = 00h		0.225		µA
I_{Q-PFM}	PFM mode supply current into SVDD	No switching(5), SMPS_CFG[5] = 1b		360		µA
		No switching(5), SMPS_CFG[5] = 1b −30°C ≤ T_J = T_A ≤ 90°C			425	
$I_{Q\ PWM}$	PWM mode supply current	No switching(5), SMPS_CFG[5] = 0b		1240		µA
		No switching(5), SMPS_CFG[5] = 0b −30°C ≤ T_J = T_A ≤ 90°C			1400	
$I_{LIM,\ PFET\ Transient}$	Positive transient peak current limit	VSET[7:0] = 64h(6)		1.9		A
		VSET[7:0] = 64h(6) −30°C ≤ T_J = T_A ≤ 90°C			2.1	
$I_{LIM,\ PFET\ Steady-State}$	Positive steady-state peak current limit	VSET[7:0] = 64h(6)		1.45		A
		VSET[7:0] = 64h(6) −30°C ≤ T_J = T_A ≤ 90°C	1.35		1.65	
$I_{LIM,\ P-ACB}$	Positive active current assist peak current limit	VSET[7:0] = 64h(6)		1.7		A
		VSET[7:0] = 64h(6) −30°C ≤ T_J = T_A ≤ 90°C	1.4		2	
$I_{LIM,NFET}$	NFET current limit	VSET[7:0] = A7h(6)		−1.5		A
f_{OSC}	Average Internal oscillator frequency	VSET[7:0] = A7h		2.7		MHz
		VSET[7:0] = A7h −30°C ≤ T_J = T_A ≤ 90°C	2.43		2.97	
I_{VIO-IN}	VIO voltage average input current	Average during a 26-MHz write			1.25	mA
V_{IORST}	RFFE I/O voltage reset voltage	VIO toggled low			0.45	V
I_{INVIO}	VIO reset current	VIO = 0.45 V	−1		1	µA
I_{IN}	SDATA, SCLK input current	VIO = 1.95 V	−1		1	µA
V_{IH}	Input high-level threshold SDATA, SCLK		0.4 × VIO		0.7 × VIO	V
V_{IL}	Input low-level threshold SDATA, SCLK		0.3 × VIO		0.6 × VIO	V
V_{IH-GPO}	Input high-level threshold GPO1	−30°C ≤ T_J = T_A ≤ 90°C	1.35			V
V_{IL-GPO}	Input low-level threshold GPO1	−30°C ≤ T_J = T_A ≤ 90°C			0.67	V

(1) All voltages are with respect to the potential at the GND pins.
(2) Minimum and Maximum limits are specified by design, test, or statistical analysis.
(3) The parameters in *Electrical Characteristics* are tested under open loop conditions at PVIN = SVDD = PACB = 3.8 V.
(4) Shutdown current includes leakage current of PFET.
(5) I_Q specified here is when the part is not switching.
(6) Current limit is built-in, fixed, and not adjustable.

Copyright © 2013–2016, Texas Instruments Incorporated

Electrical Characteristics (continued)

Unless otherwise noted, all limits apply to the *Typical Application* with V_{BATT} = 3.8 V (= PVIN = SVDD = PACB), VIO = 1.8 V, T_J = 25°C.(1)(2)(3)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	Output high-level threshold SDATA	I_{SDATA} = 2 mA	VIO × 0.8		VIO + 0.01	V
V_{OL}	Output low-level threshold SDATA	I_{SDATA} = –2 mA			VIO × 0.2	V
V_{OH-GPO}	Output high-level threshold GPO	I_{OUT} = ±200 µA	VIO – 0.15		VIO + 0.1	V
V_{OL-GPO}	Output low-level threshold GPO		–0.4		0.3	V
$V_{SET-LSB}$	Output voltage LSB	VSET[7:0] = A7h to A8h		15		mV

6.6 System Characteristics

The following spec table entries are specified by design and verifications providing the component values in the *Typical Application* are used (L = 1.5 µH, DCR = 120 mΩ, TOKO DFE201610MT-1R5N, C_{IN} = 10 µF, 6.3 V, 0402, Samsung CL05A106MP5NUN, C_{OUT} = 10 µF + 4.7 µF + 3 × 1 µF; 10 V, 0402, Samsung CL05A106MP5NUN, CL05A475MPNRN; 6.3 V, 0201, TDK, C0603X5R0J105M). *These parameters are not verified by production testing.* Minimum and maximum values are specified over the ambient temperature range T_A = –30°C to +90°C. Typical values are specified at V_{BATT} = 3.8 V (= PVIN = SVDD = PACB), VIO = 1.8 V, SMPS_CFG = 20h, and T_A = 25°C, unless otherwise stated.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{ON}	Turnon time (time for output to reach 95% of 3.4-V value from the end of the SCLK pulse)	V_{BATT} = 4.2 V, VSET[7:0] =00h to E3h, VSET = 3.4 V, I_{OUT} ≤ 1 mA			50	µs
$T_{RESPONSE}$	Time for V_{OUT} to rise from 0.09 V to 3.4 V (3.07 V, 90% of delta V_{OUT} from the end of SCLK pulse)	V_{BATT} = 3.8 V, R_{LOAD} = 68 Ω VSET[7:0] = 06h to E3h SMPS_CFG[5] = 0b/1b			15	µs
	Time for V_{OUT} to fall from 3.4 V to 0.09 V (0.42 V, 10% of delta V_{OUT} from the end of SCLK pulse)	V_{BATT} = 3.8 V, R_{LOAD} = 68 Ω VSET[7:0] = E3h to 06h SMPS_CFG[5] = 0b/1b			15	
	Time for V_{OUT} to rise from 0.8 V to 3.3 V (3.05V, 90% of delta V_{OUT} from the end of SCLK pulse)	V_{BATT} = 3.8 V, R_{LOAD} = 20 Ω VSET[7:0] =36h to DCh		7.4	12	
	Time for V_{OUT} to fall from 3.3 V to 0.8 V (1.05 V, 10% of delta V_{OUT} from the end of SCLK pulse)	V_{BATT} = 3.8 V, R_{LOAD} = 20 Ω VSET[7:0] = DCh to 36h		6.8	12	
	Time for V_{OUT} to rise from 1.4 V to 3.4 V (3.2 V, 90% of delta V_{OUT} from the end of SCLK pulse)	V_{BATT} = 3.8 V, R_{LOAD} = 6.8 Ω VSET[7:0] = 5Eh to E3h			10	
	Time for V_{OUT} to fall from 3.4 V to 1.4 V (1.6 V, 10% of delta V_{OUT} from the end of SCLK pulse)	V_{BATT} = 3.8 V, R_{LOAD} = 6.8 Ω VSET[7:0] = E3h to 5Eh			10	
	Time for V_{OUT} to rise from 1.8 V to 2.8 V (2.7 V, 90% of delta V_{OUT} from the end of SCLK pulse)	V_{BATT} = 3.8 V, R_{LOAD} = 2.2 Ω VSET[7:0] = 78h to BBh SMPS_CFG[5] = 0b			15	
	Time for V_{OUT} to fall from 2.8 V to 1.8 V (1.9 V, 10% of delta V_{OUT} from the end of SCLK pulse)	V_{BATT} = 3.8 V, R_{LOAD} = 2.2 Ω VSET[7:0] = BBh to 78h SMPS_CFG[5] = 0b			15	
T_{Bypass}	Time for VSET to rise from 0.09V to PVIN after BYPASS transition (90%)	V_{BATT} = 3.6 V, I_{OUT} ≤ 1 mA, VSET[7:0] = 06h to FFh			20	µs
$R_{tot-drop}$	Total dropout resistance in bypass mode	VSET[7:0] = FAh, Max value at V_{BATT} = 3.1 V, Inductor DCR ≤ 151 mΩ		45	55	mΩ

Copyright © 2013–2016, Texas Instruments Incorporated

System Characteristics (continued)

The following spec table entries are specified by design and verifications providing the component values in the *Typical Application* are used (L = 1.5 µH, DCR = 120 mΩ, TOKO DFE201610MT-1R5N, C_{IN} = 10 µF, 6.3 V, 0402, Samsung CL05A106MP5NUN, C_{OUT} = 10 µF + 4.7 µF + 3 × 1 µF; 10 V, 0402, Samsung CL05A106MP5NUN, CL05A475MPNRN; 6.3 V, 0201, TDK, C0603X5R0J105M). *These parameters are not verified by production testing.* Minimum and maximum values are specified over the ambient temperature range T_A = –30°C to +90°C. Typical values are specified at V_{BATT} = 3.8 V (= PVIN = SVDD = PACB), VIO = 1.8 V, SMPS_CFG = 20h, and T_A = 25°C, unless otherwise stated.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{OUT}	Maximum load current in PWM mode	Switcher + ACB	2.5			A
$I_{OUT, PU}$	Maximum output transient pullup current limit	Switcher + ACB(1)	3			
$I_{OUT, PD, PWM}$	PWM maximum output transient pulldown current limit	Switcher + ACB(1)			−3	
I_{OUT, MAX_PFM}	Maximum output load current in PFM mode	V_{BATT} = 3.8 V, VSET = 3.2 V	60			mA
Linearity	Linearity in control range of VSET = 0.4 V to 3.6 V	V_{BATT} = 3.9 V(2), Monotonic in nature; VSET[7:0] = 1Bh to F0h, SMPS_CFG[5] = 0b	–3%		3%	
			–50		50	mV
η	Efficiency	V_{BATT} = 3.8 V, VSET= 0.5 V, I_{OUT} = 5mA	52%	56%		
		V_{BATT} = 3.8 V, VSET= 1.8 V, I_{OUT} = 10 mA	78%	82%		
		V_{BATT} = 3.8 V, VSET= 1.6 V, I_{OUT} = 130 mA	83%	89%		
		V_{BATT} = 3.8 V, VSET = 2.5 V, I_{OUT} = 250 mA	90%	94%		
		V_{BATT} = 3.8 V, VSET = 3.4 V, I_{OUT} = 550 mA	93%	95%		
		V_{BATT} = 3.8 V, VSET = 1 V, I_{OUT} = 400 mA, SMPS_CFG[5] = 0b	81%	85%		
		V_{BATT} = 3.8 V, VSET = 3.5 V, I_{OUT} = 1900 mA, SMPS_CFG[5] = 0b	89%	92%		
V_{RIPPLE}	2.7-MHz PWM normal operation ripple	V_{BATT} = 3.2 V to 4.3 V, VSET = 0.4 V to 3.6 V, R_{LOAD} = 1.9 Ω(3) SMPS_CFG[5]= 0b		1	3	mV_{pp}
	Ripple voltage at pulse skipping condition	V_{BATT} = 3.2 V, VSET = 3 V, R_{LOAD} = 1.9 Ω (3) SMPS_CFG[5]= 0b			8	
	PFM ripple voltage	V_{BATT} = 3.2 V, VSET = 3 V, I_{OUT} = 40 mA			50	
		V_{BATT} = 3.2 V, VSET = 2.5 V, I_{OUT} = 10 mA			50	
		V_{BATT} = 3.2 V, VSET< 0.5 V, I_{OUT} = 5 mA			50	
Line_tr	Line transient response	V_{BATT} = 3.6 V to 4.2 V, T_R = T_F = 10 µs, VSET = 3.2 V, I_{OUT} = 500 mA		50		mV_{pk}
Load_tr	Load transient response	VSET = 3 V, T_R = T_F = 10 µs, I_{OUT} = 0 A to 1.2 A, SMPS_CFG[5] = 0b		60		mV_{pk}
Max Duty Cycle	Maximum duty cycle		100%			

(1) Current limit is built-in, fixed, and not adjustable.
(2) Linearity limits are ±3% or ±50 mV whichever is larger.
(3) Ripple voltage must be measured at C_{OUT} electrode on a well-designed PC board using suggested inductor and capacitors.

Copyright © 2013–2016, Texas Instruments Incorporated

System Characteristics (continued)

The following spec table entries are specified by design and verifications providing the component values in the *Typical Application* are used (L = 1.5 µH, DCR = 120 mΩ, TOKO DFE201610MT-1R5N, C_{IN} = 10 µF, 6.3 V, 0402, Samsung CL05A106MP5NUN, C_{OUT} = 10 µF + 4.7 µF + 3 × 1 µF; 10 V, 0402, Samsung CL05A106MP5NUN, CL05A475MPNRN; 6.3 V, 0201, TDK, C0603X5R0J105M). *These parameters are not verified by production testing.* Minimum and maximum values are specified over the ambient temperature range T_A = –30°C to +90°C. Typical values are specified at V_{BATT} = 3.8 V (= PVIN = SVDD = PACB), VIO = 1.8 V, SMPS_CFG = 20h, and T_A = 25°C, unless otherwise stated.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PFM_Freq	Minimum PFM frequency	V_{BATT} = 3.2 V, VSET = 1 V, I_{OUT} = 10 mA	100	160		KHz
		V_{BATT} = 3.2 V, VSET = 0.5 V, I_{OUT} = 5 mA	34	55		
N_{SET}	VSET DAC number of bits	Monotonic	8			Bits
T_{SETUP}	Power-up time (time for RFFE bus active after VIO applied)	VIO = Low to 1.65 V			50	ns
$T_{VIO-RST}$	VIO supply reset timing	VIO = 0.45 V	10			µs

Copyright © 2013–2016, Texas Instruments Incorporated

6.7 Typical Characteristics

V_{BATT} = 3.8 V, T_A = 25°C, unless otherwise noted

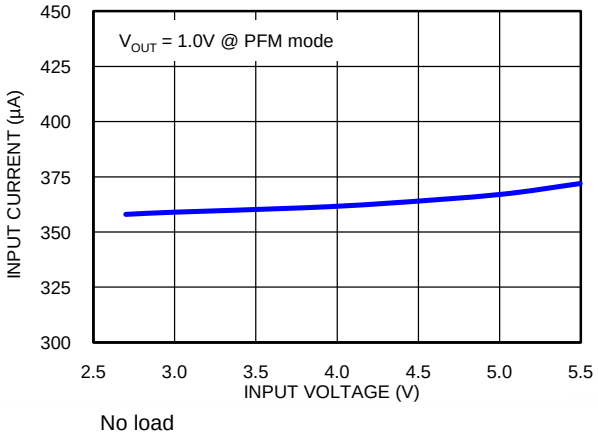


Figure 1. Input Current (PFM) vs Input Voltage

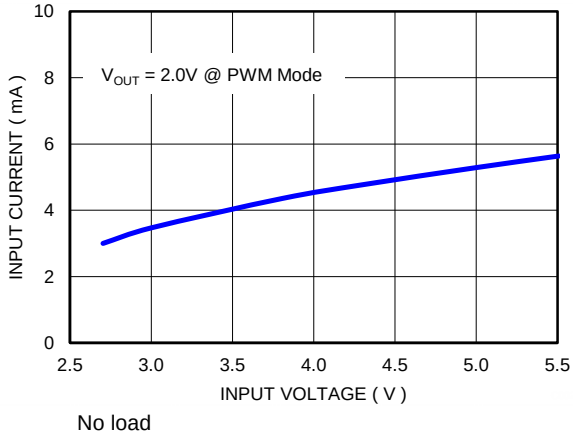


Figure 2. Input Current (PWM) vs Input Voltage

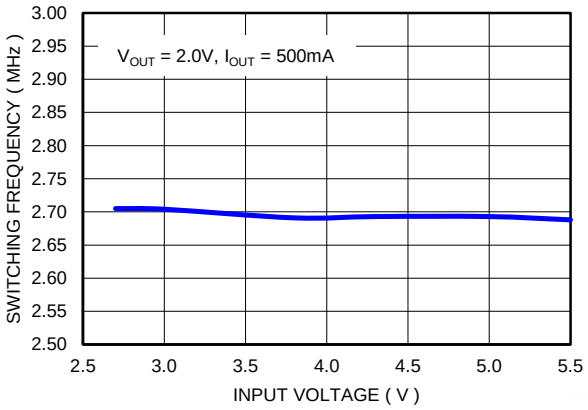


Figure 3. Average Switching Frequency vs Input Voltage

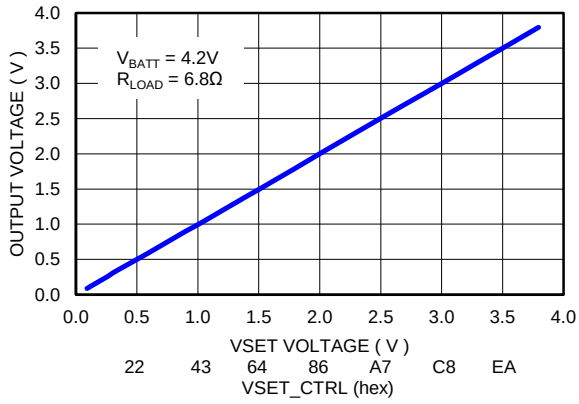


Figure 4. Output Voltage vs V_{SET_CTRL} Setting

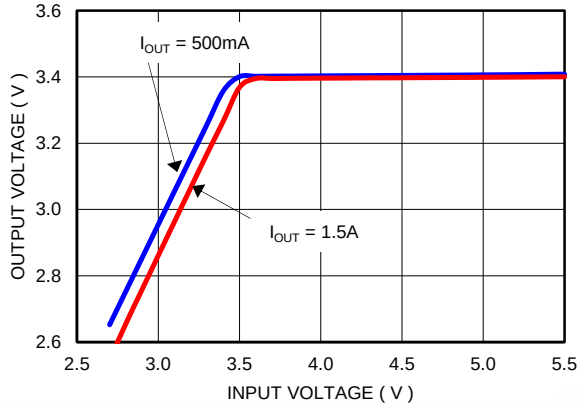


Figure 5. Output Voltage vs Input Voltage

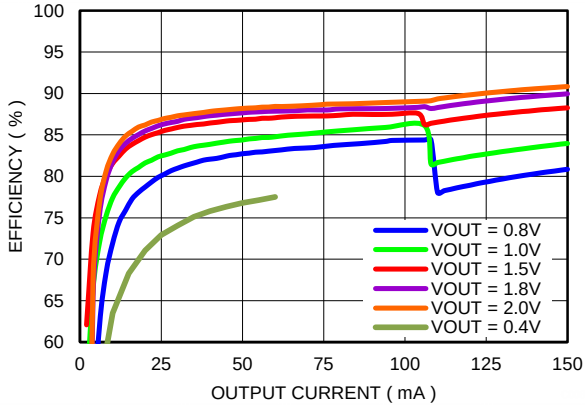
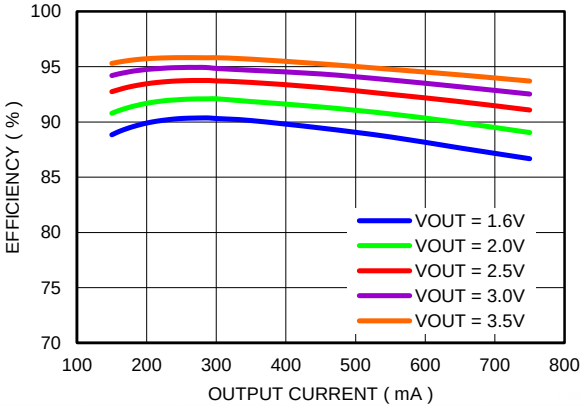


Figure 6. Efficiency vs Load Current

Copyright © 2013–2016, Texas Instruments Incorporated

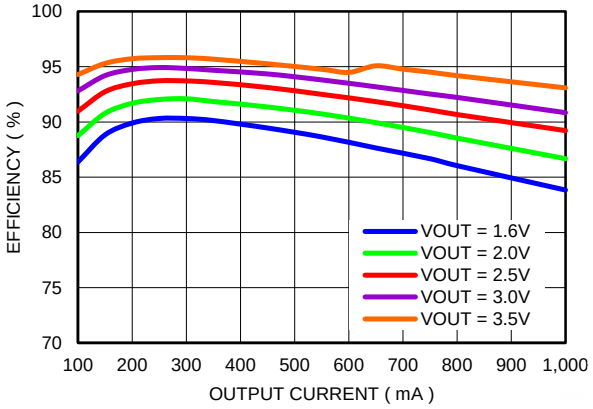
Typical Characteristics (continued)

V_{BATT} = 3.8 V, T_A = 25°C, unless otherwise noted



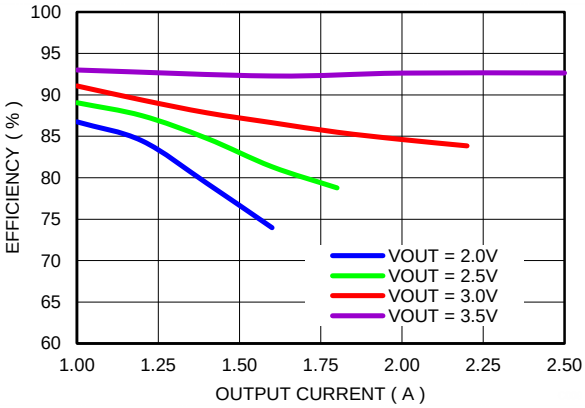
Auto-PFM Mode I_{OUT} = 150 mA to 750 mA

Figure 7. Efficiency vs Load Current



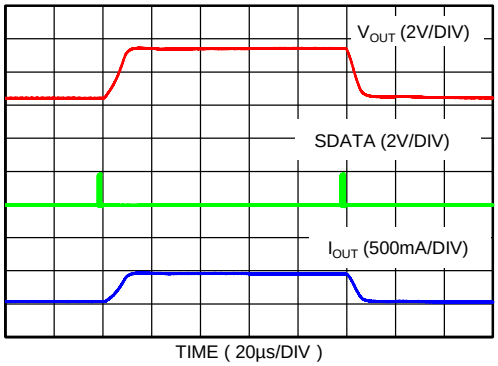
Forced PWM Mode I_{OUT} = 100 mA to 1000 mA

Figure 8. Efficiency vs Load Current



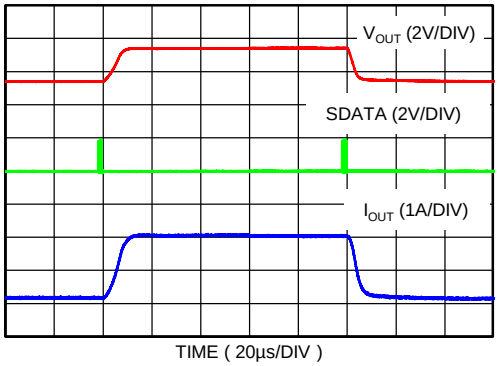
Forced PWM Mode I_{OUT} = 1 A to 2.5 A

Figure 9. Efficiency vs Load Current



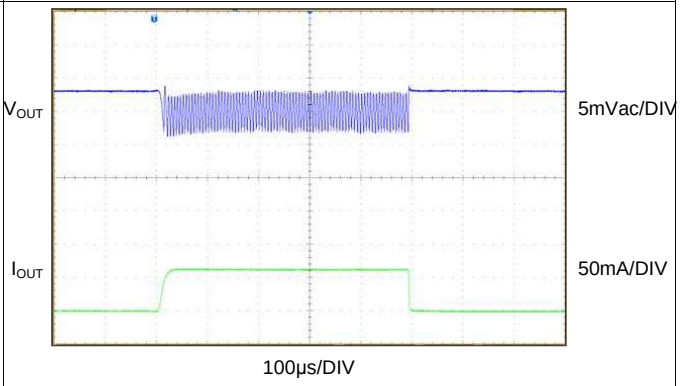
Auto PFM V_{OUT} = 0.4 V to 3.4 V R_{LOAD} = 6.8 Ω

Figure 10. V_{OUT} Transient



Forced PWM V_{OUT} = 1.4 V to 3.4 V R_{LOAD} = 1.9 Ω

Figure 11. V_{OUT} Transient



PFM Mode V_{OUT} = 1 V I_{OUT}= 0 mA to 60 mA

Figure 12. Load Transient

Copyright © 2013–2016, Texas Instruments Incorporated

Typical Characteristics (continued)

V_{BATT} = 3.8 V, T_A = 25°C, unless otherwise noted

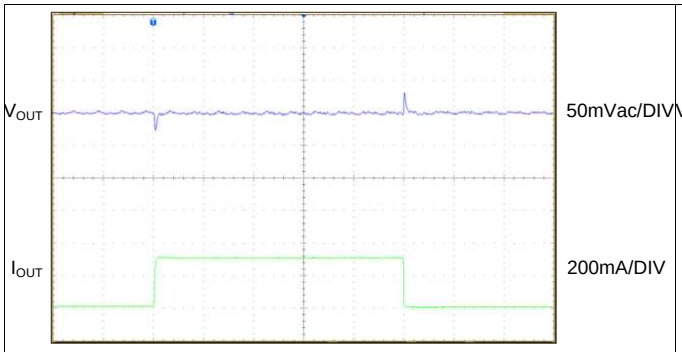


Figure 13. Load Transient

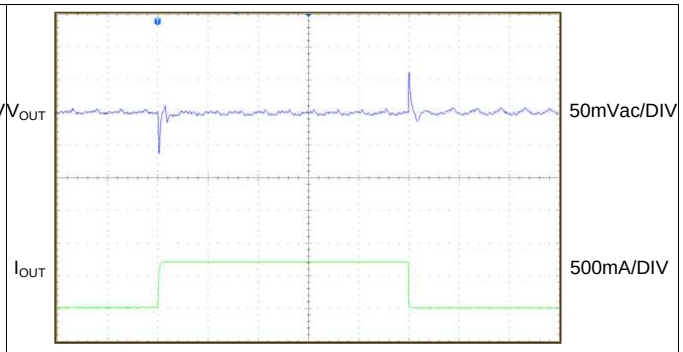


Figure 14. Load Transient

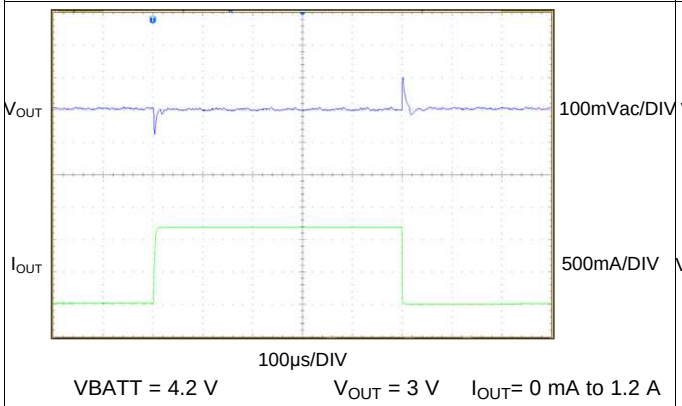


Figure 15. Load Transient

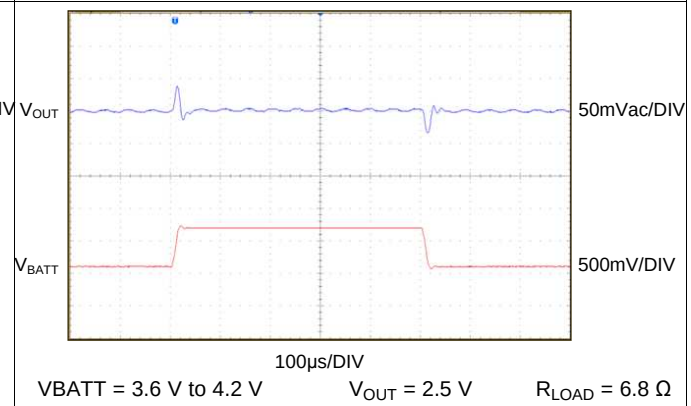


Figure 16. Line Transient

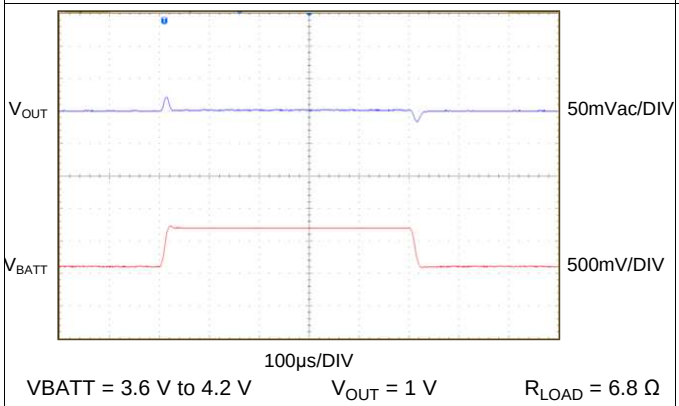


Figure 17. Line Transient

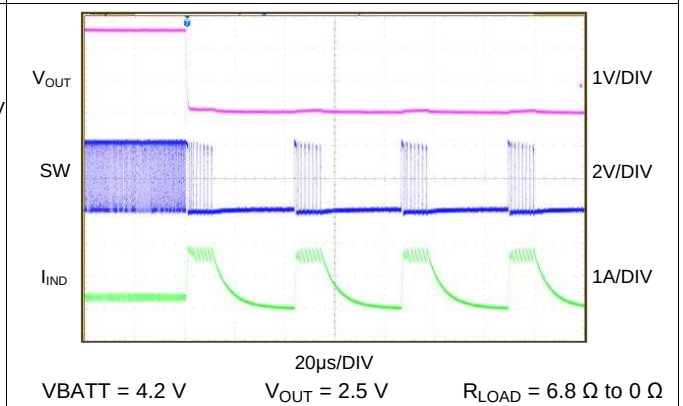


Figure 18. Timed-Current Limit

Copyright © 2013–2016, Texas Instruments Incorporated

7 Detailed Description

7.1 Overview

The LM3263 is a high-efficiency step-down DC-DC converter optimized to power the RF power amplifier (PA) in cell phones, portable communication devices, or battery-powered RF devices with a single litium-Ion battery. It operates in modulated-frequency pulsed width modulation (PWM) mode for 2G transmissions (with MODE = Forced PWM (PWM only), register 01h SMPS_CFG [5] set to 0b), automatic mode transition between pulse frequency modulation (PFM) and PWM for 3G/4G RF PA operation (with MODE = Auto-PFM (PFM/PWM), SMPS_CFG bit 5 set to 1b), or forced-bypass mode (with SMPS_CFG [4] set to 1b or REGISTER_0 [6:0] set to 7Fh or register 03h VSET_CTRL [7:0] set to FEh-FFh). Power states are also in provided shutdown, low power, standby, and active modes. The DC-DC converter operates at active mode. Please see Figure 21 and *Register Map*.

PWM mode provides high efficiency and very low output-voltage ripple. In PWM-mode operation, the modulated switching frequency helps to reduce RF transmit noise. In PFM mode, the converter operates with reduced switching frequencies and lower supply current to maintain high efficiencies. The forced-bypass mode allows the user to drive the output directly from the input supply through a bypass FET. The shutdown mode turns the LM3263 off and reduces current consumption to 0.02 µA (typical).

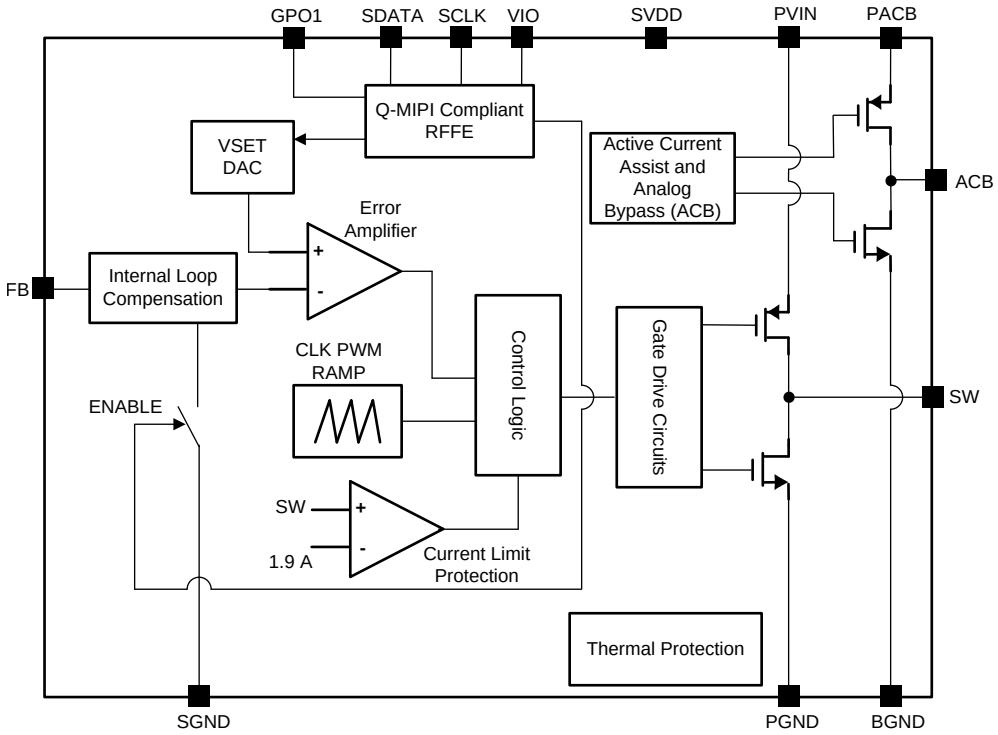
In the PWM and PFM modes of operation, the output voltage of the LM3263 can be dynamically programmed from 0.4 V to 3.6 V (typical) by setting the VSET register. Current overload protection and thermal overload protection are also provided.

The LM3263 was engineered with *A*ctive *C*urrent assist and analog *B*ypass (ACB). This unique feature allows the converter to support maximum load currents of 2.5 A (minimum) while keeping a small footprint inductor and meeting all of the transient behaviors required for operation of a multi-mode RF PA. The ACB circuit provides an additional current path when the load current exceeds 1.45 A (typical) or as the switcher approaches dropout. Similarly, the ACB circuit allows the converter to respond with faster VSET output voltage transition times by providing extra output current on rising and falling output edges. The ACB circuit also performs the function of analog bypass. Depending upon the input voltage, output voltage, and load current, the ACB circuit automatically and seamlessly transitions the converter into analog bypass, while maintaining output voltage regulation and low output voltage ripple. Full bypass (100% duty cycle operation) occurs if the total dropout resistance in bypass mode (R_{tot_drop} = 45 mΩ) is insufficient to regulate the output voltage.

The device 16-pin DSBGA package is the best solution for space-constrained applications such as cell phones and other hand-held devices. The high switching frequency, 2.7 MHz (typical) in PWM mode, reduces the size of input capacitors, output capacitor, and of the inductor. Use of a DSBGA package is best suited for opaque case applications and requires special design considerations for implementation (see *Layout Considerations*).

Copyright © 2013–2016, Texas Instruments Incorporated

7.2 Functional Block Diagram



Copyright © 2016, Texas Instruments Incorporated

7.3 Feature Description

7.3.1 PWM Operation

The LM3263 operates in PWM mode when forced-PWM mode operation is selected (SMPS_CFG [5] set to 0b). The switching frequency is modulated, and the switcher regulates the output voltage by changing the energy per cycle to support the load required. During the first portion of each switching cycle, the control block in the LM3263 turns on the internal PFET switch. This allows current to flow from the input through the inductor and to the output filter capacitor and load. The inductor limits the current to a ramp with a slope of (V_{BATT} – VSET)/L, by storing energy in its magnetic field.

During the second portion of each cycle, the control block turns the PFET switch off, blocking current flow from the input, and then turns the NFET synchronous rectifier on. The inductor draws current from ground through the NFET and to the output filter capacitor and load, which ramps the inductor current down with a slope of –VSET/L. The output filter capacitor stores charge when the inductor current is greater than the load current and releases it when the inductor current is less than the load current, smoothing the voltage across the load.

At the next rising edge of the clock, the cycle repeats. An increase of load pulls the output voltage down, increasing the error signal. As the error signal increases, the peak inductor current becomes higher therefore increasing the average inductor current. The output voltage is therefore regulated by modulating the PFET switch on time to control the average current sent to the load. The circuit generates a duty-cycle modulated rectangular signal that is averaged using a low pass filter formed by the inductor and output capacitor. The output voltage is equal to the average of the duty-cycle modulated rectangular signal.

Feature Description (continued)

7.3.2 PFM Operation

When auto-PFM mode operation is selected (SMPS_CFG [5] set to 1b), the LM3263 automatically transitions from PWM operation into PFM operation if the average inductor current is less than 60 mA (minimum) and the difference between V_{BATT} – VSET ≥ 0.6 V. The switcher regulates the fixed output voltage by transferring a fixed amount of energy during each cycle and modulating the frequency to control the total power delivered to the output. The converter switches only as needed to support the demand of the load current, therefore maximizing efficiency. If there is an increase in load current during PFM mode to more than 120 mA (typical), the part automatically transitions into PWM mode. A 20 mA (typical) hysteresis window exists between PFM and PWM transitions. After a transient event, the part temporarily operates in PWM mode to quickly charge or discharge the output. This is true for start-up conditions or if the mode operation is changed from forced-PWM to auto-PFM mode (SMPS_CFG [5] toggled from 0b to 1b). Once the output reaches its target output voltage, and the load is less than 60 mA (minimum), then the device seamlessly transitions into PFM mode (assuming the device is not in forced-bypass condition).

7.3.3 Active Current Assist and Analog Bypass (ACB)

The 3GPP time mask requirement for 2G requires high current to be sourced by the LM3263. These high currents are required for a small time during transients or under a heavy load. Overrating the switching inductor for these higher currents increases the solution size and is not an optimum solution. Thus, to allow an optimal inductor size for such a load, an alternate current path is provided from the input supply through the ACB pin. Once the switcher current limit $I_{LIM,PFET,SteadyState}$ is reached, the ACB circuit starts providing the additional current required to support the load. The ACB circuit also minimizes the dropout voltage by having the analog bypass FET in parallel with VSET. The LM3263 can provide up to 2.5 A (minimum) of current in bypass mode.

7.3.4 Bypass Operation

The bypass circuit provides an analog bypass function with very low dropout resistance (R_{tot_drop} = 45 mΩ typical). When SMPS_CFG [4] is set to 0b, the part is in automatic bypass mode which automatically determines the amount of bypass needed to maintain voltage regulation. When the input supply voltage to the LM3263 is lowered to a level where the commanded duty cycle is higher than what the converter is capable of providing, the part goes into pulse-skipping mode. The switching frequency is reduced to maintain a low and well behaved output voltage ripple. The analog bypass circuit allows the converter to stay in regulation until full bypass is reached (100% duty cycle operation). The converter comes out of full bypass and back into analog bypass regulation mode with a similar reverse process.

To operate the device at the Forced-Bypass mode, set REGISTER_0 to 7Fh or VSET_CTRL to FEh-FFh.

7.3.5 Dynamic Adjustment of Output Voltage

The LM3263 can be dynamically programmed to an output voltage from 0.4 V to 3.6 V with 30 mV or 15 mV steps. REGISTER_0 [6:0] is set to 0Dh to 78h with 30-mV output voltage steps, and VSET_CTRL [7:0] is set to 1Bh to F0h with 15-mV steps. Although the output voltage can be programmed lower than 0.4 V and higher than 3.6 V by setting the registers, the device might suffer from larger output ripple voltage, higher current limit operation, and decreased linearity.

7.3.6 DC-DC Operating Mode Selection

Programming SMPS_CFG [5] changes the state of the converter to one of the two allowed modes of operation. SMPS_CFG [5] default is 0b, and the device operates in forced-PWM mode (PWM only). Setting the register bit to 1b sets the device for automatic transition between PFM/PWM mode operation. In this mode, the converter operates in PFM mode to maintain the output voltage regulation at very light loads and transitions into PWM mode at loads exceeding 120 mA (typical). Setting the register bit to 0b sets the device for PWM mode operation. The switching operation is in PWM mode only, and the switching frequency is also 2.7 MHz (typical). The device operates in forced-bypass mode when SMPS_CFG [4] is set to 1b.

For typical operation mode is set to auto-PFM and auto-bypass modes by setting SMPS_CFG = 20h.

Table 1 shows the LM3263 parameters for the given modes.

Copyright © 2013–2016, Texas Instruments Incorporated

Feature Description (continued)

Table 1. Parameters Under Different Modes Of Operation

SMPS_CFG [5] MODE	SMPS_CFG [4] BYPS	I_{OUT} CONDITIONS	OPERATION MODE
0	0	X	Forced PWM
X(1)	1	X	Forced bypass
1	0	$I_{OUT} \leq 60$ mA	PFM
1	0	60 mA < $I_{OUT} \leq 120$ mA	PFM or PWM
1	0	$I_{OUT} > 120$ mA	PWM

(1) don't care

7.3.7 Internal Synchronous Rectification

The LM3263 uses an internal NFET as a synchronous rectifier to reduce rectifier forward voltage drop, thus increasing efficiency. The reduced forward voltage drop in the internal NFET synchronous rectifier significantly improves efficiency for low output voltage operation. The NFET is designed to conduct through its intrinsic body diode during the transient intervals, eliminating the need of an external diode.

7.3.8 Current Limit

The LM3263 current limit feature protects the converter during current overload conditions. Both SW and ACB pins have positive and negative current limits. The positive and negative current limits bound the SW and ACB currents in both directions. The SW pin has two positive current limits. The $I_{LIM,PFET,SteadyState}$ current limit triggers the ACB circuit. Once the peak inductor current exceeds $I_{LIM,PFET,SteadyState}$, the ACB circuit starts assisting the switcher and provides just enough current to keep the inductor current from exceeding $I_{LIM,PFET,SteadyState}$ allowing the switcher to operate at maximum efficiency. Transiently a second current limit ($I_{LIM,PFET,Transient}$) of 1.9 A (typical, 2.1 A maximum) limits the maximum peak inductor current possible. The output voltage falls out of regulation only after both SW and ACB output pin currents reach their respective current limits of $I_{LIM,PFET,Transient}$ and $I_{LIM,P-ACB}$.

7.3.9 Timed Current Limit

If the load or output short-circuit pulls the output voltage to 0.3 V or lower, and the peak inductor current sustains $I_{LIM,PFET,SteadyState}$ more than 10 µs, the LM3263 switches to a timed current limit mode. In this mode, the internal PFET switch is turned off. After approximately 30 µs, the device returns to the normal operation.

7.3.10 Thermal Overload Protection

The LM3263 device has a thermal overload protection that protects itself from short-term misuse and overload conditions. If the junction temperature exceeds 150°C, the LM3263 shuts down. Normal operation resumes after the temperature drops below 125°C. Prolonged operation in thermal overload condition may damage the device and is therefore not recommended.

7.3.11 Start-Up

The waveform in Figure 19 shows the start-up sequence and sample conditions. First, VBATT (=PVIN=SVDD=PACB) must take on a value from 2.7 V to 5.5 V. After VBATT is ensured to be beyond 2.7 V, VIO can be set 1.8 V. Next, setting PM_TRIG [7:6] to 38h enables active mode. Finally, VSET can be programmed to a value that corresponds to the desired output voltage. The LM3263 output voltage then goes to the programmed VSET value. To optimize the start-up time and behavior of the output voltage, the LM3263 starts up in PWM mode even when the operating mode selected is auto-PFM mode (SMPS_CFG [5] set to 1b) if the output load current is ≤ 60 mA (minimum), the LM3263 then seamlessly transitions into PFM mode.

Copyright © 2013–2016, Texas Instruments Incorporated

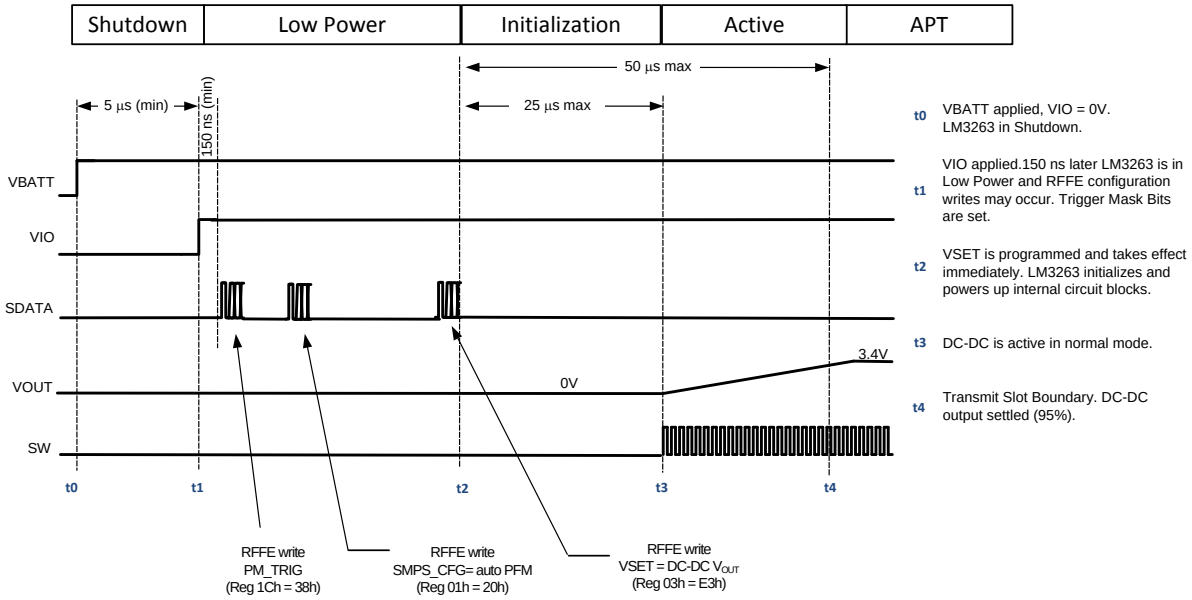


Figure 19. Non-Triggered Start-Up Sequence

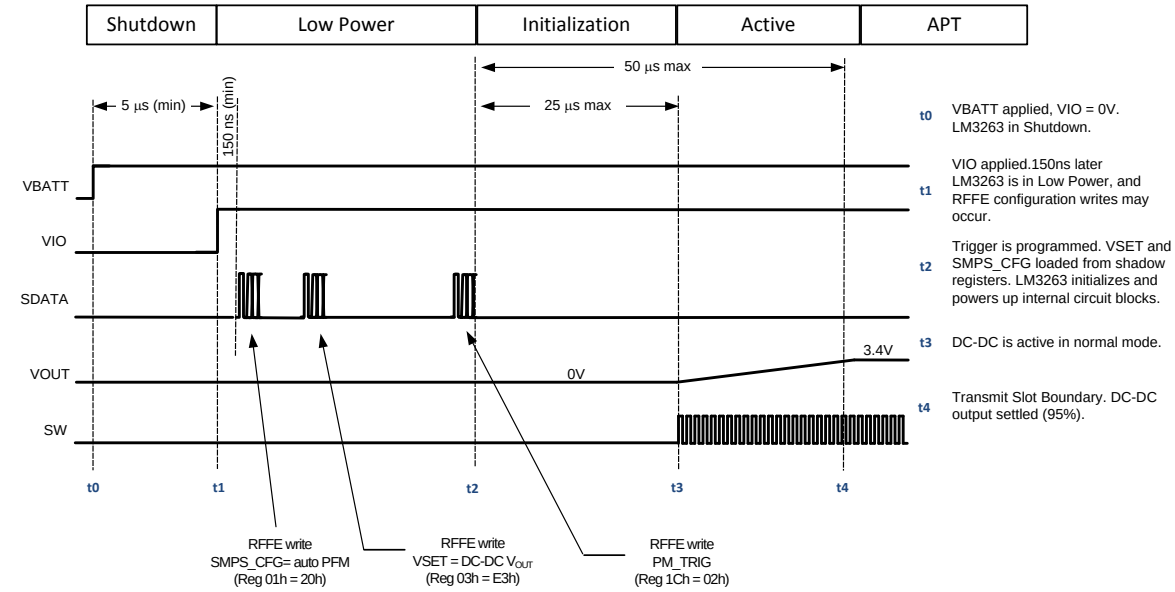


Figure 20. Triggered Start-Up Sequence

Copyright © 2013–2016, Texas Instruments Incorporated

7.4 Device Functional Modes

7.4.1 Shutdown Mode

Shutdown mode is entered whenever the voltage on the VIO pin is 0 V. The communications and the controls are not powered. In this mode, the current consumption is 0.02 µA (typical).

7.4.2 Low-Power Mode

Low-power mode is the initial default state when VIO is applied. In this mode, the DC-DC is disabled, and its SW is tri-state. The current consumption is minimized 0.225 µA (typical). This mode can be entered by programming any one of three registers below:

- Register 00h REGISTER_0 [6:0] to 00h;
- Register 03h VSET_CTRL[7:0] to 00h or 01h;
- Register 1Ch PM_TRIG [7:6] to 10b.

7.4.3 Standby Mode

In standby mode, switching is stopped, and the output power FETs are placed are tri-state. The standby mode can be entered by setting PM_TRIG [7:6] and REGISTER_0 or VSET_CTRL registers.

- Register 00h REGISTER_0 [6:0] to 02h;
- Register 03h VSET_CTRL [7:0] to 04h or 05h;
- Register 1Ch PM_TRIG [7:6] to 00b.

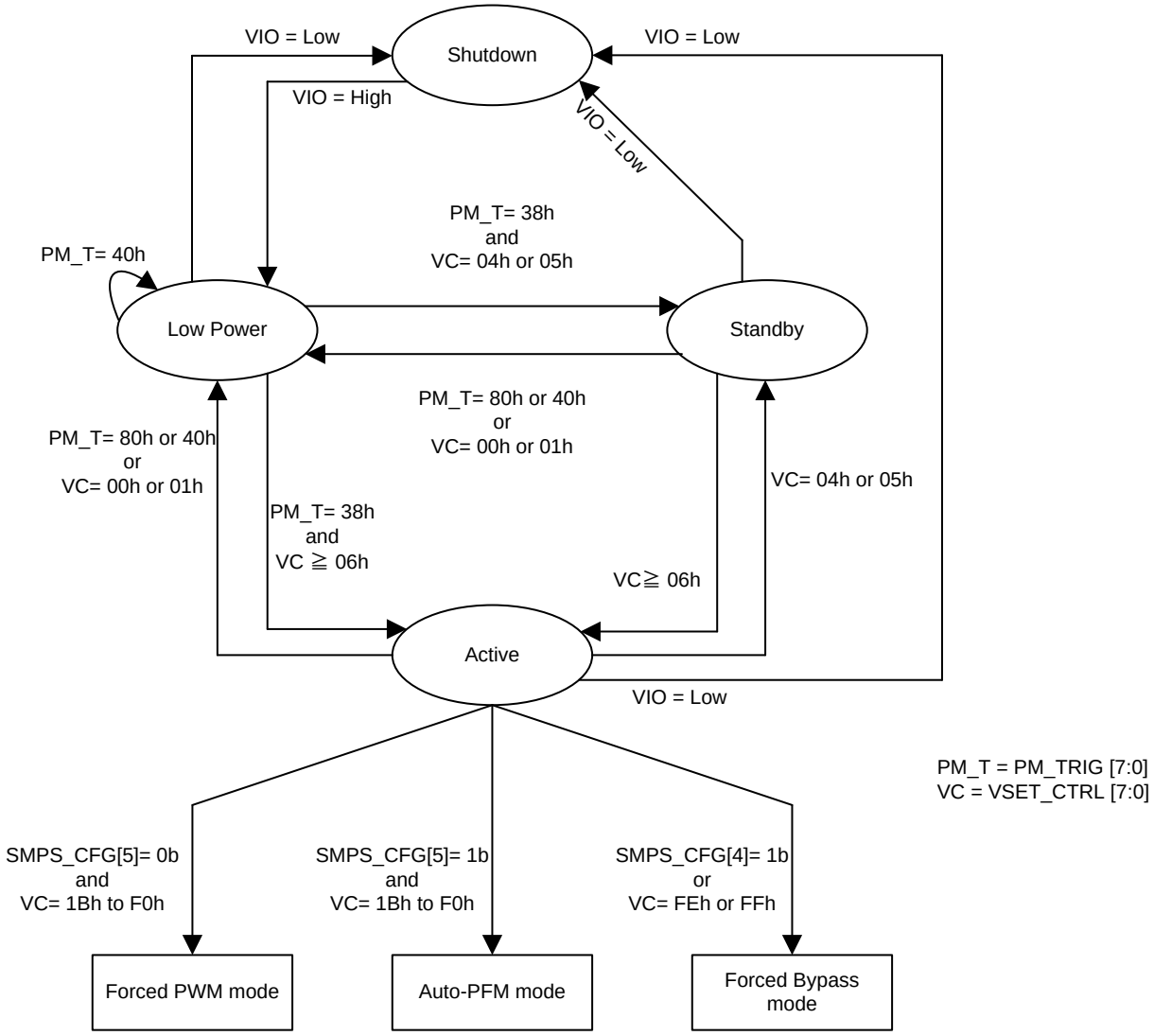
7.4.4 Active Mode

The active mode is a DC-DC converter operating mode that allows the device to function, process RFFE commands, and respond to RFFE commands. This mode can be entered by setting register 1Ch PM_TRIG [7:6] to 00b. Once the device is the active Mode, the DC-DC converter operating mode and the output voltage can be programmed by using REGISTER_0 [6:0] and VSET_CTRL[7:0] registers.

Copyright © 2013–2016, Texas Instruments Incorporated

Device Functional Modes (continued)

7.4.5 User States



Specified output voltage range is 0.4 V to 3.6 V.

Writing to and reading back from REGISTER_0 and VSET_CTRL access the same internal VSET register. Writing to VSET_CTRL programs the full 8 bits VSET value. Writing to REGISTER_0 programs 7 MSB of VSET with LSB set to zero. When REGISTER_0 is written, the internal VSET register LSB bit[0] always takes a value of 0 and subsequent read of VSET_CTRL bit[0] is read back as 0.

Figure 21. LM3263 User State Diagram

Copyright © 2013–2016, Texas Instruments Incorporated

7.5 Programming

7.5.1 RFFE Interface

The digital control serial bus interface provides MIPI RF front-end control Interface compatible access to the programmable functions and registers on the device. The LM3263 uses a three-pin digital interface: two for bidirectional communications between the IC's connected to the bus, along with an interface voltage reference VIO that also acts as asynchronous enable and reset. When VIO voltage supply is applied to the bus, it enables the Slave interface and resets the user-defined Slave registers to the default settings. The LM3263 can be set to shutdown mode via the asynchronous VIO signal or low-power mode by setting the appropriate register via the serial bus interface. The two communication lines are serial data (SDATA), and clock (SCLK). SCLK and SDATA must be held low until VIO is present. The LM3263 connects as slave on a single-master serial bus interface.

The SDATA signal is bidirectional, driven by the Master or a Slave. Data is written on the rising edge (transition from logical level zero to logical level one) of the SCLK signal by both Master and Slaves. Master and Slave both read the data on the falling edge (transition from logical level one to logical level zero) of the SCLK signal. A logic-low level applied to VIO signal powers off the digital interface.

7.5.2 Supported Command Sequences

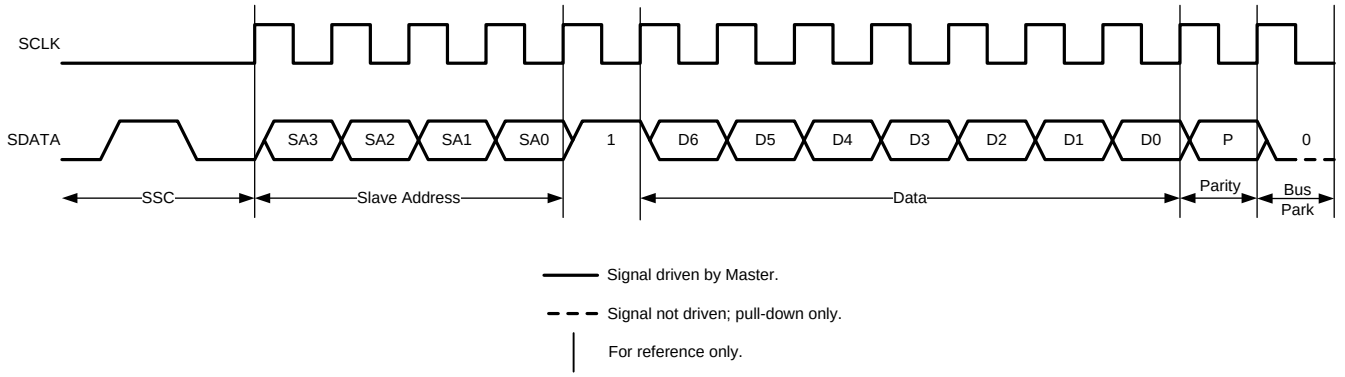


Figure 22. Register 0 Write

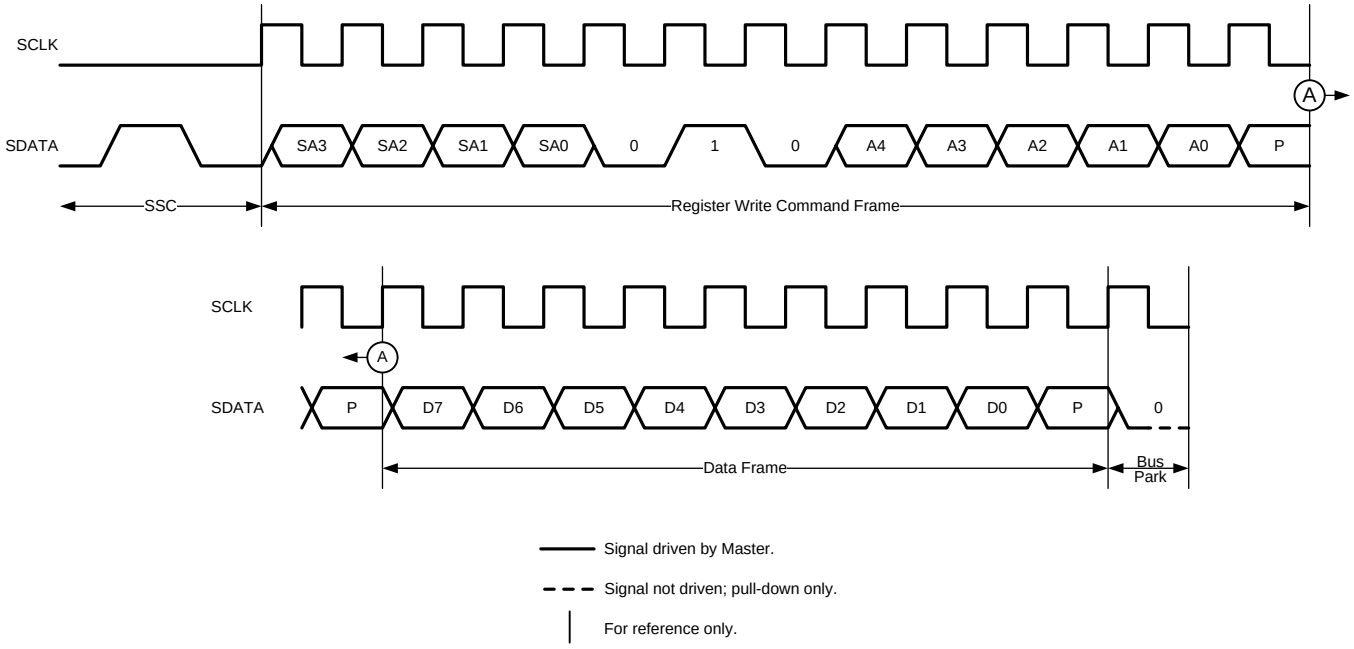


Figure 23. Register Write

Programming (continued)

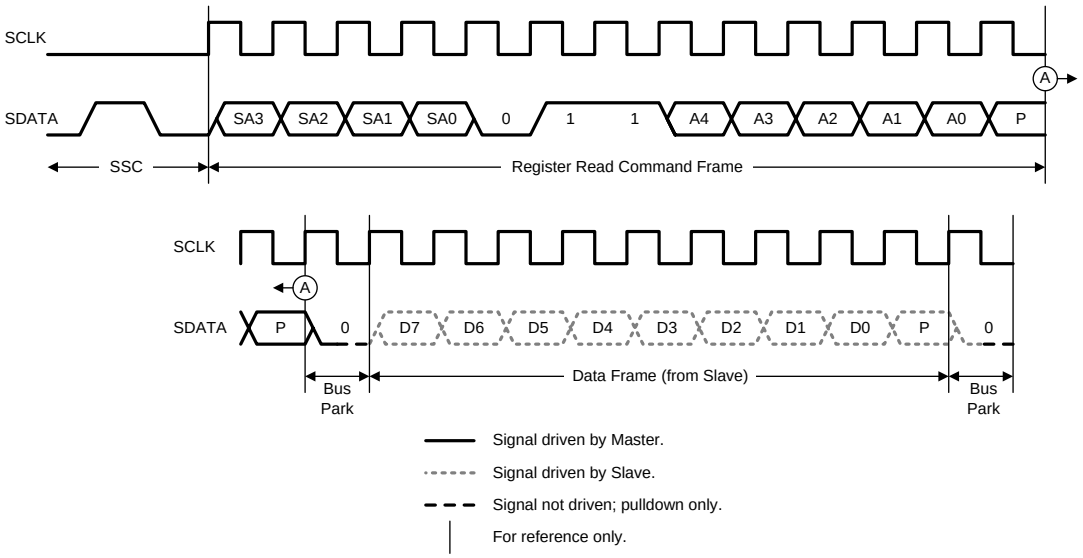


Figure 24. Register Read

7.5.3 Device Enumeration

The interface component recognizes broadcast Slave Address (SID) of 0000b and is configured, via internal interface signals, with a unique SID address (USID) and a group SID address (GSID). The USID is set to 0100b and GSID set to 0000b. The register-set component typically sets the USID to a fixed value; however, it is also possible to select a second pre-set USID if a second LM3263 device is needed on the board. This second User ID can be set by forcing a voltage > 1.36 V at the GPO1 pin for USID = 0101b. Refer to *GPO1* for detailed usage and programmability of the USID. The USID can also be re-programmed via the standard protocol for programming the RFFE as defined in the RFFE spec. The USID must not be programmed to the reserved broadcast slave id of 0000b. A value of 0000b is ignored by the device.

7.5.4 GPO1

GPO1 has two functions. The first function is an input to select the default USID, and the second function is to be a general purpose output.

The state of the GPO1 pin at start-up determines the default USID. If the GPO1 pin is low or left floating at start-up, the USID is 0100b. If the GPO1 pin is high at start-up, the USID is 0101b. One method to set the GPO1 pin high is to place a pullup resistor (39 KΩ) on the GPO1 pin.

When the GPO1 pin is used as the general purpose output, GPO_CTRL [6] must be set to 1b. Once it has been enabled as the general purpose output, GPO_CTRL [7] determines the state driven to the GPO1 pin. The pullup resistor must be placed either as an external pullup on the board or through an internal pullup on the general purpose input which is tied to the GPO1 pin.

The GPO1 pin can be left floating if unused.

7.5.5 Trigger Registers

Trigger registers are indicated in the RFFE register map by the *Trigger* column. All trigger registers are tied to each of the TRIG_0-2 register bits. When a trigger register is written directly across the RFFE interface, the new value is not loaded into the register until one of the TRIG0-2 register bits is written with a 1 and the associated TRIG_MSK_x bit for that TRIG_x is not set. (Triggers are ignored when their associated masking bit is set.) When all 3 TRIG_MSK_0-2 bits are set (all triggers are masked) the trigger feature is disabled, and any trigger registers are loaded directly at the time of the write operation to that register rather than waiting for a trigger event to update.

Copyright © 2013–2016, Texas Instruments Incorporated

Programming (continued)

7.5.6 Control Interface Timing Parameters

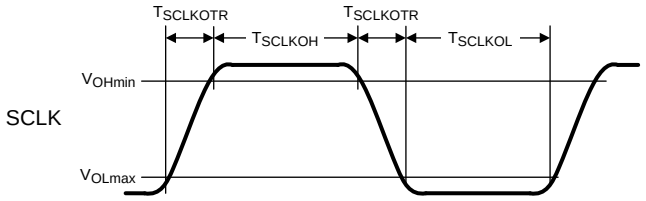


Figure 25. Clock Timing

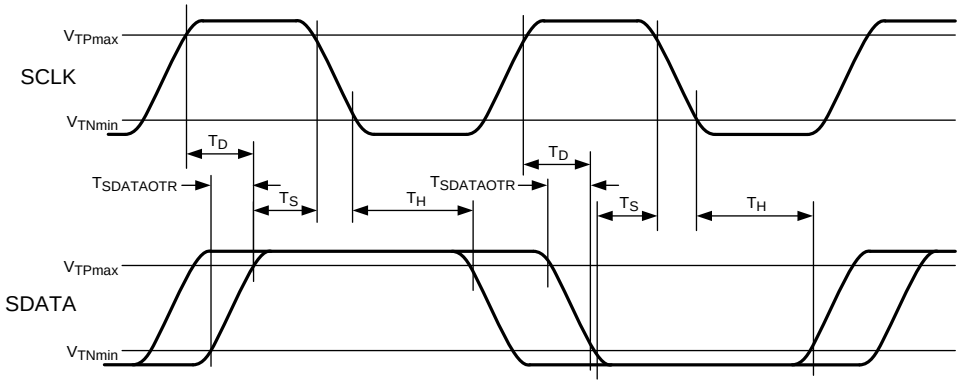


Figure 26. Setup and Hold Timing

PARAMETER		MIN	TYP	MAX	UNIT
T_{CLK}	Clock time period	38.5			ns
T_{SCLKOH}	Clock high time	11.25			ns
T_{SCLKOL}	Clock low time	11.25			ns
T_S	Data setup time	1			ns
T_H	Data hold time	5			ns
$T_{D\text{-}Forward}$	Time for data output valid from SCLK rising edge			10.25	ns
$T_{D\text{-}Reverse}$	Time for data output valid from SCLK rising edge			22	ns
$T_{SDATAOTR}$	SDATA output transition (rise/fall) time	2.1		6.5	ns

Copyright © 2013–2016, Texas Instruments Incorporated

7.6 Register Map

Addr	Register Contents					
00h	**REGISTER _0**					
	Bits	**Function**	**Default**	**Trigger***	**R/W**	**Description**
	7	RSVD	0	N/A	N/A	Reserved
	6:0	VSET[7:1]	00h	Yes	R/W	Register 00h interacts with Register 03h. DC-DC converter mode and output voltage control bits 00h : Low-power mode 01h : Reserved 02h : Standby mode 03h to 7Eh : active mode, setting output voltage is enabled. Output voltage can be set 0.4 V to 3.6 V by 0Dh to 78h with 30-mV steps 7Fh : Forced-bypass mode VSET[7:1] (dec) = Desired V_{OUT} / 0.03 (round up decimals), then converts a decimal number to hexadecimal.
01h	**SMPS_CFG**					
	Bits	**Function**	**Default**	**Trigger***	**R/W**	**Description**
	7:6	RSVD	0	N/A	N/A	Reserved
	5	MODE	0	Yes	R/W	Switching mode select bit 0: Forced-PWM mode (PWM only) 1: Auto-PFM mode (PFM/PWM)
	4	BYPS	0	Yes	R/W	Forced bypass bit 0: Auto-bypass mode 1: Forced-bypass mode
	3:0	RSVD	0h	N/A	N/A	Reserved
02h	**GPO_CTRL**					
	Bits	**Function**	**Default**	**Trigger***	**R/W**	**Description**
	7	GPO1_OUT	0	Yes	R/W	GPO1 output control 0: Low state 1: High state
	6	GPO1_MODE	0	Yes	R/W	GPO1 Mode Selection 0 : General Purpose Output disabled 1 : General Purpose output driven by GPO1_OUT
	5:0	RSVD	00h	N/A	N/A	Reserved
03h	**VSET_CTRL**					
	Bits	**Function**	**Default**	**Trigger***	**R/W**	**Description**
	7:0	VSET[7:0]	00h	Yes	R/W	DC-DC converter mode and output voltage fine control bits 00h-01h : Low-power mode 02h-03h : Reserved 04h-05h : Standby mode 06h to FDh : Active mode, setting output voltage is enabled. Output voltage can be set 0.4 V to 3.6 V by 1Bh to F0h with 15-mV steps FEh-FFh : Forced bypass mode VSET[7:0] (dec) = Desired V_{OUT} / 0.015 (round up decimals), then converts a decimal number to hexadecimal.
1Ah	**RFFE_STATUS**					
	Bits	**Function**	**Default**	**Trigger***	**R/W**	**Description**
	7	SWRESET	0	No		Software Reset. A write to 1 causes all registers except for USID to be reset. Always reads back 0.
	6	CMD_FRAME_PERR	0	No		Set if parity error detected in command frame. Cleared on read. Write has no effect on this bit.
	5	CMD_LENGTH_ERR	0	No		Error when transaction interrupted by new SSC. Cleared on read. Write has no effect on this bit.
	4	RSVD	0	No		Reserved

Copyright © 2013–2016, Texas Instruments Incorporated

Register Map (continued)

Addr	Register Contents					
	3	DATA_FRAME_PERR	0	No		Write data frame parity error. Cleared on read. Write has no effect on this bit.
	2	RD_UNUSED_REG	0	No		Read command to an invalid register. Cleared on read. Write has no effect on this bit.
	1	WR_UNUSED_REG	0	No		Write command to an invalid register. Cleared on read. Write has no effect on this bit.
	0	BID_GID_ERR	0	No		Read command with a broadcast ID or Group ID. Cleared on read. Write has no effect on this bit.
1Bh	**GROUP_ID**					
	Bits	**Function**	**Default**	**Trigger***	**R/W**	**Description**
	7:4	RSVD	0h	N/A	N/A	Reserved
	3:0	GSID	0h	No		Group slave ID
1Ch	**PM_TRIG**					
	Bits	**Function**	**Default**	**Trigger***	**R/W**	**Description**
	7:6	PWR_MODE	10b	No	R/W	Power Mode Bits. 00b = Active mode 01b = Restore default settings 10b = Low-power mode 11b = Reserved
	5	TRIG_MSK_2	0	No		Mask bit for Trigger 2. Broadcast write to this bit is ignored.
	4	TRIG_MSK_1	0	No		Mask bit for Trigger 1. Broadcast write to this bit is ignored.
	3	TRIG_MSK_0	0	No		Mask bit for Trigger 0. Broadcast write to this bit is ignored.
	2	TRIG_2	0	No		Write to a 1 loads trigger registers with last written value TRIG_MSK_2 is cleared. Write to 0 has no affect.
	1	TRIG_1	0	No		Write to a 1 loads trigger registers with last written value TRIG_MSK_1 is cleared. Write to 0 has no effect.
	0	TRIG_0	0	No		Write to a 1 loads trigger registers with last written value TRIG_MSK_0 is cleared. Write to 0 has no effect.
1Dh	**PRODUCT ID**					
	Bits	**Function**	**Default**	**Trigger***	**R/W**	**Description**
	7:0	PRODUCT_ID	82h	No	R	Product Identification Bits. Product ID default value cannot be overwritten.
1Eh	**MANUFACTURER ID, LSB**					
	Bits	**Function**	**Default**	**Trigger***	**R/W**	**Description**
	7:0	MANID[7:0]	02h	No	R	Manufacturer Identification, bits 7:0. Manufacturer ID default value cannot be overwritten.
1Fh	**MANUFACTURER ID, MSB**					
	Bits	**Function**	**Default**	**Trigger***	**R/W**	**Description**
	7:6	RSVD	00b	N/A	N/A	Reserved
	5:4	MANID[5:4]	01b	No	R	Manufacturer Identification, bits 5:4. Manufacturer ID default value cannot be overwritten.
	3:0	USID	010xb	No		Unique Slave Identifier. Bit 0 (x) of USID is tied to the state of the GPO1 pin. 0100b: GPO1= Low state or floating 0101b: GPO1= High state

* Trigger = Yes: When all PM_TRIG.TRIG_MSK_* bits are set 1, REGISTER_0 is written immediately during a write operation. If any PM_TRIG.TRIG_MSK_* bits are cleared (0), REGISTER_0 is not updated to the new value after a write operation only after an unmasked PM_TRIG.TRIG_* bit is subsequently written to a 1.

Copyright © 2013–2016, Texas Instruments Incorporated

8 Application Information

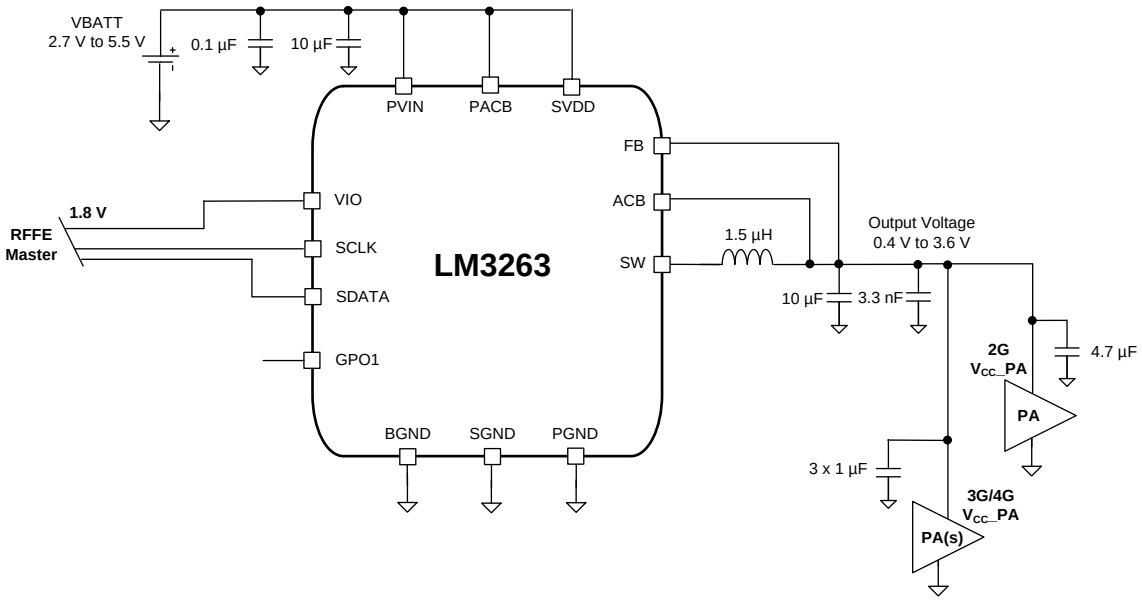
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM3262 DC-DC converter steps down an input voltage from 2.7 V to 5.5 V to a dynamically adjustable output voltage of 0.4 V to 3.6 V.

8.2 Typical Application



Copyright © 2016, Texas Instruments Incorporated

Figure 27. LM3263 Typical Application

8.2.1 Design Requirements

For typical DC-DC converter applications use the parameters listed in Table 2.

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	2.7 V to 5.5 V
Output voltage range	0.4 V to 3.6 V
Output current	1 A
Minimum effective output capacitance (including effects of AC bias, DC bias, temperature)	10 µF

Copyright © 2013–2016, Texas Instruments Incorporated

8.2.2 Detailed Design Procedure

8.2.2.1 Recommended External Components

8.2.2.1.1 Inductor Selection

A 1.5-µH inductor is needed for optimum performance and functionality of the LM3263. In the case of 2G transmission current bursts, the effective overall RMS current requirements are reduced. Therefore, consult with the inductor manufacturers to determine if some of their smaller components are suitable even if the inductor specification does not appear to meet the LM3263 RMS current specifications.

The LM3263 automatically manages the inductor peak and RMS current (or steady-state current peak) through the SW pin. The SW pin has two positive current limits. The first is the 1.45-A typical (or 1.65-A maximum) overcurrent protection. It sets the upper steady-state inductor peak current (as detailed in *Electrical Characteristics* $I_{LIM,PFET,SteadyState}$). It is the dominant factor limiting the inductors I_{SAT} requirement. The second is an over-limit current protection. It limits the maximum peak inductor current during large signal transients (for example, < 20 µs) to 1.9 A typical (or 2.1 A maximum). A minimum inductance of 0.3 µH must be maintained at the second current limit.

The ACB circuit automatically adjusts its output current to keep the steady-state inductor current below the steady-state peak current limit. Thus, the inductor RMS current is always effectively than the $I_{LIM,PFET,SteadyState}$ during the transmit burst. In addition, as in the case with 2G where the output current comes in bursts, the effective overall RMS current would be much lower.

For good efficiency, resistance of the inductor must be less than 0.2 Ω; TI recommends low-DCR inductors (< 0.2 Ω). Table 3 suggests some inductors and their suppliers.

Table 3. Suggested Inductors And Their Suppliers

MODEL	VENDOR	DIMENSIONS	I_{SAT} (30% DROP IN INDUCTANCE)	DCR
DFE201610C1R5N (1285AS-H-1R5M)	TOKO	2 mm × 1.6 mm × 1 mm	2.2 A	120 mΩ
LQM2MPN1R5MGH	Murata	2 mm × 1.6 mm × 1 mm	2 A	104 mΩ
MAKK2016T1R5M	Taiyo-Yuden	2 mm × 1.6 mm × 1 mm	1.9 A	115 mΩ
VLS201610MT-1R5N	TDK	2 mm × 1.6 mm × 1 mm	1.4 A	151 mΩ
LQM21PN1R5MGH	Murata	2 mm × 1.25 mm × 1 mm	1.2 A	110 mΩ

8.2.2.1.2 Capacitor Selection

The LM3263 is designed to use ceramic capacitors for its input and output filters. Use a 10-µF capacitor for the input and approximately 10 µF actual total output capacitance. Capacitor types such as X5R, X7R are recommended for both filters. These provide an optimal balance between small size, cost, reliability, and performance for cell phones and similar applications. Table 4 lists suggested part numbers and suppliers. DC bias characteristics of the capacitors must be considered while selecting the voltage rating and case size of the capacitor. Smaller case sizes for the output capacitor mitigate piezo-electric vibrations of the capacitor when the output voltage is stepped up and down at fast rates. However, they have a bigger percentage drop in value with dc bias. For even smaller total solution size, 0402 (1005) case size capacitors are recommended for filtering. Use of multiple 2.2-µF or 1-µF capacitors can also be considered. For RF PA applications, split the output capacitor between DC-DC converter and RF PAs; TI recomments 10 µF (C_{OUT1}) + 4.7 µF (C_{OUT2}) + 3 × 1 µF (C_{OUT3})(assuming one 2G PA and three 3G/4G PAs — C_{OUT2} is for 2G PA, and C_{OUT3} is for 3G/4G PA). The optimum capacitance split is application dependent, and for stability the actual total capacitance (taking into account effects of capacitor DC bias, temperature de-rating, aging and other capacitor tolerances) must target 10 µF with 2.5-V DC bias (measured at 0.5 V_{RMS}). Place all the output capacitors very close to the respective device. TI highly recommends placing a high-frequency capacitor (3300 pF) next to C_{OUT1}.

Copyright © 2013–2016, Texas Instruments Incorporated

Table 4. Suggested Capacitors And Their Suppliers

CAPACITANCE	MODEL	SIZE (W × L)	VENDOR
10 µF	GRM185R60J106M	1.6 mm × 0.8 mm	Murata
10 µF	CL05A106MP5NUN	1 mm × 0.5 mm	Samsung
4.7 µF	CL05A475MP5NRN	1 mm × 0.5 mm	Samsung
1 µF	CL03A105MP3CSN	0.6 mm × 0.3 mm	Samsung
1 µF	C0603X5R0J105M	0.6 mm × 0.3 mm	TDK
3300 pF	GRM022R60J332K	0.4 mm × 0.2 mm	Murata

8.2.3 Application Curves

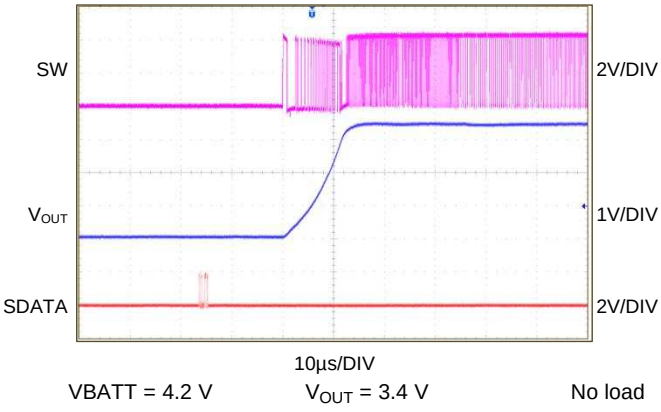


Figure 28. Start-up From Low-Power Mode

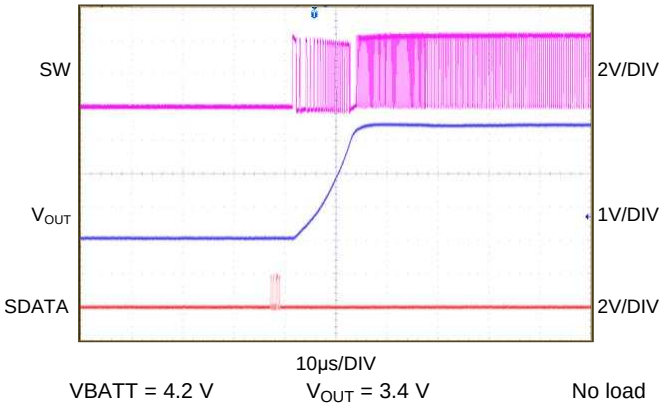


Figure 29. Start-Up From Standby Mode

9 Power Supply Recommendations

The LM3263 device is designed to operate from an input voltage supply range from 2.7 V to 5.5 V. This input supply should be well-regulated and able to withstand maximum input current and maintain stable voltage without voltage drop even under largest load transition conditions.

Copyright © 2013–2016, Texas Instruments Incorporated

10 Layout Considerations

10.1 Layout Guidelines

10.1.1 1. Overview

PC board layout is critical to successfully designing a DC-DC converter into a product. A properly planned board layout optimizes the performance of a DC-DC converter and minimizes effects on surrounding circuitry while also addressing manufacturing issues that can have adverse impacts on board quality and final product yield.

10.1.2 2. PCB

Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces. Erroneous signals could be sent to the DC-DC converter device, resulting in poor regulation or instability. Poor layout can also result in re-flow problems leading to poor solder joints between the DSBGA package and board pads. Poor solder joints can result in erratic or degraded performance of the converter.

10.1.2.1 Energy Efficiency

Minimize resistive losses by using wide traces between the power components and doubling up traces on multiple layers when possible.

10.1.2.2 EMI

By its very nature, any switching converter generates electrical noise. The circuit board designer's challenge is to minimize, contain, or attenuate such switcher-generated noise. A high-frequency switching converter, such as the LM3263, switches Ampere level currents within nanoseconds, and the traces interconnecting the associated components can act as radiating antennas. The following guidelines are offered to help to ensure that EMI is maintained within tolerable levels.

To help minimize radiated noise:

- Place the LM3263 DC-DC converter, its input capacitor, and output filter inductor and capacitor close together, and make the interconnecting traces as short as possible.
- Arrange the components so that the switching current loops curl in the same direction. During the first half of each cycle, current flows from the input filter capacitor, through the internal PFET of the LM3263 and the inductor, to the output filter capacitor, then back through ground, forming a current loop. In the second half of each cycle, current is pulled up from ground, through the internal synchronous NFET of the LM3263 by the inductor, to the output filter capacitor and then back through ground, forming a second current loop. Routing these loops so the current curls in the same direction prevents magnetic field reversal between the two half-cycles and reduces radiated noise.
- Make the current loop area(s) as small as possible. Interleave doubled traces with ground planes or return paths, where possible, to further minimize trace inductances.
- The Active Current Assist and Bypass (ACB) trace must be kept short and routed directly from ACB pads to the VOUT pad at the inductor.

To help minimize conducted noise in the ground-plane:

- Reduce the amount of switching current that circulates through the ground plane — connect PGND bump of the LM3263 and its input filter capacitor together using generous component-side copper fill as a pseudo-ground plane. Then connect this copper fill to the system ground-plane (if one is used) by multiple vias located at the input filter capacitor ground terminal. The multiple vias help to minimize ground bounce at the LM3263 by giving it a low-impedance ground connection. Do not route the PGND pad directly to the RF ground plane.
- An additional high frequency capacitor in 01005 (0402 mm) case size is also recommended between PVIN and the RF ground plane. Do not connect to PGND directly.
- For optimum RF performance connect the output capacitor ground to the RF ground or system ground plane. Do not connect to PGND directly.

Copyright © 2013–2016, Texas Instruments Incorporated

Layout Guidelines (continued)

To help minimize coupling to the voltage feedback trace of the DC-DC converter:

- Route noise sensitive traces, such as the voltage feedback path (FB), as directly as possible from the DC-DC converter FB pad to the VOUT pad of the output capacitor, but keep them away from noisy traces between the power components.

To help minimize noise coupled back into power supplies:

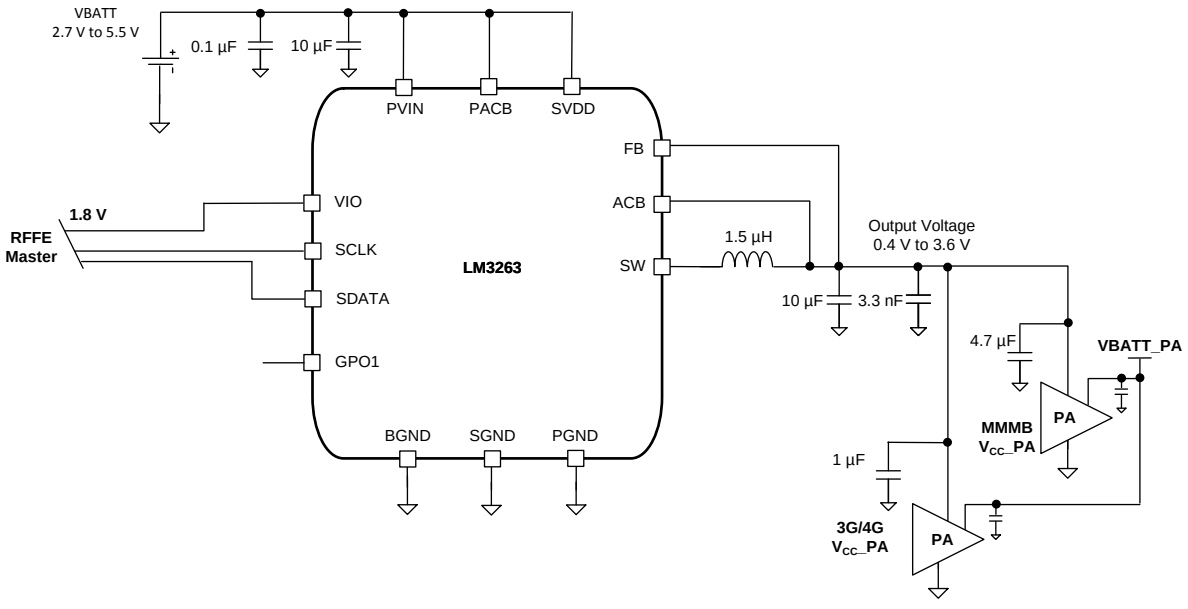
- Use a star connection to route from the VBATT power input to DC-DC converter PVIN and to VBATT_PA.
- Route traces for minimum inductance between PVIN pads and the input capacitor(s).
- Route traces to minimize inductance between the input capacitors and the ground plane.
- Maximize power supply trace inductance(s) to reduce coupling among function blocks.
- Inserting a ferrite bead in line with power supply traces can offer a favorable tradeoff in terms of board area, by attenuating noise that might otherwise propagate through the supply connections, allowing the use of fewer bypass capacitors.

10.1.3 3. Manufacturing Considerations

The LM3263 device is packaged in a 16-pin (4 × 4) array of 0.24-mm solder balls, with a 0.4-mm pad pitch. A few simple design rules go a long way to ensuring a good layout.

- Pad size must be 0.225 ± 0.02 mm. Solder mask opening must be 0.325 ± 0.02 mm.
- As a thermal relief, connect to each pad with 9-mil wide, 6-mil long traces and incrementally increase each trace to its optimal width. Symmetry is important to ensure the solder bumps re-flow evenly. Refer to*AN-1112 DSBGA Wafer Level Chip Scale Package* (SNVA009).

10.2 4. Layout Examples



Copyright © 2016, Texas Instruments Incorporated

Figure 30. Simplified LM3263 RF Evaluation Board Schematic

Copyright © 2013–2016, Texas Instruments Incorporated

4. Layout Examples (continued)

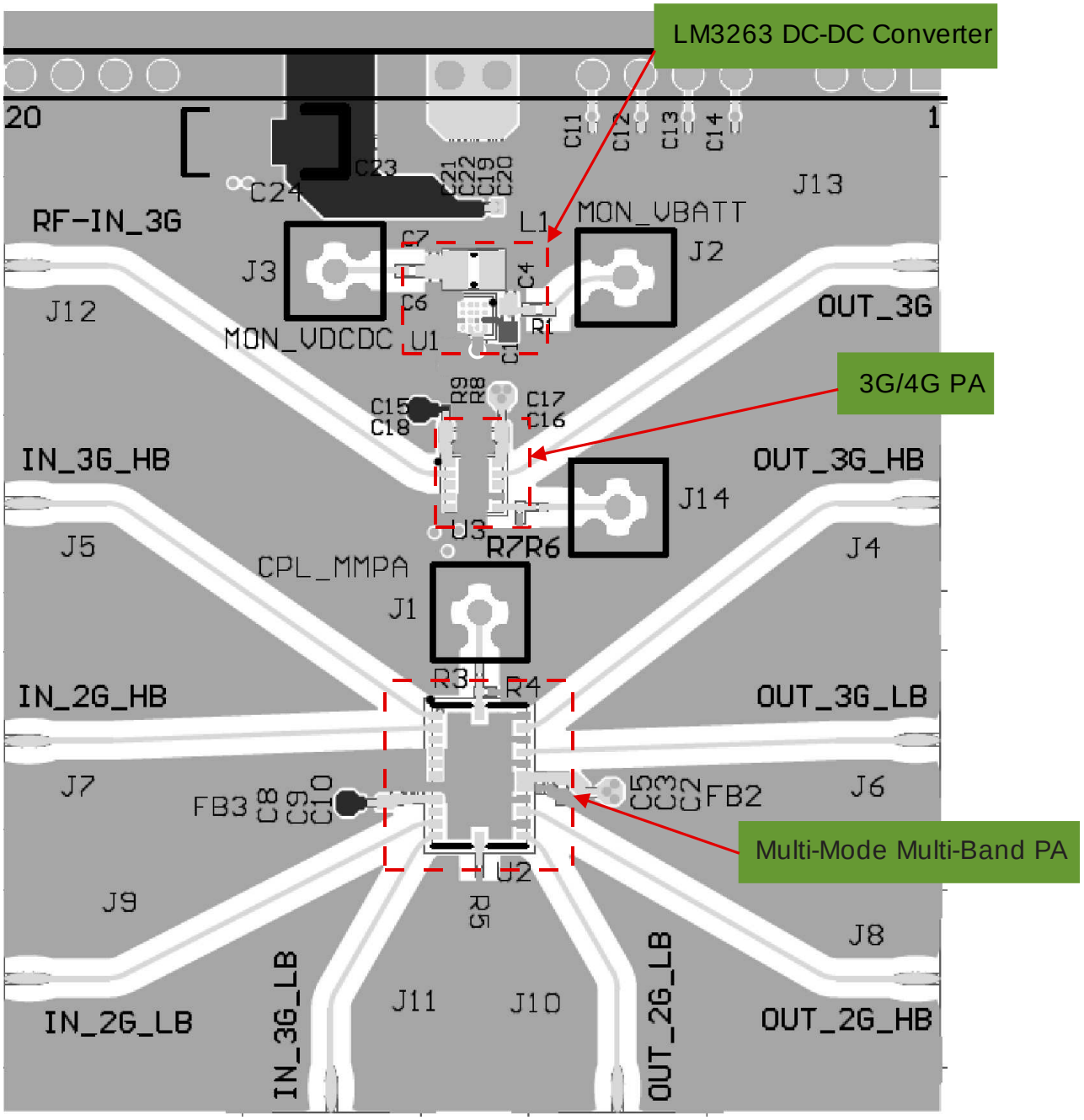


Figure 31. Top View of RF Evaluation Board With PAs

4. Layout Examples (continued)

10.2.1 DC-DC Converter

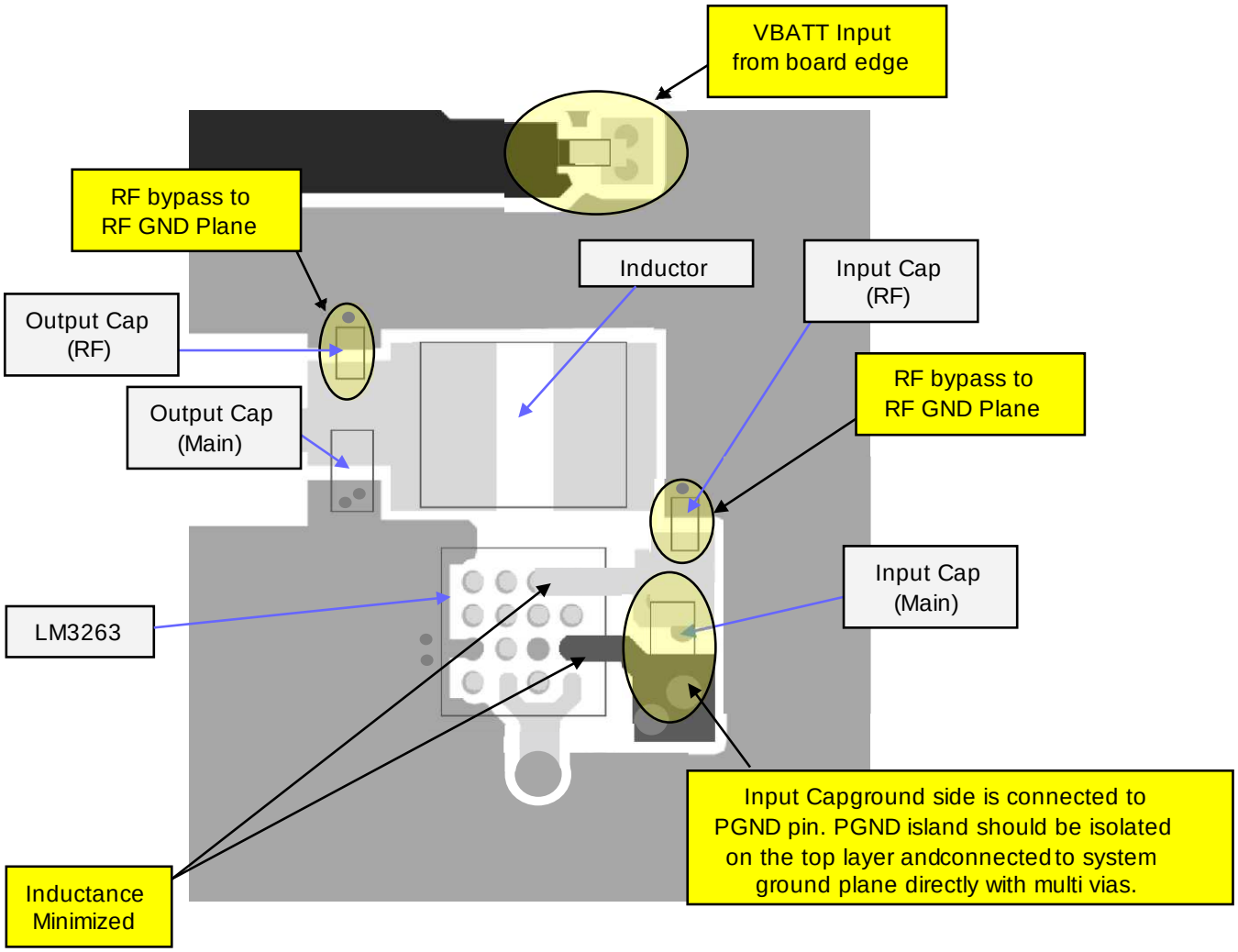


Figure 32. Top Layer

Copyright © 2013–2016, Texas Instruments Incorporated

4. Layout Examples (continued)

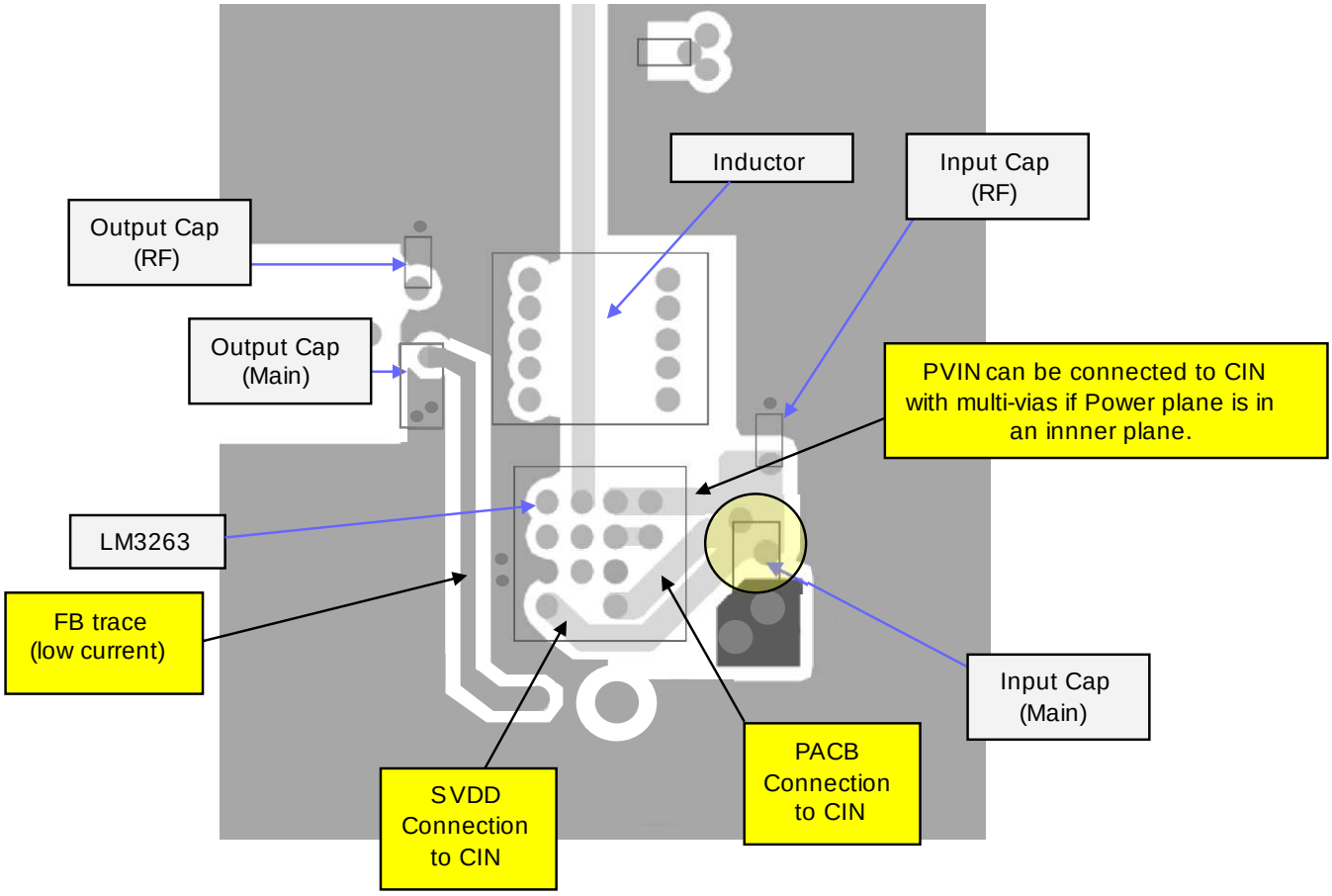


Figure 33. Board Layer 2 – FB, SVDD, PACB, PVIN

4. Layout Examples (continued)

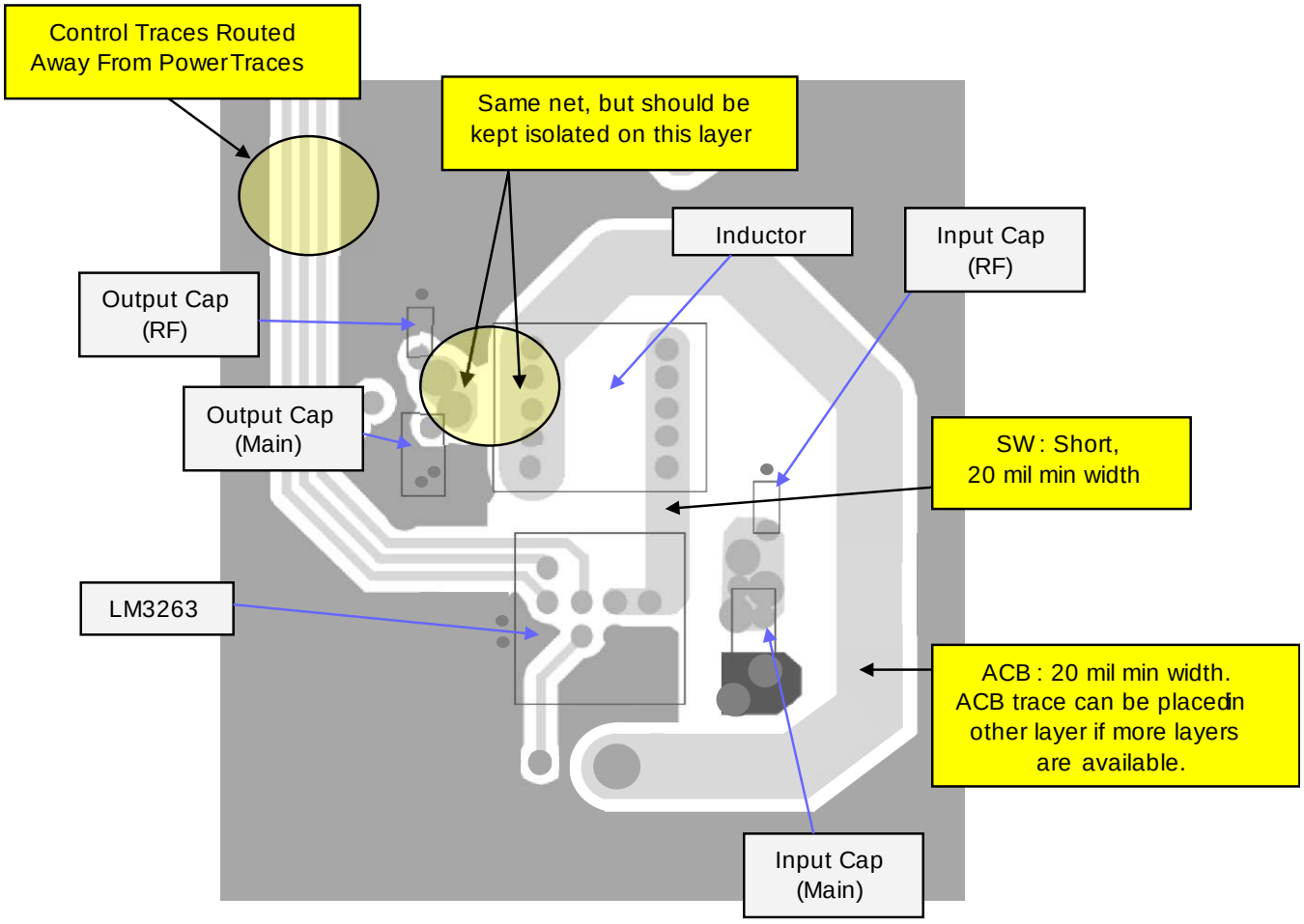


Figure 34. Board Layer 3 – SW, ACB

Copyright © 2013–2016, Texas Instruments Incorporated

4. Layout Examples (continued)

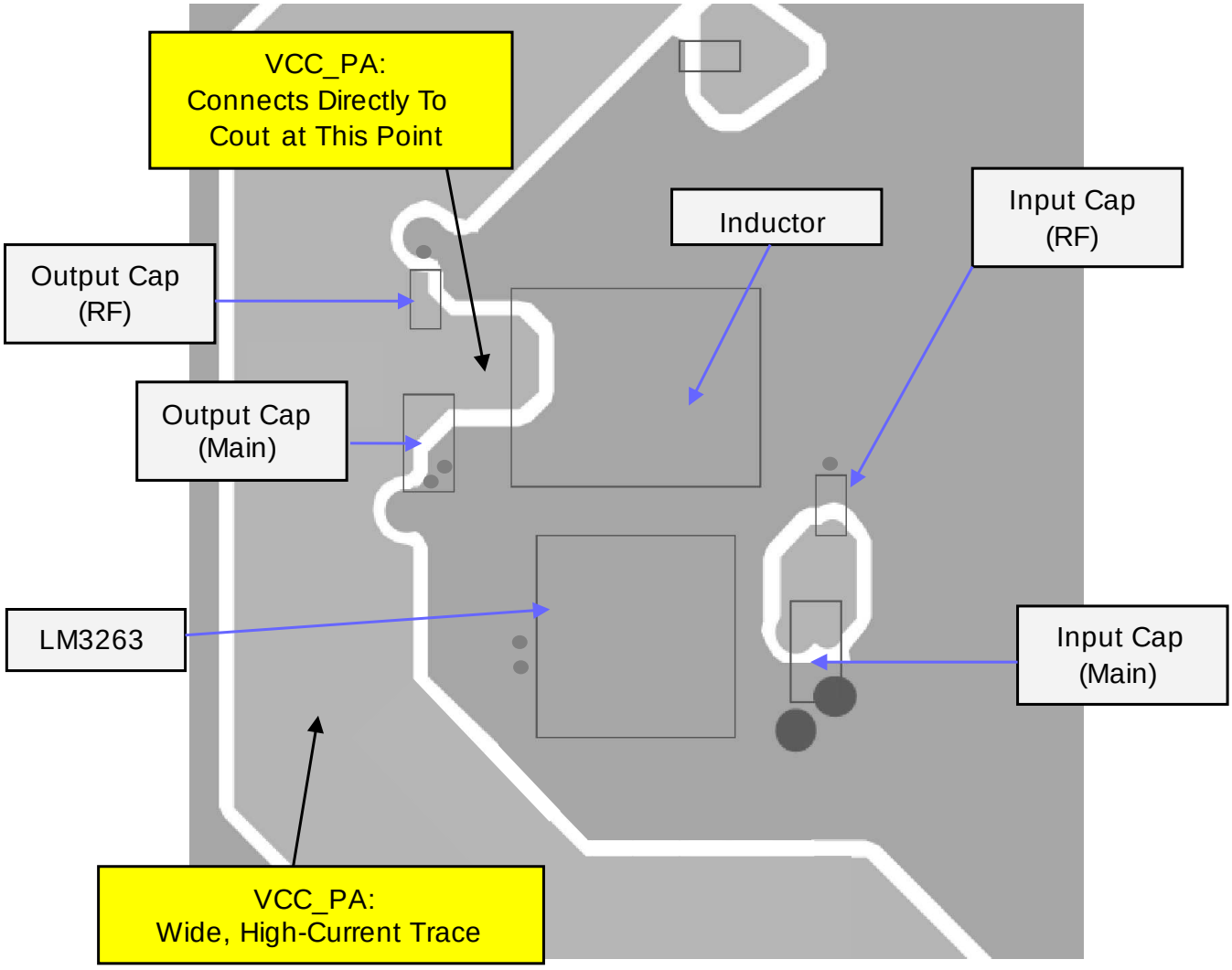


Figure 35. Board Layer 4 – VCC_PA, System GND Plane

4. Layout Examples (continued)

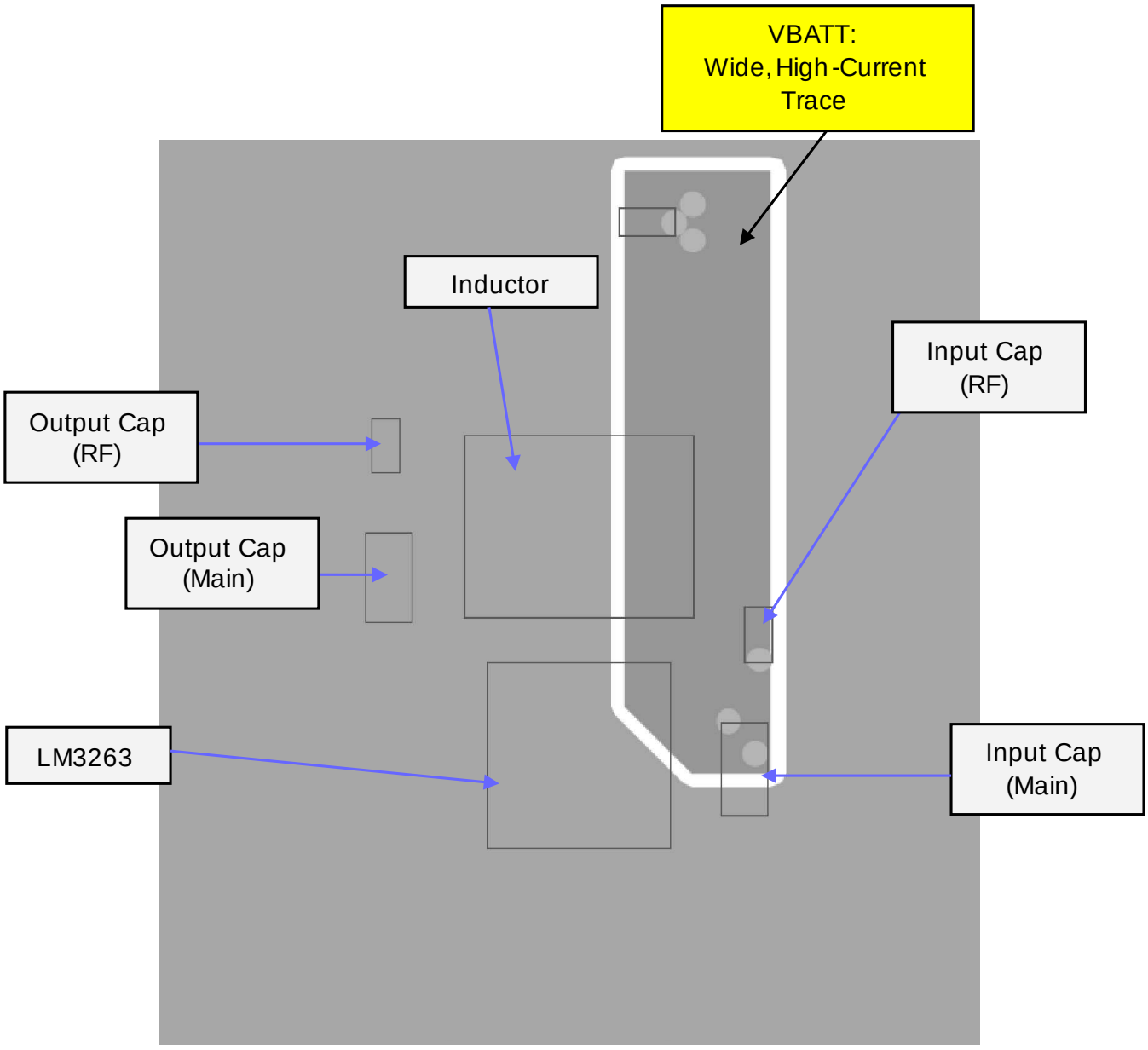


Figure 36. Board Layer 5 – VBATT Connection

Copyright © 2013–2016, Texas Instruments Incorporated

4. Layout Examples (continued)

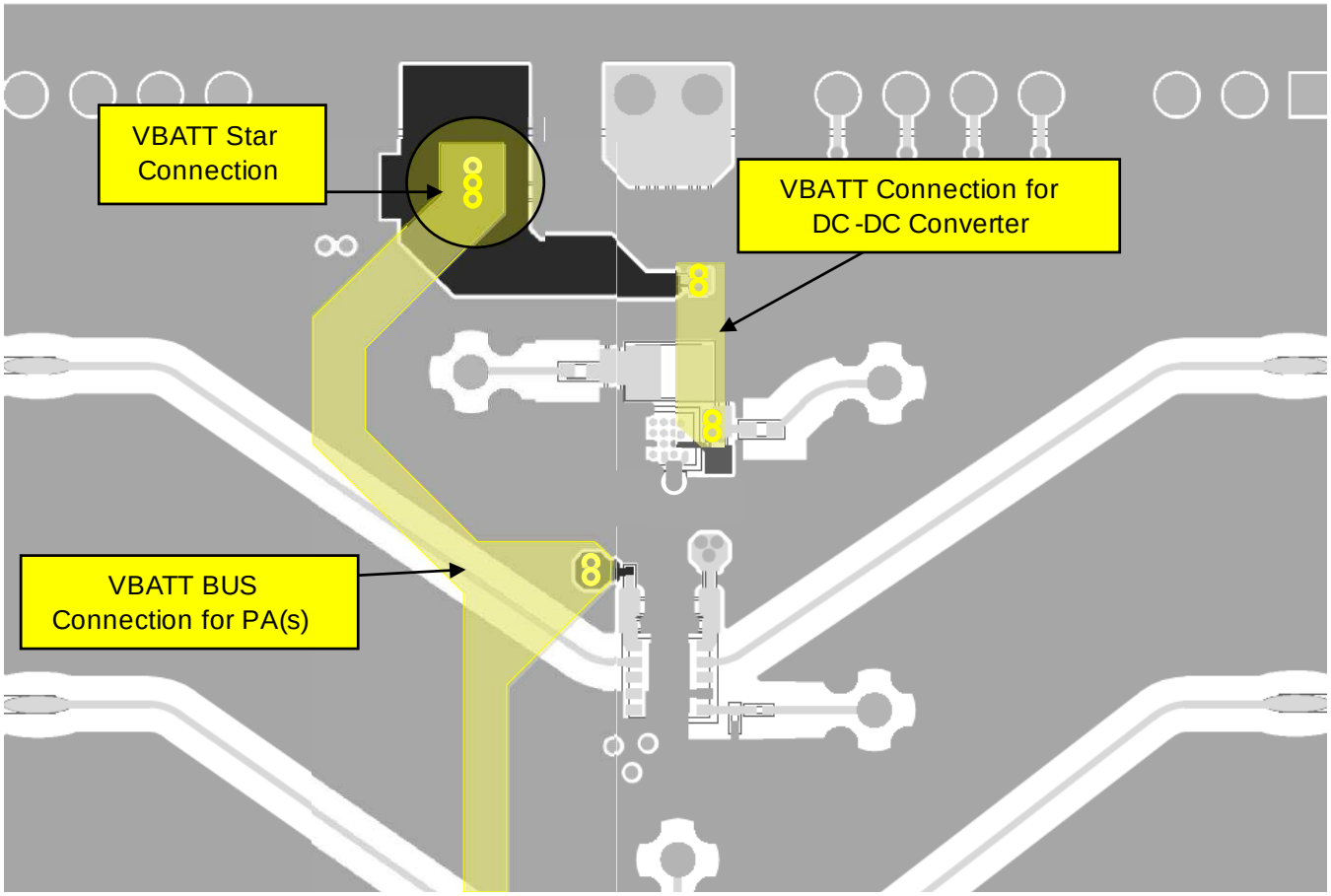


Figure 37. Multiple Board Layers – VBATT Supply Star Connection

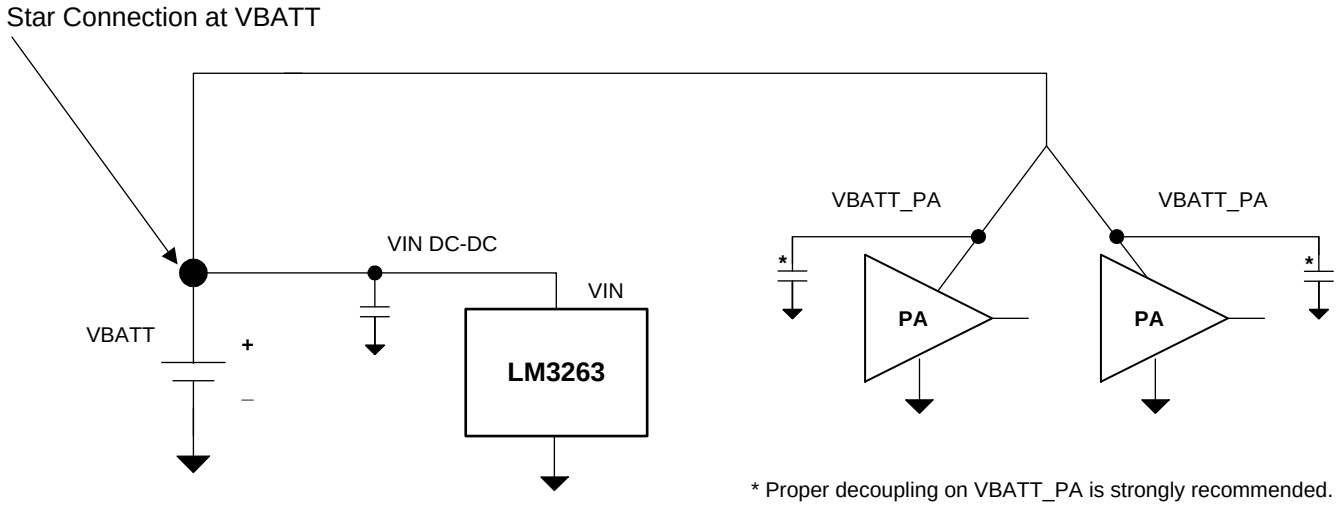
10.2.1.1 Star Connection Between VBATT, DC-DC Converter, and PA

10.2.1.1.1 VBATT Star Connection

It is critically important to use a star connection from VBATT supply to the LM3263 PVIN and from VBATT to PA modules as implementing a *daisy-chain* supply connection may add noise to the PA output.

Copyright © 2013–2016, Texas Instruments Incorporated

4. Layout Examples (continued)



Copyright © 2016, Texas Instruments Incorporated

Figure 38. VBATT Star Connection on PCIN and VBATT_PA

10.3 DSBGA Package Assembly and Use

Use of the DSBGA package requires specialized board layout, precision mounting, and careful re-flow techniques, as detailed in *AN-1112 DSBGA Wafer Level Chip Scale Package* (SNVA009). Refer to the section *Surface Mount Technology (SMD) Assembly Considerations*. For best results in assembly, alignment ordinals on the PC board must be used to facilitate placement of the device. The pad style used with DSBGA package must be the NSMD (non-solder mask defined) type. This means that the solder-mask opening is larger than the pad size. This prevents a lip that otherwise forms if the solder-mask and pad overlap from holding the device off the surface of the board and interfering with mounting. See SNVA009 for specific instructions how to do this.

The 16-pin package used for the LM3263 has 265 micron (nominal) solder balls and requires 0.225-mm pads for mounting the circuit board. The trace to each pad must enter the pad with a 90° entry angle to prevent debris from being caught in deep corners. Initially, the trace to each pad must be about 0.142-mm wide, for a section approximately 0.127-mm long, as a thermal relief. Then each trace must neck up or down to its optimal width.

An important criterion is symmetry to insure the solder bumps on the LM3263 re-flow evenly and that the device solders level to the board. In particular, special attention must be paid to the pads for bumps A1, A3, B1, and B3 because PGND, PVIN and BGND are typically connected to large copper planes; inadequate thermal relief can result in inadequate re-flow of these bumps.

The DSBGA package is optimized for the smallest possible size in applications with red-opaque or infrared-opaque cases. Because the DSBGA package lacks the plastic encapsulation characteristic of larger devices, it is vulnerable to light. Backside metallization and/or epoxy coating, along with front-side shading by the printed circuit board, reduce this sensitivity. However, the package has exposed die edges that are sensitive to light in the red and infrared range shining on the exposed die edges of the package.

Copyright © 2013–2016, Texas Instruments Incorporated

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.2 Documentation Support

11.2.1 Related Documentation

For additional information, see the following:

AN-1112 DSBGA Wafer Level Chip Scale Package (SNVA009)

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
MIPI is a registered trademark of Mobile Industry Processor Interface Alliance.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Copyright © 2013–2016, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM3263TME/NOPB	ACTIVE	DSBGA	YFQ	16	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-30 to 90	S61	Samples
LM3263TMX/NOPB	ACTIVE	DSBGA	YFQ	16	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-30 to 90	S61	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

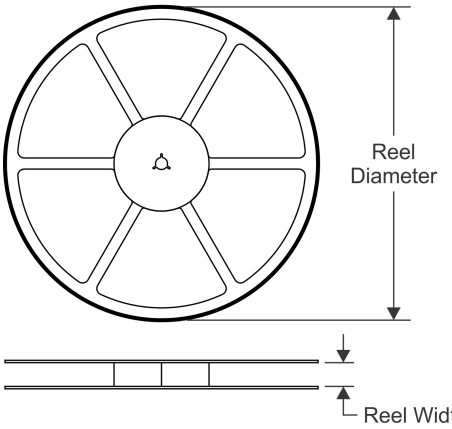
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

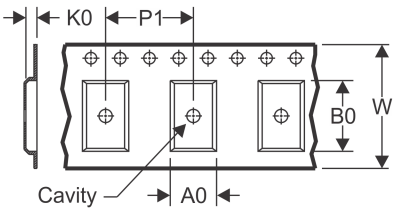
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

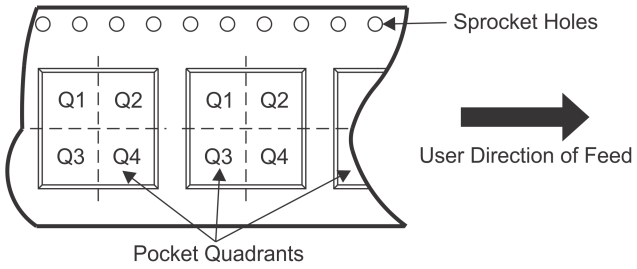


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

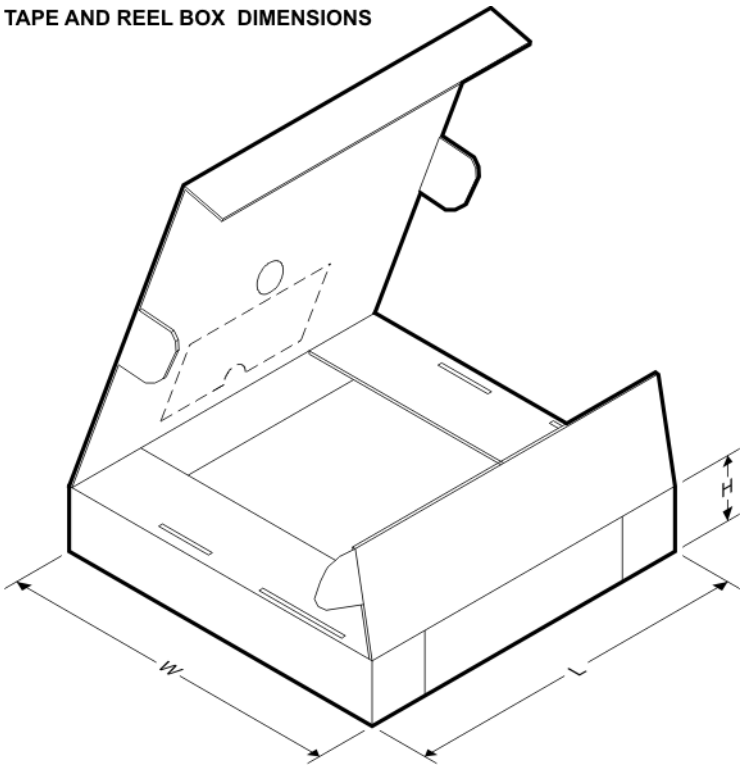
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3263TME/NOPB	DSBGA	YFQ	16	250	178.0	8.4	2.08	2.08	0.76	4.0	8.0	Q1
LM3263TMX/NOPB	DSBGA	YFQ	16	3000	178.0	8.4	2.08	2.08	0.76	4.0	8.0	Q1

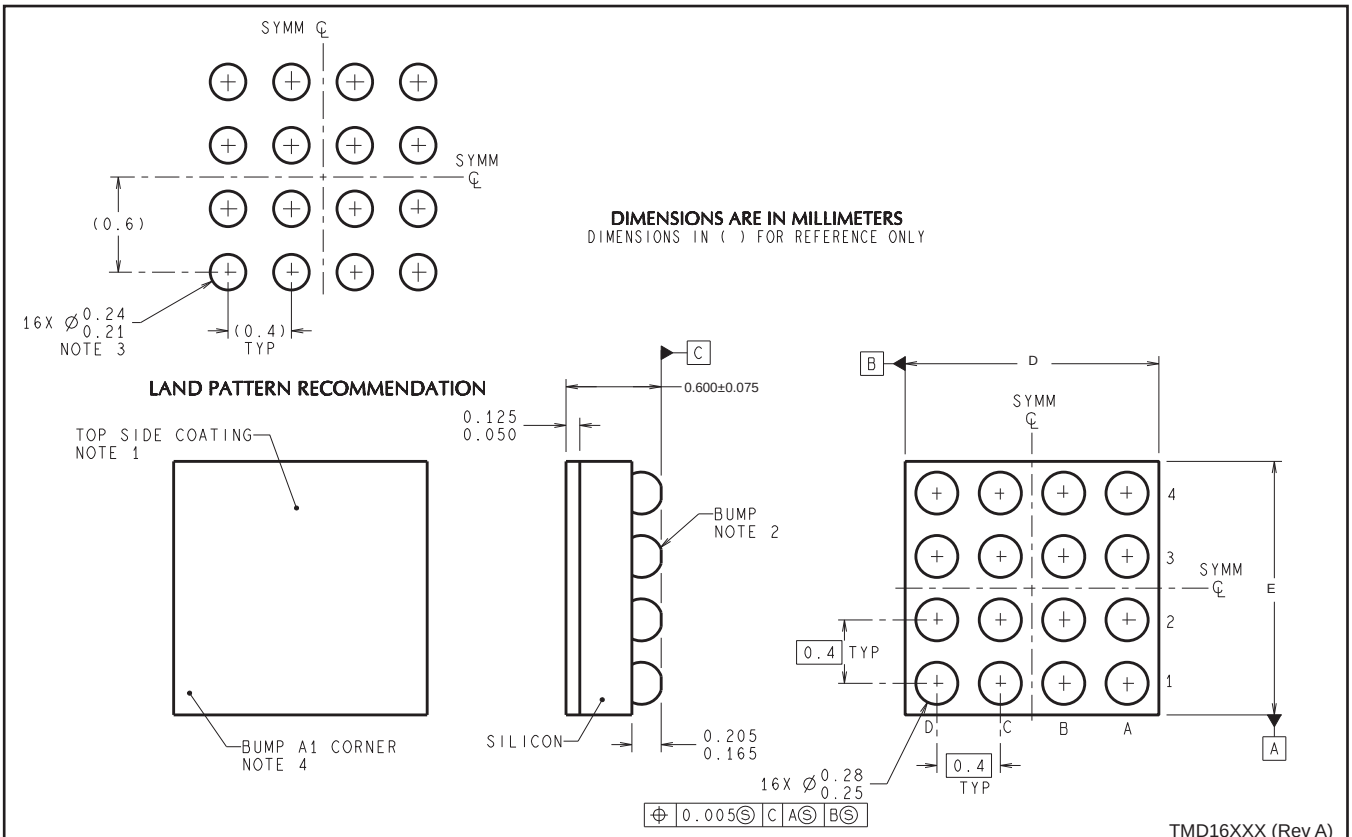
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3263TME/NOPB	DSBGA	YFQ	16	250	210.0	185.0	35.0
LM3263TMX/NOPB	DSBGA	YFQ	16	3000	210.0	185.0	35.0

YFQ0016



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2019, Texas Instruments Incorporated