# TJA1085

## FlexRay active star coupler

Rev. 2 — 7 March 2016 Product data sheet

## 1. General description

The TJA1085 is a FlexRay active star coupler that can connect up to 4 branches of a FlexRay network. The TJA1085 is compliant with the FlexRay electrical physical layer specification V3.0.1/ISO17458-4 (see Ref. 1 and Ref. 2).

Several TJA1085 devices can be connected via their TRXD0/1 interfaces to increase the number of branches in the network. A dedicated Communication Controller (CC) interface allows for integration into an ECU. The TJA1085 supports low-power management by offering bus wake-up capability along with battery supply and voltage regulator control. The TJA1085 meets industry standards for EMC/ESD performance and provides enhanced bus error detection, low current consumption and unmatched asymmetric delay performance.

The TJA1085 also fulfills the JASPAR requirements as defined by the Japanese car industry.

## 2. Features and benefits

### 2.1 General

- Compliant with FlexRay Electrical Physical Layer specification V3.0.1/ISO17458-4
- Fulfills JASPAR requirements
- Automotive product qualification in accordance with AEC-Q100
- Data transfer rates from 2.5 Mbit/s to 10 Mbit/s
- Supports 60 ns minimum bit time at 400 mV differential voltage
- Low-power management for battery-supplied ECUs
- Very low current consumption in AS_Sleep mode
- Leadless HVQFN44 package with improved Automated Optical Inspection (AOI) capability

### 2.2 Functional

- Supports autonomous active star operation independent of the host ensuring the TJA1085 remains active even if the host fails or is switched off
- Branches can be independently configured
- Branch extension via TRXD0/1 inner star interface
- 16-bit bidirectional SPI interface up to 2 Mbit/s for host communication
- Full host control over branch status
- Enhanced wake-up capability:
  - Remote wake-up via wake-up pattern and dedicated FlexRay data frames

- Local wake-up via pin LWU
- Wake-up source recognition
- configurable per branch

- Enhanced supply voltage monitoring on $V_{IO}$, $V_{CC}$, $V_{BUF}$ and $V_{BAT}$
- Auto I/O level adaptation to host controller supply voltage $V_{IO}$
- Can be used in 14 V, 24 V and 48 V powered systems
- Enhanced bus error detection - detects short-circuit conditions on the bus
- Instant transmitter shut-down interface (BGE pin)
- Selective branch shut-down (partial networking)

### 2.3 Robustness

- Bus pins protected against ±8 kV ESD pulses according to HBM and ±6 kV ESD pulses according to IEC61000-4-2
- All pins protected against ±1000 V ESD according to CDM
- All pins protected against ±200 V ESD according to MM
- No reverse currents from the digital input pins to $V_{IO}$ or $V_{CC}$ when the TJA1085 is not powered up
- Bus pins short-circuit proof to battery voltage (14 V, 24 V or 48 V) and ground
- Overtemperature detection and protection
- Bus pins protected against transients in automotive environment (according to ISO 7637 class C)

### 2.4 Active star functional classes

- Active star - communication controller interface
- Active star - bus guardian interface
- Active star - voltage regulator control
- Active star - logic level adaptation
- Active star - host interface
- Active star - increased voltage amplitude transmitter

## 3. Ordering information

**Table 1. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| TJA1085HN | HVQFN44 | plastic thermal enhanced very thin quad flat package; no leads; 44 terminals; body 9 × 9 × 0.85 mm | SOT1113-1 |


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# 4. Block diagram

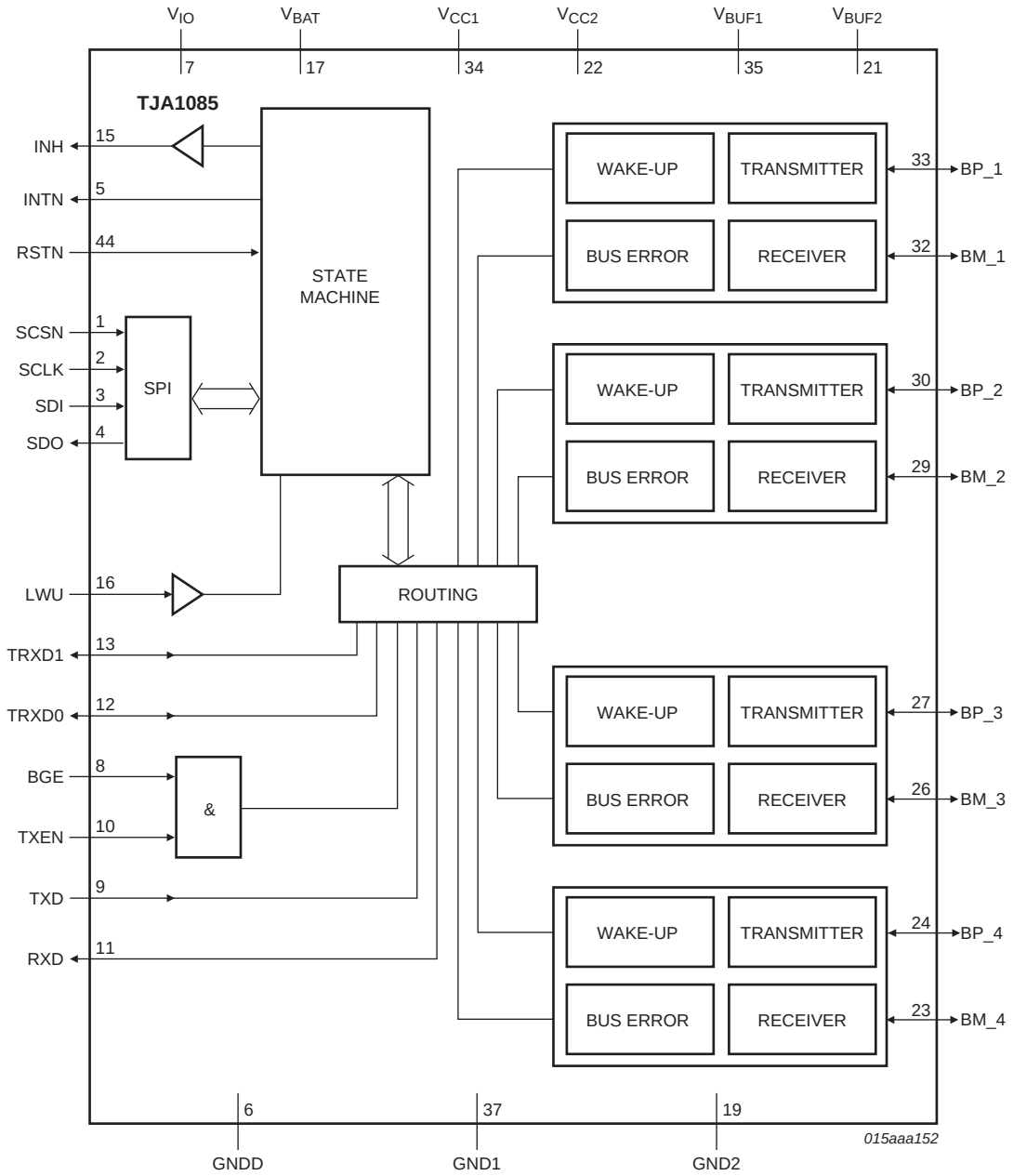


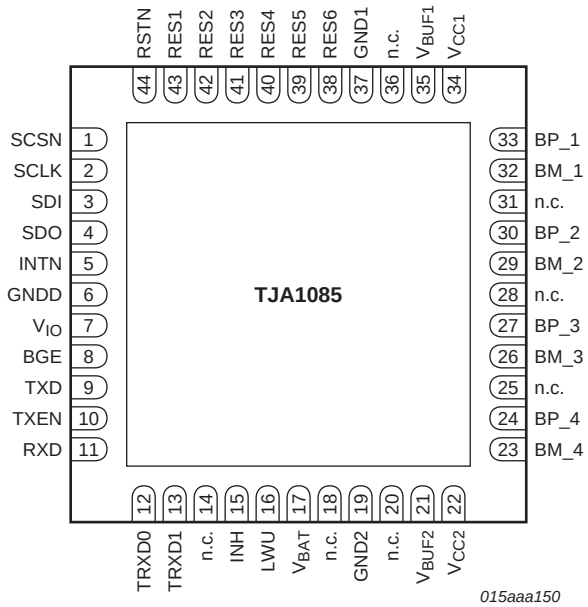

**Fig 1. Block diagram**


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# 5. Pinning information

## 5.1 Pinning




Transparent top view

**Fig 2. Pin configuration**

## 5.2 Pin description

**Table 2. Pin description**

| Symbol | Pin | Type[1] | Description |
|---|---|---|---|
| SCSN | 1 | I | SPI chip select input; internal pull-up |
| SCLK | 2 | I | SPI clock signal; internal pull-down |
| SDI | 3 | I | SPI data input; internal pull-down |
| SDO | 4 | O | SPI data output; 3-state output |
| INTN | 5 | O | interrupt output; open-drain output, low-side driver |
| GNDD | 6 | G | ground for digital circuits[2] |
| $V_{IO}$ | 7 | P | supply voltage for $V_{IO}$ voltage level adaptation |
| BGE | 8 | I | bus guardian enable input; internal pull-down |
| TXD | 9 | I | transmit data input; internal pull-down |
| TXEN | 10 | I | transmitter enable input; internal pull-up |
| RXD | 11 | O | receive data output |
| TRXD0 | 12 | IO | data bus line 0 for inner star connection |
| TRXD1 | 13 | IO | data bus line 1 for inner star connection |
| n.c. | 14 | - | not connected; to be connected to GND in application |
| INH | 15 | O | inhibit output; for switching external voltage regulator |


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**Table 2. Pin description** *...continued*

| Symbol | Pin | Type[1] | Description |
|---|---|---|---|
| LWU | 16 | I | local wake-up input; internal pull-up or pull-down (depends on voltage at pin LWU) |
| $V_{BAT}$ | 17 | P | battery supply voltage |
| n.c. | 18 | - | not connected; to be connected to GND in application |
| GND2 | 19 | G | ground connection for branches 3 and 4[2] |
| n.c. | 20 | - | not connected; to be connected to GND in application |
| $V_{BUF2}$ | 21 | P | buffer supply voltage for branches 3 and 4[3] |
| $V_{CC2}$ | 22 | P | supply voltage for branches 3 and 4[4] |
| BM_4 | 23 | IO | bus line minus for branch 4[5] |
| BP_4 | 24 | IO | bus line plus for branch 4[6] |
| n.c. | 25 | - | not connected; to be connected to GND in application |
| BM_3 | 26 | IO | bus line minus for branch 3[5] |
| BP_3 | 27 | IO | bus line plus for branch 3[6] |
| n.c. | 28 | - | not connected; to be connected to GND in application |
| BM_2 | 29 | IO | bus line minus for branch 2[5] |
| BP_2 | 30 | IO | bus line plus for branch 2[6] |
| n.c. | 31 | - | not connected; to be connected to GND in application |
| BM_1 | 32 | IO | bus line minus for branch 1[5] |
| BP_1 | 33 | IO | bus line plus for branch 1[6] |
| $V_{CC1}$ | 34 | P | supply voltage for branches 1 and 2[4] |
| $V_{BUF1}$ | 35 | P | buffer supply voltage for branches 1 and2[3] |
| n.c. | 36 | - | not connected; to be connected to GND in application |
| GND1 | 37 | G | ground connection for branches 1 and 2[2] |
| RES6 | 38 | - | reserved; to be connected to GND in application |
| RES5 | 39 | - | reserved; to be connected to GND in application |
| RES4 | 40 | - | reserved; to be connected to GND in application |
| RES3 | 41 | - | reserved; to be connected to GND in application |
| RES2 | 42 | - | reserved; to be connected to GND in application |
| RES1 | 43 | - | reserved; to be connected to GND in application |
| RSTN | 44 | I | reset input; internal pull-up |

[1] IO: input/output; O: output; I: input; P: power supply; G: ground.

[2] GND1, GND2, GNDD and the exposed center pad of HVQFN44 package must be connected together on the PCB; references in the data sheet to GND can be assumed to encompass GND1, GND2, GNDD and the exposed center pad of HVQFN4 unless stated otherwise.

[3] $V_{BUF1}$ and $V_{BUF2}$ must be connected together on the PCB; note that references in the data sheet to $V_{BUF}$ can be assumed to encompass $V_{BUF1}$ and $V_{BUF2}$ unless stated otherwise.

[4] $V_{CC1}$ and $V_{CC2}$ must be connected together on the PCB; note that references in the data sheet to $V_{CC}$ can be assumed to encompass $V_{CC1}$ and $V_{CC2}$ unless stated otherwise.

[5] References in the data sheet to BM (e.g. pin BM or $V_{BM}$) can be assumed to encompass BM_1, BM_2, BM_3 and BM_4 unless stated otherwise.

[6] References in the data sheet to BP (e.g. pin BP or $V_{BP}$) can be assumed to encompass BP_1, BP_2, BP_3 and BP_4 unless stated otherwise.


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# 6. Functional description

## 6.1 Supply voltage

The TJA1085 state machine is adequately supplied if at least one of $V_{BAT}$, $V_{CC}$ or $V_{BUF}$ is available. The internal supply voltage to the state machine is denoted by $V_{DIG}$. $V_{BUF}$ is an auxiliary supply and is only needed for forwarding the wake-up pattern when $V_{CC}$ is not available.

## 6.2 Host Control (HC) and Autonomous Power (AP) modes - APM flag

The APM flag determines whether the TJA1085 is host-controlled or is operating in Autonomous Power mode. It is in AP mode by default.

The TJA1085 sets the APM flag:

- at power-on
- when a wake-up event is detected (on TXRD0/1, local or remote)
- when a $V_{CC}$ undervoltage event is detected in AS_Normal mode
- when a $V_{IO}$ undervoltage event lasts longer than $t_{to(uvd)(VIO)}$

The host can set or reset the APM flag at any time.

## 6.3 Signal router

The signal router transfers data received on an input channel to all channels configured as outputs. If data is being received on more than one input channel at the same time, the channel that was first to signal activity is selected and data on the other channel/s is ignored. Whether or not the data on an output channel is transmitted depends on whether the output channel is enabled or disabled.

The TJA1085 contains the following data input channels:

- Branches 1 to 4
- TRXD0/1 interface (inner star interface)
- TXD/TXEN interface

The TJA1085 contains the following data output channels:

- Branches 1 to 4
- TRXD0/1 interface
- RXD pin

### 6.3.1 TRXD collision

When the TRXD0/1 interface is configured as an output channel, a TRXD collision is detected (COLL_TRXD = 1) if pins TRXD0 and TRXD1 are both LOW for longer than $t_{det(col)(TRXD)}$, generating a CLAMP_ERROR interrupt.

When a TRXD collision is detected, the TJA1085 transmits a DATA_0 to all other active output channels (irrespective of the actual data on the selected input channel), until the selected input channel detects idle state.


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## 6.4 Wake-up

The TJA1085 supports the following wake-up mechanisms:

- Remote wake-up via the bus (wake-up pattern or dedicated wake-up frame)
- Local wake-up via pin LWU
- Activity on the inner star interface (pins TRXD0 and TRXD1)

Any wake-up event will generate a WU interrupt. A remote wake-up on a branch will generate an EVENT_BRx interrupt to indicate the branch where the wake-up pattern or dedicated data frame was detected.

The host can identify the wake-up source by polling the General Status register (WU_TRXD = 1 for a TRXD0/1 wake-up; WU_LOCAL = 1 for a local wake-up) and the Branch Status register (WU_BRx = 1 for a remote wake-up).

### 6.4.1 Remote wake-up

When the TJA1085 is in AS_Standby or AS_Sleep, all branches are monitored for wake-up events. When a valid wake-up pattern or data frame is detected on a branch, the relevant WU_BRx status bit is set and the wake-up pattern/data frame is forwarded to all other enabled branches.

A remote wake-up event occurring during an AS_Normal-to-AS_Standby or AS_Normal-to-AS_Sleep transition will also be detected, setting the relevant WU_BRx status bit and generating WU and EVENT_BRx interrupts.

#### 6.4.1.1 Bus wake-up via wake-up pattern

A wake-up pattern consists of at least two consecutive wake-up symbols. A wake-up symbol consists of a DATA_0 phase lasting longer than $t_{det(wake)DATA_0}$, followed by an idle phase lasting longer than $t_{det(wake)idle}$, provided both wake-up symbols occur within a time span of $t_{det(wake)tot}$ (see Figure 3). The transceiver also wakes up if the idle phases are replaced by DATA_1 phases.

A wake-up event is not detected if an invalid wake-up pattern is received. See Ref. 1 for more details on invalid wake-up patterns.


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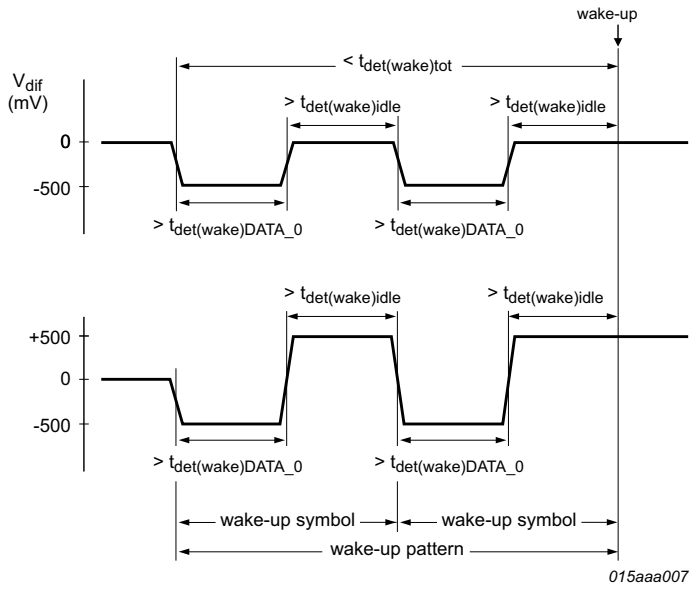



**Fig 3. Bus wake-up timing**

See Ref. 1 for more details of the wake-up mechanism.

#### 6.4.1.2 Bus wake-up via dedicated FlexRay data frame

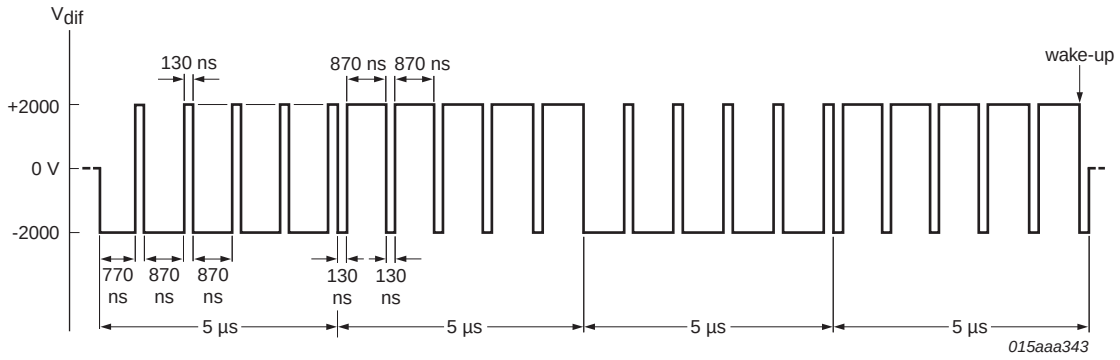
The TJA1085 detects a wake-up event when a dedicated data frame emulating a valid wake-up pattern, as shown in Figure 4, is received.

The Data_0 and Data_1 phases of the emulated wake-up symbol are interrupted by the Byte Start Sequence (BSS) preceding each byte in the data frame. With a data rate of 10 Mbit/s, the interruption has a maximum duration of 130 ns and does not prevent the transceiver from recognizing the wake-up pattern in the payload.

For longer interruptions at lower data rates (5 Mbit/s and 2.5 Mbit/s), the wake-up pattern should be used (see Section 6.4.1.1).


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The duration of each interruption is 130 ns.

The transition time from DATA_0 to DATA_1 and vice versa is about 20 ns.

The TJA1085 wake-up flag is set on receipt of the following frame payload:

0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0x00, 0x00, 0x00, 0x00, 0x00,

0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0x00, 0x00, 0x00, 0x00, 0x00,

0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0x00, 0x00, 0x00, 0x00, 0x00,

0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF

**Fig 4. Minimum bus pattern for bus wake-up via dedicated FlexRay data frame**

### 6.4.2 Local wake-up via pin LWU

Local wake-up is detected when the voltage on pin LWU is lower than $V_{th(wake)(LWU)}$ for longer than $t_{det(wake)(LWU)}$ (falling edge on pin LWU). When local wake-up is detected, the WU_LOCAL status bit is set and a WU interrupt is generated. At the same time, the internal biasing of this pin is switched to pull-down.

If the voltage on pin LWU rises and remains above $V_{th(wake)(LWU)}$ for longer than $t_{det(wake)(LWU)}$ (rising edge on pin LWU), local wake-up is not detected and the biasing on pin LWU is switched to pull-up.

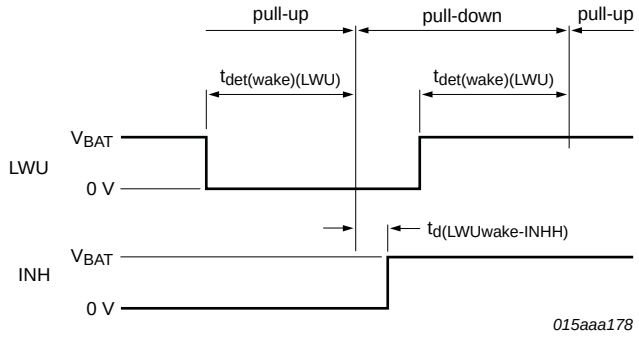



**Fig 5. Local wake-up timing on pin LWU**

### 6.4.3 Wake-up via the TRXD0/1 interface

If the voltage on pin TRXD0 or pin TRXD1 is LOW for longer than $t_{det(wake)(TRXD)}$, a WU interrupt is generated and the WU_TRXD status bit is set.


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## 6.5 Communication controller interface

### 6.5.1 Bus activity and idle detection

The following mechanisms for activity and idle detection are valid in normal power modes:

- If the absolute differential voltage on the bus lines is higher than $|V_{i(dif)det(act)}|$ for $t_{det(act)(bus)}$, activity is detected on the bus lines
- If, after bus activity detection, the differential voltage on the bus lines is higher than $V_{IH(dif)}$, pin RXD will go HIGH
- If, after bus activity detection, the differential voltage on the bus lines is lower than $V_{IL(dif)}$, pin RXD will go LOW
- If the absolute differential voltage on the bus lines is lower than $|V_{i(dif)det(act)}|$ for $t_{det(idle)(bus)}$, then idle is detected on the bus lines (pin RXD is switched HIGH or remains HIGH)

Additionally, activity and idle can be detected:

- if pin TXEN is LOW for longer than $t_{det(act)(TXEN)}$, activity is detected on pin TXEN
- if pin TXEN is HIGH for longer than $t_{det(idle)(TXEN)}$, idle is detected on pin TXEN
- if pin TRXD0 or TRXD1 is LOW for longer than $t_{det(act)(TRXD)}$, activity is detected on the TRXD0/1 interface
- if pins TRXD0 and TRXD1 are both HIGH for longer than $t_{det(idle)(TRXD)}$, idle is detected on the TRXD0/1 interface

**Table 3. Transmitter input signals: TXD, TXEN and BGE[1]**

| TXD | TXEN | BGE | $V_{IO}$ UV detected | RXD | Bus | TRXD0 | TRXD1 | Operating mode |
|---|---|---|---|---|---|---|---|---|
| X | H | X | no | HIGH | idle | high ohmic[2] | high ohmic[2] | AS_Normal |
| X | X | L | no | HIGH | idle | high ohmic[2] | high ohmic[2] | AS_Normal |
| L | L | H | no | LOW | DATA_0 | LOW | high ohmic[2] | AS_Normal |
| H | L | H | no | HIGH | DATA_1 | high ohmic[2] | LOW | AS_Normal |
| X | X | X | no | HIGH | idle | high ohmic[2] | high ohmic[2] | AS_Standby,[3] AS_Sleep[3] |
| X | X | X | yes | LOW | idle | high ohmic[2] | high ohmic[2] | AS_Normal, AS_Standby,[3] AS_Sleep[3] |
| X | X | X | X | HIGH | float | high ohmic[2] | high ohmic[2] | AS_PowerOff, AS_Reset |

[1] The transmitter is activated by a falling edge on pin TXD while TXEN is LOW and BGE is HIGH.

[2] Internal pull-up resistor ($R_{pu}$) to $V_{BUF}$.

[3] BP and BM biased to GND.

**Table 4. Bus as input**

| Bus | $V_{IO}$ UV detected | RXD | TRXD0 | TRXD1 | Operating mode |
|---|---|---|---|---|---|
| DATA_0 | no | LOW | LOW | high ohmic[1] | AS_Normal |
| DATA_1 | no | HIGH | high ohmic[1] | LOW | AS_Normal |
| idle | no | HIGH | high ohmic[1] | high ohmic[1] | AS_Normal |
| X | no | HIGH | high ohmic[1] | high ohmic[1] | AS_Standby, AS_Sleep |


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**Table 4. Bus as input**

| Bus | $V_{IO}$ UV detected | RXD | TRXD0 | TRXD1 | Operating mode |
|---|---|---|---|---|---|
| DATA_0 | yes | LOW | LOW | high ohmic[1] | AS_Normal |
| DATA_1 | yes | LOW | high ohmic[1] | LOW | AS_Normal |
| idle | yes | LOW | high ohmic[1] | high ohmic[1] | AS_Normal |
| X | yes | LOW | high ohmic[1] | high ohmic[1] | AS_Standby, AS_Sleep |
| X | X | HIGH | high ohmic[1] | high ohmic[1] | AS_PowerOff, AS_Reset |

[1] Internal pull-up resistor ($R_{pu}$) to $V_{BUF}$.

**Table 5. TRXD0/1 interface configured as input**

| TRXD0 | TRXD1 | $V_{IO}$ UV detected | RXD | Bus | Operating mode |
|---|---|---|---|---|---|
| X | falling edge | no | HIGH | DATA_1 | AS_Normal[1] |
| HIGH | HIGH | no | HIGH | idle | AS_Normal |
| falling edge | X | X | LOW | DATA_0 | AS_Normal[1] |
| X | falling edge | yes | LOW | DATA_1 | AS_Normal[1] |
| HIGH | HIGH | yes | LOW | idle | AS_Normal |
| LOW | LOW | X | LOW | DATA_0 | collision detected on TRXD0/1 |

[1] Activity detected on TRXD0/TRXD1.

## 6.6 Bus error detection

The TJA1085 provides bus error detection on each branch during data transmission. When a transmit error (TxE_BRx = 1) is detected on a branch, an EVENT_BRx interrupt is generated to notify the host.

The following conditions trigger bus error detection:

- Short circuit BP to BM
- Short-circuit BP to GND
- Short-circuit BM to GND
- Short-circuit BP to $V_{CC}$ or $V_{BAT}$
- Short-circuit BM to $V_{CC}$ or $V_{BAT}$

## 6.7 Interrupt generation

Interrupts are generated when specific events take place or associated status bits in the General or Branch X status registers are set. When an interrupt is generated, the relevant interrupt status bit is set in the Interrupt Status register (see Table 9) and pin INTN is forced LOW.

Some interrupt status bits (PWON, WU, SPI_ERROR and HC_ERROR) are reset immediately after the Interrupt Status register has been read successfully (i.e. a rising edge on SCSN with no SPI_ERROR).


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The UV_ERROR, CLAMP_ERROR, TEMP_ERROR and EVENT_BRx status bits are reset after the flag (or flags) that triggered the interrupt has been reset and a successful read operation had been performed (these two events can occur in any order). Resetting these bits triggers a further falling edge on INTN to indicate to the host that the issue that triggered the interrupt has been resolved (except in the case of EVENT_BRx if a branch wake-up event triggered the interrupt). See Section 6.10.2.3 for further details.

INTN signaling conforms to the FlexRay Electrical Physical Layer specification V3.0.1 (see Ref. 1).

## 6.8 Operating modes

The TJA1085 features five operating modes.

AS_PowerOff, AS_Sleep and AS_Standby are low-power modes in which the transceiver is unable to transmit or receive data streams on the bus. In AS_PowerOff mode, only power-on reset detection is active. The SPI, the low-power receiver and wake-up detection are active in AS_Sleep mode. Undervoltage detection is enabled on $V_{CC}$, $V_{BAT}$ and $V_{BUF}$ in AS_Standby and AS_Normal modes. $V_{IO}$ undervoltage detection is always enabled, except when the TJA1085 is in AS_PowerOff mode.

In AS_Normal mode, the TJA1085 can transmit and receive data streams on the bus.

Pin INH is HIGH in AS_Normal, AS_Standby and AS_Reset, and floating in AS_PowerOff and AS_Sleep.

The dStarGoToSleep timer is started when the TJA1085 switches to AS_Standby or AS_Normal, or when idle is detected on the bus. The timer is halted and reset when activity is detected on the bus.

### 6.8.1 Operating mode transitions

#### 6.8.1.1 AS_PowerOff

The TJA1085 switches to AS_PowerOff from any mode if the internal supply to the state machine, $V_{DIG}$, falls below the power-on detection threshold voltage ($V_{th(det)POR}$). It remains in AS_PowerOff until $V_{DIG}$ rises above the power-on recovery threshold voltage ($V_{th(rec)POR}$), when it switches to AS_Standby. Pins INTN and SDO are switched to a high-impedance state in AS_PowerOff mode.

#### 6.8.1.2 AS_Reset

The TJA1085 switches to AS_Reset from any mode if pin RSTN goes LOW with no undervoltage detected on $V_{IO}$. It remains in AS_Reset until pin RSTN goes HIGH, when it switches to AS_Standby.

#### 6.8.1.3 AS_Standby

The TJA1085 switches to AS_Standby:

- from AS_PowerOff when $V_{DIG}$ rises above the power-on recovery threshold voltage ($V_{th(rec)POR}$)
- from AS_Reset when pin RSTN goes HIGH
- from AS_Normal when a $V_{CC}$ undervoltage event is detected ($V_{CC} < V_{uvd(VCC)}$ for longer than $t_{det(uv)(VCC)}$)


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- from AS_Normal in response to a host ‘AS_Standby’ command (HC mode)
- from AS_Sleep in response to a host ‘AS_Standby’ command (HC mode)
- from AS_Sleep when a wake-up event is detected

The TJA1085 switches from AS_Standby:

- to AS_Normal when a wake-up event is detected, provided $V_{BUF} > V_{uvr(VBUF)}$
- to AS_Normal when a $V_{CC}$ undervoltage recovery event is detected ($V_{CC} > V_{uvr(VCC)}$ for longer than $t_{rec(uv)(VCC)}$), provided $V_{BUF} > V_{uvr(BUF)}$
- to AS_Normal in response to a host ‘AS_Normal’ command (HC mode)
- to AS_Sleep if the dStarGoToSleep timer expires (AP mode)
- to AS_Sleep if a $V_{CC}$ undervoltage event lasts longer than $t_{to(uvd)(VCC)}$ (HC mode)
- to AS_Sleep in response to a host ‘AS_Sleep’ command (HC mode)

#### 6.8.1.4 AS_Sleep

A wake-up event will trigger a transition to AS_Standby (followed by a transition to AS_Normal if $V_{BUF} > V_{uvr(VBUF)}$).

The TJA1085 switches to AS_Sleep:

- from AS_Standby in response to a host ‘AS_Sleep’ command (HC mode)
- from AS_Standby if the dStarGoToSleep timer expires (AP mode)
- from AS_Standby if a $V_{CC}$ undervoltage event lasts longer than $t_{to(uvd)(VCC)}$ (HC mode)
- from AS_Normal in response to a host ‘AS_Sleep’ command (HC mode)
- from AS_Normal if the dStarGoToSleep timer expires (AP mode)

The TJA1085 switches from AS_Sleep:

- to AS_Standby in response to a host ‘AS_Standby’ command (HC mode)
- to AS_Standby when a wake-up event is detected.
- to AS_Normal in response to a host ‘AS_Normal’ command (HC mode)

#### 6.8.1.5 AS_Normal

The TJA1085 switches to AS_Normal:

- from AS_Standby if a $V_{CC}$ undervoltage recovery event is detected ($V_{CC} > V_{uvr(VCC)}$ for longer than $t_{rec(uv)(VCC)}$), provided $V_{BUF} > V_{uvr(BUF)}$
- from AS_Standby if a wake-up event is detected, provided $V_{BUF} > V_{uvr(VBUF)}$ for longer than $t_{rec(uv)(VBUF)}$
- from AS_Standby or AS_Sleep in response to a host ‘AS_Normal’ command

The TJA1085 switches from AS_Normal:

- to AS_Standby when a $V_{CC}$ undervoltage event is detected ($V_{CC} < V_{uvd(VCC)}$ for longer than $t_{det(uv)(VCC)}$)


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  - if the TJA1085 is in HC mode, it will switch from AS_Standby to AS_Sleep if the $V_{CC}$ undervoltage persists for longer than $t_{to(uvd)(VCC)}$
  - if the TJA1085 is in AP mode, it will switch to AS_Sleep when the dStarGoToSleep timer expires

- to AS_Standby in response to a host ‘AS_Standby’ command (HC mode)
- to AS_Sleep in response to a host ‘AS_Sleep’ command (HC mode)
- to AS_Sleep if the dStarGoToSleep timer expires (AP mode)


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### 6.8.1.6 Operating mode transition diagram

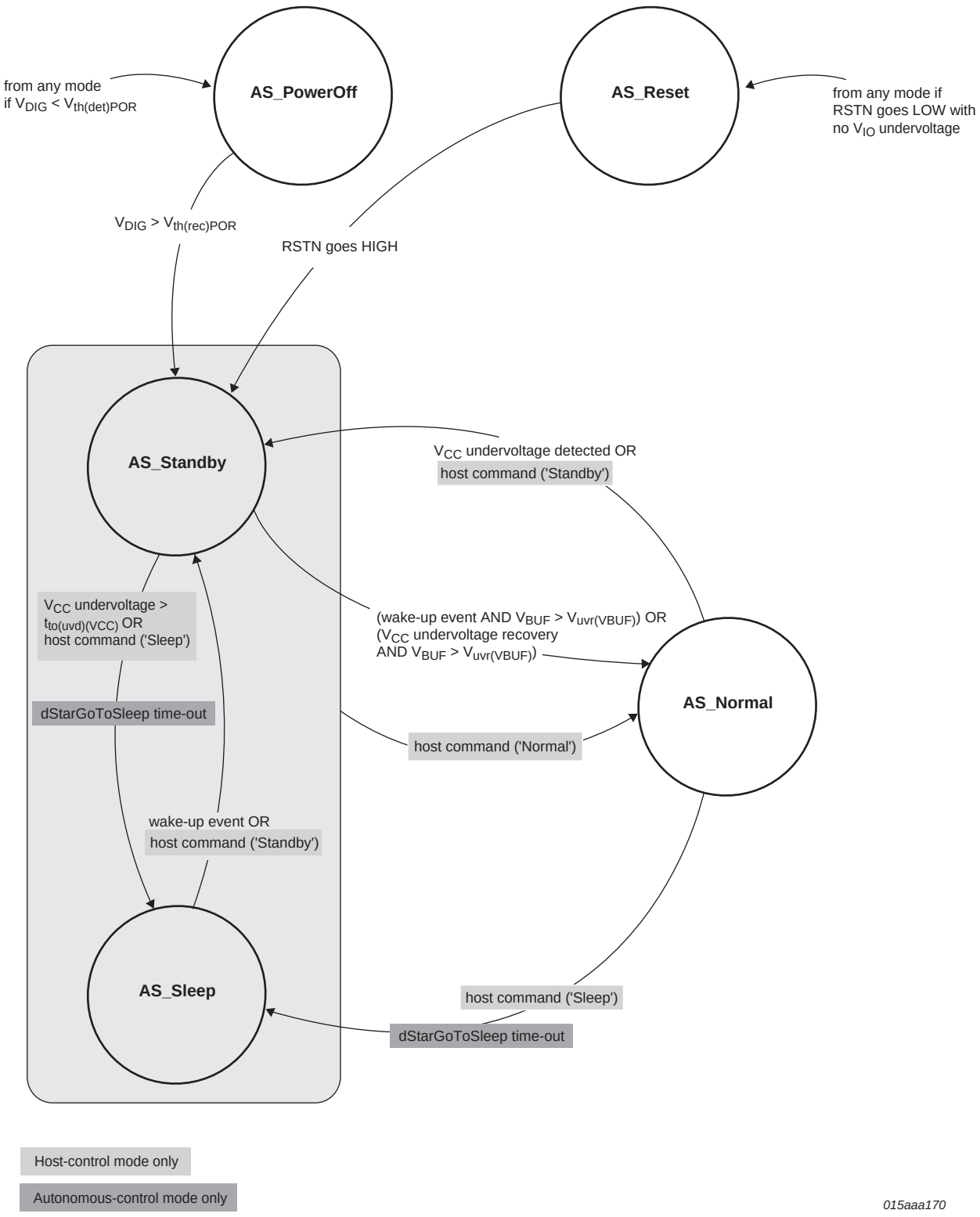



**Fig 6. Mode transition diagram**


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## 6.9 Branch operating modes

Each of the four branches in the TJA1085 features six branch operating modes:

- Branch_Off
  All branches are in Branch_Off mode when the TJA1085 is in AS_PowerOff or AS_Reset mode. The transmitter, normal receiver, low-power receiver and bus error detection are disabled. The bus pins are floating.
- Branch_LowPower
  All branches are in Branch_LowPower mode when the TJA1085 is in AS_Standby or AS_Sleep mode. The transmitter, the normal receiver and bus error detection are disabled. The low-power receiver is active (i.e. remote wake-up is possible). The bus pins are biased to ground.
- Branch_Disabled
  The TJA1085 switches to Branch_Disabled if an overtemperature is detected. The 'Branch_Disabled' and 'Branch_Normal' commands allow the host to enable/disable a branch without affecting the remaining branches. The transmitter, normal receiver and bus error detection are disabled. Only the low-power receiver is active (remote wake-up is possible). The bus pins are biased to $V_{o(idle)(BP)}$ and $V_{o(idle)(BM)}$.
- Branch_Normal
  When a branch is in Branch_Normal, the TJA1085 will be in AS_Normal. The transmitter, normal receiver and bus error detection are active. The bus pins are biased to $V_{o(idle)(BP)}$ and $V_{o(idle)(BM)}$.
- Branch_TxOnly1
  In Branch_TxOnly1 mode, the receiver is disabled, i.e. the received data is not forwarded to the signal router. The transmitter is active and bus error detection is active. The bus pins are biased to $V_{o(idle)(BP)}$ and $V_{o(idle)(BM)}$.
- Branch_TxOnly2
  This mode is host-controlled only and is operationally identical to Branch_TxOnly1. It allows the host to switch off the receiver in response to error conditions.
- Branch_FailSilent
  The transmitter, the low-power receiver and bus error detection are disabled. Only the receiver remains active to monitor the branch for idle or activity. Received data is not forwarded to the signal router. The bus pins are biased to $V_{o(idle)(BP)}$ and $V_{o(idle)(BM)}$.

### 6.9.1 Branch operating mode transitions

Branch-related host commands can only be issued when the TJA1085 is in AS_Normal mode.

#### 6.9.1.1 Branch_Off

When the TJA1085 enters AS_PowerOff or AS_Reset, all four branches switch to Branch-Off. When the TJA1085 subsequently switches to AS_Standby, all four branches switch to Branch_LowPower.

#### 6.9.1.2 Branch_LowPower

All four branches switch to Branch_LowPower when the TJA1085 enters AS_Standby or AS_Sleep. All branches remain in this mode until the TJA1085 enters AS_Normal. When this transition happens, branches that were in Branch_Disabled before switching to Branch_LowPower return to Branch_Disabled. The remaining branches switch to Branch_Normal.


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#### 6.9.1.3 Branch_Disabled

An overtemperature event (TEMP_HIGH flag set) triggers a transition from Branch_Normal to Branch_Disabled in all branches.

If an overtemperature event triggered the transition from Branch_Normal to Branch_Disabled, all branches return to Branch_Normal when the overtemperature problem has been resolved (TEMP_WARN flag reset).

The ‘Branch_Disabled’ and ‘Branch_Normal’ commands can be used to enable/disable individual branches. A host command is also available to trigger a transition from Branch_Disabled to Branch_TxOnly1 (‘Branch_TxOnly').

If a branch switches from Branch_Disabled to Branch_LowPower because the TJA1085 has entered AS_Standby or AS_Sleep, it will return to Branch_Disabled when the TJA1085 enters AS_Normal.

#### 6.9.1.4 Branch_FailSilent

A branch switches to Branch_FailSilent:

- from Branch_Normal if a branch is clamped (Clamp_BRx flag set), provided clamp-detection is enabled (bit CLAMP_DET set; see Table 8)
- from Branch_Normal if a transmit error (TxE_BRx = 1) is detected, provided autonomous error confinement is enabled (bit AEC set; see Table 8)
- from Branch_TxOnly1 if a transmit error (TxE_BRx = 1) is detected.

The branch remains in Branch_FailSilent until idle is detected on all branches, when it switches to Branch_TxOnly1 (a ‘Branch_TxOnly’ command is needed in HC mode).

#### 6.9.1.5 Branch_TxOnly1

A branch switches to Branch_TxOnly1:

- from Branch_Disabled in response to a ‘Branch_TxOnly’ command (HC mode)
- from Branch_FailSilent in response to a ‘Branch_TxOnly’ command when all branches are idle (HC mode)
- from Branch_FailSilent when all branches are idle (AP mode)

A branch switches from Branch_TxOnly1:

- to Branch_Normal when a transmission ends without error
- to Branch_FailSilent if a transmit error is detected (TxE_BRx = 1)

#### 6.9.1.6 Branch_TxOnly2

This mode is purely host controlled. A branch switches to Branch_TxOnly2 only in response to a ‘Branch_TxOnly’ command issued in Branch_Normal mode. The branch remains in Branch_TxOnly2 mode until a ‘Branch_Normal’ command is received.

#### 6.9.1.7 Branch_Normal

A branch switches to Branch_Normal:

- from Branch_LowPower when the TJA1085 enters AS_Normal mode (provided it was not in Branch_Disabled before the transition to Branch_LowPower mode)


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- from Branch_TxOnly2 in response to a host ‘Branch_Normal’ command
- from Branch_TxOnly1 when a transmission ends without error
- from Branch_Disabled in response to a host ‘Branch_Normal’ command
- from Branch_Disabled when an overtemperature is resolved (TEMP_WARN = 0), provided the overtemperature triggered the earlier transition to Branch_Disabled.

A branch switches from Branch_Normal:

- to Branch_FailSilent if a branch is clamped, provided clamp-detection is enabled (CLAMP_DET = 1)
- to Branch_FailSilent if a transmit error is detected, provided bit AEC = 1
- to Branch_TxOnly2 if a host ‘Branch_TxOnly’ command is received
- to Branch_Disabled if an overtemperature event is detected (TEMP_HIGH = 1)


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### 6.9.1.8 Branch operating mode transition diagram

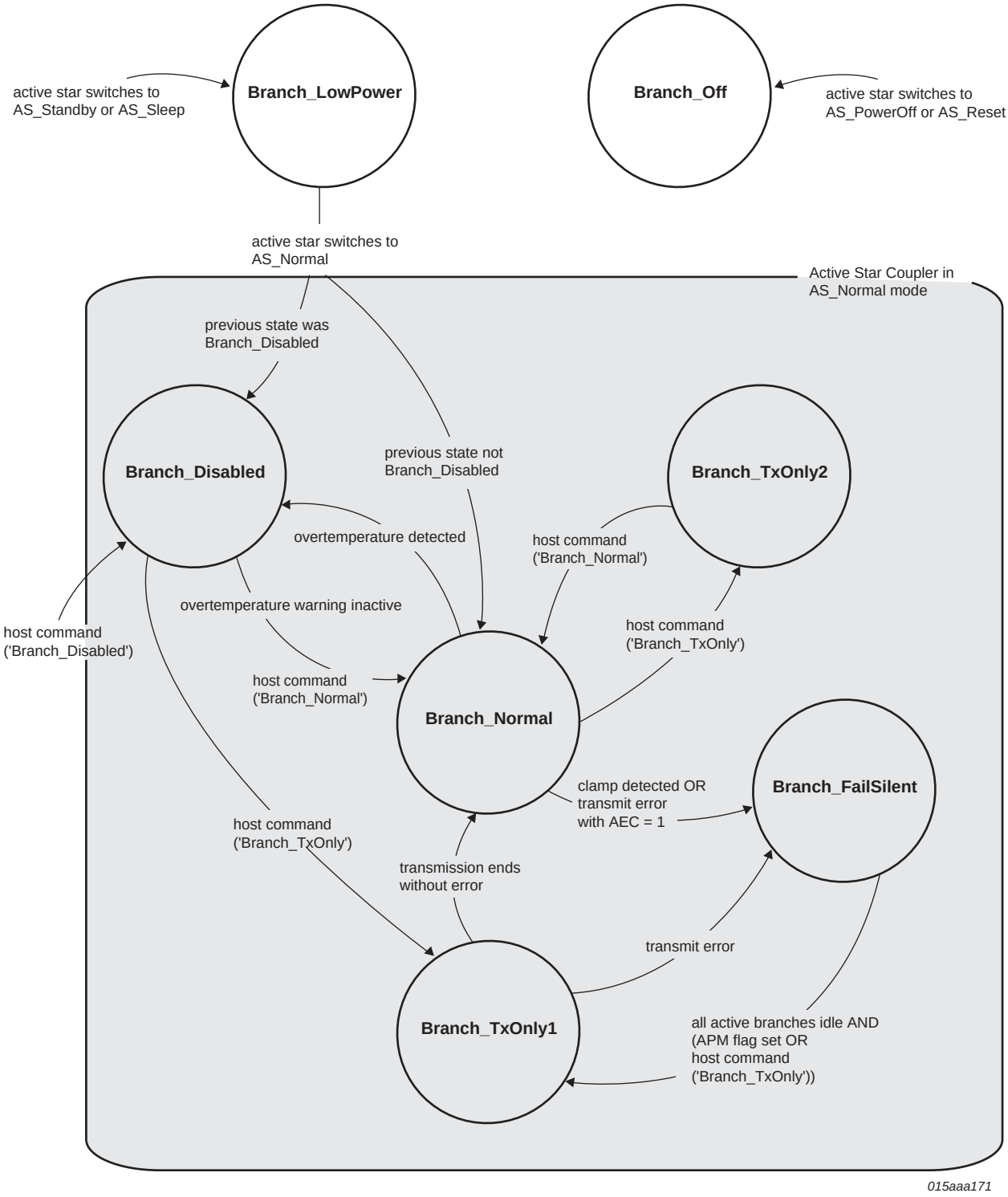



**Fig 7. Branch mode transition diagram**


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## 6.10 SPI interface

The TJA1085 contains a bidirectional 16-bit Serial Peripheral Interface (SPI) for communicating with a host. The SPI allows the host to configure the TJA1085 and to access error and status information.

### 6.10.1 Register access

The SPI supports full duplex data transfer, so status information is read out on pin SDO while control data is being shifted in on pin SDI. Bit sampling is performed on the falling edge of the clock signal on pin SCLK and data is shifted on the rising edge (MSB first; see Figure 8).

The clock signal must be LOW when SCSN goes LOW to initiate an SPI register access cycle.

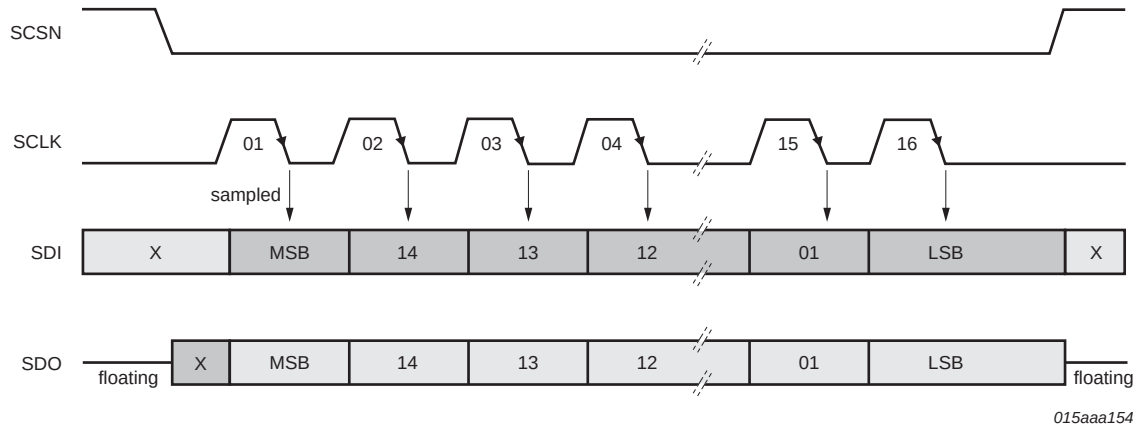



**Fig 8. SPI register access**

### 6.10.2 SPI registers

The SPI register structure in the TJA1085 is illustrated in Figure 9. The three MSBs (bits15 to 13) contain the 3-bit register address. Bit 12 defines the selected register access as read/write or read only. If bit 12 is 1, the SPI data transfer will be read only and all data on the SDI pin will be ignored. If bit 12 is 0, data bits 11 to 0 will be written to the selected register.

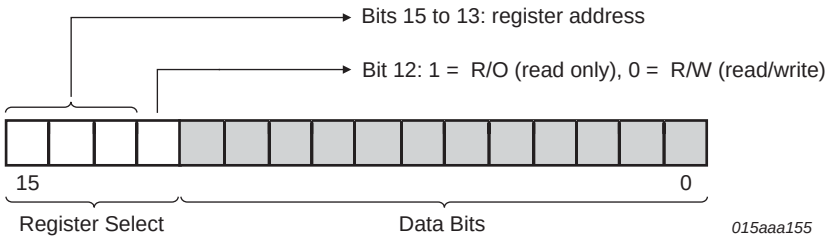



**Fig 9. SPI register structure**


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The assignment of control and status register addresses is detailed in Table 6. Data can only be written to the Control and Configuration registers (status registers are read-only by definition). Therefore the state of bit 12 is only evaluated when these registers are being accessed.

**Table 6. Register map**

| Address bits 15, 14 and 13 | Write access bit 12[1] | Register |
|---|---|---|
| 000 | 0 =R/W, 1 = R/O | Control register; see Table 7 |
| 001 | 1 = R/O | Interrupt status register; see Table 9 |
| 010 | 1 = R/O | General status register; see Table 10 |
| 011 | 1 = R/O | Branch 1 status register; see Table 11 |
| 100 | 1 = R/O | Branch 2 status register; see Table 11 |
| 101 | 1 = R/O | Branch 3 status register; see Table 11 |
| 110 | 1 = R/O | Branch 4 status register; see Table 11 |
| 111 | 0 =R/W, 1 = R/O | Configuration register; see Table 8 |

[1] Bit 12 is assumed to be 1 for status registers

The following subsections provide details of the bits in these registers and the control and status functionality assigned to each.


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#### 6.10.2.1 Control register

The read/write Control register allows the host controller to set the operating modes and to switch the TJA1085 between HC and AP modes.

**Table 7. Control register bit description**

| Bit | Symbol | Access | Default | Description |
|---|---|---|---|---|
| 11:10 | OPM | R/W | 00 | operating mode: |
| | | | | 00: no change |
| | | | | 01: AS_Standby |
| | | | | 10: AS_Sleep |
| | | | | 11: AS_Normal |
| 9:8 | CTRL_BR1 | R/W | 00 | branch 1 control: |
| | | | | 00: no change |
| | | | | 01: Branch_Normal |
| | | | | 10: Branch_TxOnly |
| | | | | 11: Branch_Disabled |
| 7:6 | CTRL_BR2 | R/W | 00 | branch 2 control: |
| | | | | 00: no change |
| | | | | 01: Branch_Normal |
| | | | | 10: Branch_TxOnly |
| | | | | 11: Branch_Disabled |
| 5:4 | CTRL_BR3 | R/W | 00 | branch 3 control: |
| | | | | 00: no change |
| | | | | 01: Branch_Normal |
| | | | | 10: Branch_TxOnly |
| | | | | 11: Branch_Disabled |
| 3:2 | CTRL_BR4 | R/W | 00 | branch 4 control: |
| | | | | 00: no change |
| | | | | 01: Branch_Normal |
| | | | | 10: Branch_TxOnly |
| | | | | 11: Branch_Disabled |
| 1 | APM[1] | R/W | 1 | Autonomous Power mode |
| | | | | 0: disabled |
| | | | | 1: enabled |
| 0 | RESET_ERROR[2] | R/W | 0 | reset error flags and status bits |
| | | | | 0: no change |
| | | | | 1: reset flags/bits |

[1] The TJA1085 sets the APM flag at power-on, in response to a wake-up event (local, remote or TRXD), if a $V_{CC}$ undervoltage is detected in AS_Normal or a $V_{IO}$ undervoltage is detected for longer than $t_{to(uvd)(VIO)}$.

[2] Setting the RESET_ERROR bit resets all error status bits in the General Status (bits 8 to 1) and Branch Status registers (bits 7 to 4).


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#### 6.10.2.2 Configuration register

The read/write Configuration register allows the host controller to configure a number of TJA1085 parameters and functions.

**Table 8. Configuration register bit description**

| Bit | Symbol | Access | Default | Description |
|---|---|---|---|---|
| 11 | AEC | R/W | 0 | Autonomous error confinement: |
| | | | | 0: disabled |
| | | | | 1: enabled |
| 10 | BFT | R/W | 1 | Bus failure timer |
| | | | | 0: disabled |
| | | | | 1: enabled |
| 9 | WUD_BR1 | R/W | 1 | wake-up detection on branch 1: |
| | | | | 0: disabled |
| | | | | 1: enabled |
| 8 | WUD_BR2 | R/W | 1 | wake-up detection on branch 2: |
| | | | | 0: disabled |
| | | | | 1: enabled |
| 7 | WUD_BR3 | R/W | 1 | wake-up detection on branch 3: |
| | | | | 0: disabled |
| | | | | 1: enabled |
| 6 | WUD_BR4 | R/W | 1 | wake-up detection on branch 4: |
| | | | | 0: disabled |
| | | | | 1: enabled |
| 5 | CC_EN | R/W | 0 | CC interface enable (TXD and TXEN inputs; RXD output): |
| | | | | 0: disabled |
| | | | | 1: enabled |
| 4 | TRXD_EN | R/W | 1 | TRXD interface enable: |
| | | | | 0: disabled |
| | | | | 1: enabled |
| 3 | reserved | | | always 0 |
| 2 | CLAMP_DET | R/W | 1 | clamping detection: |
| | | | | 0: disabled |
| | | | | 1: enabled |
| 1 | BIT_LATCHING | R/W | 0 | status bit latching: |
| | | | | 0: disabled |
| | | | | 1: enabled |
| 0 | PARITY | R | - | parity bit - odd parity (including parity bit) |


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**Autonomous Error Confinement (AEC):**
Setting the AEC bit enables the autonomous error confinement feature of the TJA1085.

When AEC is enabled, a bus error (TxE_BRx = 1) triggers a transition from Branch_Normal to Branch_FailSilent. AEC is disabled by default.

**Bus Failure Timer (BFT):**
Setting the BFT bit enables the bus failure timer.

When the BFT is enabled, pulses shorter than $t_{to(BFT)}$ are ignored, resulting in more robust bus error detection. The BFT is enabled by default.

**Wake-up detection on branch x (WUD_BRx):**
Setting the WUD_BRx bit enables wake-up detection on the specified branch.

Each branch in a TJA1085 star network contains a low-power receiver for detecting remote wake-up events. These events can be enabled and disabled individually. This feature makes it possible to minimize quiescent current consumption, especially in AS_Sleep mode. Wake-up detection is enabled by default on all branches.

**Communication Controller interface Enable (CC_EN):**
Setting bit CC_EN enables the communication controller interface.

A communication controller can be connected to the TJA1085 when CC_EN = 1. If CC_EN = 0, the RXD output driver is switched off to minimize current consumption in AS_Normal mode. The CC interface is disabled by default.

**TRXD0/1 interface Enable (TRXD_EN):**
Setting bit TRXD_EN enables the TRXD0 and TRXD1 interfaces.

When the TRXD0/1 interfaces are enabled, several TJA1085 devices can be connected together to form a single active star. If only one TJA1085 is needed at any time, the TRXD0/1 interfaces can be disabled to minimize current consumption in AS_Normal mode. The TRXD0 and TRXD1 interfaces are enabled by default.

**Clamp detection (CLAMP_DET):**
Setting bit CLAMP_DET enables clamp detection on TXEN, TRXD and on the four branches.

When clamp detection is enabled, a CLAMP_ERROR interrupt is generated if clamping is detected on TXEN (CLAMP_TXEN = 1), TRXD (CLAMP_TRXD = 1) or on a branch (CLAMP_BRx). Clamp detection is enabled by default.

**Bit latching (BIT_LATCHING):**
When bit latching is enabled (BIT_LATCHING = 1), the status bits in the General and Branch X status registers reflect the latched state until the register is read. Once the register has been read, latching is released and the bits then reflect the current ‘live’ status. When bit latching is disabled, the status bits reflect the ‘live’ status at all times. Bit latching is disabled by default.


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#### 6.10.2.3 Interrupt Status register

The Interrupt Status register is read-only. When the TJA1085 sets a bit in this register, it triggers a falling edge on pin INTN. Bits PWON, WU, SPI_ERROR and HC_ERROR are reset after a successful read operation. The remaining bits are reset after the flag (or flags) that triggered the interrupt has been reset and a successful read operation has been performed (see Section 6.7).

**Table 9. Interrupt status register**

| Bit | Symbol | Description |
|---|---|---|
| 11 | PWON | power-on detection: |
| | | 0: no power-on detected |
| | | 1: power-on detected |
| 10 | WU | wake-up event detection (any): |
| | | 0: no wake-up event detected |
| | | 1: wake-up event detected |
| 9 | EVENT_BR1 | wake-up or bus error detection on branch 1: |
| | | 0: no wake-up or bus error detected |
| | | 1: wake-up or bus error detected |
| 8 | EVENT_BR2 | wake-up or bus error detection on branch 2: |
| | | 0: no wake-up or bus error detected |
| | | 1: wake-up or bus error detected |
| 7 | EVENT_BR3 | wake-up or bus error detection on branch 3: |
| | | 0: no wake-up or bus error detected |
| | | 1: wake-up or bus error detected |
| 6 | EVENT_BR4 | wake-up or bus error detection on branch 4: |
| | | 0: no wake-up or bus error detected |
| | | 1: wake-up or bus error detected |
| 5 | UV_ERROR | undervoltage detected on $V_{BAT}$, $V_{CC}$ or $V_{IO}$: |
| | | 0: no undervoltage detected |
| | | 1: undervoltage detected |
| 4 | CLAMP_ERROR | clamp error on TRXD, TXEN or branch or collision on TRXD: |
| | | 0: no clamping error detected |
| | | 1: clamping error detected |
| 3 | SPI_ERROR | SPI communication error: |
| | | 0: not detected |
| | | 1: detected |
| 2 | HC_ERROR | host command error: |
| | | 0: not detected |
| | | 1: detected |
| 1 | TEMP_ERROR | overtemperature error: |
| | | 0: not detected |
| | | 1:detected |
| 0 | PARITY | parity bit - odd parity (including parity bit) |


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**PWON:** A PWON interrupt is generated to signal a power-on event.

The PWON interrupt status bit is set when the TJA1085 leaves AS_PowerOff or AS_Reset. It is reset after a successful read operation on the Interrupt Status register.

**WU:** A WU interrupt indicates the occurrence of a wake-up event.

The WU interrupt status bit is set when a wake-up event is detected on a branch (WU_BRx = 1), on TRXD0/1 (WU_TRXD = 1), or on LWU (WU_LOCAL = 1). It is reset after a successful read operation on the Interrupt Status register.

**EVENT_BRx:** An EVENT_BRx interrupt signals the occurrence of a significant event on the relevant branch.

The EVENT_BRx interrupt status bit is set when any of the following events is detected on a branch:

- a wake-up event (WU_BRx = 1)
- a bus error (TxE_BRx = 1)
- clamping (CLAMP_BRx = 1)

It is reset after the flag (or flags) that triggered the interrupt has been reset and the Interrupt Status register has been read successfully. Resetting EVENT_BRx will trigger a falling edge on INTN to indicate to the host that the event that triggered the interrupt has been resolved (except when the interrupt was triggered by a branch wake-up event).

**UV_ERROR:** A UV_ERROR interrupt indicates that an undervoltage has occurred.

The UV_ERROR interrupt status bit is set when a $V_{BAT}$ (UV_VBAT = 1), $V_{CC}$ (UV_VCC = 1) or $V_{IO}$ (UV_VIO = 1) undervoltage is detected. It is reset after the flag (or flags) that triggered the interrupt has been reset and the Interrupt Status register has been read successfully. Resetting UV_ERROR triggers a falling edge on INTN to indicate to the host that the undervoltage condition is no longer present.

**CLAMP_ERROR:** A CLAMP_ERROR interrupt indicates that an input channel has become clamped or a collision has occurred on the TRXDO/1 interface.

The CLAMP_ERROR interrupt status bit is set when clamping is detected on TRXD (CLAMP_TRXD = 1), on TXEN (CLAMP_TXEN = 1) or on a branch (CLAMP_BRx = 1) or if a collision is detected on TRXD0/TRXD1 (COLL_TRXD = 1). It is reset after the flag (or flags) that triggered the interrupt has been reset and the Interrupt Status register has been read successfully. Resetting CLAMP_ERROR triggers a falling edge on INTN to indicate to the host that the clamp or collision error has been corrected.

**SPI_ERROR:** An SPI_ERROR interrupt indicates that an error has occurred during SPI communications.

The SPI_ERROR interrupt status bit is set if the number of SCLK cycles generated during a LOW phase on SCSN does not equal 16. It is reset after a successful read operation on the Interrupt Status register.

**HC_ERROR:** A HC_ERROR interrupt indicates that an invalid host command has been received.


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The HC_ERROR interrupt status bit is set when the host requests an illegal mode transition (as defined in the Section 6.8.1 and Section 6.9.1). It is reset after a successful read operation on the Interrupt Status register.

**TEMP_ERROR:** A TEMP_ERROR interrupt signals the presence of an overtemperature condition.

The TEMP_ERROR interrupt status bit is set when the temperature warning level (TEMP_WARN = 1) or temperature high level (TEMP_HIGH = 1) is exceeded. It is reset after the flag (or flags) that triggered the interrupt has been reset and the Interrupt Status register has been read successfully. Resetting TEMP_ERROR triggers a falling edge on INTN to indicate to the host that the overtemperature condition is no longer present.


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#### 6.10.2.4 General Status register

The read-only General Status register contains status information not included in the Interrupt status register.

**Table 10. General status register**

| Bit | Symbol | Description |
|---|---|---|
| 11 | WU_LOCAL | local wake-up on pin LWU: |
| | | 0: no wake-up detected |
| | | 1: wake-up detected |
| 10 | WU_TRXD | wake-up via TRXD0/TRXD1 |
| | | 0: no wake-up detected |
| | | 1: wake-up detected |
| 9 | BGE_FB | BGE status feedback: |
| | | 0: if BGE is LOW |
| | | 1: if BGE is HIGH |
| 8 | UV_VBAT | $V_{BAT}$ undervoltage |
| | | 0: no undervoltage detected |
| | | 1: undervoltage detected |
| 7 | UV_VCC | $V_{CC}$ undervoltage |
| | | 0: no undervoltage detected |
| | | 1: undervoltage detected |
| 6 | UV_VIO | $V_{IO}$ undervoltage |
| | | 0: no undervoltage detected |
| | | 1: undervoltage detected |
| 5 | TEMP_WARN | temperature warning level |
| | | 0: not exceeded |
| | | 1: exceeded |
| 4 | TEMP_HIGH | temperature high level |
| | | 0: not exceeded |
| | | 1: exceeded |
| 3 | CLAMP_TRXD | clamping detection on TRXD: |
| | | 0: not detected |
| | | 1: detected |
| 2 | CLAMP_TXEN | clamping detection on TXEN: |
| | | 0: not detected |
| | | 1: detected |
| 1 | COLL_TRXD | collision detection on TRXDO and TRXD1: |
| | | 0: not detected |
| | | 1:detected |
| 0 | PARITY | parity bit - odd parity (including parity bit) |


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**WU_LOCAL:**
WU_LOCAL is set when a local wake-up event is detected. A WU interrupt is generated.

WU_LOCAL is reset after the General Status register has been read successfully or when the TJA1085 switches from AS_Normal to AS_Standby or AS_Sleep. This ensures that a new wake-up event will be detected.

**WU_TRXD:**
WU_TRXD is set when a wake-up event is detected on the TRXD0/1 interface. A WU interrupt is generated.

WU_TRXD is reset after the General Status register has been read successfully or when the TJA1085 switches from AS_Normal to AS_Standby or AS_Sleep. This ensures that a new wake-up event will be detected.

**BGE_FB:**
Bit BGE_FB provides information about the voltage level on pin BGE.

BGE_FB is set when the voltage on BGE is HIGH and reset when the voltage on BGE is LOW.

**UV_VBAT:**
UV_VBAT is set when a $V_{BAT}$ undervoltage is detected, generating a UV_ERROR interrupt.

If bit latching is enabled (BIT_LATCHING = 1), UV_BAT will remain set until the General Status register has been read, after which it will reflect the current 'live' situation (set if $V_{BAT} < V_{uvd(VBAT)}$ for longer than $t_{det(uv)(VBAT)}$ and reset if $V_{BAT} > V_{uvr(VBAT)}$ for longer than $t_{rec(uv)(VBAT)}$). If bit latching is not enabled, UV_BAT will reflect the 'live' situation at all times.

**UV_VCC:**
UV_VCC is set when a $V_{CC}$ undervoltage is detected, generating a UV_ERROR interrupt.

If bit latching is enabled (BIT_LATCHING = 1), UV_VCC will remain set until the General Status register has been read, after which it will reflect the current 'live' situation (set if $V_{CC} < V_{uvd(VCC)}$ for longer than $t_{to(uvd)(VCC)}$ and reset if $V_{CC} > V_{uvr(VCC)}$ for longer than $t_{to(uvr)(VCC)}$). If bit latching is not enabled, UV_VCC will reflect the 'live' situation at all times.

**UV_VIO:**
UV_VIO is set when a $V_{IO}$ undervoltage is detected, generating a UV_ERROR interrupt.

If bit latching is enabled (BIT_LATCHING = 1), UV_VIO will remain set until the General Status register has been read, after which it will reflect the current 'live' situation (set if $V_{IO} < V_{uvd(VIO)}$ for longer than $t_{to(uvd)(VIO)}$ and reset if $V_{IO} > V_{uvr(VIO)}$ for longer than $t_{to(uvr)(VIO)}$). If bit latching is not enabled, UV_VIO will reflect the 'live' situation at all times.

When a $V_{IO}$ undervoltage is active, the digital inputs are disabled and the TJA1085 is unable to accept Host commands. If the $V_{IO}$ undervoltage persists for longer than $t_{to(uvd)(VIO)}$, the APM flag is set and the TJA1085 switches from Host control to Autonomous control.


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**TEMP_WARN:**
TEMP_WARN is set when the junction temperature rises above the temperature warning level, generating a TEMP_ERROR interrupt.

If bit latching is enabled (BIT_LATCHING = 1), TEMP_WARN will remain set until the General Status register has been read, after which it will reflect the current 'live' situation (set when $T_j > T_{j(warn)}$ and reset when $T_j < T_{j(warn)}$ with no activity on the bus or on the CC and TRXD0/1 interfaces). If bit latching is not enabled, TEMP_WARN will reflect the 'live' situation at all times.

**TEMP_HIGH:**
TEMP_HIGH is set when the junction temperature rises above the temperature high level. The output driver on the TRXD0/1 interface is disabled along with the branch transmitters (all branches switch to Branch_Disabled). A TEMP_ERROR interrupt is generated.

If bit latching is enabled (BIT_LATCHING = 1), TEMP_HIGH will remain set until the General Status register has been read, after which it will reflect the current 'live' situation (set when $T_j > T_{j(high)}$ and reset when $T_j < T_{j(high)}$ with no activity on the bus or on the CC and TRXD0/1 interfaces). If bit latching is not enabled, TEMP_HIGH will reflect the 'live' situation at all times.

**CLAMP_TRXD:**
CLAMP_TRXD is set when the TRXD0/1 interface is configured as an input and TRXD0 or TRXD1 is clamped LOW for longer than $t_{detCL(TRXD)}$. The output driver on the TRXD0/1 interface is disabled and data on the inputs is ignored. A CLAMP_ERROR interrupt is generated.

If bit latching is enabled, CLAMP_TRXD will remain set until the General Status register has been read, after which it will reflect the current 'live' situation (set when TRXD0 or TRXD1 clamped LOW and reset when TRXD0 and TRXD1 are HIGH). If bit latching is not enabled, CLAMP_TRXD will reflect the 'live' situation at all times.

**CLAMP_TXEN:**
CLAMP_TXEN is set when the TXEN is clamped LOW for longer than $t_{detCL(TXEN)}$. Data on TXD/TXEN is ignored and a CLAMP_ERROR interrupt is generated.

If bit latching is enabled, CLAMP_TXEN will remain set until the General Status register has been read, after which it will reflect the current 'live' situation (set when TXEN clamped LOW and reset when TXEN is HIGH). If bit latching is not enabled, CLAMP_TXEN will reflect the 'live' situation at all times.

**COLL_TRXD:**
COLL_TRXD is set when a collision is detected on the TRXD0/1 interface (TRXD0 and TRXD1 LOW for longer than $t_{det(col)(TRXD)}$). A CLAMP_ERROR interrupt is generated.

COLL_TRXD is reset once the General Status register has been read.


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#### 6.10.2.5 Branch X status registers

There is a dedicated read-only status register for each branch, i.e. there are four Branch X status registers in total. Each register contains relevant status information of a branch.

**Table 11. Branch X status register**

| Bit | Symbol | Description |
|---|---|---|
| 11-9 | STATE_BRx | state of active branch: |
| | | 000: Branch_Normal mode |
| | | 001: Branch_Disabled mode |
| | | 010: Branch_LowPower mode |
| | | 011: Branch_TxOnly_2 mode |
| | | 100: Branch_FailSilent mode |
| | | 101: Branch_TxOnly_1 mode |
| 8 | WU_BRx | wake-up status |
| | | 0: no wake-up detected |
| | | 1: wake-up detected |
| 7 | reserved | always 0 |
| 6 | TxE_BRx | transmit error on branch |
| | | 0: not detected |
| | | 1: detected |
| 5 | reserved | always 0 |
| 4 | CLAMP_BRx | clamp detection on branch |
| | | 0: not detected |
| | | 1: detected |
| 3 | reserved | always 0 |
| 2 | reserved | always 1 |
| 1 | reserved | always 0 |
| 0 | PARITY | parity bit - odd parity (including parity bit) |


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**STATE_BRx:**
Bits STATE_BRx indicate the current branch operating mode.

**WU_BRx:**
WU_BRx is set when a remote wake-up event is detected on a branch. A WU interrupt is generated along with an EVENT_BRx interrupt to indicate the branch where the wake-up pattern or dedicated data frame was detected.

WU_BRx is reset after the Branch Status register has been read successfully or when the TJA1085 switches from AS_Normal to AS_Standby or AS_Sleep. This ensures that a new wake-up event will be detected.

**TxE_BRx:**
TxE_BRx is set when a transmit error is detected on a branch, generating an EVENT_BRx interrupt. A transmit error is detected when there is a mismatch between the transmitted and received signals.

If bit latching is enabled (BIT_LATCHING = 1), TxE_BRx will remain set until the register has been read, after which it is reset if no mismatch is found between transmitted and received signals or the branch leaves Branch_Normal. If bit latching is not enabled, TxE_BRx is reset if no mismatch is found in a data frame or the branch leaves Branch_Normal.

**CLAMP_BRx:**
CLAMP_BRx is set when a branch is clamped for longer than $t_{detCL(bus)}$, generating a CLAMP_ERROR interrupt along with an EVENT_BRx interrupt to indicate the branch.

If bit latching is enabled (BIT_LATCHING = 1), CLAMP_BRx will remain set until the register has been read, after which it is reset when idle is detected on the branch. If bit latching is not enabled, CLAMP_BRx is reset when idle is detected on the branch.


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# 7. Limiting values

**Table 12. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages are referenced to GND.*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{BAT}$ | battery supply voltage | | [1] | –0.3 | +48 | V |
| | | during load dump (400 ms max.) | | –0.3 | +60 | V |
| $I_{INH}$ | current on pin INH | AS_Normal, AS_Standby or AS_Reset | | –1 | 0 | mA |
| $V_x$ | voltage on pin x[1] | on pins $V_{CC}$, $V_{BUF}$, $V_{IO}$, TRXD0, TRXD1, BGE, TXD, TXEN, RSTN, INTN, SCSN, SCLK, SDI, SDO | | –0.3 | +5.5 | V |
| | | on pins INH, LWU | | –0.3 | $V_{BAT}$ + 0.3 | V |
| | | on pin RXD | | –0.3 | min($V_{IO}$ + 0.3, 5.5) | V |
| | | on any BM/BP pin with respect to other BP/BM pins and GND | | –60 | +60 | V |
| $I_{O(LWU)}$ | output current on pin LWU | | | –15 | - | mA |
| $V_{trt}$ | transient voltage | on pins LWU, $V_{BAT}$, BP and BM | [2] | –100 | - | V |
| | | | [3] | - | 75 | V |
| | | | [4] | –150 | - | V |
| | | | [5] | - | 100 | V |
| $T_{amb}$ | ambient temperature | | | –40 | +125 | °C |
| $T_{vj}$ | virtual junction temperature | | [6] | –40 | +150 | °C |
| $T_{stg}$ | storage temperature | | | –55 | +150 | °C |
| $V_{ESD}$ | electrostatic discharge voltage | IEC 61000-4-2 (150 pF, 330 Ω) | [7] | | | |
| | | on pins BP and BM to GND | | –6.0 | +6.0 | kV |
| | | on pin LWU to GND | [8] | –6.0 | +6.0 | kV |
| | | on pin $V_{BAT}$ to GND | [9] | –6.0 | +6.0 | kV |
| | | Human Body Model (HBM); 100 pF, 1.5 kΩ | [10] | | | |
| | | on pins BP and BM to GND | | –8.0 | +8.0 | kV |
| | | on pins LWU and $V_{BAT}$ to GND | [11] | –6.0 | +6.0 | kV |
| | | on any other pin | | –4.0 | +4.0 | kV |
| | | Machine Model (MM); 200 pF, 0.75 μH, 10 Ω | [12] | | | |
| | | on any pin | | –200 | +200 | V |
| | | Charged Device Model (CDM); field Induced charge; 4 pF | [13] | | | |
| | | on any pin | | –1000 | +1000 | V |

[1] The device can sustain voltages up to the specified values over the product lifetime, provided applied voltages (including transients) never exceed these values.

[2] According to ISO7637, test pulse 1, class C; verified by an external test house.

[3] According to ISO7637, test pulse 2a, class C; verified by an external test house.

[4] According to ISO7637, test pulse 3a, class C; verified by an external test house.

[5] According to ISO7637, test pulse 3b, class C; verified by an external test house.

[6] In accordance with IEC 60747-1. An alternative definition of $T_{vj}$ is: $T_{vj} = T_{amb} + P \times R_{th(j-a)}$, where $R_{th(j-a)}$ is a fixed value used in the calculation of $T_{vj}$. The rating for $T_{vj}$ limits the allowable combinations of power dissipation (P) and ambient temperature ($T_{amb}$).


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[7] According to IEC TS 62228 (2007), Section 4.3; DIN EN 61000-4-2; verified by an external test house. The test result is equal to or better than ±6 kV (unaided).

[8] With 3.3 kΩ in series.

[9] With 100 nF from $V_{BAT}$ to GND.

[10] According to AEC-Q100-002.

[11] Guaranteed only when all n.c. pins are connected to GND.

[12] According to AEC-Q100-003.

[13] According to AEC-Q100-011 Rev-C1. The classification level is C6.

# 8. Thermal characteristics

**Table 13. Thermal characteristics**

| Symbol | Parameter | | Conditions | Typ | Unit |
|---|---|---|---|---|---|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | [1] | in free air | 24 | K/W |
| $R_{th(j-c)}$ | thermal resistance from junction to case | | in free air | 2.5 | K/W |

[1] TJA1085 mounted on a JEDEC 2s2p board with 36 vias between layer 1 and layer 2; via diameter: 0.5 mm, wall thickness: 18 μm.


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# 9. Static characteristics

**Table 14. Static characteristics**

*All parameters are guaranteed for $V_{BAT}$ = 4.45 V to 60 V; $V_{CC}$ = 4.45 V to 5.25 V; $V_{BUF}$ = 4.45 V to 5.25 V; $V_{IO}$ = 2.55 V to 5.25 V; $T_{vj}$ = −40 °C to +150 °C; $C_{bus}$ = 100 pF; $R_{bus}$ = 40 Ω to 55 Ω; $C_{RXD}$ = 15 pF and $C_{TRXD0}$ = $C_{TRXD1}$ = 50 pF unless otherwise specified. All voltages are defined with respect to ground; positive currents flow into the IC.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Power-on reset for $V_{DIG}$** | | | | | | |
| $V_{th(det)POR}$ | power-on reset detection threshold voltage | of internal digital circuitry | 3 | - | 3.4 | V |
| $V_{th(rec)POR}$ | power-on reset recovery threshold voltage | of internal digital circuitry | 3.1 | - | 3.5 | V |
| $V_{hys(POR)}$ | power-on reset hysteresis voltage | of internal digital circuitry | 100 | | 500 | mV |
| $\Delta V_{(VCC-VDIG)}$ | voltage difference between $V_{CC}$ and $V_{DIG}$ | $V_{CC}$ = 4.45 V; $V_{BAT}$ = $V_{BUF}$ = 0 V | - | - | 1.0 | V |
| $\Delta V_{(VBAT-VDIG)}$ | voltage difference between $V_{BAT}$ and $V_{DIG}$ | $V_{BAT}$ = 4.45 V; $V_{CC}$ = $V_{BUF}$ = 0 V | - | - | 1.0 | V |
| $\Delta V_{(VBUF-VDIG)}$ | voltage difference between $V_{BUF}$ and $V_{DIG}$ | $V_{BUF}$ = 4.45 V; $V_{CC}$ = $V_{BAT}$ = 0 V | - | - | 1.0 | V |
| **Supply: pin $V_{BAT}$** | | | | | | |
| $V_{BAT}$ | battery supply voltage | operating range | 4.75 | - | 60 | V |
| $I_{BAT}$ | battery supply current | AS_Normal; no load on INH | - | 0.1 | 1 | mA |
| | | AS_Standby; no load on INH; wake-up enabled on all branches | - | 50 | 100 | µA |
| | | AS_Sleep; wake-up enabled on all branches | - | 50 | 100 | µA |
| | | AS_Sleep; wake-up enabled on all branches; $T_{vj} \leq 85$ °C | - | 50 | 90 | µA |
| | | AS_Sleep; wake-up disabled on all branches | - | 25 | 55 | µA |
| | | AS_Sleep; wake-up disabled on all branches; $T_{vj} \leq 85$ °C | - | 25 | 45 | µA |
| $V_{uvd}$ | undervoltage detection voltage | | 4.45 | - | 4.715 | V |
| $V_{uvr}$ | undervoltage recovery voltage | | 4.475 | - | 4.74 | V |
| $V_{uvhys}$ | undervoltage hysteresis voltage | | 25 | - | 290 | mV |
| **Supply: pins $V_{CC1}$ and $V_{CC2}$ (connected on the PCB)** | | | | | | |
| $V_{CC}$ | supply voltage | operating range | 4.75 | - | 5.25 | V |


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**Table 14. Static characteristics** *...continued*

*All parameters are guaranteed for $V_{BAT}$ = 4.45 V to 60 V; $V_{CC}$ = 4.45 V to 5.25 V; $V_{BUF}$ = 4.45 V to 5.25 V; $V_{IO}$ = 2.55 V to 5.25 V; $T_{vj}$ = −40 °C to +150 °C; $C_{bus}$ = 100 pF; $R_{bus}$ = 40 Ω to 55 Ω; $C_{RXD}$ = 15 pF and $C_{TRXD0}$ = $C_{TRXD1}$ = 50 pF unless otherwise specified. All voltages are defined with respect to ground; positive currents flow into the IC.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $I_{CC}$ | supply current | AS_Normal; $V_{TXEN}$ = 0 V; $V_{BGE}$ = $V_{IO}$; $R_{bus}$ = 45 Ω; all branches in Branch_Normal | [1] | - | 180 | 210 | mA |
| | | AS_Normal; $V_{TXEN}$ = $V_{IO}$; $V_{BGE}$ = 0 V; $R_{bus}$ = 45 Ω; all branches in Branch_Normal and/or Branch_Disabled | [1] | - | - | 80 | mA |
| | | AS_Standby | [1][2] | - | 4 | 35 | µA |
| | | AS_Standby; $T_{vj}$ ≤ 85 °C | [1][2] | - | 4 | 15 | µA |
| | | AS_Sleep, AS_Reset | [1][2] | - | 0 | 30 | µA |
| | | AS_Sleep, AS_Reset; $T_{vj}$ ≤ 85 °C | [1][2] | - | 0 | 10 | µA |
| $V_{uvd}$ | undervoltage detection voltage | | | 4.45 | - | 4.715 | V |
| $V_{uvr}$ | undervoltage recovery voltage | | | 4.475 | - | 4.74 | V |
| $V_{uvhys}$ | undervoltage hysteresis voltage | | | 25 | - | 290 | mV |
| **Supply: pins $V_{BUF1}$ and $V_{BUF2}$ (connected on the PCB)** | | | | | | | |
| $V_{BUF}$ | supply voltage on pin $V_{BUF}$ | 5.5 V ≤ $V_{BAT}$ ≤ 60 V; $V_{CC}$ ≤ $V_{uvd(VCC)}$ | | 4.5 | - | 5.25 | V |
| | | 4.5 V ≤ $V_{BAT}$ ≤ 5.5 V; $V_{CC}$ ≤ $V_{uvd(VCC)}$ | | 3.5 | - | 5.25 | V |
| $\Delta V_{(VCC-VBUF)}$ | voltage difference between $V_{CC}$ and $V_{BUF}$ | $V_{CC}$ ≥ $V_{uvr(VCC)}$ | | 0 | - | 0.25 | V |
| $I_{ch(VBAT-VBUF)}$ | charge current from $V_{BAT}$ to $V_{BUF}$ | 5.5 V ≤ $V_{BAT}$ ≤ 60 V; $V_{CC}$ ≤ $V_{uvd(VCC)}$; 0 V ≤ $V_{BUF}$ ≤ 4 V | | −200 | −100 | −30 | µA |
| $V_{uvd}$ | undervoltage detection voltage | | | 4.2 | - | 4.474 | V |
| $V_{uvr}$ | undervoltage recovery voltage | | | 4.225 | - | 4.499 | V |
| $V_{uvhys}$ | undervoltage hysteresis voltage | | | 25 | - | 299 | mV |
| **Supply: pin $V_{IO}$** | | | | | | | |
| $V_{IO}$ | supply voltage on pin $V_{IO}$ | operating range | | 2.8 | - | 5.25 | V |
| $I_{IO}$ | supply current on pin $V_{IO}$ | AS_Normal; $V_{TXD}$ = $V_{IO}$ | | - | - | 1000 | µA |
| | | AS_Standby; AS_Sleep; AS_PowerOff; $V_{SCSN}$ = $V_{TXEN}$ = $V_{RSTN}$ = $V_{VIO}$ | | - | 2 | 7 | µA |
| $I_r$ | reverse current | from digital input pin to $V_{IO}$; AS_PowerOff; $V_{TXEN}$ = $V_{TXD}$ = $V_{BGE}$ = $V_{SCSN}$ = $V_{SCLK}$ = $V_{SDI}$ = $V_{RSTN}$ = 5.25 V; $V_{CC}$ = $V_{IO}$ = 0 V | | −5 | - | +5 | µA |


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**Table 14. Static characteristics** *...continued*

*All parameters are guaranteed for $V_{BAT}$ = 4.45 V to 60 V; $V_{CC}$ = 4.45 V to 5.25 V; $V_{BUF}$ = 4.45 V to 5.25 V; $V_{IO}$ = 2.55 V to 5.25 V; $T_{vj}$ = −40 °C to +150 °C; $C_{bus}$ = 100 pF; $R_{bus}$ = 40 Ω to 55 Ω; $C_{RXD}$ = 15 pF and $C_{TRXD0}$ = $C_{TRXD1}$ = 50 pF unless otherwise specified. All voltages are defined with respect to ground; positive currents flow into the IC.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{uvd}$ | undervoltage detection voltage | | | 2.55 | - | 2.765 | V |
| $V_{uvr}$ | undervoltage recovery voltage | | | 2.575 | - | 2.79 | V |
| $V_{uvhys}$ | undervoltage hysteresis voltage | | | 25 | - | 240 | mV |
| **Pin TXEN** | | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | AS_Normal | | $0.7V_{IO}$ | - | 5.5 | V |
| $V_{IL}$ | LOW-level input voltage | AS_Normal | | −0.3 | - | $0.3V_{IO}$ | V |
| $I_{IH}$ | HIGH-level input current | $V_{TXEN} = V_{IO}$ | | −2 | - | +2 | µA |
| $I_{IL}$ | LOW-level input current | $V_{TXEN} = 0.3V_{IO}$ | | −300 | - | −50 | µA |
| **Pin TXD** | | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | AS_Normal | | $0.6V_{IO}$ | - | 5.5 | V |
| $V_{IL}$ | LOW-level input voltage | AS_Normal | | −0.3 | - | $0.4V_{IO}$ | V |
| $R_{pd}$ | pull-down resistance | to GND | | 50 | 150 | 400 | kΩ |
| $C_i$ | input capacitance | with respect to all other pins at ground; $V_{TXD}$ = 100 mV; f = 5 MHz | [3] | - | - | 10 | pF |
| **Pin BGE** | | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | AS_Normal | | $0.7V_{IO}$ | - | 5.5 | V |
| $V_{IL}$ | LOW-level input voltage | AS_Normal | | −0.3 | - | $0.3V_{IO}$ | V |
| $R_{pd}$ | pull-down resistance | to GND | | 50 | 150 | 400 | kΩ |
| **Pin RXD** | | | | | | | |
| $I_{OH}$ | HIGH-level output current | $V_{RXD} = V_{IO} - 0.4$ V | | −15 | - | −1 | mA |
| $I_{OL}$ | LOW-level output current | $V_{RXD}$ = 0.4 V | | 1 | - | 15 | mA |
| $V_{OH}$ | HIGH-level output voltage | $I_{OH(RXD)}$ = −1 mA | | $V_{IO}$ − 0.4 | - | $V_{IO}$ | V |
| $V_{OL}$ | LOW-level output voltage | $I_{OL(RXD)}$ = 1 mA | | - | - | 0.4 | V |
| $V_O$ | output voltage | when undervoltage on $V_{IO}$; $V_{CC} \geq$ 4.75 V; $R_L$ = 100 kΩ to GND | | - | - | 500 | mV |
| | | $V_{CC} = V_{BAT} = V_{BUF}$ = 0 V; $R_L$ = 100 kΩ to $V_{IO}$ | | $V_{IO}$ − 500 | - | $V_{IO}$ | mV |
| **Pin RSTN** | | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | | | $0.7V_{IO}$ | - | 5.5 | V |
| $V_{IL}$ | LOW-level input voltage | | | −0.3 | - | $0.3V_{IO}$ | V |
| $I_{IH}$ | HIGH-level input current | $V_{RSTN} = V_{IO}$ | | −1 | - | +1 | µA |
| $I_{IL}$ | LOW-level input current | $V_{RSTN} = 0.3V_{IO}$ | | −300 | - | −30 | µA |
| **Pins TRXD0 and TRXD1** | | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | | | $0.7V_{BUF}$ | - | 5.5 | V |
| $V_{IL}$ | LOW-level input voltage | | | −0.3 | - | $0.3V_{BUF}$ | V |
| $V_{OL}$ | LOW-level output voltage | $R_{pu}$ = 200 Ω | | −0.3 | - | +0.8 | V |


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**Table 14. Static characteristics** *...continued*

*All parameters are guaranteed for $V_{BAT}$ = 4.45 V to 60 V; $V_{CC}$ = 4.45 V to 5.25 V; $V_{BUF}$ = 4.45 V to 5.25 V; $V_{IO}$ = 2.55 V to 5.25 V; $T_{vj}$ = −40 °C to +150 °C; $C_{bus}$ = 100 pF; $R_{bus}$ = 40 Ω to 55 Ω; $C_{RXD}$ = 15 pF and $C_{TRXD0}$ = $C_{TRXD1}$ = 50 pF unless otherwise specified. All voltages are defined with respect to ground; positive currents flow into the IC.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $C_i$ | input capacitance | with respect to all other pins at GND; $V_{TXD}$ = 100 mV; f = 5 MHz | [3] | - | - | 15 | pF |
| $R_{pu}$ | pull-up resistance | to $V_{BUF}$ | | 2.5 | 5 | 10 | kΩ |
| **Pins BP and BM** | | | | | | | |
| $V_{IH(dif)}$ | differential HIGH-level input voltage | AS_Normal; −10 V ≤ $V_{cm}$ ≤ +15 V | [4] | 150 | - | 300 | mV |
| $V_{IL(dif)}$ | differential LOW-level input voltage | AS_Normal; −10 V ≤ $V_{cm}$ ≤ +15 V | [4] | −300 | - | −150 | mV |
| | | AS_Standby; AS_Sleep; −10 V ≤ $V_{cm}$ ≤ +15 V | [4] | −400 | - | −125 | mV |
| $\Delta V_{i(dif)(H-L)}$ | differential input voltage difference between HIGH-level and LOW-level | $V_{cm}$ = 2.5 V; AS_Normal | [4] | −30 | - | +30 | mV |
| $V_{OH(dif)}$ | differential HIGH-level output voltage | 4.75 V ≤ $V_{BUF}$ ≤ 5.25 V | | 900 | - | 2000 | mV |
| | | 4.45 V ≤ $V_{BUF}$ ≤ 5.25 V | | 700 | - | 2000 | mV |
| $V_{OL(dif)}$ | differential LOW-level output voltage | 4.75 V ≤ $V_{BUF}$ ≤ 5.25 V | | −2000 | - | −900 | mV |
| | | 4.45 V ≤ $V_{BUF}$ ≤ 5.25 V | | −2000 | - | −700 | mV |
| $V_{o(idle)(BP)}$ | idle output voltage on pin BP | Branch_Normal | | 0.4$V_{BUF}$ | - | 0.6$V_{BUF}$ | V |
| | | Branch_LowPower | | −0.1 | - | +0.1 | V |
| $V_{o(idle)(BM)}$ | idle output voltage on pin BM | Branch_Normal | | 0.4$V_{BUF}$ | - | 0.6$V_{BUF}$ | V |
| | | Branch_LowPower | | −0.1 | - | +0.1 | V |
| $I_{o(idle)BP}$ | idle output current on pin BP | −60 V ≤ $V_{BP}$ ≤ +60 V; no bus load | | −7.5 | - | +7.5 | mA |
| $I_{o(idle)BM}$ | idle output current on pin BM | −60 V ≤ $V_{BM}$ ≤ +60 V; no bus load | | −7.5 | - | +7.5 | mA |
| $V_{o(idle)(dif)}$ | differential idle output voltage | | | −25 | 0 | +25 | mV |
| $\lvert V_{i(dif)det(act)} \rvert$ | activity detection differential input voltage (absolute value) | AS_Normal; −10 V ≤ $V_{cm}$ ≤ +15 V | [4] | 150 | - | 300 | mV |
| $V_{cm(bus)(DATA_0)}$ | DATA_0 bus common-mode voltage | Branch_Transmit | | 0.4$V_{BUF}$ | - | 0.65 × $V_{BUF}$ | V |
| $V_{cm(bus)(DATA_1)}$ | DATA_1 bus common-mode voltage | Branch_Transmit | | 0.4$V_{BUF}$ | - | 0.65 × $V_{BUF}$ | V |
| $R_i$ | input resistance | $R_{bus}$ = ∞ Ω | | 10 | 20 | 40 | kΩ |
| $R_{i(dif)(BP-BM)}$ | differential input resistance between pin BP and pin BM | $R_{bus}$ = ∞ Ω | | 20 | 40 | 80 | kΩ |
| $Z_{o(eq)TX}$ | transmitter equivalent output impedance | $C_{bus}$ = 100 pF; $R_{bus}$ = 40 Ω or 100 Ω | [5] | 10 | - | 600 | Ω |
| $C_{i(BP)}$ | input capacitance on pin BP | with respect to all other pins at GND; $V_{BP}$ = 100 mV; f = 5 MHz | [3] | - | - | 15 | pF |
| $C_{i(BM)}$ | input capacitance on pin BM | with respect to all other pins at GND; $V_{BM}$ = 100 mV; f = 5 MHz | [3] | - | - | 15 | pF |
| $C_{i(dif)(BP-BM)}$ | differential input capacitance between pin BP and pin BM | $V_{BP}$ = 100 mV; $V_{BM}$ = 100 mV; f = 5 MHz | [3] | - | - | 5 | pF |


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**Table 14. Static characteristics** *...continued*

*All parameters are guaranteed for $V_{BAT}$ = 4.45 V to 60 V; $V_{CC}$ = 4.45 V to 5.25 V; $V_{BUF}$ = 4.45 V to 5.25 V; $V_{IO}$ = 2.55 V to 5.25 V; $T_{vj}$ = −40 °C to +150 °C; $C_{bus}$ = 100 pF; $R_{bus}$ = 40 Ω to 55 Ω; $C_{RXD}$ = 15 pF and $C_{TRXD0}$ = $C_{TRXD1}$ = 50 pF unless otherwise specified. All voltages are defined with respect to ground; positive currents flow into the IC.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $I_{LI(BP)}$ | input leakage current on pin BP | AS_PowerOff; $V_{BP}$ = $V_{BM}$; 0 V ≤ $V_{BP}$ ≤ 5 V | | −5 | 0 | +5 | µA |
| | | loss of ground; $V_{BP}$ = $V_{BM}$ = 0 V; all other pins connected to 16 V via 0 Ω | [3] | −1600 | - | +1600 | µA |
| $I_{LI(BM)}$ | input leakage current on pin BM | AS_PowerOff; $V_{BP}$ = $V_{BM}$; 0 V ≤ $V_{BM}$ ≤ 5 V | | −5 | 0 | +5 | µA |
| | | loss of ground; $V_{BP}$ = $V_{BM}$ = 0 V; all other pins connected to 16 V via 0 Ω | [3] | −1600 | - | +1600 | µA |
| $\lvert I_{O(sc)} \rvert$ | short-circuit output current (absolute value) | on pin BP; −5 V ≤ $V_{BP}$ ≤ +60 V; $R_{sc}$ ≤ 1 Ω; $t_{sc}$ ≥ 1500 µs | [6][8] | - | - | 72 | mA |
| | | on pin BP; −5 V ≤ $V_{BP}$ ≤ +27 V; $R_{sc}$ ≤ 1 Ω; $t_{sc}$ ≥ 1500 µs | [6][8] | - | - | 60 | mA |
| | | on pin BM; −5 V ≤ $V_{BM}$ ≤ +60 V; $R_{sc}$ ≤ 1 Ω; $t_{sc}$ ≥ 1500 µs | [6][8] | - | - | 72 | mA |
| | | on pin BM; −5 V ≤ $V_{BM}$ ≤ +27 V; $R_{sc}$ ≤ 1 Ω; $t_{sc}$ ≥ 1500 µs | [6][8] | - | - | 60 | mA |
| | | on pins BP and BM; $V_{BP}$ = $V_{BM}$; $R_{sc}$ ≤ 1 Ω; $t_{sc}$ ≥ 1500 µs | [7][8] | - | - | 60 | mA |
| **Pin INH** | | | | | | | |
| $V_{OH}$ | HIGH-level output voltage | $I_{INH}$ = −0.2 mA: AS_Normal; AS_Standby; AS_Reset | | $V_{BAT}$ − 0.8 | - | $V_{BAT}$ | V |
| $I_L$ | leakage current | AS_Sleep; AS_PowerOff | | −3 | - | +3 | µA |
| $I_{O(sc)}$ | short-circuit output current | $V_{INH}$ = 0 V; AS_Normal; AS_Standby; AS_Reset | | −7 | - | −1 | mA |
| **Pin LWU** | | | | | | | |
| $V_{th(wake)LWU}$ | wake-up threshold voltage on pin LWU | AS_Sleep; AS_Standby | | 2 | - | 3.75 | V |
| $V_{hys(wake)LWU}$ | wake-up hysteresis voltage on pin LWU | | | 0.3 | - | 1.2 | V |
| $I_{IL}$ | LOW-level input current | $V_{LWU}$ = 2 V for t > $t_{det(wake)(LWU)}$ | | 3 | - | 11 | µA |
| | | $V_{LWU}$ = 0 V | | −2 | - | −0.3 | µA |
| $I_{IH}$ | HIGH-level input current | $V_{LWU}$ = 3.75 V for t > $t_{det(wake)(LWU)}$; 4.75 V ≤ $V_{BAT}$ ≤ +60 V | | −11 | - | −3 | µA |
| | | $V_{LWU}$ = $V_{BAT}$ | | 0.2 | - | 1.2 | µA |
| **Pin SDO** | | | | | | | |
| $V_{OH}$ | HIGH-level output voltage | $I_{OH(SDO)}$ = −0.5 mA | | $V_{IO}$ − 0.4 | - | $V_{IO}$ | V |
| $V_{OL}$ | LOW-level output voltage | $I_{OL(SDO)}$ = 0.5 mA | | - | - | 0.4 | V |
| $I_{OH}$ | HIGH-level output current | $V_{SDO}$ = $V_{IO}$ − 0.4 V | | −8 | −2 | −0.5 | mA |
| $I_{OL}$ | LOW-level output current | $V_{SDO}$ = 0.4 V | | 0.5 | 2 | 8 | mA |
| $I_L$ | leakage current | SCSN HIGH | | −5 | - | +5 | µA |


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**Table 14. Static characteristics** *...continued*

*All parameters are guaranteed for $V_{BAT}$ = 4.45 V to 60 V; $V_{CC}$ = 4.45 V to 5.25 V; $V_{BUF}$ = 4.45 V to 5.25 V; $V_{IO}$ = 2.55 V to 5.25 V; $T_{vj}$ = −40 °C to +150 °C; $C_{bus}$ = 100 pF; $R_{bus}$ = 40 Ω to 55 Ω; $C_{RXD}$ = 15 pF and $C_{TRXD0}$ = $C_{TRXD1}$ = 50 pF unless otherwise specified. All voltages are defined with respect to ground; positive currents flow into the IC.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_O$ | output voltage | when undervoltage on $V_{IO}$; $V_{CC} \geq 4.75$ V; $R_L$ = 100 kΩ to GND | - | - | 500 | mV |
| | | $V_{CC}$ = $V_{BAT}$ = $V_{BUF}$ = 0 V; $R_L$ = 100 kΩ to GND | - | - | 500 | mV |
| **Pin SDI** | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | | $0.7V_{IO}$ | - | 5.5 | V |
| $V_{IL}$ | LOW-level input voltage | | −0.3 | - | $0.3V_{IO}$ | V |
| $R_{pd}$ | pull-down resistance | to GND | 50 | 150 | 400 | kΩ |
| **Pin SCSN** | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | | $0.7V_{IO}$ | - | 5.5 | V |
| $V_{IL}$ | LOW-level input voltage | | −0.3 | - | $0.3V_{IO}$ | V |
| $I_{IH}$ | HIGH-level input current | $V_{SCSN}$ = $V_{IO}$ | −1 | - | +1 | µA |
| $I_{IL}$ | LOW-level input current | $V_{SCSN}$ = $0.3V_{IO}$ | −15 | - | −3 | µA |
| **Pin SCLK** | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | | $0.7V_{IO}$ | - | 5.5 | V |
| $V_{IL}$ | LOW-level input voltage | | −0.3 | - | $0.3V_{IO}$ | V |
| $R_{pd}$ | pull-down resistance | to GND | 50 | 150 | 400 | kΩ |
| **Pin INTN** | | | | | | |
| $V_{OL}$ | LOW-level output voltage | $I_{OL(INTN)}$ = 0.5 mA | - | - | 0.4 | V |
| $V_O$ | output voltage | when undervoltage on $V_{IO}$; $V_{CC} \geq 4.75$ V; $R_L$ = 100 kΩ to GND | - | - | 500 | mV |
| | | $V_{CC}$ = $V_{BAT}$ = $V_{BUF}$ = 0 V; $R_L$ = 100 kΩ to GND | - | - | 500 | mV |
| **Temperature protection** | | | | | | |
| $T_{j(warn)}$ | warning junction temperature | | 155 | - | 190 | °C |
| $T_{j(high)}$ | high junction temperature | | 165 | - | 200 | °C |
| $\Delta T_{j(high-warn)}$ | difference between high and warning junction temperature | | 10 | - | 45 | °C |

[1] Specified current is the sum of currents $I_{CC1}$ and $I_{CC2}$.

[2] These values are guaranteed under the condition that the internal digital block is supplied from $V_{BAT}$.

[3] Guaranteed by design.

[4] $V_{cm}$ is the BP/BM common mode voltage.

[5] $Z_{o(eq)(TX)} = 50\ \Omega \times (V_{bus(100)} - V_{bus(40)})/(2.5 \times V_{bus(40)} - V_{bus(100)})$ where:
- $V_{bus(100)}$ is the differential output voltage on a load of 100 Ω and 100 pF in parallel
- $V_{bus(40)}$ is the differential output voltage on a load of 40 Ω and 100 pF in parallel when driving a DATA_1.

[6] $R_{sc}$ is the short-circuit resistance; voltage difference between bus pins BP and BM is 60 V max.

[7] $R_{sc}$ is the short-circuit resistance between BP and BM.

[8] $t_{sc}$ is the minimum duration of the short-circuit


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# 10. Dynamic characteristics

**Table 15. Dynamic characteristics**

*All parameters are guaranteed for $V_{BAT}$ = 4.45 V to 60 V; $V_{CC}$ = 4.45 V to 5.25 V; $V_{BUF}$ = 4.45 V to 5.25 V; $V_{IO}$ = 2.55 V to 5.25 V; $T_{vj}$ = −40 °C to + 150 °C; $R_{bus}$ = 40 Ω, $C_{bus}$ = 100 pF; $C_{RXD}$ = 15 pF; $C_{TRXD0}$ = $C_{TRXD1}$ = 50 pF and $C_{SDO}$ = 50 pF unless otherwise specified. All voltages are defined with respect to ground; positive currents flow into the IC.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Undervoltage detection** | | | | | | |
| $t_{det(uv)(VBAT)}$ | undervoltage detection time on pin $V_{BAT}$ | $V_{BAT}$ = 4.35 V | 5 | - | 150 | µs |
| $t_{rec(uv)(VBAT)}$ | undervoltage recovery time on pin $V_{BAT}$ | $V_{BAT}$ = 4.85 V | 5 | - | 150 | µs |
| $t_{det(uv)(VCC)}$ | undervoltage detection time on pin $V_{CC}$ | $V_{CC}$ = 4.35 V | 5 | - | 100 | µs |
| $t_{rec(uv)(VCC)}$ | undervoltage recovery time on pin $V_{CC}$ | $V_{CC}$ = 4.85 V | 5 | - | 100 | µs |
| $t_{det(uv)(VBUF)}$ | undervoltage detection time on pin $V_{BUF}$ | $V_{BUF}$ = 4.10 V | 5 | - | 100 | µs |
| $t_{rec(uv)(VBUF)}$ | undervoltage recovery time on pin $V_{BUF}$ | $V_{BUF}$ = 4.6 V | 5 | - | 100 | µs |
| $t_{det(uv)(VIO)}$ | undervoltage detection time on pin $V_{IO}$ | $V_{IO}$ = 2.45 V | 5 | - | 100 | µs |
| $t_{rec(uv)(VIO)}$ | undervoltage recovery time on pin $V_{IO}$ | $V_{IO}$ = 2.9 V | 5 | - | 100 | µs |
| $t_{to(uvd)(VCC)}$ | undervoltage detection time-out time on pin $V_{CC}$ | | 100 | - | 670 | ms |
| $t_{to(uvd)(VIO)}$ | undervoltage detection time-out time on pin $V_{IO}$ | | 100 | - | 670 | ms |
| $t_{to(uvr)(VCC)}$ | undervoltage recovery time-out time on pin $V_{CC}$ | | 1 | - | 5 | ms |
| $t_{to(uvr)(VIO)}$ | undervoltage recovery time-out time on pin $V_{IO}$ | | 1 | - | 5 | ms |
| **SPI** | | | | | | |
| $t_{cy(clk)}$ | clock cycle time | | 0.5 | - | 100 | µs |
| $t_{SPILEAD}$ | SPI enable lead time | | 250 | - | - | ns |
| $t_{SPILAG}$ | SPI enable lag time | | 250 | - | - | ns |
| $t_{su(D)}$ | data input set-up time | | 150 | - | - | ns |
| $t_{h(D)}$ | data input hold time | | 100 | - | - | ns |
| $t_{d(SCLK-SDO)}$ | delay time from SCLK to SDO | | - | - | 200 | ns |
| $t_{WH(S)}$ | chip select pulse width HIGH | | 10 | - | - | µs |
| $t_{d(SCSNHL-SDOL)}$ | SCSN falling edge to SDO LOW-level delay time | | - | - | 250 | ns |
| $t_{d(SCSNLH-SDOZ)}$ | SCSN rising edge to SDO three-state delay time | | - | - | 500 | ns |


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**Table 15. Dynamic characteristics** *...continued*

*All parameters are guaranteed for $V_{BAT}$ = 4.45 V to 60 V; $V_{CC}$ = 4.45 V to 5.25 V; $V_{BUF}$ = 4.45 V to 5.25 V; $V_{IO}$ = 2.55 V to 5.25 V; $T_{vj}$ = −40 °C to + 150 °C; $R_{bus}$ = 40 Ω, $C_{bus}$ = 100 pF; $C_{RXD}$ = 15 pF; $C_{TRXD0}$ = $C_{TRXD1}$ = 50 pF and $C_{SDO}$ = 50 pF unless otherwise specified. All voltages are defined with respect to ground; positive currents flow into the IC.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Transmit path** | | | | | | | |
| $t_{d(TXD-bus)}$ | delay time from TXD to bus | AS_Normal; see Figure 10 | [1] | | | | |
| | | DATA_0 | | - | - | 75 | ns |
| | | DATA_1 | | - | - | 75 | ns |
| $\Delta t_{d(TXD-bus)}$ | delay time difference from TXD to bus | between DATA_0 and DATA_1; AS_Normal | [1] [2] | −5 | - | +5 | ns |
| $t_{d(TXD-TRXD)}$ | delay time from TXD to TRXD | AS_Normal; see Figure 10 | [1] | | | | |
| | | DATA_0 | | - | - | 60 | ns |
| | | DATA_1 | | - | - | 60 | ns |
| $\Delta t_{d(TXD-TRXD)}$ | delay time difference from TXD to TRXD | between DATA_0 and DATA_1; AS_Normal | [1] | −5 | - | +5 | ns |
| $t_{d(TRXD-bus)}$ | delay time from TRXD to bus | AS_Normal; see Figure 12 | | | | | |
| | | DATA_0 | | - | - | 75 | ns |
| | | DATA_1 | | - | - | 75 | ns |
| $\Delta t_{d(TRXD-bus)}$ | delay time difference from TRXD to bus | between DATA_0 and DATA_1; AS_Normal | [2] | −5 | - | +5 | ns |
| $t_{d(TXEN-busact)}$ | delay time from TXEN to bus active | AS_Normal; from idle to active | | - | - | 150 | ns |
| $t_{d(TXEN-busidle)}$ | delay time from TXEN to bus idle | AS_Normal; from active to idle | | - | - | 150 | ns |
| $t_{d(TXEN-RXD)}$ | delay time from TXEN to RXD | | | - | - | 150 | ns |
| $t_{d(TRXD-busact)}$ | delay time from TRXD to bus active | $t_{det(act)(TRXD)} + t_{d(TRXD-bus)}$ | | - | - | 275 | ns |
| $t_{d(TRXD-busidle)}$ | delay time from TRXD to bus idle | $t_{det(idle)(TRXD)} + t_{d(TRXD-bus)}$ | | - | - | 275 | ns |
| $t_{d(busact-TRXD)}$ | delay time from bus active to TRXD | $t_{det(act)(bus)} + t_{d(bus-TRXD)}$ | | - | - | 285 | ns |
| $t_{d(busidle-TRXD)}$ | delay time from bus idle to TRXD | $t_{det(idle)(bus)} + t_{d(bus-TRXD)}$ | | - | - | 275 | ns |
| $t_{d(TRXDact-RXD)}$ | delay time from TRXD activity detection to RXD | $t_{det(act)(TRXD)} + t_{d(TRXD-RXD)}$ | | - | - | 260 | ns |
| $t_{d(busact-bus)}$ | delay time from bus active to bus | from one branch to another, including activity detection time; $t_{det(act)(bus)} + t_{d(bus-bus)}$ | | - | - | 310 | ns |
| $t_{d(busidle-bus)}$ | delay time from bus idle to bus | from one branch to another, including idle detection time; $t_{det(idle)(bus)} + t_{d(bus-bus)}$ | | - | - | 300 | ns |
| **Receive path** | | | | | | | |
| $t_{d(bus-TRXD)}$ | delay time from bus to TRXD | AS_Normal; see Figure 11 | | | | | |
| | | DATA_0 | | - | - | 75 | ns |
| | | DATA_1 | | - | - | 75 | ns |
| $\Delta t_{d(bus-TRXD)}$ | delay time difference from bus to TRXD | between DATA_0 and DATA_1 AS_Normal; $V_{cm}$ = 2.5 V $R_{pu}$ = 200 Ω | [2] [3] | −5 | - | +5 | ns |


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**Table 15. Dynamic characteristics** *...continued*

*All parameters are guaranteed for $V_{BAT}$ = 4.45 V to 60 V; $V_{CC}$ = 4.45 V to 5.25 V; $V_{BUF}$ = 4.45 V to 5.25 V; $V_{IO}$ = 2.55 V to 5.25 V; $T_{vj}$ = −40 °C to + 150 °C; $R_{bus}$ = 40 Ω, $C_{bus}$ = 100 pF; $C_{RXD}$ = 15 pF; $C_{TRXD0}$ = $C_{TRXD1}$ = 50 pF and $C_{SDO}$ = 50 pF unless otherwise specified. All voltages are defined with respect to ground; positive currents flow into the IC.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $t_{d(bus-RXD)}$ | delay time from bus to RXD | AS_Normal; see Figure 11 | | | | | |
| | | DATA_0 | | - | - | 75 | ns |
| | | DATA_1 | | - | - | 75 | ns |
| $\Delta t_{d(bus-RXD)}$ | delay time difference from bus to RXD | between DATA_0 and DATA_1 AS_Normal; $V_{cm}$ = 2.5 V | [2] [3] | −5 | - | +5 | ns |
| $t_{d(TRXD-RXD)}$ | delay time from TRXD to RXD | AS_Normal; see Figure 12 | | | | | |
| | | DATA_0 | | - | - | 60 | ns |
| | | DATA_1 | | - | - | 60 | ns |
| $\Delta t_{d(TRXD-RXD)}$ | delay time difference from TRXD to RXD | between DATA_0 and DATA_1 AS_Normal | | −5 | - | +5 | ns |
| $t_{d(TXD-RXD)}$ | delay time from TXD to RXD | AS_Normal; see Figure 10 | [1] | | | | |
| | | DATA_0 | | - | 30 | 60 | ns |
| | | DATA_1 | | - | 30 | 60 | ns |
| $t_{d(bus-bus)}$ | delay time from bus to bus | from one branch to another AS_Normal; see Figure 11 | | | | | |
| | | DATA_0 | | - | - | 100 | ns |
| | | DATA_1 | | - | - | 100 | ns |
| $\Delta t_{d(bus-bus)}$ | delay time difference from bus to bus | between DATA_0 and DATA_1 AS_Normal | | −8 | - | +8 | ns |
| **Bus slope** | | | | | | | |
| $t_{r(dif)(bus)}$ | bus differential rise time | DATA_0 to DATA_1; 20 % to 80 % | | 6 | - | 18.75 | ns |
| | | DATA_0 to idle; −300 mV to −30 mV | | - | - | 30 | ns |
| $t_{f(dif)(bus)}$ | bus differential fall time | DATA_1 to DATA_0; 20 % to 80 % | | 6 | - | 18.75 | ns |
| | | DATA_1 to idle; 300 mV to 30 mV | | - | - | 30 | ns |
| | | idle to DATA_0; −30 mV to −300 mV | | - | - | 30 | ns |
| $\Delta t_{(r-f)(dif)}$ | difference between differential rise and fall time | between DATA_0 and DATA_1 | | −3 | - | +3 | ns |
| **Pin RXD** | | | | | | | |
| $t_r$ | rise time | 20 % to 80 % | | - | - | 9 | ns |
| $t_f$ | fall time | 80 % to 20 % | | - | - | 9 | ns |
| $t_{(r+f)}$ | sum of rise and fall time | 20 % to 80 % and 80 % to 20 % | | - | - | 13 | ns |
| $\Delta t_{(r-f)}$ | difference between rise and fall time | 20 % to 80 % | | −5 | - | +5 | ns |
| **Pin RSTN** | | | | | | | |
| $t_{det(rst)}$ | reset detection time | | | 5 | - | 20 | µs |
| **Pin BGE** | | | | | | | |
| $t_{d(BGE-busact)}$ | delay time from BGE to bus active | activity detected on TXEN | | - | - | 100 | ns |
| $t_{d(BGE-busidle)}$ | delay time from BGE to bus idle | activity detected on TXEN | | - | - | 100 | ns |


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**Table 15. Dynamic characteristics** *...continued*

*All parameters are guaranteed for $V_{BAT}$ = 4.45 V to 60 V; $V_{CC}$ = 4.45 V to 5.25 V; $V_{BUF}$ = 4.45 V to 5.25 V; $V_{IO}$ = 2.55 V to 5.25 V; $T_{vj}$ = −40 °C to + 150 °C; $R_{bus}$ = 40 Ω, $C_{bus}$ = 100 pF; $C_{RXD}$ = 15 pF; $C_{TRXD0}$ = $C_{TRXD1}$ = 50 pF and $C_{SDO}$ = 50 pF unless otherwise specified. All voltages are defined with respect to ground; positive currents flow into the IC.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Activity detection** | | | | | | | |
| $t_{det(act)(TXEN)}$ | activity detection time on pin TXEN | AS_Normal; from idle to active | | 20 | - | 70 | ns |
| $t_{det(idle)(TXEN)}$ | idle detection time on pin TXEN | AS_Normal; from active to idle | | 20 | - | 70 | ns |
| $\Delta t_{det(act-idle)}$ | difference between active and idle detection time | | | | | | |
| | on pin TXEN | AS_Normal | | −25 | - | +25 | ns |
| | on pin TRXD | pins TRXD0 and TRXD1; AS_Normal | | −50 | - | +50 | ns |
| | on bus | AS_Normal | | −50 | - | +50 | ns |
| $t_{det(act)(TRXD)}$ | activity detection time on pin TRXD | pins TRXD0 and TRXD1; AS_Normal; from idle to active | | 100 | - | 200 | ns |
| $t_{det(idle)(TRXD)}$ | idle detection time on pin TRXD | pins TRXD0 and TRXD1; AS_Normal; from active to idle | | 100 | - | 200 | ns |
| $t_{det(act)(bus)}$ | activity detection time on bus pins | AS_Normal; from idle to active | | 100 | - | 210 | ns |
| $t_{det(idle)(bus)}$ | idle detection time on bus pins | AS_Normal; from active to idle | | 100 | - | 200 | ns |
| $t_{det(int)}$ | interrupt detection time | from interrupt detection to falling edge on INTN | | - | - | 100 | µs |
| $t_{INTNH(min)}$ | minimum INTN HIGH time | | | 10 | - | 40 | µs |
| **Wake-up detection** | | | | | | | |
| $t_{det(wake)DATA_0}$ | DATA_0 wake-up detection time | $-10\ V \leq V_{cm} \leq +15\ V$ | [3] | 1 | - | 4 | µs |
| $t_{det(wake)idle}$ | idle wake-up detection time | $-10\ V \leq V_{cm} \leq +15\ V$ | [3] | 1 | - | 4 | µs |
| $t_{det(wake)tot}$ | total wake-up detection time | $-10\ V \leq V_{cm} \leq +15\ V$ | [3] | 50 | - | 115 | µs |
| $t_{sup(int)wake}$ | wake-up interruption suppression time | $-10\ V \leq V_{cm} \leq +15\ V$ | [3] | 130 | - | 1000 | ns |
| $t_{d(bus)(wake-act)}$ | bus delay time from wake-up to active | | | - | - | 18 | µs |
| $t_{det(wake)(LWU)}$ | wake-up detection time on pin LWU | | | 2.9 | - | 175 | µs |
| $t_{det(wake)(TRXD)}$ | wake-up detection time on pin TRXD | falling edge on TRXD_0 or TRXD_1 | | 100 | - | 400 | ns |
| $t_{d(LWUwake-INHH)}$ | delay time from LWU wake-up to INH HIGH | falling edge on LWU to INH HIGH AS_Sleep; 5.5 V < $V_{BAT}$ < 27 V $R_{L(INH-GND)}$ = 100 kΩ | [4] | 2.9 | - | 100 | µs |
| | | falling edge on LWU to INH HIGH AS_Sleep; 27 V < $V_{BAT}$ < 60 V $R_{L(INH-GND)}$ = 100 kΩ | [4] | - | - | 175 | µs |
| $t_{d(buswake-INHH)}$ | delay time from bus wake-up to INH HIGH | AS_Sleep; $V_{BAT}$ > 5.5 V $R_{L(INH-GND)}$ = 100 kΩ | [4] | - | - | 55 | µs |
| $t_{d(buswake-INTNL)}$ | delay time from bus wake-up to INTN LOW | AS_Sleep; AS_Standby $V_{BAT}$ > 5.5 V | | - | - | 10 | µs |
| $t_{d(TRXDwake-INHH)}$ | delay time from TRXD wake-up to INH HIGH | falling edge on TRXDx to INH HIGH AS_Sleep; $R_{L(INH-GND)}$ = 100 kΩ | [4] | - | - | 55 | µs |


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**Table 15. Dynamic characteristics** *...continued*

*All parameters are guaranteed for $V_{BAT}$ = 4.45 V to 60 V; $V_{CC}$ = 4.45 V to 5.25 V; $V_{BUF}$ = 4.45 V to 5.25 V; $V_{IO}$ = 2.55 V to 5.25 V; $T_{vj}$ = −40 °C to + 150 °C; $R_{bus}$ = 40 Ω, $C_{bus}$ = 100 pF; $C_{RXD}$ = 15 pF; $C_{TRXD0}$ = $C_{TRXD1}$ = 50 pF and $C_{SDO}$ = 50 pF unless otherwise specified. All voltages are defined with respect to ground; positive currents flow into the IC.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Bus error diagnosis** | | | | | | |
| $t_{to(BFT)}$ | BFT time-out time | | 80 | - | 180 | ns |
| **Clamp detection** | | | | | | |
| $t_{detCL(bus)}$ | bus clamp detection time | | 650 | - | 2600 | µs |
| $t_{detCL(TRXD)}$ | TRXD clamp detection time | | 650 | - | 2600 | µs |
| $t_{detCL(TXEN)}$ | TXEN clamp detection time | | 650 | - | 2600 | µs |
| $t_{det(col)(TRXD)}$ | TRXD collision detection time | | 40 | - | 120 | ns |
| **Transition timing** | | | | | | |
| $t_{to_stargotosleep}$ | dStarGoToSleep time-out time | | 640 | - | 6400 | ms |
| $t_{t(bnorm-bdis)}$ | branch normal to branch disabled transition time | AS_Normal; after a host 'Branch_Disabled' command; rising edge on SCSN to transmitter deactivated | - | - | 1 | µs |
| $t_{t(bdis-bnorm)}$ | branch disabled to branch normal transition time | AS_Normal; after a host 'Branch_Normal' command; rising edge on SCSN to transmitter activated | - | - | 1 | µs |
| $t_{t(bnorm-btx2)}$ | branch normal to branch TxOnly2 transition time | AS_Normal; after a host 'Branch_TxOnly' command; rising edge on SCSN to deactivating receive function | - | - | 1 | µs |
| $t_{t(btx2-bnorm)}$ | branch TxOnly2 to branch normal transition time | AS_Normal; after a host 'Branch_Normal' command; rising edge on SCSN to activating receive function | - | - | 1 | µs |
| $t_{t(moch)}$ | mode change transition time | after host command AS_Sleep to AS_Standby rising edge on SCSN to rising edge on INH | - | - | 25 | µs |

[1] Sum of rise and fall times on TXD (20 % to 80 % on $V_{IO}$) is 9 ns (max).

[2] Guaranteed for $V_{bus(dif)}$ = ±300 mV and $V_{bus(dif)}$ = ±150 mV; $V_{bus(dif)}$ is the differential bus voltage, $V_{BP}$ - $V_{BM}$.

[3] $V_{cm}$ is the BP/BM common mode voltage ($V_{cm}$ = ($V_{BP}$ + $V_{BM}$)/2).

[4] Defined for $V_{INH}$ = 2 V.


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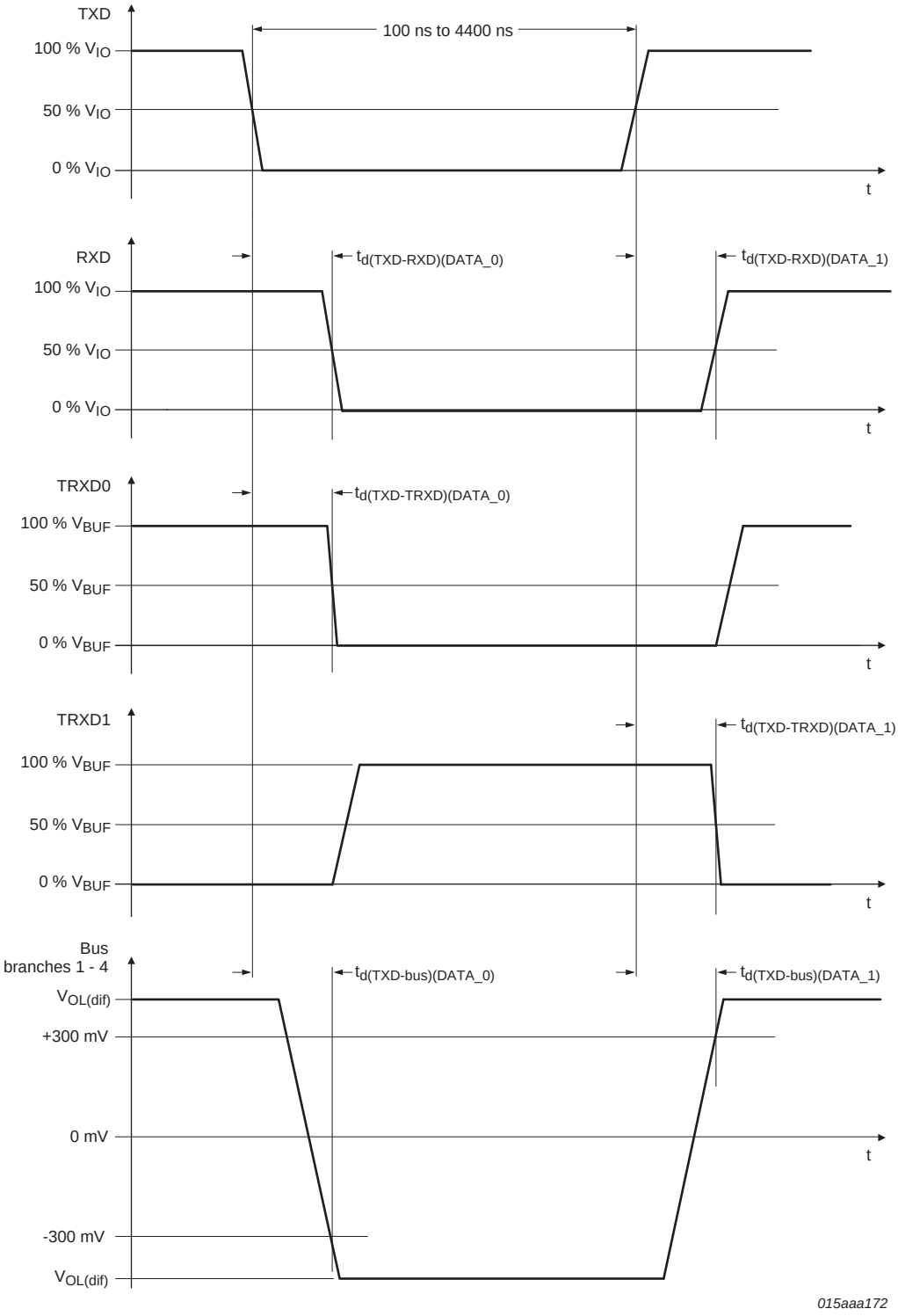
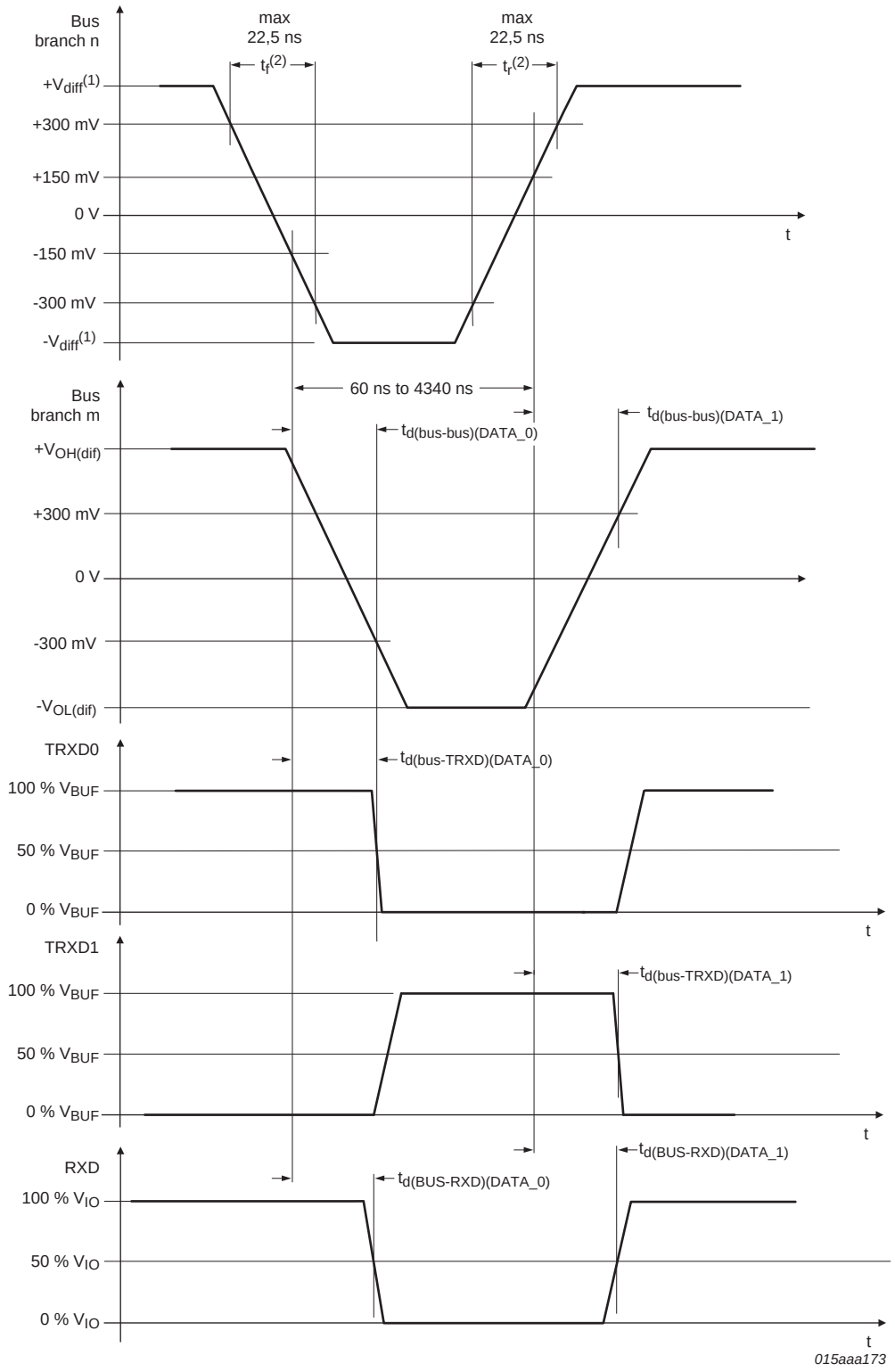



**Fig 10. Timing diagram when the CC interface is the input channel**


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(1) $V_{dif}$ = 400 mV to 3000 mV.

(2) $t_r$ and $t_f$, defined between ±300 mV, are both 22.5 ns for bus amplitudes of 800 mV (max), and lower for higher bus amplitudes.

**Fig 11. Timing diagram when one of the branches is the input channel**


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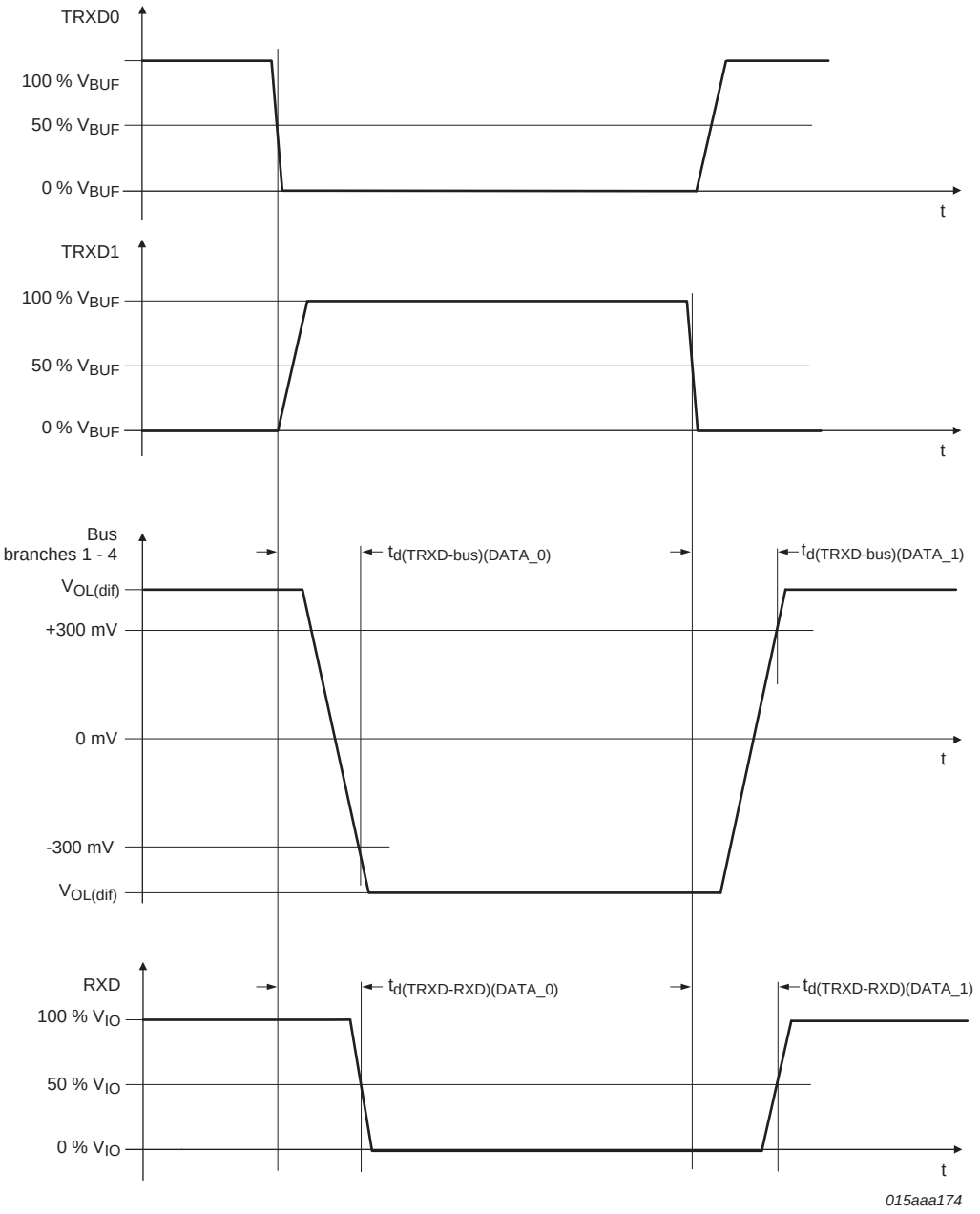



**Fig 12. Timing diagram when the internal bus (TRXD0/1) is the input channel**


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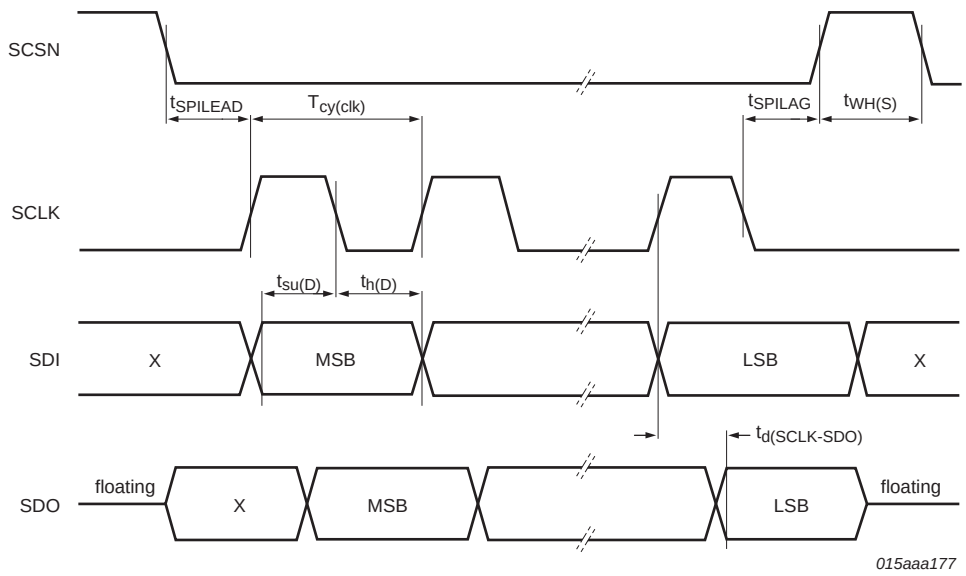



**Fig 13. SPI timing**

## 11. Application information

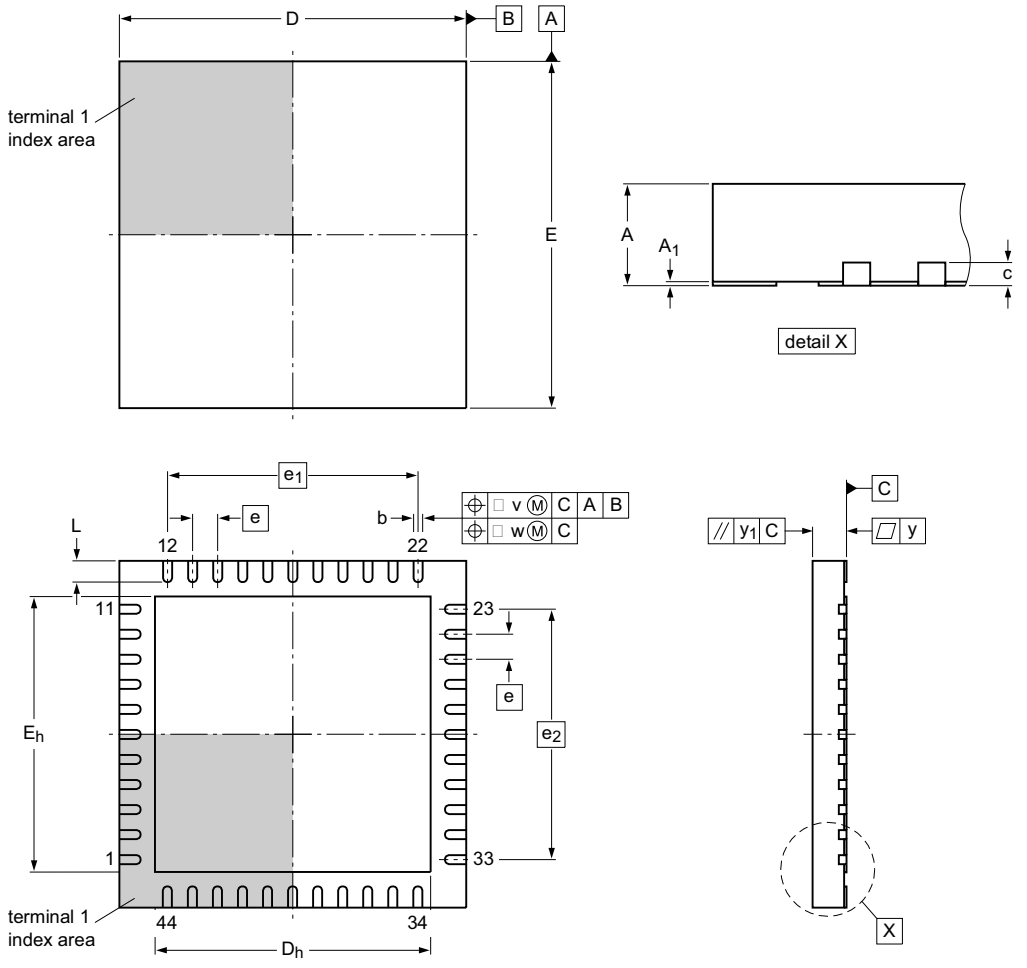
Further information on the application of the TJA1085 can be found in NXP application hints *AH1001_v1.0_TJA1085 FlexRay Active Star Coupler.*


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## 12. Package outline

**HVQFN44: plastic thermal enhanced very thin quad flat package; no leads**
**44 terminals; body 9 x 9 x 0.85 mm** **SOT1113-1**




Dimensions

| Unit | | $A^{(1)}$ | $A_1$ | b | c | $D^{(1)}$ | $D_h$ | $E^{(1)}$ | $E_h$ | e | $e_1$ | $e_2$ | L | v | w | y | $y_1$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | max | 1.00 | 0.05 | 0.35 | | 9.1 | 7.25 | 9.1 | 7.25 | | | | 0.63 | | | | |
| mm | nom | 0.85 | 0.03 | 0.30 | 0.2 | 9.0 | 7.15 | 9.0 | 7.15 | 0.65 | 6.5 | 6.5 | 0.55 | 0.1 | 0.05 | 0.08 | 01 |
| | min | 0.80 | 0.00 | 0.25 | | 8.9 | 7.05 | 8.9 | 7.05 | | | | 0.47 | | | | |

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

*sot1113-1_po*

| Outline version | References | | | European projection | Issue date |
|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | |
| SOT1113-1 | --- | --- | --- | | ~~09-07-17~~ 10-07-23 |

**Fig 14. Package outline SOT1113-1 (HVQFN44)**


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# 13. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

## 13.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

## 13.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

## 13.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities


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## 13.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 15) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 16 and 17

**Table 16. SnPb eutectic process (from J-STD-020D)**

| Package thickness (mm) | Package reflow temperature (°C) | |
|---|---|---|
| | Volume ($mm^3$) | |
| | < 350 | ≥ 350 |
| < 2.5 | 235 | 220 |
| ≥ 2.5 | 220 | 220 |

**Table 17. Lead-free process (from J-STD-020D)**

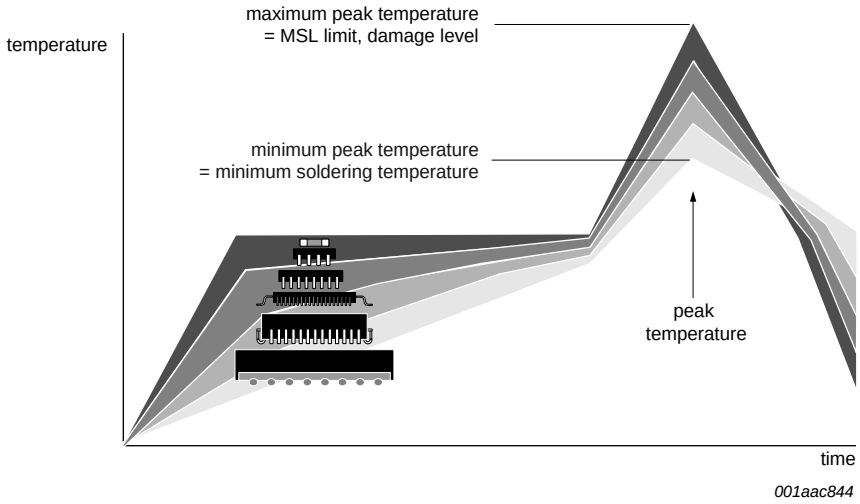
| Package thickness (mm) | Package reflow temperature (°C) | | |
|---|---|---|---|
| | Volume ($mm^3$) | | |
| | < 350 | 350 to 2000 | > 2000 |
| < 1.6 | 260 | 260 | 260 |
| 1.6 to 2.5 | 260 | 250 | 245 |
| > 2.5 | 250 | 245 | 245 |

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 15.


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MSL: Moisture Sensitivity Level

**Fig 15. Temperature profiles for large and small components**

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.


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# 14. Appendix: EPL 3.0.1/ISO17458-4 to TJA1085 parameter conversion

**Table 18. EPL 3.0.1/ISO17458-4 to TJA1085 conversion**

| EPL 3.0.1 | | | | TJA1085 | | | |
|---|---|---|---|---|---|---|---|
| **Symbol** | **Min** | **Max** | **Unit** | **Symbol** | **Min** | **Max** | **Unit** |
| dBusTx01 | 6 | 18.75 | ns | $t_{r(dif)(bus)}$ | 6 | 18.75 | ns |
| dBusTx10 | 6 | 18.75 | ns | $t_{f(dif)(bus)}$ | 6 | 18.75 | ns |
| uStarTxactive | 600 | 2000 | mV | $\|V_{OH(dif)}\|$, $\|V_{OL(dif)}\|$ | 900 | 2000 | mV |
| uStarTxidle | 0 | 30 | mV | $\|V_{o(idle)(dif)}\|$ | 0 | 25 | mV |
| dBranchRxActiveMax | 650 | 2600 | µs | $t_{detCL(bus)}$ | 650 | 2600 | µs |
| $R_{CM1}$, $R_{CM2}$ | 10 | 40 | kΩ | $R_i$ (pins BP and BM) | 10 | 40 | kΩ |
| uCM | −10 | +15 | V | $V_{cm}$[1] | −10 | +15 | V |
| $uStarUVV_{BAT}$ | 4 | 5.5 | V | $V_{uvd(VBAT)}$ | 4.45 | 4.715 | V |
| $uStarUVV_{CC}$ | 4 | - | V | $V_{uvd(VCC)}$ | 4.45 | 4.715 | V |
| $dStarUVV_{CC}$ | - | 1000 | ms | $t_{det(uv)(VCC)}$ | 5 | 100 | µs |
| $iBP_{Leak}$ | - | 25 | µA | $\|I_{LI(BP)}\|$ | - | 5 | µA |
| $iBM_{Leak}$ | - | 25 | µA | $\|I_{LI(BM)}\|$ | - | 5 | µA |
| $iBM_{GNDShortMax}$ | - | 60 | mA | $\|I_{O(sc)}\|$ (pin BM) | - | 60 | mA |
| $iBP_{GNDShortMax}$ | - | 60 | mA | $\|I_{O(sc)}\|$ (pin BP) | - | 60 | mA |
| $iBM_{BAT48ShortMax}$ | - | 72 | mA | $\|I_{O(sc)}\|$ (pin BM) | - | 72 | mA |
| $iBP_{BAT48ShortMax}$ | - | 72 | mA | $\|I_{O(sc)}\|$ (pin BP) | - | 72 | mA |
| $iBM_{BAT27ShortMax}$ | - | 60 | mA | $\|I_{O(sc)}\|$ (pin BM) | - | 60 | mA |
| $iBP_{BAT27ShortMax}$ | - | 60 | mA | $\|I_{O(sc)}\|$ (pin BP) | - | 60 | mA |
| functional class: Active Star - bus guardian interface | | | | implemented (see Section 2.4) | | | |
| dStarDelay10 | - | 150 | ns | $t_{d(bus-TRXD)} + t_{d(TRXD-bus)}$ | - | 150 | ns |
| dStarDelay01 | - | 150 | ns | $t_{d(bus-TRXD)} + t_{d(TRXD-bus)}$ | - | 150 | ns |
| dStarAsym | 0 | 8 | ns | $\|\Delta t_{d(bus-bus)}\|$ | - | 8 | ns |
| dStarAsym2 | 0 | 10 | ns | $\|\Delta t_{d(bus-TRXD)}\| + \|\Delta t_{d(TRXD-bus)}\|$ | - | 10 | ns |
| dStarSetUpDelay | - | 500 | ns | $t_{det(act)(TXEN)} + t_{d(TXD-TRXD)}$ | 20 | 110 | ns |
| | | | | $t_{det(act)(bus)} + t_{d(bus-TRXD)}$ | 100 | 285 | ns |
| dStarGoToSleep | 640 | 6400 | ms | $t_{to_stargotosleep}$ | 640 | 6400 | ms |
| dStarWakeupReactionTime | - | 70 | µs | $t_{d(bus)(wake-act)}$ | - | 18 | µs |
| device qualification according to AEC-Q100 (Rev. F) | | | | see Section 2.1 | | | |
| $T_{AMB_Class1}$ | −40 | +125 | °C | $T_{amb}$ | −40 | +125 | °C |
| $iBM_{-5VshortMax}$ | - | 60 | mA | $\|I_{O(sc)}\|$ (pin BM) | - | 60 | mA |
| $iBP_{-5VshortMax}$ | - | 60 | mA | $\|I_{O(sc)}\|$ (pin BP) | - | 60 | mA |
| functional class: Active Star - voltage regulator control | | | | implemented (see Section 2.4) | | | |
| $iBM_{BPShortMax}$ | - | 60 | mA | $\|I_{O(sc)}\|$ (BP to BM) | - | 60 | mA |
| $iBP_{BMShortMax}$ | - | 60 | mA | $\|I_{O(sc)}\|$ (BM to BP) | - | 60 | mA |
| $iBM_{BAT60ShortMax}$ | - | 90 | mA | $\|I_{O(sc)}\|$ (pin BP) | - | 72 | mA |
| $iBP_{BAT60ShortMax}$ | - | 90 | mA | $\|I_{O(sc)}\|$ (pin BM) | - | 72 | mA |
| uBias - Non-Low Power | 1800 | 3200 | mV | $V_{o(idle)(BP)}$, $V_{o(idle)(BM)}$[2] | 1800 | 3150 | mV |
| uBias - Low Power | −200 | +200 | mV | $V_{o(idle)(BP)}$, $V_{o(idle)(BM)}$[3] | −100 | +100 | mV |


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**Table 18. EPL 3.0.1/ISO17458-4 to TJA1085 conversion** *...continued*

| EPL 3.0.1 | | | | TJA1085 | | | |
|---|---|---|---|---|---|---|---|
| **Symbol** | **Min** | **Max** | **Unit** | **Symbol** | **Min** | **Max** | **Unit** |
| $dStarUVV_{BAT}$ | - | 1000 | ms | $t_{det(uv)(VBAT)}$ | 5 | 150 | µs |
| $uStarUVV_{IO}$ | 2 | - | V | $V_{uvd(VIO)}$ | 2.55 | 2.765 | V |
| $dStarUVV_{IO}$ | - | 1000 | ms | $t_{det(uv)(VIO)}$ | 5 | 100 | µs |
| $uINH1_{Not_Sleep}$ | uVBAT − 1 V | - | V | $V_{OH}$ (pin INH) | $V_{BAT}$ − 0.8 V | $V_{BAT}$ | V |
| $iINH1_{Leak}$ | - | 10 | µA | $I_L$ (pin INH) | −3 | +3 | µA |
| dStarTSSLengthChange | −450 | 0 | ns | $-(t_{det(act)(bus)} + t_{det(act)(TRXD)})$ | −410 | - | ns |
| | | | | $-t_{det(act)(bus)}$ | - | −100 | ns |
| dStarFES1LengthChange | 0 | 450 | ns | $t_{det(idle)(bus)}$ | 100 | - | ns |
| | | | | $t_{det(idle)(bus)} + t_{det(idle)(TRXD)}$ | - | 400 | ns |
| $dStarUVV_{Supply}$ | - | 1 | ms | $t_{det(uv)(VBUF)}$ | 5 | 100 | µs |
| $dStarRV_{Supply}$ | - | 10 | ms | $t_{rec(uv)(VBUF)}$ | 5 | 100 | µs |
| $uStarUVV_{Supply}$ | 4 | - | V | $V_{uvd(VBUF)}$ | 4.2 | 4.474 | V |
| $dStarRV_{BAT}$ | - | 10 | ms | $t_{rec(uv)(VBAT)}$ | 5 | 150 | µs |
| $dStarRV_{CC}$ | - | 10 | ms | $t_{rec(uv)(VCC)}$ | 5 | 100 | µs |
| $dStarRV_{IO}$ | - | 10 | ms | $t_{rec(uv)(VIO)}$ | 5 | 100 | µs |
| $dWU_{Interrupt}$ | 0.13 | 1 | µs | $t_{sup(int)wake}$ | 130 | 1000 | ns |
| $dWU_{0Detect}$ | 1 | 4 | µs | $t_{det(wake)DATA_0}$ | 1 | 4 | µs |
| $dWU_{IdleDetect}$ | 1 | 4 | µs | $t_{det(wake)idle}$ | 1 | 4 | µs |
| $dWU_{Timeout}$ | 48 | 140 | µs | $t_{det(wake)tot}$ | 50 | 115 | µs |
| dStarWakePulseFilter | 1 | 500 | µs | $t_{det(wake)(LWU)}$ | 2.9 | 175 | µs |
| $iBP_{LeakGND}$ | - | 1600 | µA | $\|I_{LI(BP)}\|$ | - | 1600 | µA |
| $iBM_{LeakGND}$ | - | 1600 | µA | $\|I_{LI(BM)}\|$ | - | 1600 | µA |
| $dStarWakeupReaction_{local}$ | - | 100 | µs | $t_{d(LWUwake-INHH)}$ | 0 | 100 | µs |
| dStarSymbolLengthChange | −300 | +450 | ns | $\Delta t_{det(act-idle)(bus)} + \Delta t_{det(act-idle)(TRXD)}$ | −100 | +100 | ns |
| functional class: Active Star - logic level adaptation | | | | implemented (see Section 2.4) | | | |
| functional class: Active Star - increased voltage amplitude transmitter | | | | implemented (see Section 2.4) | | | |
| $uESD_{EXT}$ | 6 | - | kV | $\|V_{ESD}\|$: HBM on pins BP and BM to GND | 8 | - | kV |
| | | | | $\|V_{ESD}\|$: HBM on pins LWU and $V_{BAT}$ to GND | 6 | - | kV |
| $uESD_{INT}$ | 2 | - | kV | $\|V_{ESD}\|$ (HBM on any other pin) | 4 | - | kV |
| $uESD_{IEC}$ | 6 | - | kV | IEC61000-4-2 on pins BP and BM to GND | 6 | - | kV |
| $uV_{BAT-WAKE}$ | - | 7 | V | $V_{BAT}$ | 4.75 | 60 | V |
| dBusTxai | - | 30 | ns | $t_{r(dif)(bus)}$ (DATA_0 to idle) | - | 30 | ns |
| dBusTxia | - | 30 | ns | $t_{f(dif)(bus)}$ (idle to DATA_0) | - | 30 | ns |
| valid operating modes when $V_{StarSupply}$ = nominal; $V_{BAT} \geq$ 7 V; $V_{CC}$ = nominal | | | | AS_Sleep, AS_Standby, AS_Normal | | | |


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**Table 18. EPL 3.0.1/ISO17458-4 to TJA1085 conversion** *...continued*

| EPL 3.0.1 | | | | TJA1085 | | | |
|---|---|---|---|---|---|---|---|
| **Symbol** | **Min** | **Max** | **Unit** | **Symbol** | **Min** | **Max** | **Unit** |
| valid operating modes when $V_{StarSupply}$ = nominal; $V_{BAT} \geq$ 5.5 V; $V_{CC}$ = nominal | | | | AS_Sleep, AS_Standby, AS_Normal | | | |
| dBusTxDif | - | 3 | ns | $\lvert\Delta t_{(r\text{-}f)(dif)}\rvert$ | - | 3 | ns |
| $R_{StarTransmitter}$ | product-specific | | | $Z_{o(eq)(TX)}$ | 10 | 600 | Ω |
| dStarSymbolEndLengthChange | 0 | 450 | ns | $t_{det(idle)(bus)}$ | 100 | - | ns |
| | | | | $t_{det(idle)(bus)} + t_{det(idle)(TRXD)}$ | - | 400 | ns |
| **Active star with communication controller interface** | | | | | | | |
| dStarRxAsym | - | 10 | ns | $\lvert\Delta t_{d(bus\text{-}TRXD)}\rvert + \lvert\Delta t_{d(TRXD\text{-}RXD)}\rvert$ | - | 10 | ns |
| dStarRx10 | - | 225 | ns | $t_{d(bus\text{-}TRXD)} + t_{d(TRXD\text{-}RXD)}$ | - | 135 | ns |
| dStarRx01 | - | 225 | ns | $t_{d(bus\text{-}TRXD)} + t_{d(TRXD\text{-}RXD)}$ | - | 135 | ns |
| dStarRxai | 50 | 550 | ns | $t_{det(idle)(bus)} + t_{d(bus\text{-}RXD)}$ | 100 | - | ns |
| | | | | $t_{det(idle)(bus)} + t_{d(bus\text{-}TRXD)} + t_{det(idle)(TRXD)} + t_{d(TRXD\text{-}RXD)}$ | - | 535 | ns |
| dStarRxia | 100 | 550 | ns | $t_{det(act)(bus)} + t_{d(bus\text{-}RXD)}$ | 100 | - | ns |
| | | | | $t_{det(act)(bus)} + t_{d(bus\text{-}TRXD)} + t_{det(act)(TRXD)} + t_{d(TRXD\text{-}RXD)}$ | - | 545 | ns |
| dStarTxAsym | - | 10 | ns | $\lvert\Delta t_{d(TXD\text{-}TRXD)}\rvert + \Delta\lvert t_{d(TRXD\text{-}bus)}\rvert$ | - | 10 | ns |
| dStarTx10 | - | 225 | ns | $t_{d(TXD\text{-}TRXD)} + t_{d(TRXD\text{-}bus)}$ | - | 135 | ns |
| dStarTx01 | - | 225 | ns | $t_{d(TXD\text{-}TRXD)} + t_{d(TRXD\text{-}bus)}$ | - | 135 | ns |
| dStarTxai | - | 550 | ns | $t_{det(idle)(TXEN)} + t_{d(TXD\text{-}TRXD)} + t_{det(idle)(TRXD)} + t_{d(TRXD\text{-}bus)}$ | - | 385 | ns |
| dStarTxia | - | 550 | ns | $t_{det(act)(TXEN)} + t_{d(TXD\text{-}TRXD)} + t_{det(act)(TRXD)} + t_{d(TRXD\text{-}bus)}$ | - | 385 | ns |
| $uV_{DIG\text{-}OUT\text{-}HIGH}$ | 80 | 100 | % | $V_{OH}$ (pin RXD) | $V_{IO}$ – 0.4 | $V_{IO}$ | V |
| $uV_{DIG\text{-}OUT\text{-}LOW}$ | - | 20 | % | $V_{OL}$ (pin RXD) | - | 0.4 | V |
| $uV_{DIG\text{-}IN\text{-}HIGH}$ | - | 70 | % | $V_{IH}$ (pins TXEN and BGE) | $0.7V_{IO}$ | 5.5 | V |
| $uV_{DIG\text{-}IN\text{-}LOW}$ | 30 | - | % | $V_{IL}$ (pins TXEN and BGE) | –0.3 | $0.3V_{IO}$ | V |
| uData0 | –300 | –150 | mV | $V_{IL(dif)}$ (pins BP and BM) | –300 | –150 | mV |
| uData1 | 150 | 300 | mV | $V_{IH(dif)}$ (pins BP and BM) | 150 | 300 | mV |
| uData1 - \|uData0\| | –30 | +30 | mV | $\Delta V_{i(dif)(H\text{-}L)}$ | –30 | +30 | mV |
| uStarLogic_1 | - | 60 | % | $V_{IH}$ (pin TXD) | $0.6V_{IO}$ | 5.5 | V |
| uStarLogic_0 | 40 | - | % | $V_{IL}$ (pin TXD) | –0.3 | $0.4V_{IO}$ | V |
| $dStarRxD_{R15}$ + $dStarRxD_{F15}$ | - | 13 | ns | $t_{(r+f)}$ (pin RXD) | - | 13 | ns |
| functional class: Active Star - communication controller interface | | | | implemented | | | |
| dStarTxRxai | - | 325 | ns | $t_{d(TXEN\text{-}RXD)}$ | - | 150 | ns |
| C_StarTxD | - | 10 | pF | $C_i$ (pin TXD) | - | 10 | pF |
| $uV_{DIG\text{-}OUT\text{-}UV}$ | - | 500 | mV | $V_O$ (pin RXD)[4] | - | 500 | mV |
| uData0_LP | –400 | –100 | mV | $V_{IL(dif)}$ (pins BP and BM) | –400 | –125 | mV |
| $uV_{DIG\text{-}OUT\text{-}OFF}$ | product specific | | | $V_O$ (pin RXD)[5] | $V_{IO}$ – 500 | $V_{IO}$ | mV |


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**Table 18. EPL 3.0.1/ISO17458-4 to TJA1085 conversion** *...continued*

| EPL 3.0.1 | | | | TJA1085 | | | |
|---|---|---|---|---|---|---|---|
| **Symbol** | **Min** | **Max** | **Unit** | **Symbol** | **Min** | **Max** | **Unit** |
| dStarTSSLengthChange_TxD_Bus | –450 | 0 | ns | $-(t_{det(act)(TXEN)} + t_{det(act)(TRXD)})$ | –250 | - | ns |
| | | | | $-t_{det(act)(TXEN)}$ | - | –20 | ns |
| dStarFES1LengthChange_TxD_Bus | 0 | 450 | ns | $t_{det(idle)(TXEN)}$ | 20 | - | ns |
| | | | | $t_{det(idle)(TXEN)} + t_{det(idle)(TRXD)}$ | - | 250 | ns |
| dStarSymbolLengthChange_TxD_Bus | –300 | +400 | ns | $\Delta t_{det(act-idle)(TXEN)} + \Delta t_{det(act-idle)(TRXD)}$ | –75 | +75 | ns |
| dStarTSSLengthChange_Bus_RxD | –450 | 0 | ns | $-(t_{det(act)(bus)} + t_{det(act)(TRXD)})$ | –410 | - | ns |
| | | | | $-t_{det(act)(bus)}$ | - | –100 | ns |
| dStarFES1LengthChange_Bus_RxD | 0 | 450 | ns | $t_{det(idle)(bus)}$ | 100 | - | ns |
| | | | | $t_{det(idle)(bus)} + t_{det(idle)(TRXD)}$ | - | 400 | ns |
| dStarSymbolLengthChange_Bus_RxD | –300 | +400 | ns | $\Delta t_{det(act-idle)(bus)} + \Delta t_{det(act-idle)(TRXD)}$ | –100 | +100 | ns |
| dStarActivityDetection | 100 | 250 | ns | $t_{det(act)(bus)}$ | 100 | 210 | ns |
| dStarIdleDetection | 50 | 200 | ns | $t_{det(idle)(bus)}$ | 100 | 200 | ns |
| $\lvert dStarRxD_{R15} - dStarRxD_{F15} \rvert$ | - | 5 | ns | $\lvert\Delta t_{(r-f)}\rvert$ (pin RXD) | - | 5 | ns |
| dStarTxActiveMax | 650 | 2600 | µs | $t_{detCL(TXEN)}$ | 650 | 2600 | µs |
| $dStarTx_{reaction}$ | - | 75 | ns | $t_{det(idle)(TXEN)}$ | 20 | 50 | ns |
| Active Star with host interface | | | | | | | |
| $dStarModeChange_{SPI}$ | - | 100 | µs | $t_{t(moch)}$ | - | 25 | µs |
| $dStarReactionTime_{SPI}$ | - | 200 | µs | $t_{det(int)}$ | - | 100 | µs |
| $uV_{DIG-OUT-HIGH}$ | 80 | 100 | % | $V_{OH}$ (pin SDO) | $V_{IO}$ – 0.4 | $V_{IO}$ | V |
| $uV_{DIG-OUT-LOW}$ | - | 20 | % | $V_{OL}$ (pins SDO, INTN) | - | 0.4 | V |
| $uV_{DIG-IN-HIGH}$ | - | 70 | % | $V_{IH}$ (pins SDI, SCSN, SCLK) | $0.7V_{IO}$ | 5.5 | V |
| $uV_{DIG-IN-LOW}$ | 30 | - | % | $V_{IL}$ (pins SDI, SCSN, SCLK) | –0.3 | $0.3V_{IO}$ | V |
| Functional class: Active Star - host interface | | | | implemented | | | |
| SPI | 0.01 | 1 | Mbit/s | $t_{cl(clk)}$ | 0.5 | 100 | µs |
| $uV_{DIG-OUT-UV}$ | - | 500 | mV | $V_O$ (pins SDO, INTN)[4] | - | 500 | mV |
| $uV_{DIG-OUT-OFF}$ | product specific | | | $V_O$ (pins SDO, INTN)[5] | - | 500 | mV |
| behavior when SCK not connected | | | | pull-down behavior on SCLK | | | |
| behavior when SDI not connected | | | | pull-down behavior on SDI | | | |
| behavior when SCSN not connected | | | | pull-up behavior on SCSN | | | |

[1] $V_{cm}$ is the BP/BM common mode voltage, $(V_{BP} + V_{BM})/2$, and is specified in conditions column for parameters $V_{IH(dif)}$ and $V_{IL(dif)}$ for pins BP and BM; see Table 14. $V_{cm}$ is tested on a receiving bus driver with a transmitting bus driver that has a ground offset voltage in the range –12.5 V to +12.5 V and transmits a 50/50 pattern.

[2] Min: $V_{o(idle)(BP)} = V_{o(idle)(BM)} = 0.4V_{BUF} = 0.4 \times 4.5\ V = 1800\ mV$; max value: $V_{o(idle)(BP)} = V_{o(idle)(BM)} = 0.6V_{BUF} = 0.6 \times 5.25\ V = 3150\ mV$; the nominal voltage is 2500 mV.

[3] The nominal voltage is 0 mV.

[4] When undervoltage on $V_{IO}$

[5] When $V_{CC} = V_{BAT} = V_{BUF} = 0$ V.


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## 15. Abbreviations

Table 19. Abbreviations

| Abbreviation | Description |
|---|---|
| AS | Active Star |
| CC | Communication Controller |
| ECU | Engine Control Unit |
| EMC | Electro Magnetic Compatibility |
| ESD | ElectroStatic Discharge |

## 16. References

**[1]** **EPL —** FlexRay Communications System Electrical Physical Layer Specification Version 3.0.1, FlexRay Consortium

**[2]** **ISO 17458-4:2013 —** Road vehicles - FlexRay Communications System part 4: Electrical physical layer specification

## 17. Revision history

Table 20. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| TJA1085 v.2 | 20160307 | Product data sheet | - | TJA1085 v.1 |
| Modifications: | • Section 1, Section 2.1, Section 14: text amended (specification updated)<br>• Table 12: Table note 1 added; measurement conditions and table notes changed for parameter $V_{ESD}$; no time limit removed from measurement conditions throughout; table reformatted<br>• Table 14: max. value changed for parameter $I_{CC}$<br>• Section 11 added<br>• Table 16, Table 17: JEDEC standard updated in table headers<br>• Table 19 updated<br>• Ref. 2 added | | | |
| TJA1085 v.1 | 20121023 | Product data sheet | - | - |


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| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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## 20. Contents


**1 General description . . . . . 1**
**2 Features and benefits . . . . . 1**
2.1 General . . . . . 1
2.2 Functional . . . . . 1
2.3 Robustness . . . . . 2
2.4 Active star functional classes . . . . . 2
**3 Ordering information . . . . . 2**
**4 Block diagram . . . . . 3**
**5 Pinning information . . . . . 4**
5.1 Pinning . . . . . 4
5.2 Pin description . . . . . 4
**6 Functional description . . . . . 6**
6.1 Supply voltage . . . . . 6
6.2 Host Control (HC) and Autonomous Power (AP) modes - APM flag . . . . . 6
6.3 Signal router . . . . . 6
6.3.1 TRXD collision . . . . . 6
6.4 Wake-up . . . . . 7
6.4.1 Remote wake-up . . . . . 7
6.4.1.1 Bus wake-up via wake-up pattern . . . . . 7
6.4.1.2 Bus wake-up via dedicated FlexRay data frame . . . . . 8
6.4.2 Local wake-up via pin LWU . . . . . 9
6.4.3 Wake-up via the TRXD0/1 interface . . . . . 9
6.5 Communication controller interface . . . . . 10
6.5.1 Bus activity and idle detection . . . . . 10
6.6 Bus error detection . . . . . 11
6.7 Interrupt generation . . . . . 11
6.8 Operating modes . . . . . 12
6.8.1 Operating mode transitions . . . . . 12
6.8.1.1 AS_PowerOff . . . . . 12
6.8.1.2 AS_Reset . . . . . 12
6.8.1.3 AS_Standby . . . . . 12
6.8.1.4 AS_Sleep . . . . . 13
6.8.1.5 AS_Normal . . . . . 13
6.8.1.6 Operating mode transition diagram . . . . . 15
6.9 Branch operating modes . . . . . 16
6.9.1 Branch operating mode transitions . . . . . 16
6.9.1.1 Branch_Off . . . . . 16
6.9.1.2 Branch_LowPower . . . . . 16
6.9.1.3 Branch_Disabled . . . . . 17
6.9.1.4 Branch_FailSilent . . . . . 17
6.9.1.5 Branch_TxOnly1 . . . . . 17
6.9.1.6 Branch_TxOnly2 . . . . . 17
6.9.1.7 Branch_Normal . . . . . 17
6.9.1.8 Branch operating mode transition diagram . . . 19
6.10 SPI interface . . . . . 20
6.10.1 Register access . . . . . 20
6.10.2 SPI registers . . . . . 20
6.10.2.1 Control register . . . . . 22
6.10.2.2 Configuration register . . . . . 23
6.10.2.3 Interrupt Status register . . . . . 25
6.10.2.4 General Status register . . . . . 28
6.10.2.5 Branch X status registers . . . . . 31
**7 Limiting values . . . . . 33**
**8 Thermal characteristics . . . . . 34**
**9 Static characteristics . . . . . 35**
**10 Dynamic characteristics . . . . . 41**
**11 Application information . . . . . 49**
**12 Package outline . . . . . 50**
**13 Soldering of SMD packages . . . . . 51**
13.1 Introduction to soldering . . . . . 51
13.2 Wave and reflow soldering . . . . . 51
13.3 Wave soldering . . . . . 51
13.4 Reflow soldering . . . . . 52
**14 Appendix: EPL 3.0.1/ISO17458-4 to TJA1085 parameter conversion . . . . . 54**
**15 Abbreviations . . . . . 58**
**16 References . . . . . 58**
**17 Revision history . . . . . 58**
**18 Legal information . . . . . 59**
18.1 Data sheet status . . . . . 59
18.2 Definitions . . . . . 59
18.3 Disclaimers . . . . . 59
18.4 Licenses . . . . . 60
18.5 Trademarks . . . . . 60
**19 Contact information . . . . . 60**
**20 Contents . . . . . 61**


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