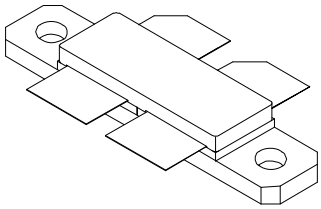
SD56060

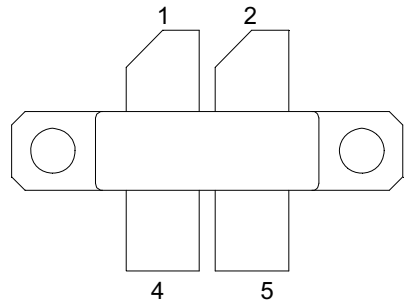
RF power transistor from the LdmoST family of N-channel enhancement-mode lateral MOSFETs

Datasheet - target specification



M246
Epoxy sealed

Figure 1. Pin connections



Features

- Excellent thermal stability
- Common source configuration Push-pull
- P_{OUT} = 60 W with 16 dB gain @ 860 MHz
- BeO-free package

Description

The device is a common source N-channel enhancement-mode lateral field-effect RF power transistor designed for broadband commercial and industrial applications at frequencies up to 1 GHz. It is designed for high gain and broadband performance operating in common source mode at 28 V. It is ideal for applications from 1 to 1000 MHz.

Table 1. Device summary

Order code	Package	Branding
SD56060	M246	SD56060

This is preliminary information on a new product foreseen to be developed. Details are subject to change without notice. www.st.com

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1 Electrical data

1.1 Maximum ratings

Table 2. Absolute maximum ratings (T_{CASE} = 25 °C)

Symbol	Parameter	Value	Unit
$V_{(BR)DSS}$	Drain-source voltage	65	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current	8	A
P_{DISS}	Power dissipation (@ Tc = 70 °C)	148	W
T_J	Max. operating junction temperature	200	°C
T_{STG}	Storage temperature	-65 to +150	°C

1.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Junction - case thermal resistance	0.875	°C/W

2 Electrical characteristics

T_{CASE} = +25 ^{o}C

2.1 Static

Table 4. Static (per section)

Symbol	Test conditions			Min	Typ	Max	Unit
$V_{(BR)DSS}$	V_{GS} = 0 V	I_{DS} = 1 mA		65			V
I_{DSS}	V_{GS} = 0 V	V_{DS} = 28 V				1	µA
I_{GSS}	V_{GS} = 20 V	V_{DS} = 0 V				1	µA
$V_{GS(Q)}$	V_{DS} = 28 V	I_D = 100 mA		3.0		5.0	V
$V_{DS(ON)}$	V_{GS} = 10 V	I_D = 3 A			1.3		V
G_{FS}	V_{DS} = 10 V	I_D = 3 A			1.8		mho
C_{ISS}	V_{GS} = 0 V	V_{DS} = 28 V	f = 1 MHz		58		pF
C_{OSS}	V_{GS} = 0 V	V_{DS} = 28 V	f = 1 MHz		34		pF
C_{RSS}	V_{GS} = 0 V	V_{DS} = 28 V	f = 1 MHz		2.7		pF

Note: REF. 7194566A

2.2 Dynamic

Table 5. Dynamic

Symbol	Test conditions	Min	Typ	Max	Unit
P_{OUT}	V_{DD} = 28 V I_{DQ} = 100 mA f = 860 MHz	60		-	W
G_{PS}	V_{DD} = 28 V I_{DQ} = 100 mA P_{OUT} = 60 W f = 860 MHz	14	16		dB
η_D	V_{DD} = 28 V I_{DQ} = 100 mA P_{OUT} = 60 W f = 860 MHz	50	60		%
IMD (1)	V_{DD} = 28 V I_{DQ} = 100 mA P_{OUT} = 60 W PEP		-28		dB_C
Load mismatch	V_{DD} = 28 V I_{DQ} = 100 mA P_{OUT} = 60 W f = 860 MHz All phase angles	5:1			VSWR

Note: 1 PEP f1 = 860 MHz, f2 = 860.1 MHz

3 Impedances

Figure 2. Current conventions

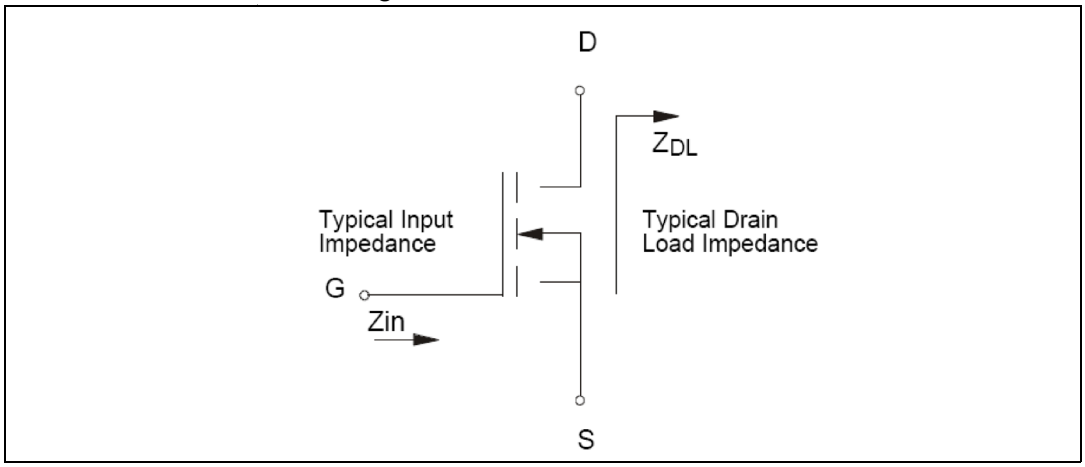


Table 6. Impedance data

Freq. (MHz)	Z_{IN} (Ω)	Z_{DL}(Ω)
860 MHz	TBD	TBD

Measured drain to drain and gate to gate respectively.

4 Typical performances

Figure 3. Capacitance vs drain voltage (per section)

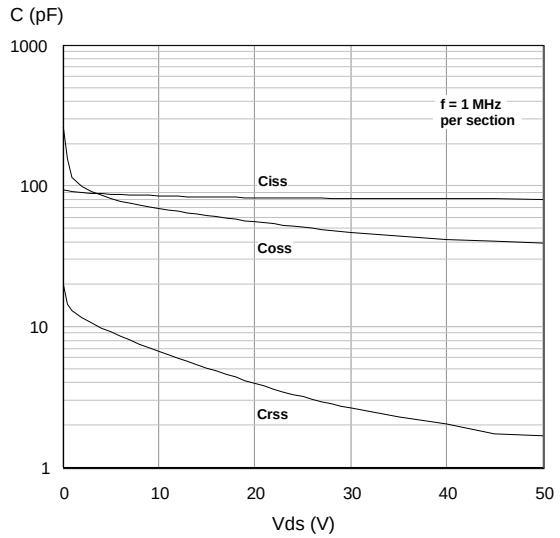


Figure 4. Gate-source voltage vs case temperature

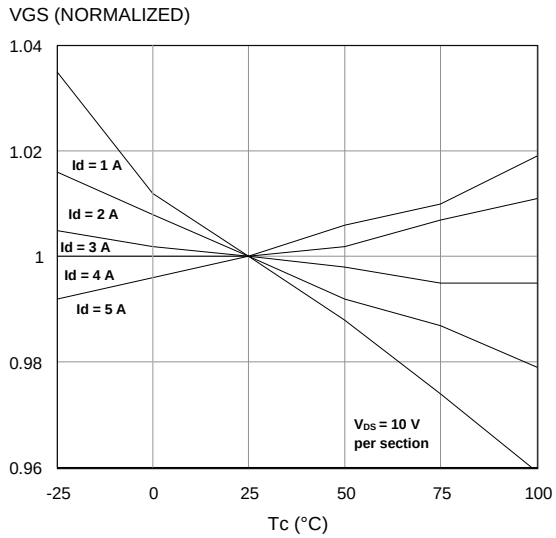


Figure 5. Drain current vs gate voltage

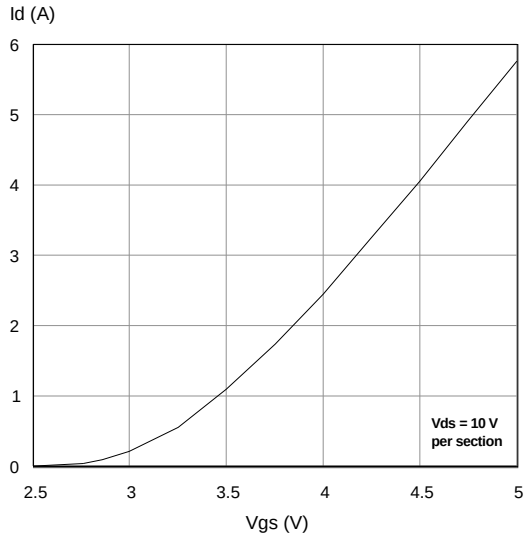


Figure 6. Output power vs input power

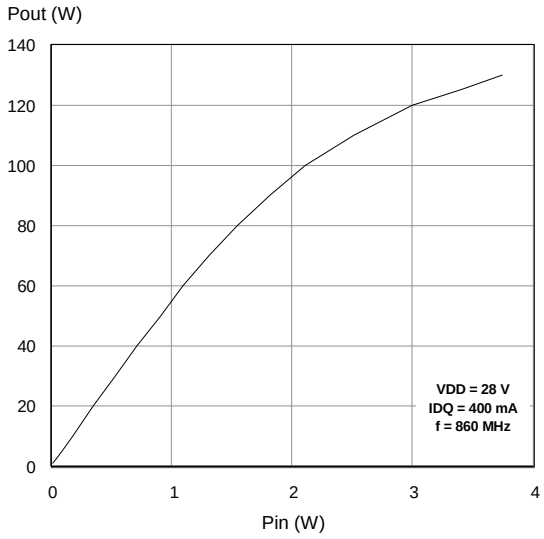


Figure 7. Power gain vs input power

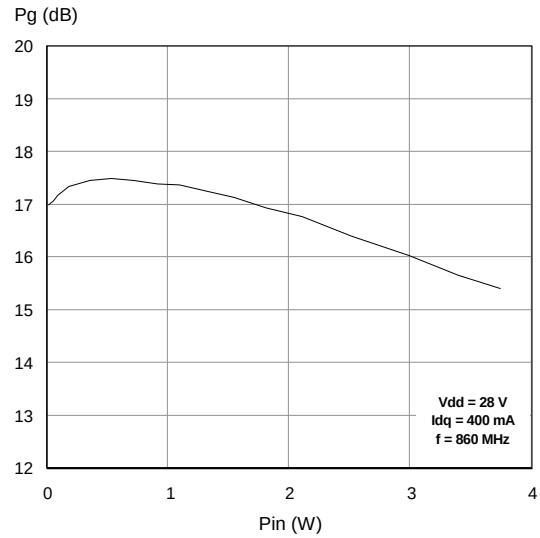


Figure 8. Efficiency vs output power

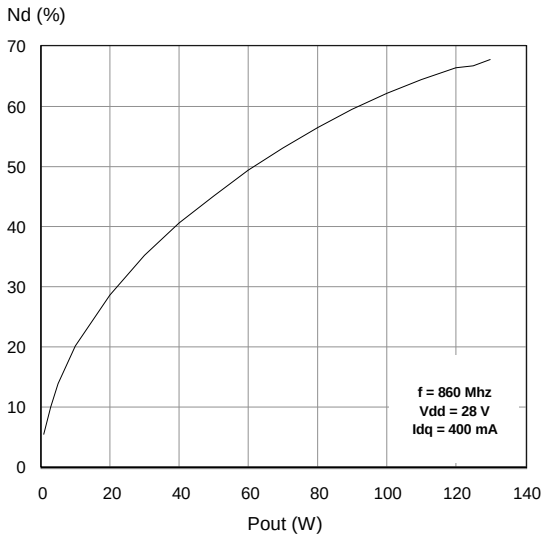


Figure 9. Power gain vs output power

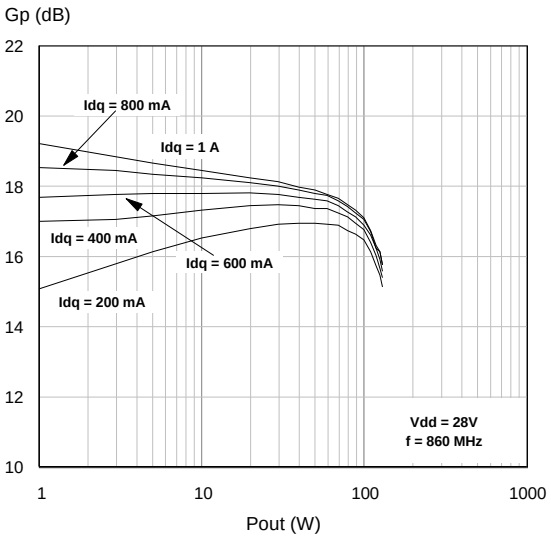


Figure 10. Intermodulation distortion vs output power

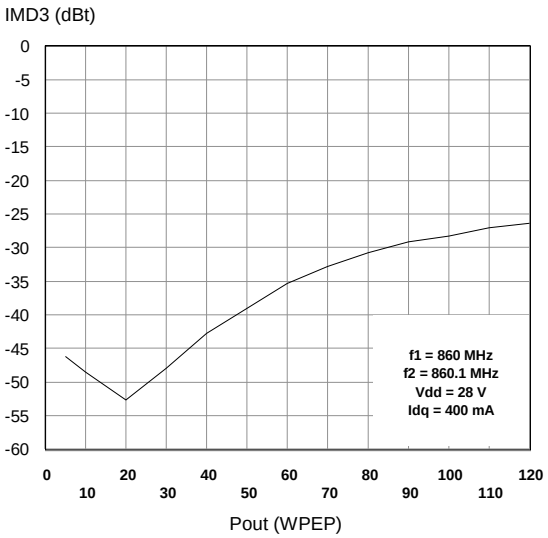


Figure 11. Output power vs drain voltage

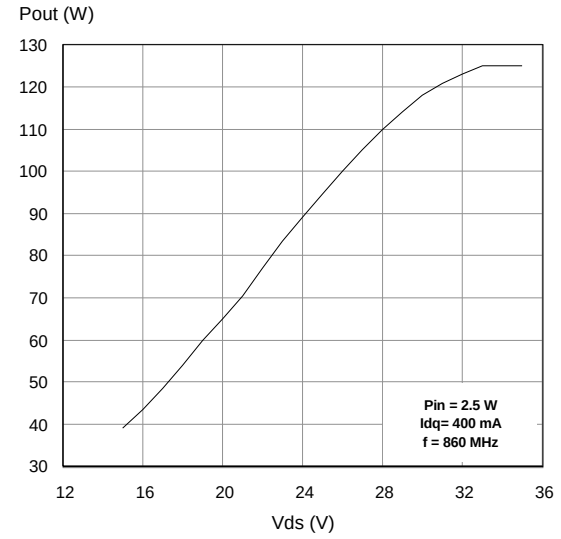


Figure 12. Output power vs bias current

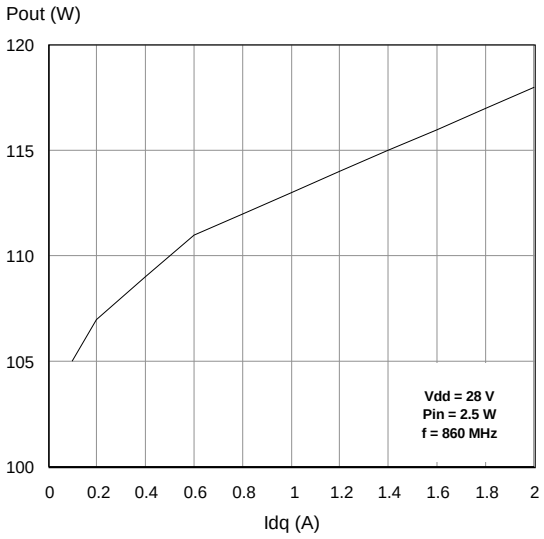
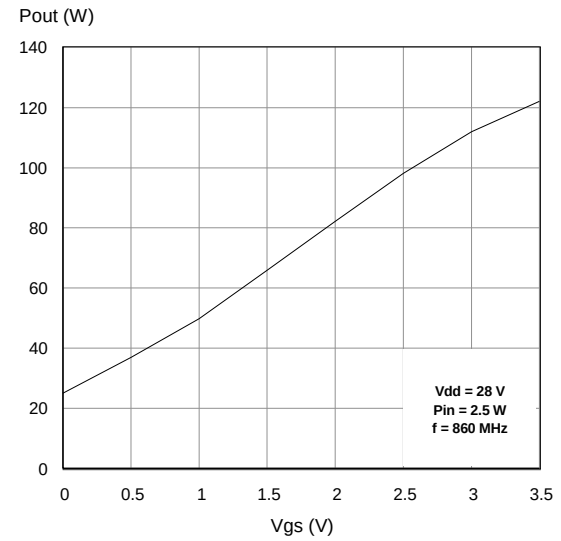
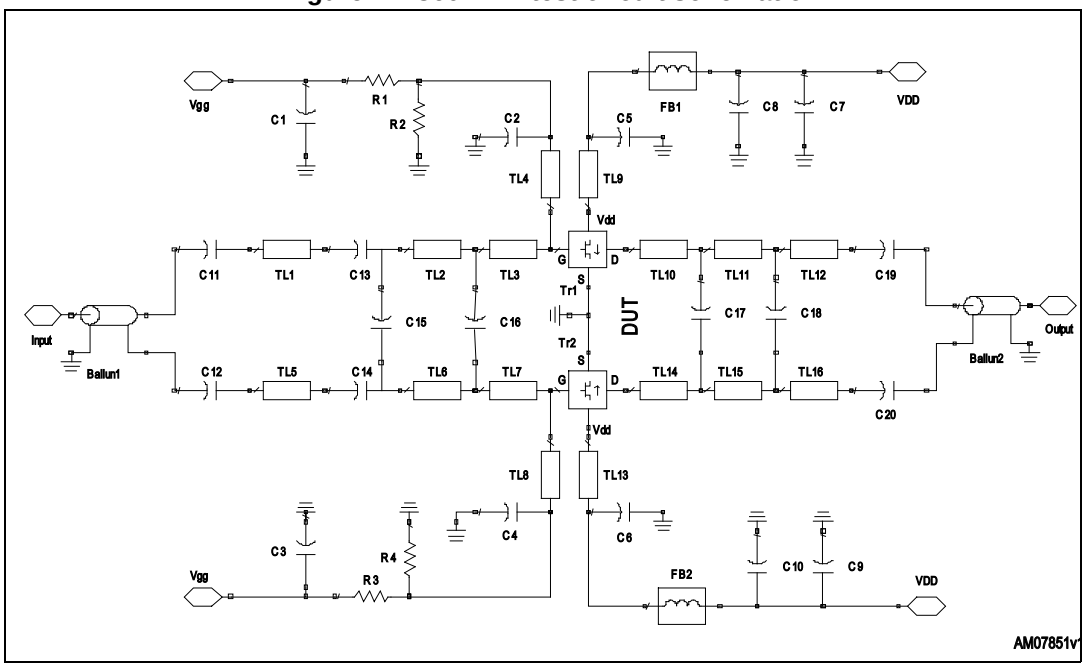


Figure 13. Output power vs gate-source voltage



5 Test circuits

Figure 14. 860 MHz test circuit schematic



Note: 1 Dimensions at component symbols are reference for component placement.

2 Gap between ground & transmission line = 0.056 [1.42] +0.002 [0.05] -0.000 [0.00] typ.

Table 7. Circuit component list

Item	Q.ty	Part number	Vendor	Description
R1, R3	2	CR1206-8W-130JB	VENKEL	13 Ω, 1/8 W surface mount chip resistor
R2, R4	2	CR1206-8W-122JB	VENKEL	1.2 kΩ, 1/8 W surface mount chip resistor
R5, R6	2	CR1206-8W-250JB	VENKEL	25 Ω, 1/8 W surface mount chip resistor
B1, B2	2	2743021447	FAIR-RITE CORP	Surface mount EMI shield bead
C1, C3, C7, C9	4			100 µF, 63 V electrolytic capacitor
C2, C4, C5, C6	4	ATC100B910XXXX	ATC	91 pF chip capacitor
C8, C10	2	C1812X7R501-104KNE	VENKEL	0.1 F 500 V surface mount ceramic chip capacitor
C11, C12	2	ATC100B620XXXX	ATC	62 pF chip capacitor
C13, C14	2	ATC100B151XXXX	ATC	150 pF chip capacitor
C15	1	ATC100B110XXXX	ATC	5.1 pF chip capacitor
C16	1	ATC100B7R5XXXX	ATC	7.5 pF chip capacitor
C17	1	ATC100B1R1XXXX	ATC	1.1 pF chip capacitor

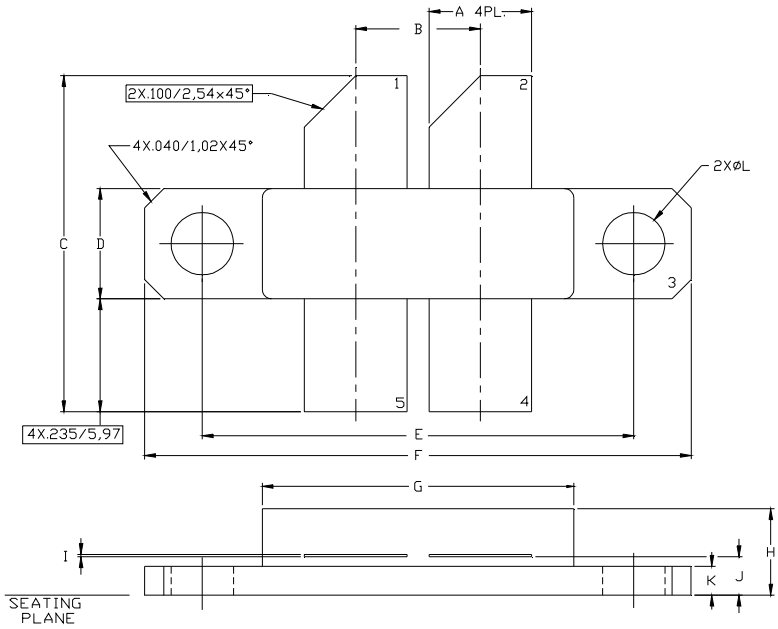
Table 7. Circuit component list (continued)

Item	Q.ty	Part number	Vendor	Description
C18	1	27291PC	JOHANSON	0.8 - 8 pF giga trim variable capacitor
C19, C20	2	ATC100B101XXXX	ATC	100 pF chip capacitor
TL1, TL5				L= 0.250in [6.35mm] W=0.214in [5.44mm]
TL2, TL6				L= 0.182in [4.62mm] W=0.284in [7.21mm]
TL3, TL7				L= 0.318in [8.08mm] W=0.284in [7.21mm]
TL4, TL8, TL9, TL13				L= 2.37in [60.19mm] W=0.082in [2.08mm]
TL10, TL14				L= 0.314in [7.97mm] W=0.230in [5.84mm]
TL11, TL15				L= 0.460in [11.68mm] W=0.230in [5.84mm]
TL12, TL16				L= 0.280in [7.11mm] W=0.230in [5.84mm]
Board 3X5	1		Rogers Corp	Er=2.55 t=0.0026in h=0.030in

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 15. M246 (.230 x .650 WIDE 4/L BAL N/HERM W/FLG) package outline



Controlling dimension: Inches

Ref. 7145054A

Table 8. M246 (.230 x .650 WIDE 4/L BAL N/HERM W/FLG) package mechanical data

Dim.	mm.			Inch		
	Min	Typ	Max	Min	Typ	Max
A	5.33		5.59	.210		.220
B	6.48		6.73	.255		.265
C	17.27		18.29	.680		.720
D	5.72		5.97	.225		.235
E		22.86			.900	
F	28.83		29.08	1.135		1.145
G	16.26		16.76	.640		.660
H	4.19		5.08	.165		.200
I	0.08		0.15	.003		.006
J	1.83		2.24	.072		.088
K	1.40		1.65	.055		.065
L	3.18		3.43	.125		.135

7 Revision history

Table 9. Document revision history

Date	Revision	Changes
15-Jun-2015	1	Initial release

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