MC9S08LH64 Series Data Sheet

by: Automotive and Industrial Solutions Group

This is the MC9S08LH64 Series Data Sheet set consisting of the following files:

- MC9S08LH64 Data Sheet Addendum, Rev 1
- MC9S08LH64 Series Data Sheet, Rev 6

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Freescale Semiconductor
Data Sheet Addendum

MC9S08LH64AD
Rev. 1, 08/2012

MC9S08LH64 Data Sheet Addendum

by: Automotive and Industrial Solutions Group

This document describes corrections to the *MC9S08LH64 Series Data Sheet*, order number MC9S08LH64. For convenience, the addenda items are grouped by revision. Please check our website at http://www.freescale.com for the latest updates.

The current available version of the *MC9S08LH64 Series Data Sheet* is Revision 6.

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1 Addendum for Revision 6

Table 1. MC9S08LH64 Data Sheet Rev 6 Addendum

Location	Description
Section 3.7, “Supply Current Characteristics”/Table 9/Page 23	In the table, for numbers 3 and 4, change “LPS” to “LPR”.

2 Revision History

Table 2 provides a revision history for this document.

Table 2. Revision History Table

Rev. Number	Substantive Changes	Date of Release
1.0	Initial release. Correct errors in the following sections: • Section 3.7, “Supply Current Characteristics”	07/2012

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Rev. 1
08/2012

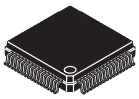
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Data Sheet: Advanced Information

Document Number: MC9S08LH64
Rev. 6, 4/2012

An Energy Efficient Solution by Freescale

MC9S08LH64 Series

Covers: MC9S08LH64 and MC9S08LH36



64-LQFP
Case 840F



80-LQFP
Case 917A

- 8-bit HCS08 Central Processor Unit (CPU)
  - Up to 40 MHz CPU at 3.6 V to 2.1 V across temperature range of –40 °C to 85 °C
  - Up to 20 MHz at 2.1 V to 1.8 V across temperature range of –40 °C to 85 °C
  - HC08 instruction set with added BGND instruction
  - Support for up to 32 interrupt/reset sources
- On-Chip Memory
  - Dual array flash read/program/erase over full operating voltage and temperature
  - Random-access memory (RAM)
  - Security circuitry to prevent unauthorized access to RAM and flash contents
- Power-Saving Modes
  - Two low-power stop modes
  - Reduced-power wait mode
  - Low-power run and wait modes allow peripherals to run while voltage regulator is in standby
  - Peripheral clock gating register can disable clocks to unused modules, thereby reducing currents
  - Very low-power external oscillator that can be used in stop2 or stop3 modes to provide accurate clock source to time-of-day (TOD) module
  - 6 µs typical wakeup time from stop3 mode
- Clock Source Options
  - Oscillator (XOSC) — Loop-control Pierce oscillator; crystal or ceramic resonator range of 31.25 kHz to 38.4 kHz or 1 MHz to 16 MHz
  - Internal Clock Source (ICS) — Internal clock source module containing a frequency-locked-loop (FLL) controlled by internal or external reference; precision trimming of internal reference allows 0.2% resolution and 2% deviation over temperature and voltage; supporting bus frequencies from 1 MHz to 20 MHz
- System Protection
  - Watchdog computer operating properly (COP) reset with option to run from dedicated 1 kHz internal clock source or bus clock
  - Low-voltage warning with interrupt
  - Low-voltage detection with reset or interrupt
  - Illegal opcode detection with reset; illegal address detection with reset
  - Flash block protection
- Development Support
  - Single-wire background debug interface
  - Breakpoint capability to allow single breakpoint setting during in-circuit debugging (plus two more breakpoints in on-chip debug module)
  - On-chip in-circuit emulator (ICE) debug module containing three comparators and nine trigger modes
- Peripherals
  - LCD — Up to 8×36 or 4×40 LCD driver with internal charge pump and option to provide an internally-regulated LCD reference that can be trimmed for contrast control
  - ADC —16-bit resolution; with a dedicated differential ADC input, and 8 single-ended ADC inputs; up to 2.5 µs conversion time; hardware averaging; calibration registers, automatic compare function; temperature sensor; operation in stop3; fully functional from 3.6 V to 1.8 V
  - IIC — Inter-integrated circuit bus module to operate at up to 100 kbps with maximum bus loading; multi-master operation; programmable slave address; interrupt-driven byte-by-byte data transfer; broadcast mode; 10-bit addressing
  - ACMP — Analog comparator with selectable interrupt on rising, falling, or either edge of comparator output; compare option to fixed internal reference voltage; outputs can be optionally routed to TPM module; operation in stop3
  - SCIx — Two full-duplex non-return to zero (NRZ) modules (SCI1 and SCI2); LIN master extended break generation; LIN slave extended break detection; wakeup on active edge
  - SPI — Full-duplex or single-wire bidirectional; double-buffered transmit and receive; master or slave mode; MSB-first or LSB-first shifting
  - TPMx — Two 2-channel (TPM1 and TPM2); selectable input capture, output compare, or buffered edge- or center-aligned PWM on each channel
  - TOD — (Time-of-day) 8-bit, quarter second counter with match register; external clock source for precise time base, time-of-day, calendar, or task scheduling functions
  - VREFx — Trimmable via an 8-bit register in 0.5 mV steps; automatically loaded with room temperature value upon reset; can be enabled to operate in stop3 mode; trim register is not available in stop modes
- Input/Output
  - Dedicated accurate voltage reference output pin, 1.15 V output (VREFOx); trimmable with 0.5 mV resolution
  - Up to 39 GPIOs, two output-only pins
  - Hysteresis and configurable pullup device on all input pins; configurable slew rate and drive strength on all output pins
- Package Options
  - 14mm × 14mm 80-pin LQFP, 10 mm × 10 mm 64-pin LQFP

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Revision History

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http://www.freescale.com/

The following revision history table summarizes changes contained in this document.

Rev	Date	Description of Changes
3	1/2009	Refreshed the draft to include the new VREF module and the latest revisions.
4	4/8/2010	Completed RIDD in the Table 9; updated EREFSTEN in the Table 10; changed all V_{DDAD} to V_{DDA}, V_{SSAD} to V_{SSA}; updated the min. of V_{REFH}; Added 64-pin LQFP package information for LH36 MCU; Updated V Room Temp in the Table 20. Updated $S2I_{DD}$ at V_{DD} = 2 and Temp at –40 to 25 °C Added 64-pin LQFP package for LH36. Updated ADC data in the 3.12/33
5	6/20/2011	Added t_{extrst} in the Table 13; changed the ERREFSTEN to EREFSTEN; updated the VREFOx to 1.15 V. Added LCD specification in the Table 10.
6	4/11/2012	Updated |IIn| in the Table 8.

Related Documentation

Find the most current versions of all documents at: http://www.freescale.com

Reference Manual —MC9S08LH64RM

Contains extensive product information including modes of operation, memory, resets and interrupts, register definition, port pins, CPU, and all module information.

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1 Devices in the MC9S08LH64 Series

Table 1 summarizes the feature set available in the MC9S08LH64 Series of MCUs.

Table 1. MC9S08LH64 Series Features by MCU and Package

Feature	MC9S08LH64		MC9S08LH36	
Package	**80-pin LQFP**	**64-pin LQFP**	**80-pin LQFP**	**64-pin LQFP**
FLASH	64 KB (32,768 and 32,768 Arrays)		36 KB (24,576 and 12,288 Arrays)	
RAM	4000		4000	
ACMP	yes		yes	
ADC Single-ended Channels	8-ch	8-ch	8-ch	8-ch
ADC Differential Channels[1]	1	0	1	0
IIC	yes		yes	
IRQ	yes		yes	
KBI	8		8	
SCI1	yes		yes	
SCI2	yes		yes	
SPI	yes		yes	
TPM1	2-ch		2-ch	
TPM2	2-ch		2-ch	
TOD	yes		yes	
LCD	8×36 4×40	8×24 4×28	8×36 4×40	8×24 4×28
VREFO1	yes	no	yes	no
VREFO2	no	yes	no	yes
I/O pins[2]	39	37	39	37

1 Each differential channel consists of two pins (DADPx and DADMx).

2 The 39 I/O pins include two output-only pins and 18 LCD GPIO.

The block diagram in Figure 1 shows the structure of the MC9S08LH64 Series MCU.

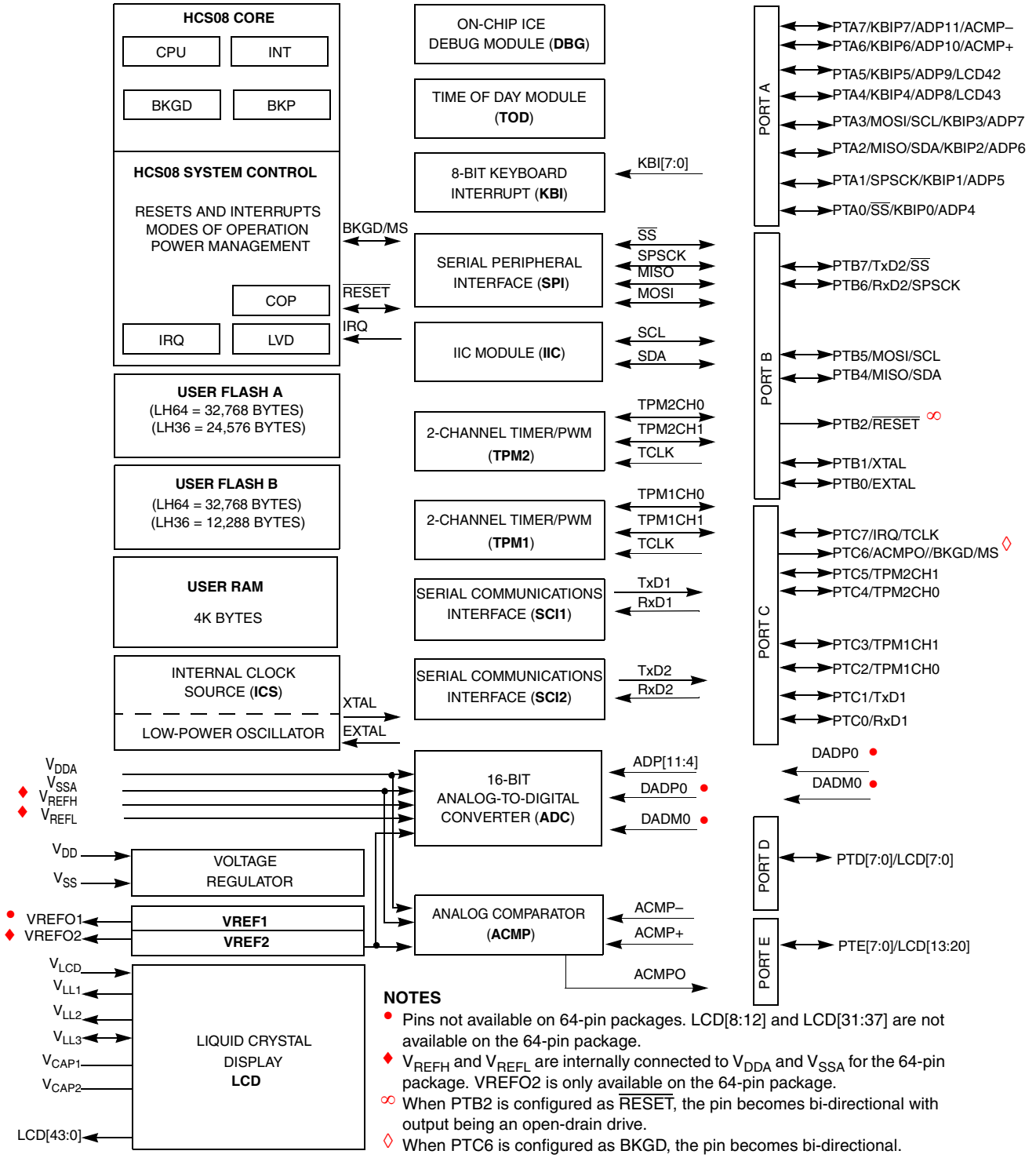


Figure 1. MC9S08LH64 Series Block Diagram

2 Pin Assignments

This section shows the pin assignments for the MC9S08LH64 Series devices.

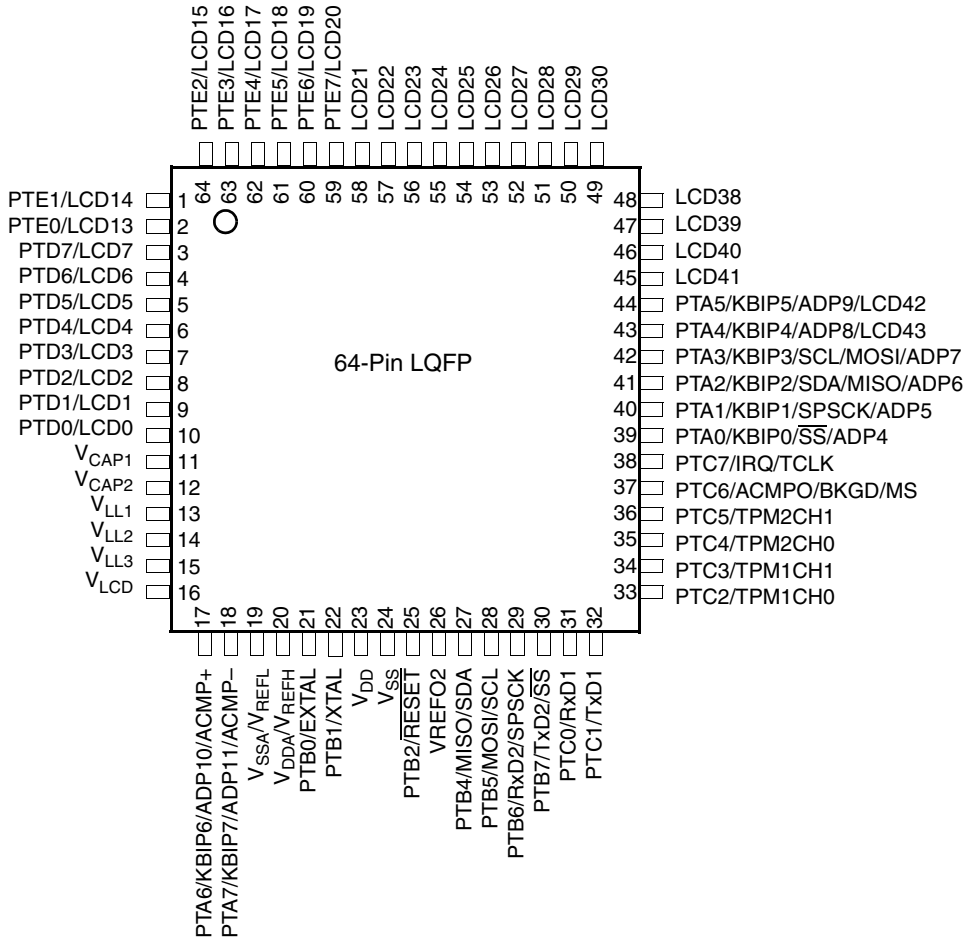


Figure 2. 64-Pin LQFP

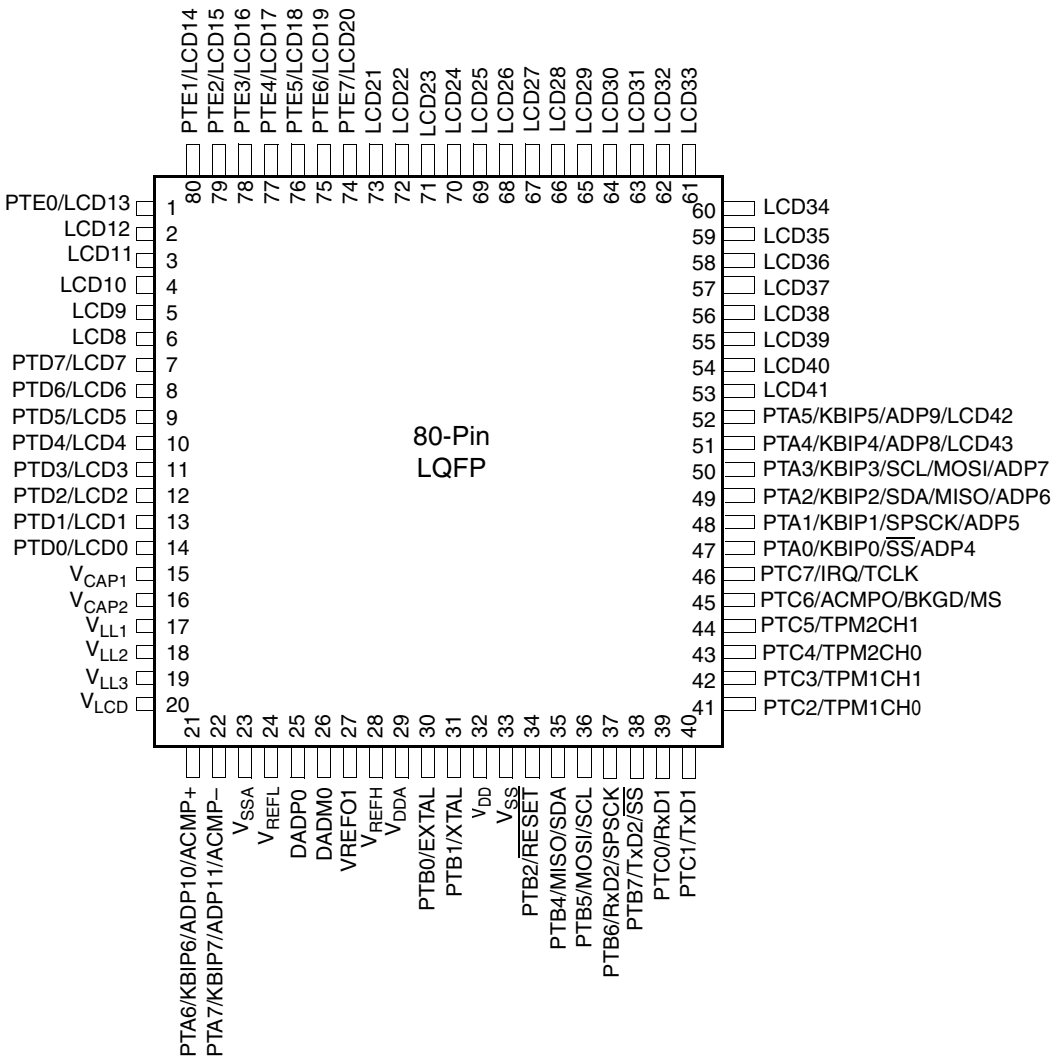


Figure 3. 80-Pin LQFP

Table 2. Pin Availability by Package Pin-Count

		<-- Lowest **Priority** --> Highest				
80	**64**	**Port Pin**	**Alt 1**	**Alt 2**	**Alt3**	**Alt4**
1	2	PTE0	LCD13			
2		LCD12				
3		LCD11				
4		LCD10				
5		LCD9				
6		LCD8				
7	3	PTD7	LCD7			
8	4	PTD6	LCD6			

Table 2. Pin Availability by Package Pin-Count (continued)

		<-- Lowest **Priority** --> Highest				
80	**64**	**Port Pin**	**Alt 1**	**Alt 2**	**Alt3**	**Alt4**
9	5	PTD5	LCD5			
10	6	PTD4	LCD4			
11	7	PTD3	LCD3			
12	8	PTD2	LCD2			
13	9	PTD1	LCD1			
14	10	PTD0	LCD0			
15	11	V_{CAP1}				
16	12	V_{CAP2}				
17	13	V_{LL1}				
18	14	V_{LL2}				
19	15	V_{LL3}				
20	16	V_{LCD}				
21	17	PTA6	KBIP6	ADP10	ACMP+	
22	18	PTA7	KBIP7	ADP11	ACMP–	
23	19	V_{SSA}				
24		V_{REFL}				
25		DADP0				
26		DADM0				
27		VREFO1				
28	20	V_{REFH}				
29		V_{DDA}				
30	21	PTB0		EXTAL		
31	22	PTB1		XTAL		
32	23	V_{DD}				
33	24	V_{SS}				
34	25	PTB2	$\overline{\text{RESET}}$			
	26	VREFO2				
35	27	PTB4	MISO	SDA		
36	28	PTB5	MOSI	SCL		
37	29	PTB6	RxD2	SPSCK		
38	30	PTB7	TxD2	$\overline{\text{SS}}$		
39	31	PTC0	RxD1			
40	32	PTC1	TxD1			
41	33	PTC2	TPM1CH0			
42	34	PTC3	TPM1CH1			
43	35	PTC4	TPM2CH0			
44	36	PTC5	TPM2CH1			
45	37	PTC6	ACMPO	BKGD	MS	

Table 2. Pin Availability by Package Pin-Count (continued)

		<-- Lowest **Priority** --> Highest				
80	**64**	**Port Pin**	**Alt 1**	**Alt 2**	**Alt3**	**Alt4**
46	38	PTC7	IRQ	TCLK		
47	39	PTA0	KBIP0		$\overline{SS}$	ADP4
48	40	PTA1	KBIP1		SPSCK	ADP5
49	41	PTA2	KBIP2	SDA	MISO	ADP6
50	42	PTA3	KBIP3	SCL	MOSI	ADP7
51	43	PTA4	KBIP4	ADP8	LCD43	
52	44	PTA5	KBIP5	ADP9	LCD42	
53	45	LCD41				
54	46	LCD40				
55	47	LCD39				
56	48	LCD38				
57		LCD37				
58		LCD36				
59		LCD35				
60		LCD34				
61		LCD33				
62		LCD32				
63		LCD31				
64	49	LCD30				
65	50	LCD29				
66	51	LCD28				
67	52	LCD27				
68	53	LCD26				
69	54	LCD25				
70	55	LCD24				
71	56	LCD23				
72	57	LCD22				
73	58	LCD21				
74	59	PTE7	LCD20			
75	60	PTE6	LCD19			
76	61	PTE5	LCD18			
77	62	PTE4	LCD17			
78	63	PTE3	LCD16			
79	64	PTE2	LCD15			
80	1	PTE1	LCD14			

3 Electrical Characteristics

3.1 Introduction

This section contains electrical and timing specifications for the MC9S08LH64 Series of microcontrollers available at the time of publication.

3.2 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 3. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

3.3 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table 4 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high-static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}) or the programmable pullup resistor associated with the pin is enabled.

Table 4. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to +3.8	V
Maximum current into V_{DD}	I_{DD}	120	mA
Digital input voltage	V_{In}	–0.3 to V_{DD} + 0.3	V
Instantaneous maximum current Single pin limit (applies to all port pins)[1, 2, 3]	I_D	± 25	mA
Storage temperature range	T_{stg}	–55 to 150	°C

1 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

2 All functional non-supply pins, except for PTB2 are internally clamped to V_{SS} and V_{DD}.

3 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low (which would reduce overall power consumption).

3.4 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 5. Thermal Characteristics

Rating	Symbol	Value	Unit
Operating temperature range (packaged)	T_A	T_L to T_H –40 to 85	°C
Maximum junction temperature	T_J	95	°C
Thermal resistance Single-layer board			
80-pin LQFP	θ_{JA}	55	°C/W
64-pin LQFP		73	
Thermal resistance Four-layer board			
80-pin LQFP	θ_{JA}	42	°C/W
64-pin LQFP		54	

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad \textit{Eqn. 1}$$

where:

T_A = Ambient temperature, °C
θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W
$P_D = P_{int} + P_{I/O}$
$P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power
$P_{I/O}$ = Power dissipation on input and output pins — user determined

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273\ °C) \quad \textit{Eqn. 2}$$

Solving Equation 1 and Equation 2 for K gives:

$$K = P_D \times (T_A + 273\ °C) + \theta_{JA} \times (P_D)^2 \quad \textit{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

3.5 ESD Protection and Latch-Up Immunity

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, normal handling precautions should be taken to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits. During the device qualification, ESD stresses were performed for the human body model (HBM), the machine model (MM) and the charge device model (CDM).

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless instructed otherwise in the device specification.

Table 6. ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body Model	Series resistance	R1	1500	Ω
	Storage capacitance	C	100	pF
	Number of pulses per pin	—	3	
Charge Device Model	Series resistance	R1	0	Ω
	Storage capacitance	C	200	pF
	Number of pulses per pin	—	3	

Table 6. ESD and Latch-up Test Conditions (continued)

Latch-up	Minimum input voltage limit		–2.5	V
	Maximum input voltage limit		7.5	V

Table 7. ESD and Latch-Up Protection Characteristics

No.	Rating[1]	Symbol	Min	Max	Unit
1	Human body model (HBM)	V_{HBM}	±2000	—	V
2	Charge device model (CDM)	V_{CDM}	±500	—	V
3	Latch-up current at T_A = 85 °C	I_{LAT}	±100	—	mA

1 Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

3.6 DC Characteristics

This section includes information about power supply requirements and I/O pin characteristics.

Table 8. DC Characteristics

Num	C	Characteristic	Symbol	Condition	Min	Typ[1]	Max	Unit
1		Operating Voltage			1.8		3.6	V
2	C	Output high voltage — PTA[0:3], PTA[6:7], PTB[0:7], PTC[0:7][2], low-drive strength	V_{OH}	V_{DD} >1.8 V, I_{Load} = –0.6 mA	V_{DD} – 0.5	—	—	V
	P	Output high voltage — PTA[0:3], PTA[6:7], PTB[0:7], PTC[0:7][2], high-drive strength		V_{DD} > 2.7 V, I_{Load} = –10 mA	V_{DD} – 0.5	—	—	
	C			V_{DD} > 1.8 V, I_{Load} = –3 mA	V_{DD} – 0.5	—	—	
3	C	Output high voltage — PTA[4:5], PTD[0:7], PTE[0:7], low-drive strength	V_{OH}	V_{DD} > 1.8 V, I_{Load} = –0.5 mA	V_{DD} – 0.5	—	—	V
	P	Output high voltage — PTA[4:5], PTD[0:7], PTE[0:7], high-drive strength		V_{DD} > 2.7 V, I_{Load} = –2.5 mA	V_{DD} – 0.5	—	—	
	C			V_{DD} > 1.8 V, I_{Load} = –1 mA	V_{DD} – 0.5	—	—	
4	D	Output high current — Max total I_{OH} for all ports	I_{OHT}		—	—	100	mA
5	C	Output low voltage — PTA[0:3], PTA[6:7], PTB[0:7], PTC[0:7], low-drive strength	V_{OL}	V_{DD} >1.8 V, I_{Load} = 0.6 mA	—	—	0.5	V
	P	Output low voltage — PTA[0:3], PTA[6:7], PTB[0:7], PTC[0:7], high-drive strength		V_{DD} > 2.7 V, I_{Load} = 10 mA	—	—	0.5	
	C			V_{DD} > 1.8 V, I_{Load} = 3 mA	—	—	0.5	

Table 8. DC Characteristics (continued)

Num	C	Characteristic	Symbol	Condition	Min	Typ[1]	Max	Unit
6	C	Output low voltage — PTA[4:5], PTD[0:7], PTE[0:7], low-drive strength	V_{OL}	V_{DD} > 1.8 V, I_{Load} = 0.5 mA	—	—	0.5	V
	P	Output low voltage — PTA[4:5], PTD[0:7], PTE[0:7], high-drive strength		V_{DD} > 2.7 V, I_{Load} = 3 mA	—	—	0.5	
	C			V_{DD} > 1.8 V, I_{Load} = 1 mA	—	—	0.5	
7	D	Output low current — Max total I_{OL} for all ports	I_{OLT}		—	—	100	mA
8	P	Input high voltage — all digital inputs	V_{IH}	V_{DD} > 2.7 V	0.70 x V_{DD}	—	—	V
	C			V_{DD} > 1.8 V	0.85 x V_{DD}	—	—	
9	P	Input low voltage — all digital inputs	V_{IL}	V_{DD} > 2.7 V	—	—	0.35 x V_{DD}	
	C			V_{DD} > 1.8 V	—	—	0.30 x V_{DD}	
10	C	Input hysteresis — all digital inputs	V_{hys}		0.06 x V_{DD}	—	—	mV
11	P	Input leakage current — all input only pins except for LCD only pins (LCD 8-12, 21-41)	$\lvert I_{In} \rvert$	V_{In} = V_{DD}	—	0.025	1	µA
				V_{In} = V_{SS}	—	0.025	1	µA
		Input leakage current — LCD only pins (LCD 8-12, 21-41)		V_{In} = V_{DD}	—	100	150	µA
				V_{In} = V_{SS}	—	0.025	1	µA
12	P	Hi-Z (off-state) leakage current — all input/output (per pin)	$\lvert I_{OZ} \rvert$	V_{In} = V_{DD} or V_{SS}	—	0.025	1	µA
13	P	Total leakage current[3] — Total leakage current for all pins	$\lvert I_{InT} \rvert$	V_{In} = V_{DD} or V_{SS}	—	—	3	µA
14	P	Pullup, Pulldown resistors — all non-LCD pins when enabled	R_{PU}, R_{PD}		17.5	—	52.5	kΩ
15	P	Pullup, Pulldown resistors — LCD/GPIO pins when enabled	R_{PU}, R_{PD}		35	—	77	kΩ
16	D	DC injection current[4, 5, 6] — Single pin limit	I_{IC}	V_{IN} < V_{SS}, V_{IN} > V_{DD}	–0.2	—	0.2	mA
		DC injection current[4, 5, 6] — Total MCU limit, includes sum of all stressed pins			–5	—	5	mA
17	C	Input Capacitance, all pins	C_{In}		—	—	8	pF
18	C	RAM retention voltage	V_{RAM}		—	0.6	1.0	V
19	C	POR re-arm voltage[7]	V_{POR}		0.9	1.4	2.0	V
20	D	POR re-arm time	t_{POR}		10	—	—	µs
21	P	Low-voltage detection threshold	V_{LVD}	V_{DD} falling V_{DD} rising	1.80 1.88	1.84 1.92	1.88 1.96	V

Table 8. DC Characteristics (continued)

Num	C	Characteristic	Symbol	Condition	Min	Typ[1]	Max	Unit
22	P	Low-voltage warning threshold	V_{LVW}	V_{DD} falling V_{DD} rising	2.08	2.14	2.2	V
23	P	Low-voltage inhibit reset/recover hysteresis	V_{hys}		—	80	—	mV
24	P	Bandgap Voltage Reference[8]	V_{BG}		1.15	1.17	1.18	V

1 Typical values are measured at 25 °C. Characterized, not tested

2 All I/O pins except for LCD pins in Open Drain mode.

3 Total leakage current is the sum value for all GPIO pins. This leakage current is not distributed evenly across all pins but characterization data shows that individual pin leakage current maximums are less than 250 nA.

4 All functional non-supply pins, except for PTB2 are internally clamped to V_{SS} and V_{DD}.

5 Input current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

6 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If the positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure that external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

7 POR will occur below the minimum voltage.

8 Factory trimmed at V_{DD} = 3.0 V, Temp = 25 °C

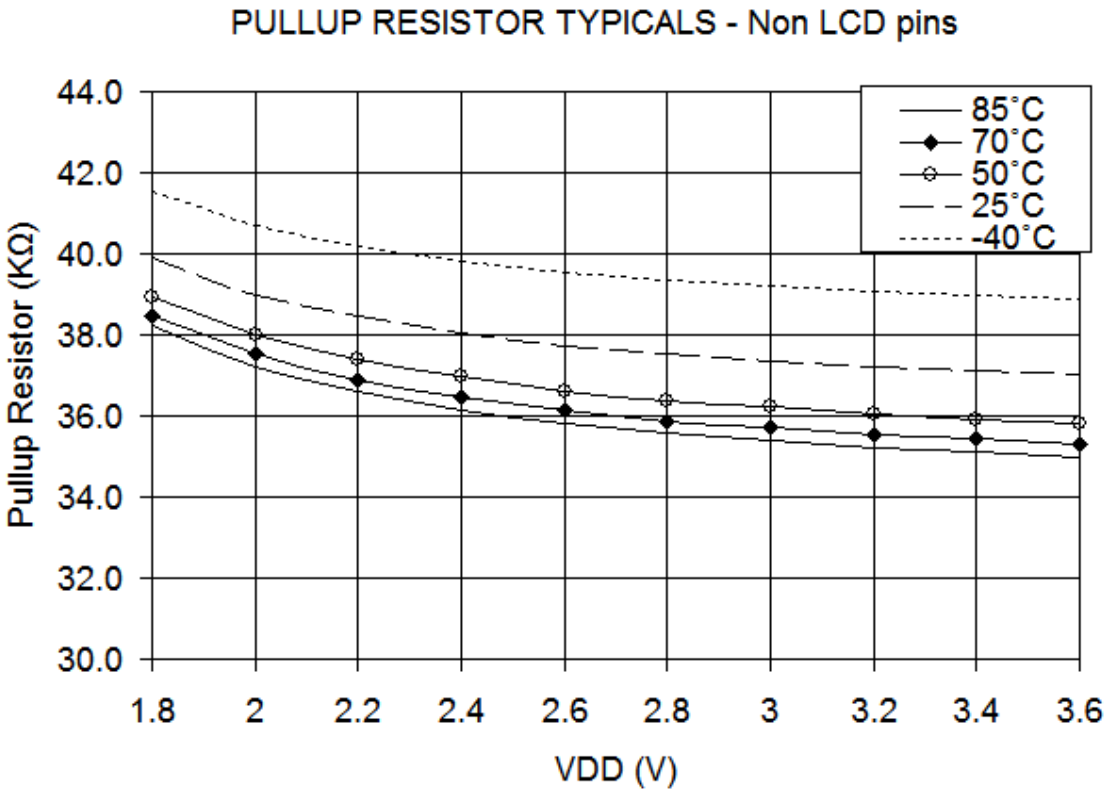


Figure 4. Non LCD pins I/O Pullup Typical Resistor Values

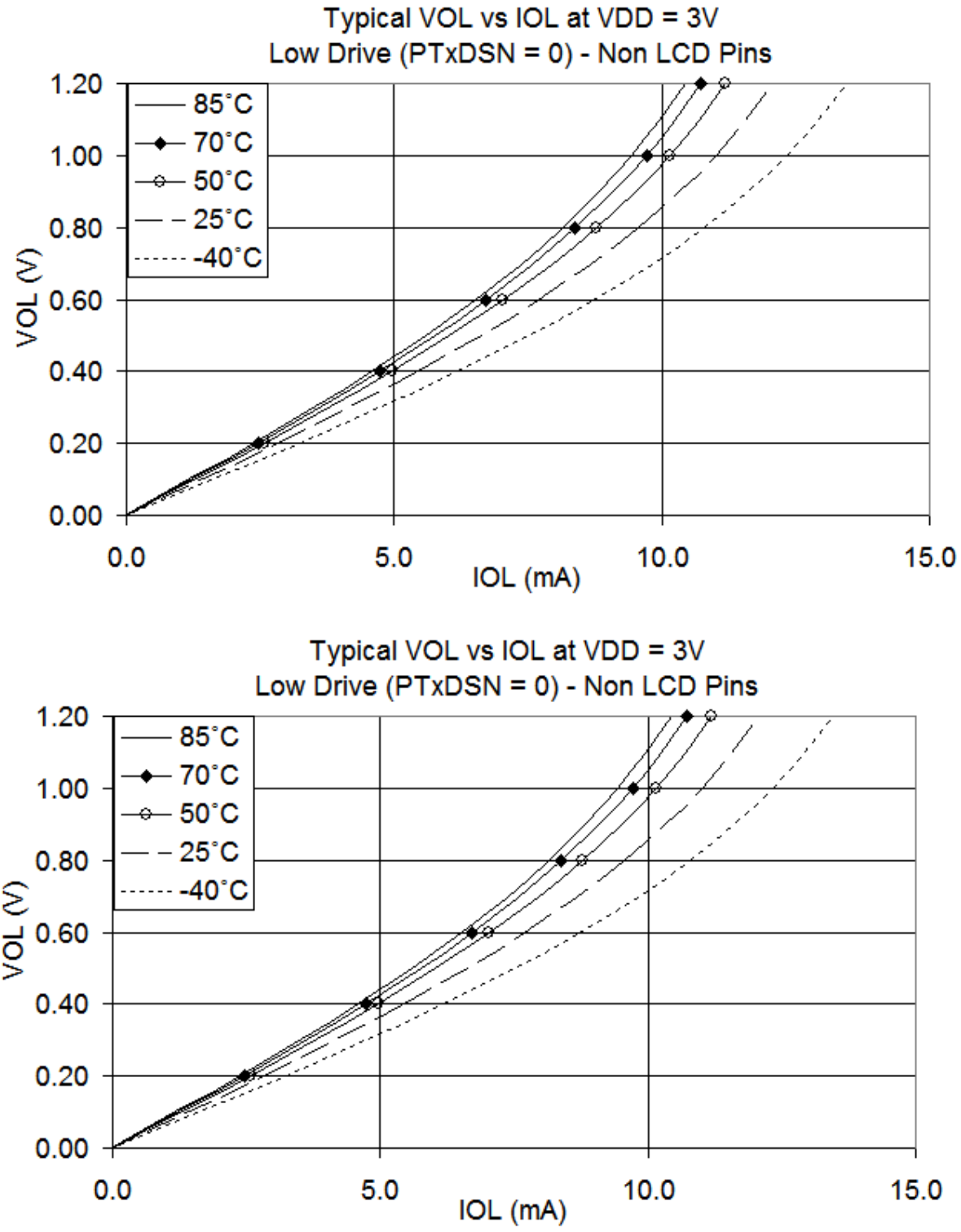


Figure 5. Typical Low-Side Driver (Sink) Characteristics (Non LCD Pins) — Low Drive (PTxDSn = 0)

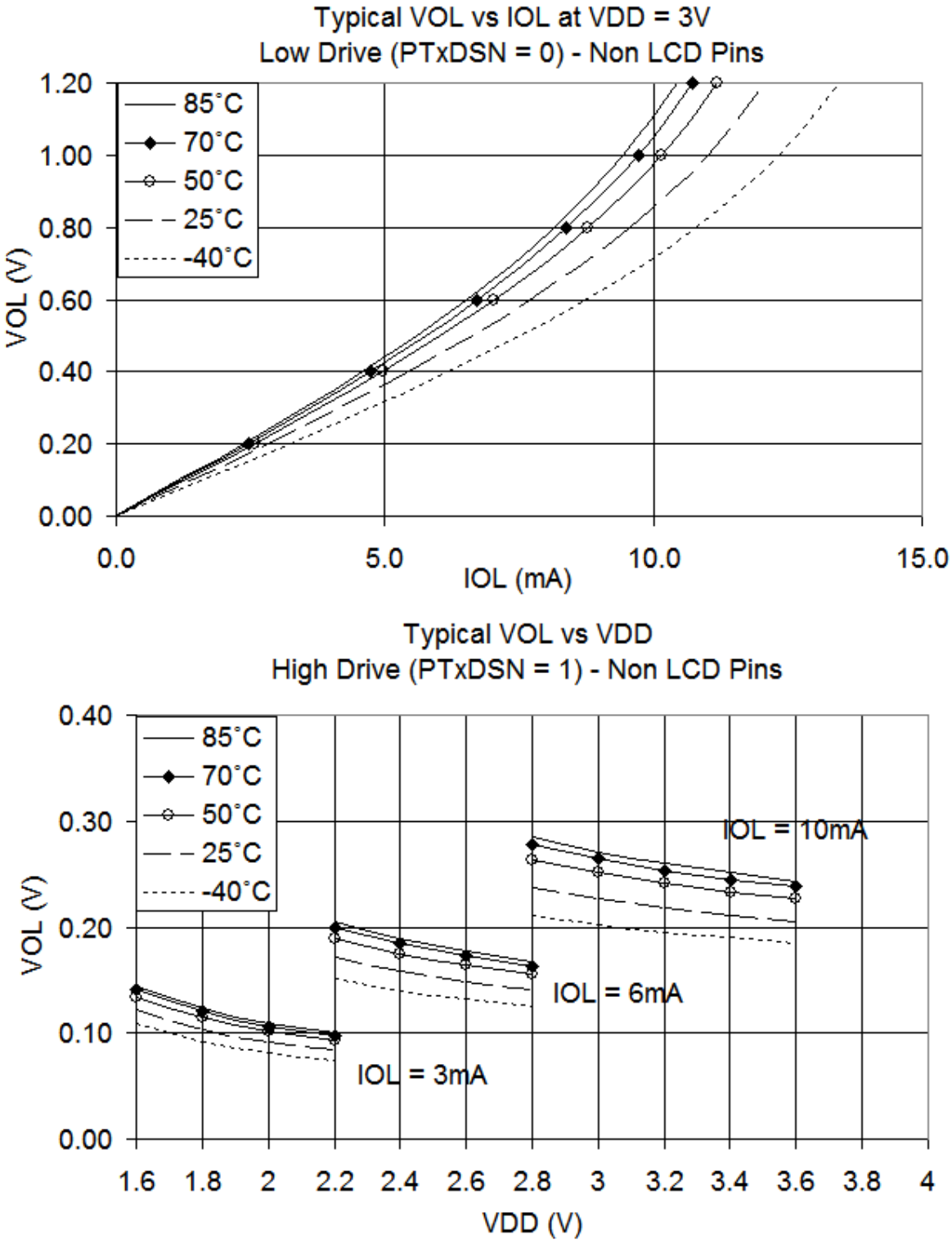


Figure 6. Typical Low-Side Driver (Sink) Characteristics(Non LCD Pins) — High Drive (PTxDSn = 1)

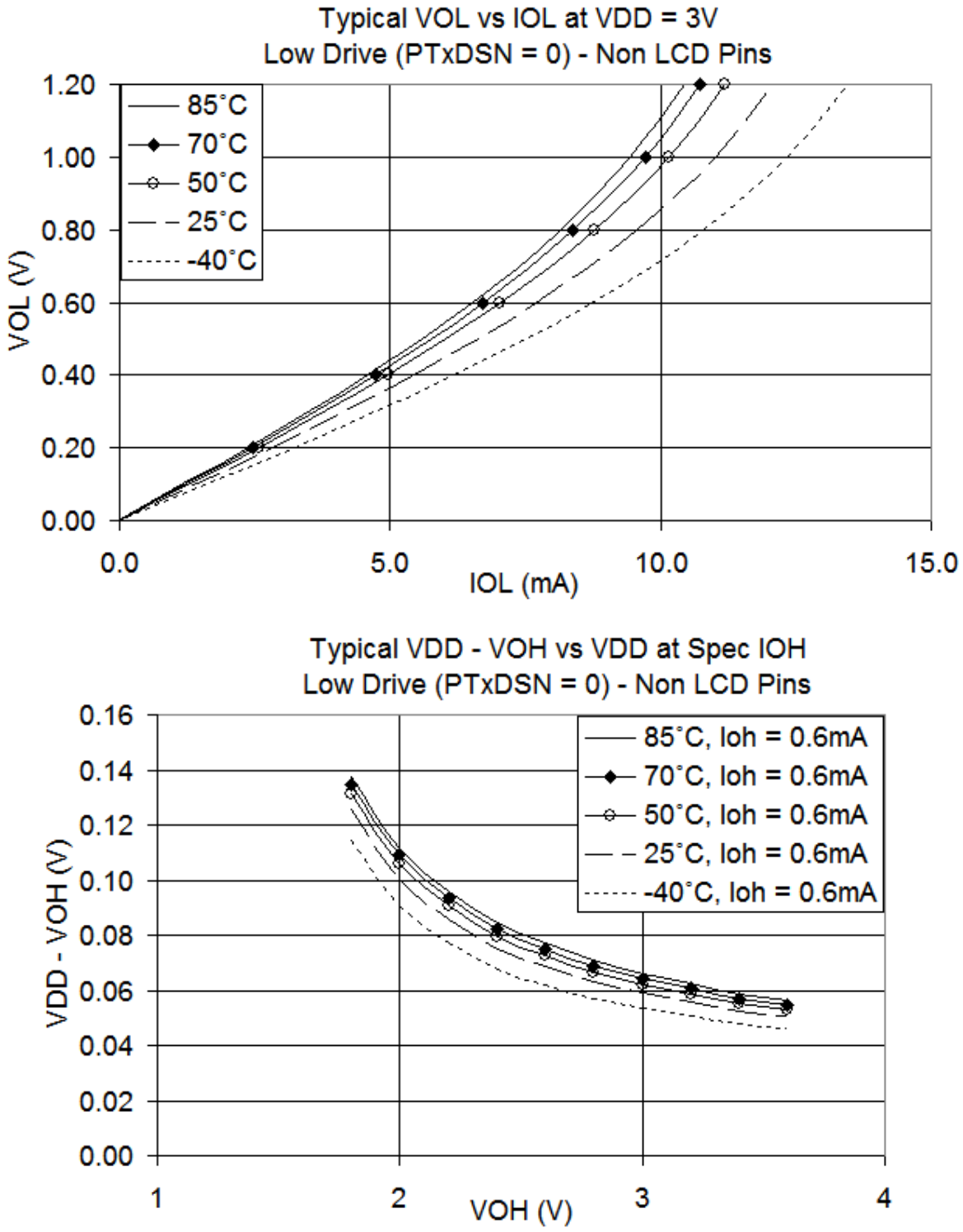


Figure 7. Typical High-Side (Source) Characteristics (Non LCD Pins)— Low Drive (PTxDSn = 0)

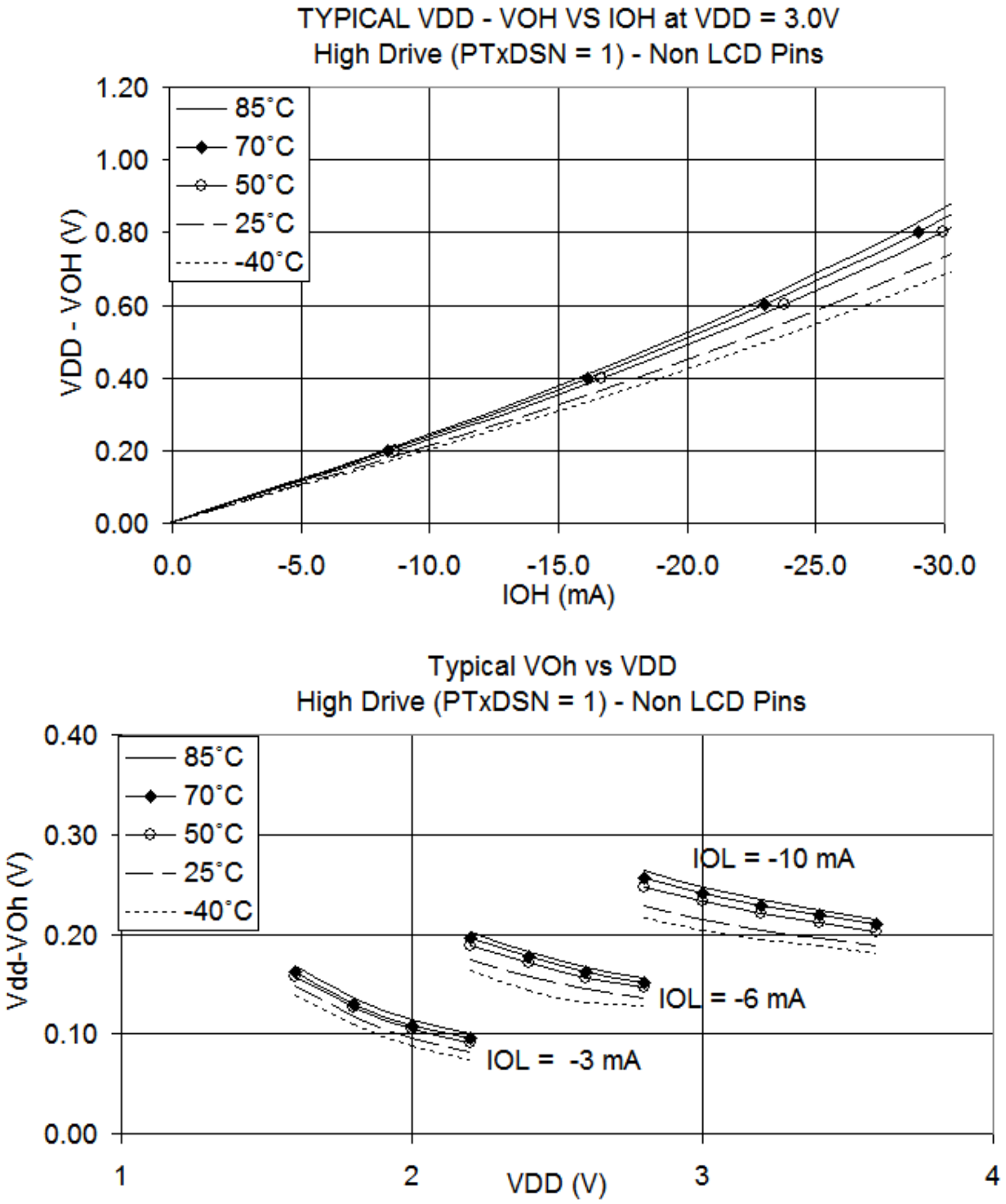


Figure 8. Typical High-Side (Source) Characteristics(Non LCD Pins) — High Drive (PTxDSn = 1)

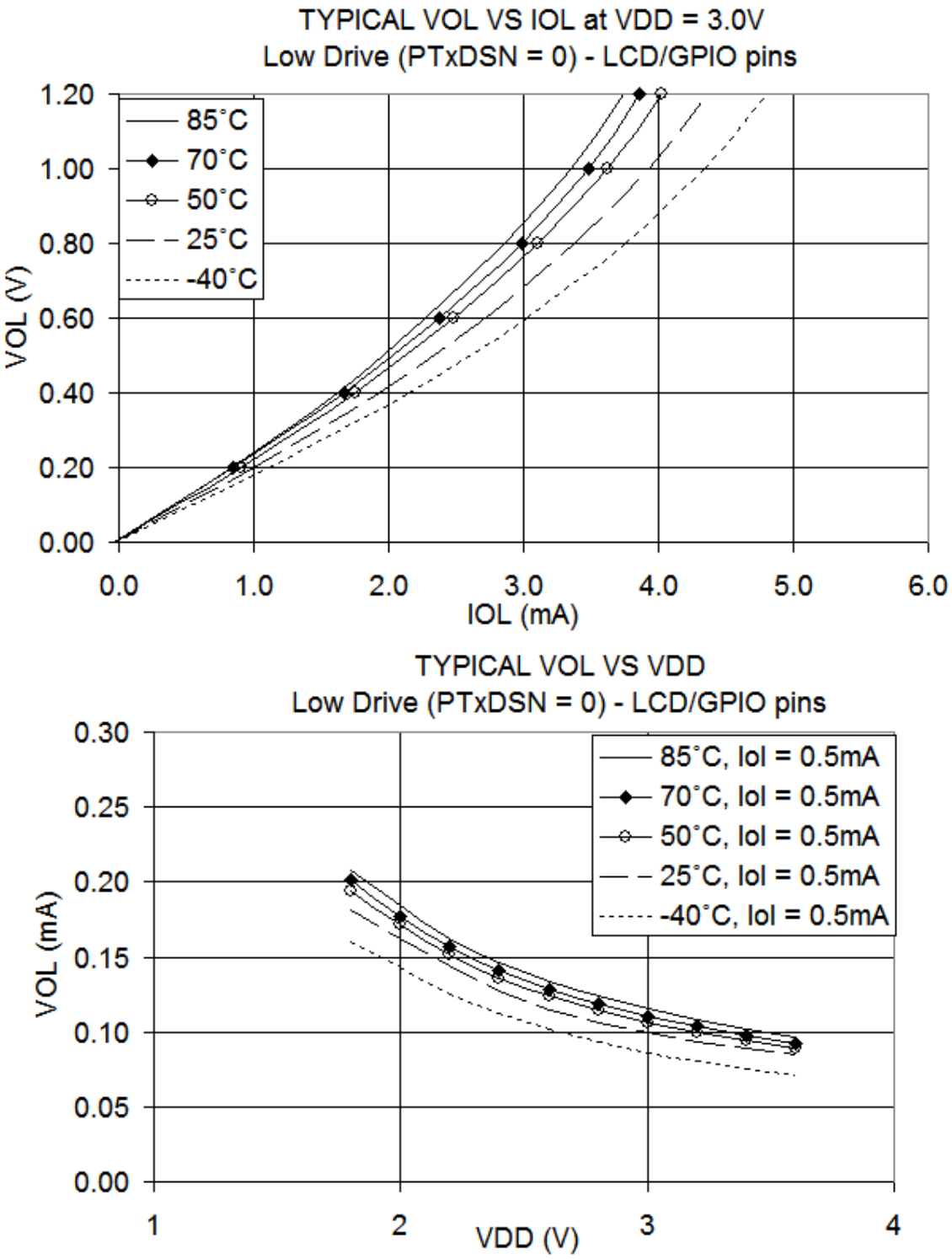


Figure 9. Typical Low-Side Driver (Sink) Characteristics (LCD/GPIO Pins)— Low Drive (PTxDSn = 0)

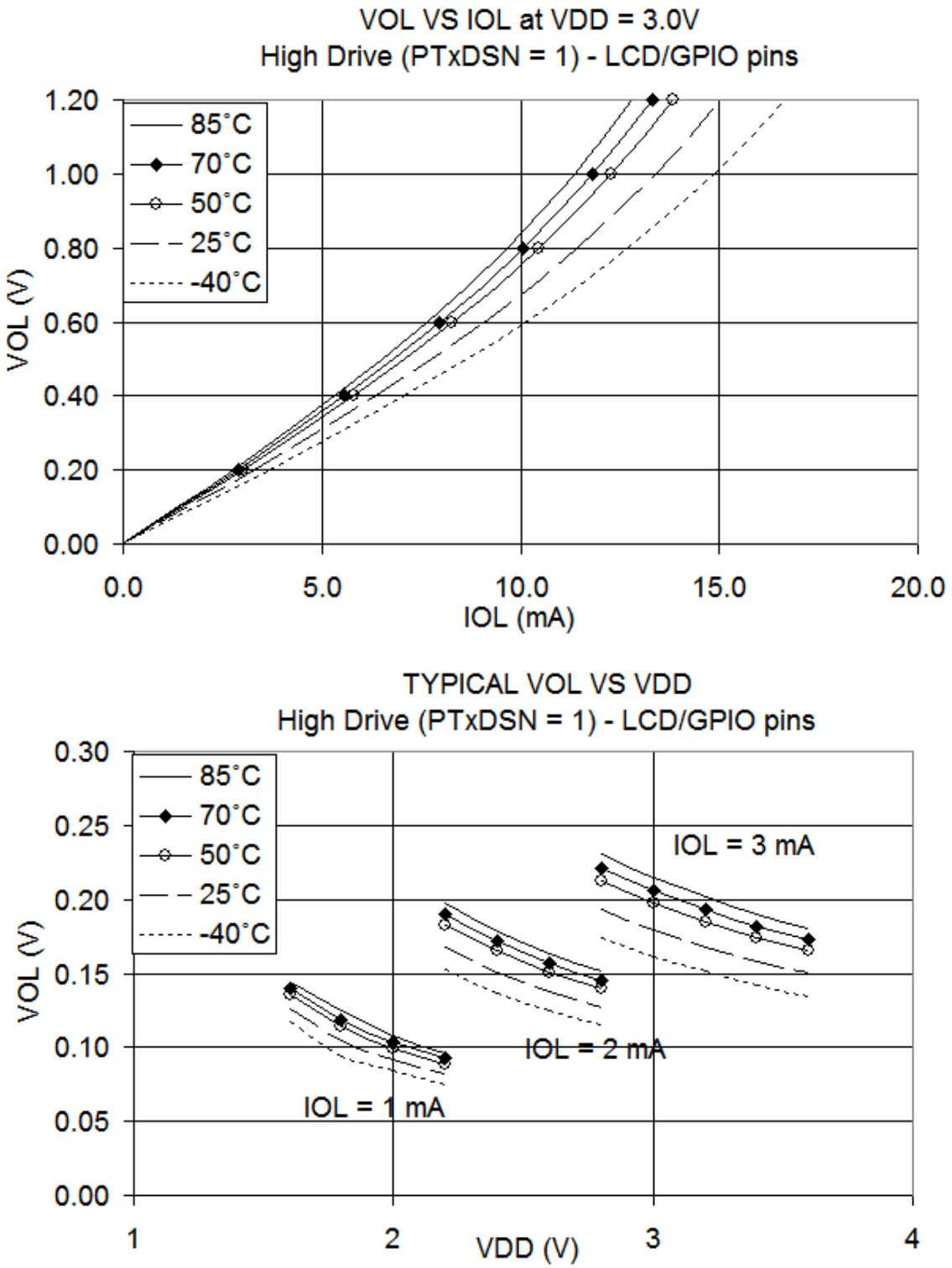


Figure 10. Typical Low-Side Driver (Sink) Characteristics (LCD/GPIO Pins) — High Drive (PTxDSn = 1)

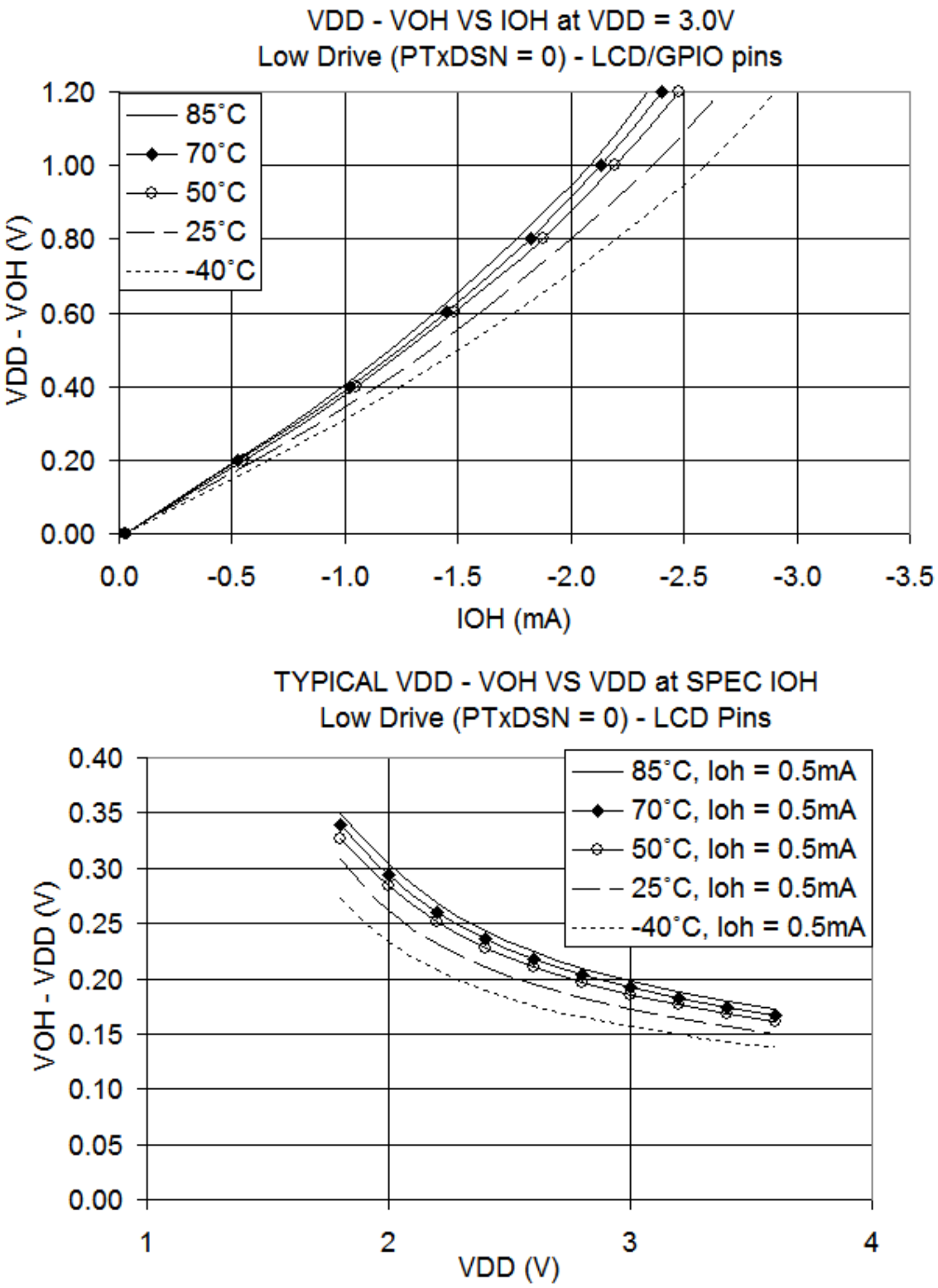


Figure 11. Typical High-Side (Source) Characteristics (LCD/GPIO Pins)— Low Drive (PTxDSn = 0)

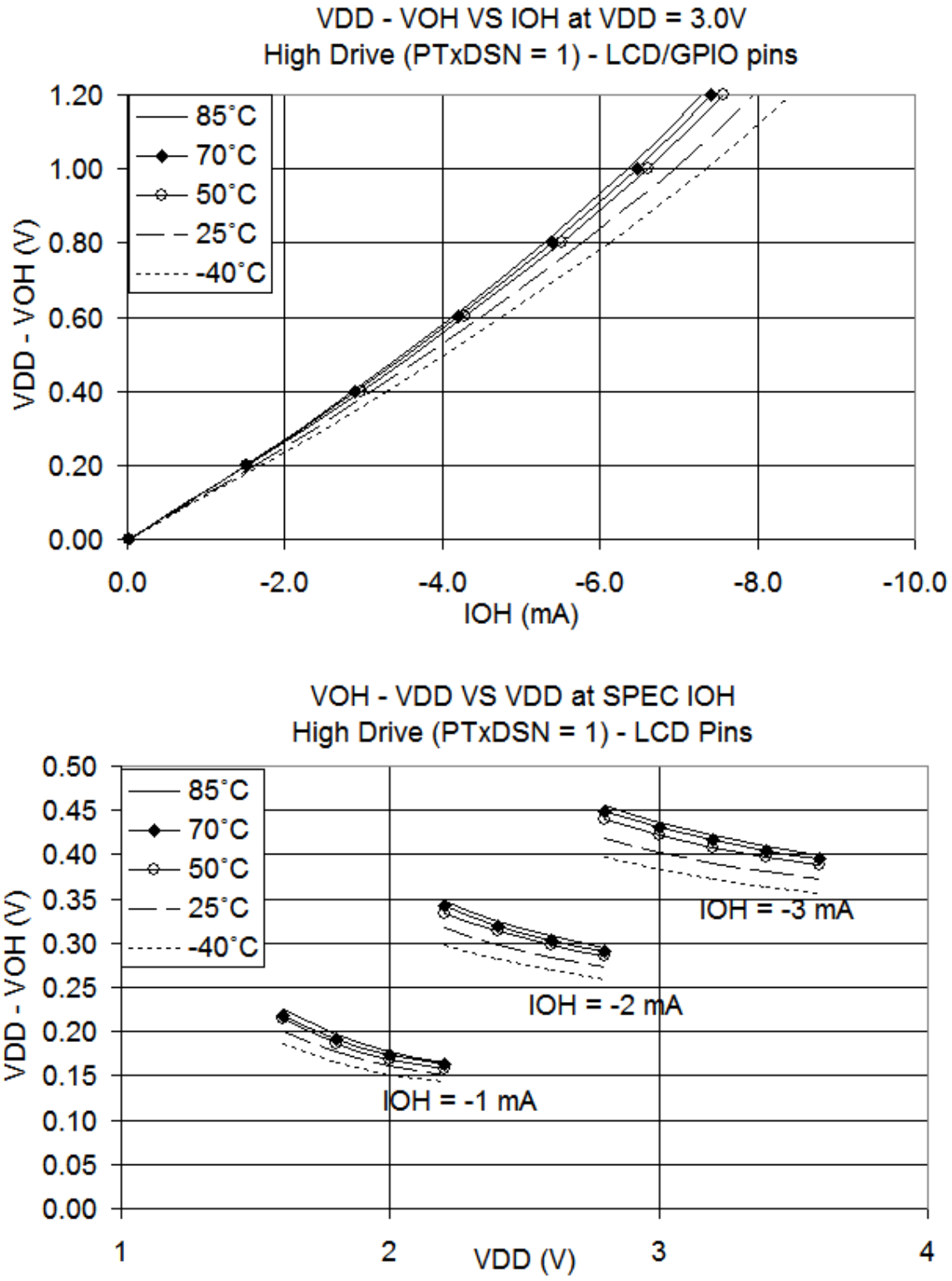


Figure 12. Typical High-Side (Source) Characteristics (LCD/GPIO Pins) — High Drive (PTxDSn = 1)

3.7 Supply Current Characteristics

This section includes information about power supply current in various operating modes.

Table 9. Supply Current Characteristics

Num	C	Parameter	Symbol	Bus Freq	V_{DD} (V)	Typ[1]	Max	Unit	Temp (°C)
1	T	Run supply current FEI mode, all modules on	RI_{DD}	20 MHz	3	13.75	17.9	mA	–40 to 85
	T			8 MHz		7	—		
	T			1 MHz		2	—		
2	T	Run supply current FEI mode, all modules off	RI_{DD}	20 MHz	3	8.9	—	mA	–40 to 85
	T			8 MHz		5.5	—		
	T			1 MHz		0.9	—		
3	T	Run supply current LPS=0, all modules off	RI_{DD}	32 kHz FBILP	3	185	—	µA	–-40 to 85
	T			16 kHz FBELP		115	—		
4	T	Run supply current LPS=1, all modules off, running from Flash	RI_{DD}	16 kHz FBELP	3	21.9	—	µA	0 to 70
							—		–40 to 85
	T	Run supply current LPS=1, all modules off, running from RAM				7.3	—		0 to 70
							—		–40 to 85
5	T	Wait mode supply current FEI mode, all modules off	WI_{DD}	20 MHz	3	4.57	6	mA	–40 to 85
	T			8 MHz		2	—		
	T			1 MHz		0.73	—		
6	P	Stop2 mode supply current	$S2I_{DD}$	n/a	3	0.4	1.3	µA	–40 to 25
	C					4	6		70
	P					8.5	13		85
	C				2	0.35	1.0		–40 to 25
	C					3.9	5		70
	C					7.7	10		85
7	P	Stop3 mode supply current No clocks active	$S3I_{DD}$	n/a	3	0.65	1.8	µA	–40 to 25
	C					5.7	8.0		70
	P					12.2	20		85
	C				2	0.6	1.5		–40 to 25
	C					5	6.8		70
	C					11.5	14		85

[1] Typical values are measured at 25 °C. Characterized, not tested

Table 10. Stop Mode Adders

Num	C	Parameter	Condition	Temperature (°C)				Units
				–40	25	70	85	
1	T	LPO		100	100	150	175	nA
2	T	EREFSTEN	RANGE = HGO = 0	750	750	800	850	nA
3	T	IREFSTEN[1]		63	70	77	81	µA
4	T	TOD	Does not include clock source current	50	50	75	100	nA
5	T	LVD[1]	LVDSE = 1	110	110	112	115	µA
6	T	ACMP[1]	Not using the bandgap (BGBE = 0)	12	12	20	23	µA
7	T	ADC[1]	ADLPC = ADLSMP = 1 Not using the bandgap (BGBE = 0)	95	95	101	120	µA
8	T	LCD	VIREG enabled for Contrast control, 1/8 Duty cycle, 8x24 configuration for driving 192 segments, 32 Hz frame rate, No LCD glass connected.	1	1	6	13	µA
9	T	LCD	LCD configured for 1/8 duty cycle, 8x24 configuration for driving 192 segments, 32 Hz frame rate, no LCD glass connected.	0.2	0.24	0.5	0.65	µA

1 Not available in stop2 mode.

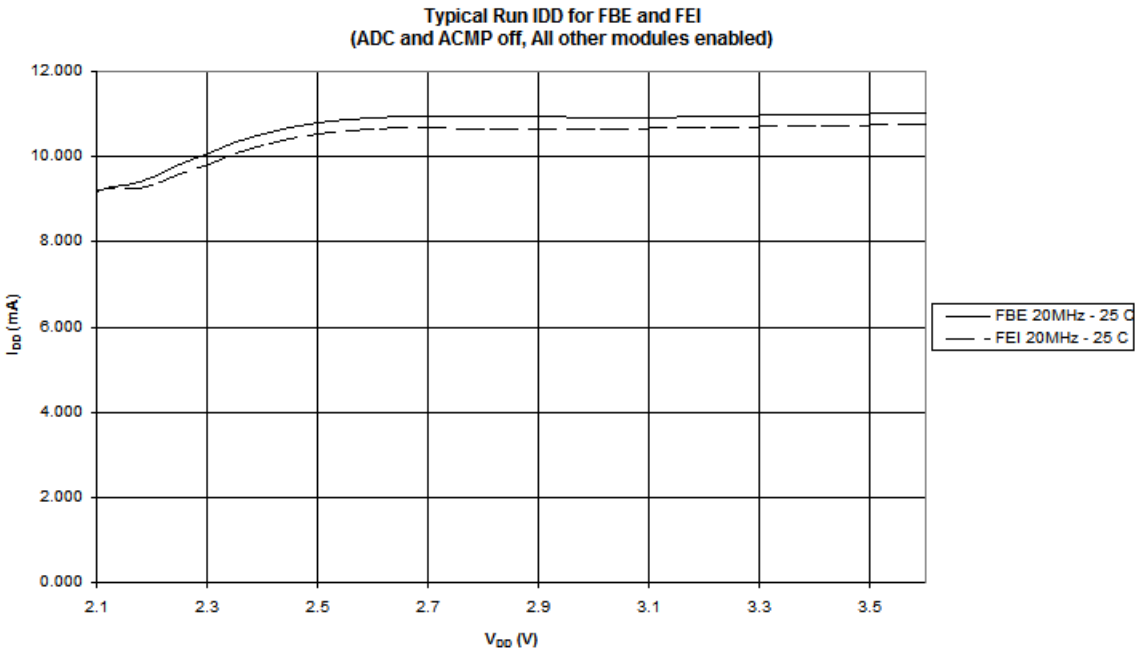


Figure 13. Typical Run I_{DD} for FBE and FEI, I_{DD} vs. V_{DD} (ACMP and ADC off, All Other Modules Enabled)

3.8 External Oscillator (XOSCVLP) Characteristics

See Figure 14 and Figure 15 for crystal or resonator circuits.

Table 11. XOSCVLP and ICS Specifications (Temperature Range = –40 to 85°C Ambient)

Num	C	Characteristic	Symbol	Min	Typ[1]	Max	Unit
1	C	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1) Low range (RANGE = 0) High range (RANGE = 1), high gain (HGO = 1) High range (RANGE = 1), low power (HGO = 0)	 f_{lo} f_{hi} f_{hi}	 32 1 1	 — — —	 38.4 16 8	 kHz MHz MHz
2	D	Load capacitors Low range (RANGE=0), low power (HGO=0) Other oscillator settings	C_1, C_2	See Note [2] See Note [3]			
3	D	Feedback resistor Low range, low power (RANGE=0, HGO=0)[2] Low range, high gain (RANGE=0, HGO=1) High range (RANGE=1, HGO=X)	R_F	 — — —	 — 10 1	 — — —	MΩ
4	D	Series resistor — Low range, low power (RANGE = 0, HGO = 0)[2] Low range, high gain (RANGE = 0, HGO = 1) High range, low power (RANGE = 1, HGO = 0) High range, high gain (RANGE = 1, HGO = 1) ≥ 8 MHz 4 MHz 1 MHz	R_S	 — — — — — —	 — 100 0 0 0 0	 — — — 0 10 20	kΩ
5	C	Crystal start-up time [4] Low range, low power Low range, high gain High range, low power High range, high gain	 t_{CSTL} t_{CSTH}	 — — — —	 600 400 5 15	 — — — —	ms
6	D	Square wave input clock frequency (EREFS = 0, ERCLKEN = 1) FEE mode FBE or FBELP mode	f_{extal}	 0.03125 0	 — —	 20 20	 MHz MHz

1 Data in Typical column was characterized at 3.0 V, 25 °C or is typical recommended value.

2 Load capacitors (C_1, C_2), feedback resistor (R_F) and series resistor (R_S) are incorporated internally when RANGE=HGO=0.

3 See crystal or resonator manufacturer's recommendation.

4 Proper PC board layout procedures must be followed to achieve specifications.

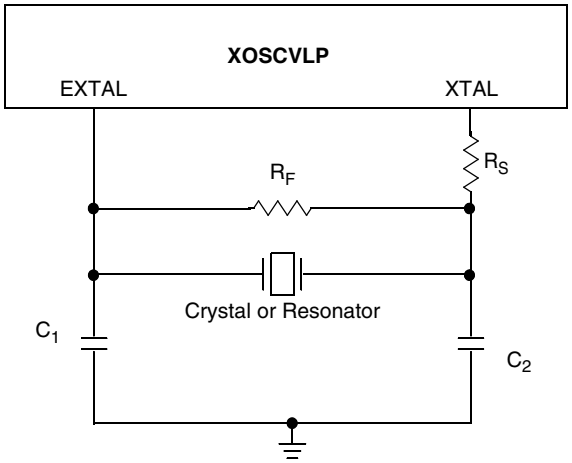


Figure 14. Typical Crystal or Resonator Circuit: High Range and Low Range/High Gain

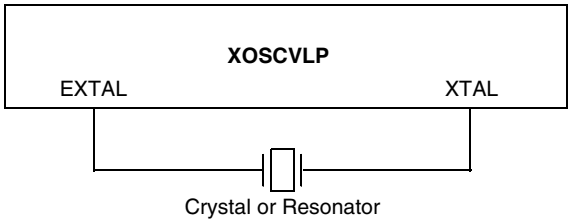


Figure 15. Typical Crystal or Resonator Circuit: Low Range/Low Power

3.9 Internal Clock Source (ICS) Characteristics

Table 12. ICS Frequency Specifications (Temperature Range = –40 to 85 °C Ambient)

Num	C	Characteristic		Symbol	Min	Typ[1]	Max	Unit
1	C	Average internal reference frequency — untrimmed		f_{int_ut}	25	32.7	41.66	kHz
2	P	Average internal reference frequency — user-trimmed		f_{int_t}	31.25	—	39.06	kHz
3	P	Average internal reference frequency — factory-trimmed		f_{int_t}	—	32.7	—	kHz
4	T	Internal reference start-up time		t_{IRST}	—	60	100	µs
5	P	DCO output frequency range — untrimmed	Low range (DFR = 00)	f_{dco_ut}	12.8	16.8	21.33	MHz
	C		Mid range (DFR = 01)		25.6	33.6	42.67	
6	P	DCO output frequency range — trimmed	Low range (DFR = 00)	f_{dco_t}	16	—	20	MHz
	P		Mid range (DFR = 01)		32	—	40	
7	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (using FTRIM)		$\Delta f_{dco_res_t}$	—	±0.1	±0.2	$\%f_{dco}$
8	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (not using FTRIM)		$\Delta f_{dco_res_t}$	—	±0.2	±0.4	$\%f_{dco}$

Table 12. ICS Frequency Specifications (Temperature Range = –40 to 85 °C Ambient) (continued)

Num	C	Characteristic	Symbol	Min	Typ[1]	Max	Unit
9	C	Total deviation of trimmed DCO output frequency over voltage and temperature	Δf_{dco_t}	—	+0.5 –1.0	±2	$\%f_{dco}$
10	C	Total deviation of trimmed DCO output frequency over fixed voltage and temperature range of 0 °C to 70 °C	Δf_{dco_t}	—	±0.5	±1	$\%f_{dco}$
11	C	FLL acquisition time[2]	$t_{Acquire}$	—	—	1	ms
12	C	Long term jitter of DCO output clock (averaged over 2-ms interval)[3]	C_{Jitter}	—	0.02	0.2	$\%f_{dco}$

1 Data in Typical column was characterized at 3.0 V, 25 °C or is typical recommended value.

2 This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

3 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{Bus}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

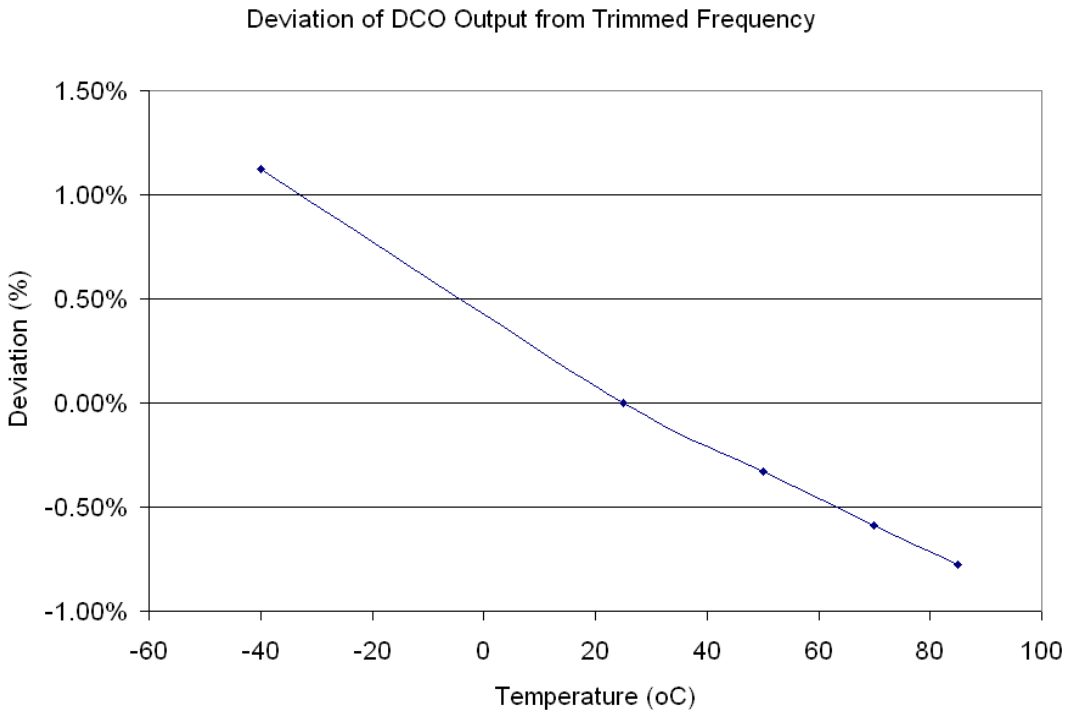


Figure 16. Deviation of DCO Output from Trimmed Frequency (20 MHz, 3.0 V)

3.10 AC Characteristics

This section describes timing characteristics for each peripheral system.

3.10.1 Control Timing

Table 13. Control Timing

Num	C	Rating	Symbol	Min	Typ[1]	Max	Unit
1	D	Bus frequency (t_{cyc} = 1/f_{Bus}) $V_{DD} \leq 2.1V$ $V_{DD} > 2.1V$	f_{Bus}	 dc dc	 — —	 10 20	MHz
2	D	Internal low power oscillator period	t_{LPO}	700	—	1300	µs
3	D	External reset pulse width[2]	t_{extrst}	100	—	—	ns
4	D	Reset low drive	t_{rstdrv}	34 x t_{cyc}	—	—	ns
5	D	BKGD/MS setup time after issuing background debug force reset to enter user or BDM modes	t_{MSSU}	500	—	—	ns
6	D	BKGD/MS hold time after issuing background debug force reset to enter user or BDM modes [3]	t_{MSH}	100	—	—	µs
7	D	IRQ pulse width Asynchronous path[2] Synchronous path[4]	t_{ILIH}, t_{IHIL}	 100 1.5 × t_{cyc}	 — —	 — —	ns
8	D	Keyboard interrupt pulse width Asynchronous path[2] Synchronous path[4]	t_{ILIH}, t_{IHIL}	 100 1.5 × t_{cyc}	 — —	 — —	ns
9	C	Port rise and fall time — Low output drive (PTxDS = 0) (load = 50 pF)[5, 6] Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	 — —	 16 23	 — —	ns
		Port rise and fall time — High output drive (PTxDS = 1) (load = 50 pF)[5, 6] Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	 — —	 5 9	 — —	ns
10	P	Reset pulse width with digital filter	t_{extrst}	—	2	—	ms

1 Typical values are based on characterization data at V_{DD} = 3.0 V, 25 °C unless otherwise stated.

2 This is the shortest pulse that is guaranteed to be recognized as a reset pin request.

3 To enter BDM mode following a POR, BKGD/MS should be held low during the power-up and for a hold time of t_{MSH} after V_{DD} rises above V_{LVD}.

4 This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized.

5 Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40 °C to 85 °C.

6 Except for LCD pins in Open Drain mode.

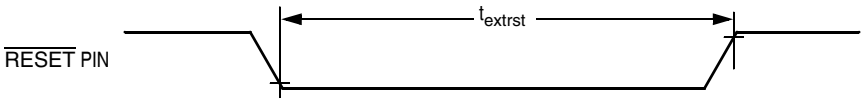


Figure 17. Reset Timing

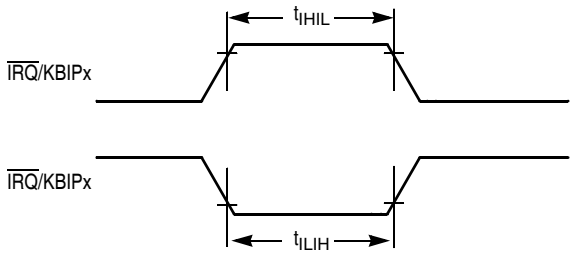


Figure 18. IRQ/KBIPx Timing

3.10.2 TPM Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 14. TPM Input Timing

No.	C	Function	Symbol	Min	Max	Unit
1	D	External clock frequency	f_{TCLK}	0	$f_{Bus}/4$	Hz
2	D	External clock period	t_{TCLK}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

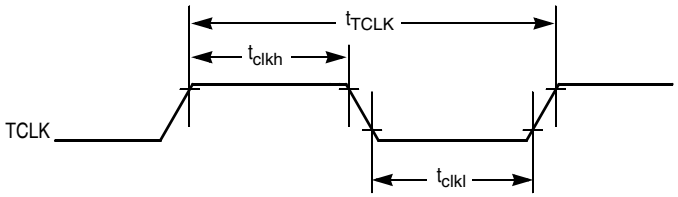


Figure 19. Timer External Clock

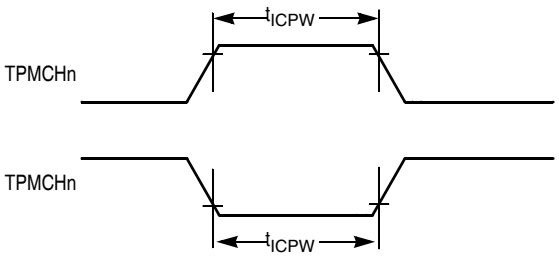


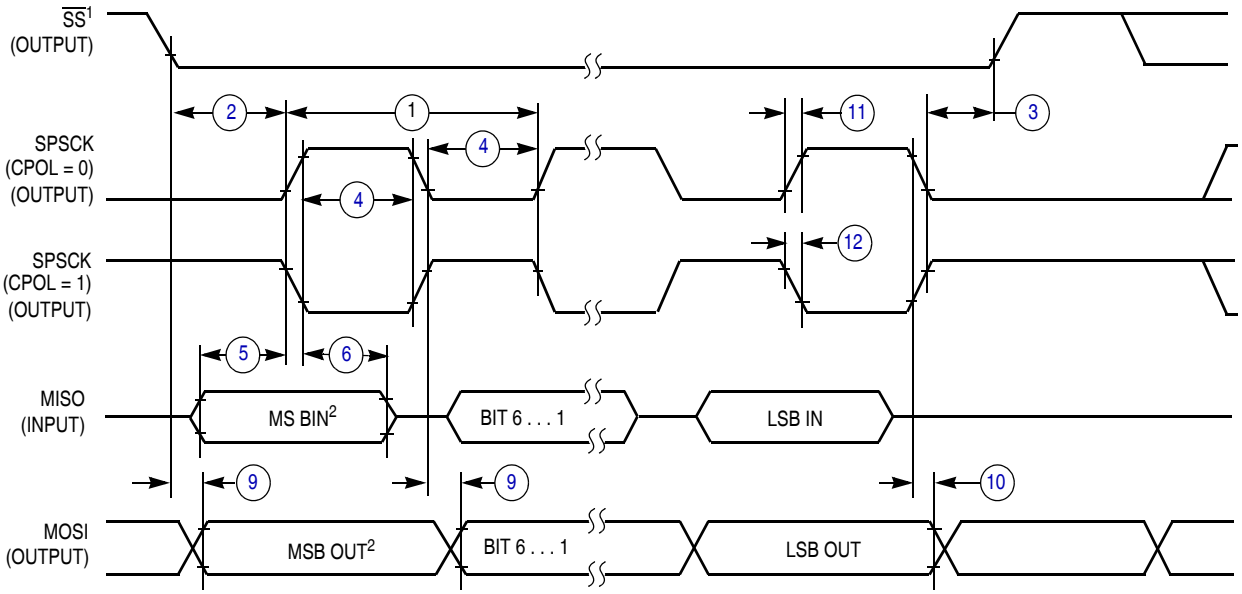
Figure 20. Timer Input Capture Pulse

3.10.3 SPI Timing

Table 15 and Figure 21 through Figure 24 describe the timing requirements for the SPI system.

Table 15. SPI Timing

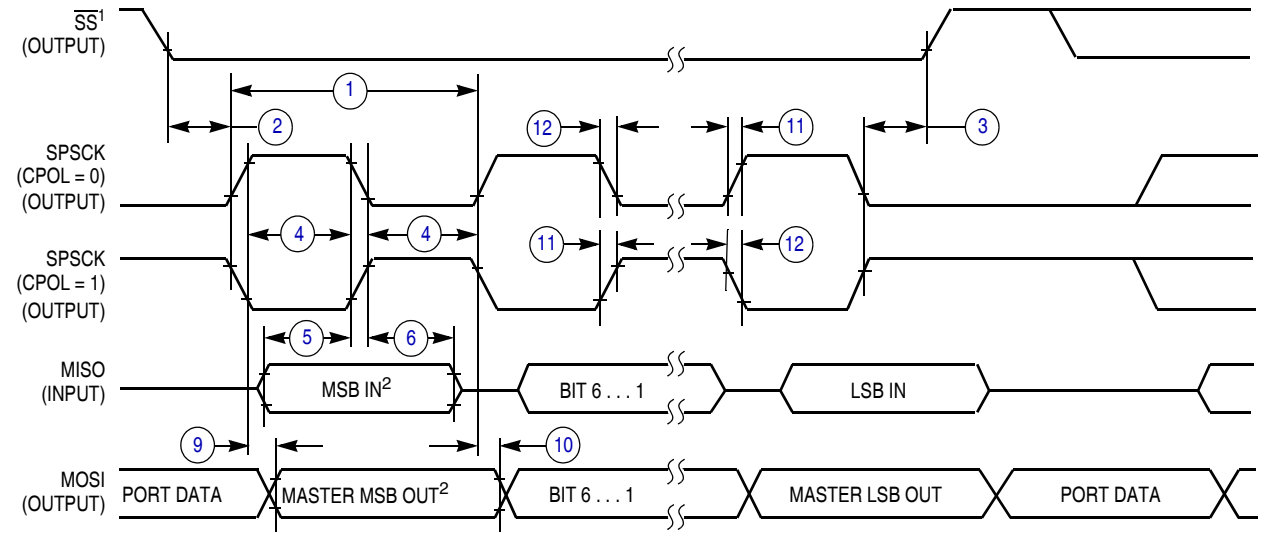
No.	C	Function	Symbol	Min	Max	Unit
—	D	Operating frequency Master Slave	f_{op}	$f_{Bus}/2048$ 0	$f_{Bus}/2$ $f_{Bus}/4$	Hz
①	D	SPSCK period Master Slave	t_{SPSCK}	2 4	2048 —	t_{cyc} t_{cyc}
②	D	Enable lead time Master Slave	t_{Lead}	1/2 1	— —	t_{SPSCK} t_{cyc}
③	D	Enable lag time Master Slave	t_{Lag}	1/2 1	— —	t_{SPSCK} t_{cyc}
④	D	Clock (SPSCK) high or low time Master Slave	t_{WSPSCK}	$t_{cyc} - 30$ $t_{cyc} - 30$	1024 t_{cyc} —	ns ns
⑤	D	Data setup time (inputs) Master Slave	t_{SU}	15 15	— —	ns ns
⑥	D	Data hold time (inputs) Master Slave	t_{HI}	0 25	— —	ns ns
⑦	D	Slave access time	t_a	—	1	t_{cyc}
⑧	D	Slave MISO disable time	t_{dis}	—	1	t_{cyc}
⑨	D	Data valid (after SPSCK edge) Master Slave	t_v	— —	25 25	ns ns
⑩	D	Data hold time (outputs) Master Slave	t_{HO}	0 0	— —	ns ns
⑪	D	Rise time Input Output	t_{RI} t_{RO}	— —	$t_{cyc} - 25$ 25	ns ns
⑫	D	Fall time Input Output	t_{FI} t_{FO}	— —	$t_{cyc} - 25$ 25	ns ns



NOTES:

1. SS output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

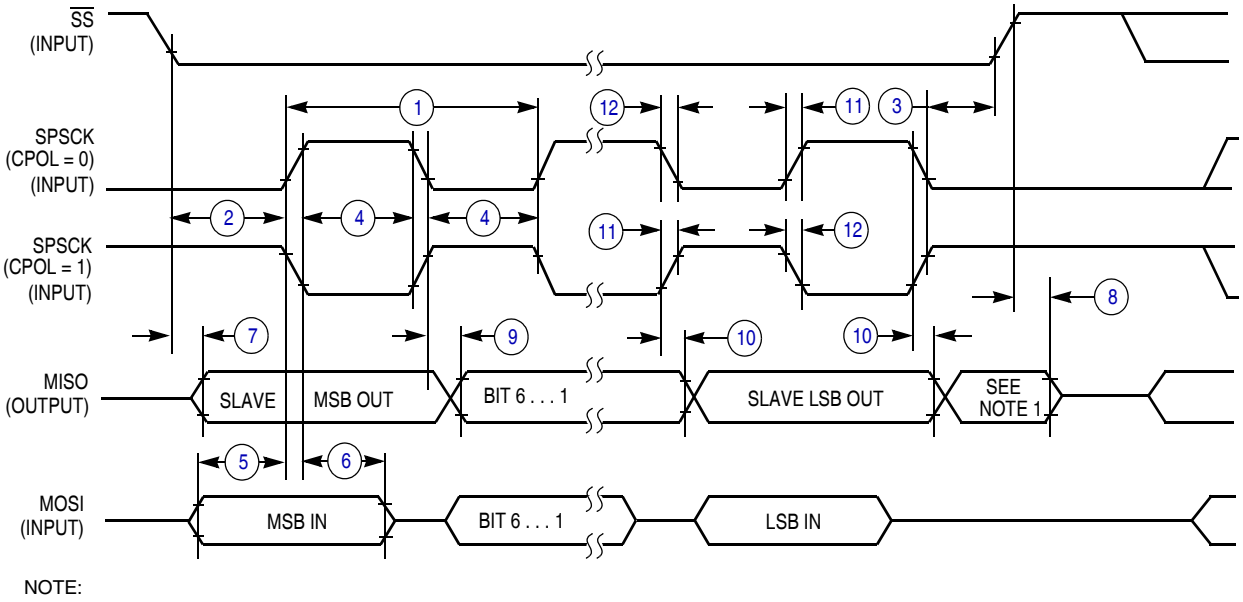
Figure 21. SPI Master Timing (CPHA = 0)



NOTES:

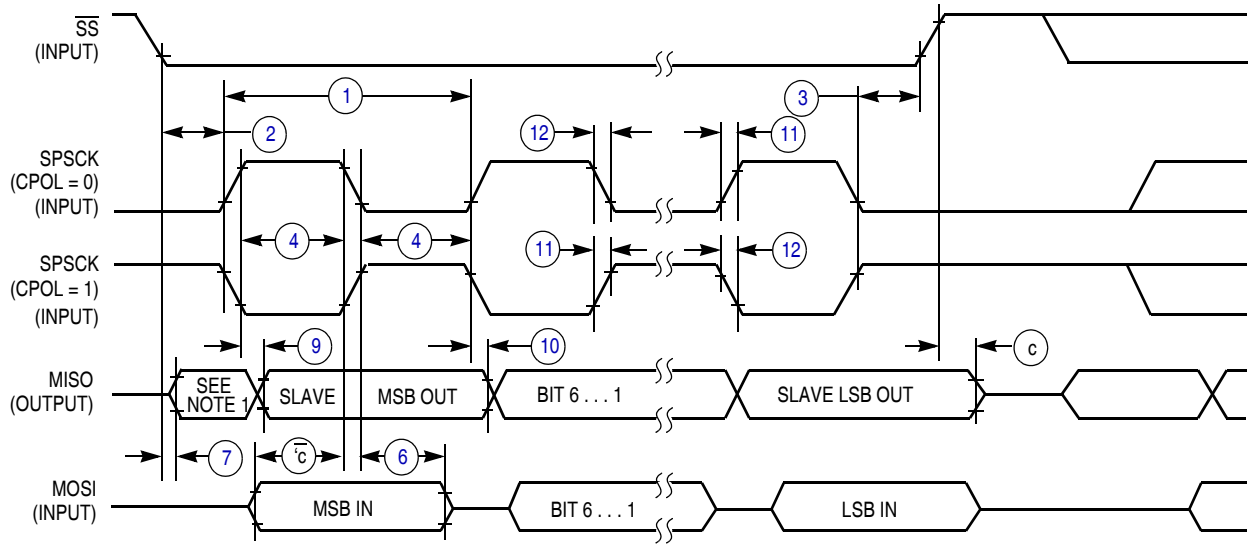
1. $\overline{SS}$ output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 22. SPI Master Timing (CPHA =1)



NOTE:
1. Not defined but normally MSB of character just received.

Figure 23. SPI Slave Timing (CPHA = 0)



NOTE:
1. Not defined but normally LSB of character just received

Figure 24. SPI Slave Timing (CPHA = 1)

3.11 Analog Comparator (ACMP) Electricals

Table 16. Analog Comparator Electrical Specifications

C	Characteristic	Symbol	Min	Typical	Max	Unit
D	Supply voltage	V_{DD}	1.8	—	3.6	V
P	Supply current (active)	I_{DDAC}	—	20	35	μA
D	Analog input voltage	V_{AIN}	V_{SS} – 0.3	—	V_{DD}	V
P	Analog input offset voltage	V_{AIO}		20	40	mV
C	Analog comparator hysteresis	V_H	3.0	9.0	15.0	mV
P	Analog input leakage current	I_{ALKG}	—	—	1.0	μA
C	Analog comparator initialization delay	t_{AINIT}	—	—	1.0	μs

3.12 ADC Characteristics

Table 17. 16-bit ADC Operating Conditions

Num	Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
1	Supply voltage	Absolute	V_{DDA}	1.8	—	3.6	V	
2		Delta to V_{DD} (V_{DD}–V_{DDA})[2]	ΔV_{DDA}	–100	0	100	mV	
3	Ground voltage	Delta to V_{SS} (V_{SS}–V_{SSA})[2]	ΔV_{SSA}	–100	0	100	mV	
4	Ref Voltage High		V_{REFH}	1.15	V_{DDA}	V_{DDA}	V	
5	Ref Voltage Low		V_{REFL}	V_{SSA}	V_{SSA}	V_{SSA}	V	
6	Input Voltage		V_{ADIN}	V_{REFL}	—	V_{REFH}	V	
7	Input Capacitance	16-bit modes 8/10/12-bit modes	C_{ADIN}	—	8 4	10 5	pF	
8	Input Resistance		R_{ADIN}	—	2	5	kΩ	

Table 17. 16-bit ADC Operating Conditions

Num	Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
9	Analog Source Resistance	16 bit modes $f_{ADCK} > 8MHz$ $4MHz < f_{ADCK} < 8MHz$ $f_{ADCK} < 4MHz$	R_{AS}	— — —	— — —	0.5 1 2	kΩ	External to MCU Assumes ADLSMP=0
10		13/12 bit modes $f_{ADCK} > 8MHz$ $4MHz < f_{ADCK} < 8MHz$ $f_{ADCK} < 4MHz$		— — —	— — —	1 2 5		
11		11/10 bit modes $f_{ADCK} > 8MHz$ $4MHz < f_{ADCK} < 8MHz$ $f_{ADCK} < 4MHz$		— — —	— — —	2 5 10		
12		9/8 bit modes $f_{ADCK} > 8MHz$ $f_{ADCK} < 8MHz$		— —	— —	5 10		
13	ADC Conversion Clock Freq.	ADLPC = 0, ADHSC = 1	f_{ADCK}	1.0	—	8	MHz	
14		ADLPC = 0, ADHSC = 0		1.0	—	5		
15		ADLPC = 1, ADHSC = 0		1.0	—	2.5		

1 Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 DC potential difference.

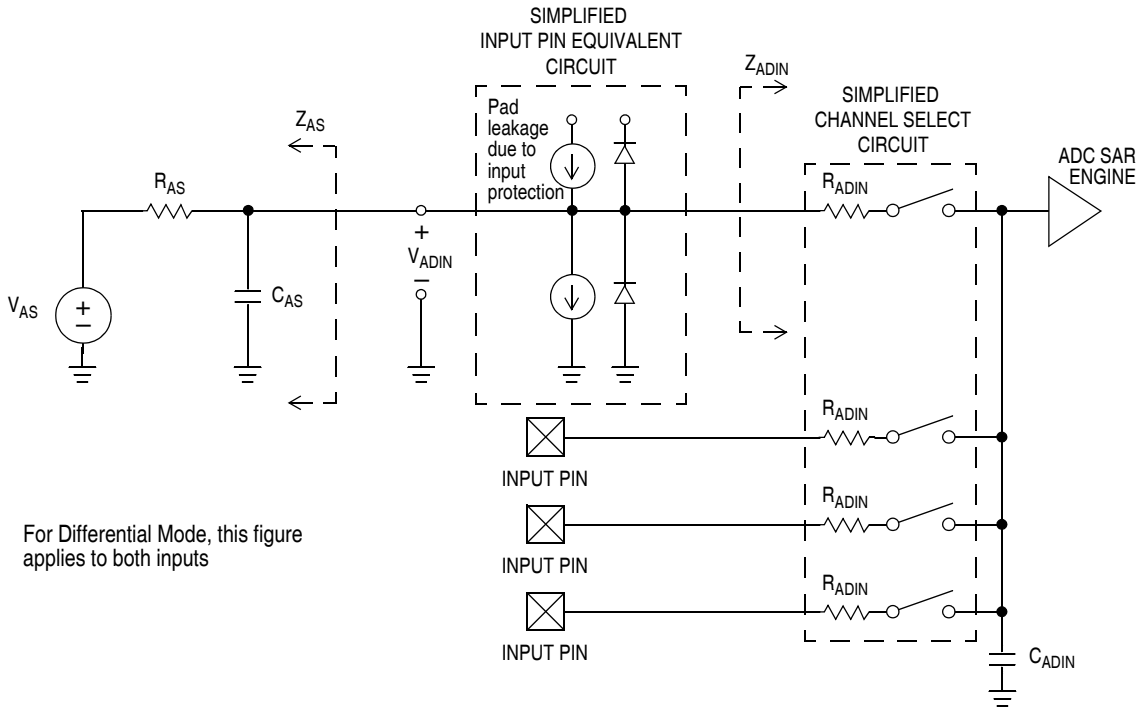


Figure 25. ADC Input Impedance Equivalency Diagram

Table 18. 16-bit ADC Characteristics full operating range($V_{REFH} = V_{DDA} > 1.8$, $V_{REFL} = V_{SSA}$, $F_{ADCK} \leq 8MHz$)

Characteristic	Conditions[1]	C	Symb	Min	Typ[2]	Max	Unit	Comment
Supply Current	ADLPC = 1, ADHSC = 0	T	I_{DDA}	—	215	—	μA	ADLSMP = 0 ADCO = 1
	ADLPC = 0, ADHSC = 0			—	470	—		
	ADLPC=0, ADHSC=1			—	610	—		
Supply Current	Stop, Reset, Module Off	C	I_{DDA}	—	0.01	—	μA	
ADC Asynchronous Clock Source	ADLPC = 1, ADHSC = 0	P	f_{ADACK}	—	2.4	—	MHz	$t_{ADACK} = 1/f_{ADACK}$
	ADLPC = 0, ADHSC = 0			—	5.2	—		
	ADLPC = 0, ADHSC = 1			—	6.2	—		
Sample Time	See reference manual for sample times							
Conversion Time	See reference manual for conversion times							

Table 18. 16-bit ADC Characteristics full operating range($V_{REFH} = V_{DDA} > 1.8$, $V_{REFL} = V_{SSA}$, $F_{ADCK} \leq 8MHz$)

Characteristic	Conditions[1]	C	Symb	Min	Typ[2]	Max	Unit	Comment
Total Unadjusted Error	16-bit differential mode 16-bit single-ended mode	T	TUE	— —	±16 ±20	+48/-40 +56/-28	LSB[3]	32x Hardware Averaging (AVGE = %1 AVGS = %11)
	13-bit differential mode 12-bit single-ended mode	T		— —	±1.5 ±1.75	±3.0 ±3.5		
	11-bit differential mode 10-bit single-ended mode	T		— —	±0.7 ±0.8	±1.5 ±1.5		
	9-bit differential mode 8-bit single-ended mode	T		— —	±0.5 ±0.5	±1.0 ±1.0		
Differential Non-Linearity	16-bit differential mode 16-bit single-ended mode	T	DNL	— —	±2.5 ±2.5	+5/-3 +5/-3	LSB[2]	
	13-bit differential mode 12-bit single-ended mode	T		— —	±0.7 ±0.7	±1 ±1		
	11-bit differential mode 10-bit single-ended mode	T		— —	±0.5 ±0.5	±0.75 ±0.75		
	9-bit differential mode 8-bit single-ended mode	T		— —	±0.2 ±0.2	±0.5 ±0.5		
Integral Non-Linearity	16-bit differential mode 16-bit single-ended mode	T	INL	— —	±6.0 ±10.0	±16.0 ±20.0	LSB[2]	
	13-bit differential mode 12-bit single-ended mode	T		— —	±1.0 ±1.0	±2.5 ±2.5		
	11-bit differential mode 10-bit single-ended mode	T		— —	±0.5 ±0.5	±1.0 ±1.0		
	9-bit differential mode 8-bit single-ended mode	T		— —	±0.3 ±0.3	±0.5 ±0.5		
Zero-Scale Error	16-bit differential mode 16-bit single-ended mode	T	E_{ZS}	— —	±4.0 ±4.0	+32/-24 +24/-16	LSB[2]	$V_{ADIN} = V_{SSA}$
	13-bit differential mode 12-bit single-ended mode	T		— —	±0.7 ±0.7	±2.5 ±2.0		
	11-bit differential mode 10-bit single-ended mode	T		— —	±0.4 ±0.4	±1.0 ±1.0		
	9-bit differential mode 8-bit single-ended mode	T		— —	±0.2 ±0.2	±0.5 ±0.5		

Table 18. 16-bit ADC Characteristics full operating range(V_{REFH} = V_{DDA} > 1.8, V_{REFL} = V_{SSA}, F_{ADCK} ≤ 8MHz)

Characteristic	Conditions[1]	C	Symb	Min	Typ[2]	Max	Unit	Comment
Full-Scale Error	16-bit differential mode 16-bit single-ended mode	T	E_{FS}	— —	+10/0 +14/0	+42/-2 +46/-2	LSB[2]	V_{ADIN} = V_{DDA}
	13-bit differential mode 12-bit single-ended mode	T		— —	±1.0 ±1.0	±3.5 ±3.5		
	11-bit differential mode 10-bit single-ended mode	T		— —	±0.4 ±0.4	±1.5 ±1.5		
	9-bit differential mode 8-bit single-ended mode	T		— —	±0.2 ±0.2	±0.5 ±0.5		
Quantization Error	16-bit modes	D	E_Q	—	-1 to 0	—	LSB[2]	
	≤13-bit modes			—	—	±0.5		
Effective Number of Bits	16-bit differential mode Avg = 32 Avg = 16 Avg = 8 Avg = 4 Avg = 1	C	ENOB	 12.8 12.7 12.6 12.5 11.9	 14.2 13.8 13.6 13.3 12.5	 — — — — —	Bits	F_{in} = F_{sample}/100
	16-bit single-ended mode Avg = 32 Avg = 16 Avg = 8 Avg = 4 Avg = 1	D		 — — — — —	 13.2 12.8 12.6 12.3 11.5	 — — — — —		
Signal to Noise plus Distortion	See ENOB		SINAD	$SINAD = 6.02 \cdot ENOB + 1.76$			dB	
Total Harmonic Distortion	16-bit differential mode Avg = 32	C	THD	—	-91.5	-74.3	dB	F_{in} = F_{sample}/100
	16-bit single-ended mode Avg = 32	D		—	-85.5	—		
Spurious Free Dynamic Range	16-bit differential mode Avg = 32	C	SFDR	75.0	92.2	—	dB	F_{in} = F_{sample}/100
	16-bit single-ended mode Avg = 32	D		—	86.2	—		
Input Leakage Error	all modes	D	E_{IL}	I_{In} * R_{AS}			mV	I_{In} = leakage current (refer to DC characteristics)
Temp Sensor Slope	-40 °C– 25 °C	C	m	—	1.646	—	mV/°C	
	25 °C– 125 °C			—	1.769	—		
Temp Sensor Voltage	25 °C	C	V_{TEMP25}	—	701.2	—	mV	

1 All accuracy numbers assume the ADC is calibrated with V_{REFH}=V_{DDA}

2 Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK}=2.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

3 1 LSB = (V_{REFH} - V_{REFL})/2^N

Table 19. 16-bit ADC Characteristics(V_{REFH} = V_{DDA} ≥ 2.7V, V_{REFL} = V_{SSA}, F_{ADCK} ≤ 4MHz, ADHSC=1)

Characteristic	Conditions[1]	C	Symb	Min	Typ[2]	Max	Unit	Comment
Total Unadjusted Error	16-bit differential mode 16-bit single-ended mode	T	TUE	— —	±16 ±20	+24/-24 +32/-20	LSB[3]	32x Hardware Averaging (AVGE = %1 AVGS = %11)
	13-bit differential mode 12-bit single-ended mode	T		— —	±1.5 ±1.75	±2.0 ±2.5		
	11-bit differential mode 10-bit single-ended mode	T		— —	±0.7 ±0.8	±1.0 ±1.25		
	9-bit differential mode 8-bit single-ended mode	T		— —	±0.5 ±0.5	±1.0 ±1.0		
Differential Non-Linearity	16-bit differential mode 16-bit single-ended mode	T	DNL	— —	±2.5 ±2.5	±3 ±3	LSB[2]	
	13-bit differential mode 12-bit single-ended mode	T		— —	±0.7 ±0.7	±1 ±1		
	11-bit differential mode 10-bit single-ended mode	T		— —	±0.5 ±0.5	±0.75 ±0.75		
	9-bit differential mode 8-bit single-ended mode	T		— —	±0.2 ±0.2	±0.5 ±0.5		
Integral Non-Linearity	16-bit differential mode 16-bit single-ended mode	T	INL	— —	±6.0 ±10.0	±12.0 ±16.0	LSB[2]	
	13-bit differential mode 12-bit single-ended mode	T		— —	±1.0 ±1.0	±2.0 ±2.0		
	11-bit differential mode 10-bit single-ended mode	T		— —	±0.5 ±0.5	±1.0 ±1.0		
	9-bit differential mode 8-bit single-ended mode	T		— —	±0.3 ±0.3	±0.5 ±0.5		
Zero-Scale Error	16-bit differential mode 16-bit single-ended mode	T	E_{ZS}	— —	±4.0 ±4.0	+16/0 +16/-8	LSB[2]	V_{ADIN} = V_{SSA}
	13-bit differential mode 12-bit single-ended mode	T		— —	±0.7 ±0.7	±2.0 ±2.0		
	11-bit differential mode 10-bit single-ended mode	T		— —	±0.4 ±0.4	±1.0 ±1.0		
	9-bit differential mode 8-bit single-ended mode	T		— —	±0.2 ±0.2	±0.5 ±0.5		

Table 19. 16-bit ADC Characteristics(V_{REFH} = V_{DDA} ≥ 2.7V, V_{REFL} = V_{SSA}, F_{ADCK} ≤ 4MHz, ADHSC=1)

Characteristic	Conditions[1]	C	Symb	Min	Typ[2]	Max	Unit	Comment
Full-Scale Error	16-bit differential mode 16-bit single-ended mode	T	E_{FS}	— —	+8/0 +12/0	+24/0 +24/0	LSB[2]	V_{ADIN} = V_{DDA}
	13-bit differential mode 12-bit single-ended mode	T		— —	±0.7 ±0.7	±2.0 ±2.5		
	11-bit differential mode 10-bit single-ended mode	T		— —	±0.4 ±0.4	±1.0 ±1.0		
	9-bit differential mode 8-bit single-ended mode	T		— —	±0.2 ±0.2	±0.5 ±0.5		
Quantization Error	16 bit modes	D	E_Q	—	-1 to 0	—	LSB[2]	
	≤13 bit modes			—	—	±0.5		
Effective Number of Bits	16 bit differential mode Avg=32 Avg=16 Avg=8 Avg=4 Avg=1	C	ENOB	 14.3 13.8 13.4 13.1 12.4	 14.5 14.0 13.7 13.4 12.6	 — — — — —	Bits	F_{in} = F_{sample}/100
	16 bit single-ended mode Avg=32 Avg=16 Avg=8 Avg=4 Avg=1			 TBD TBD TBD TBD TBD	 13.5 13.0 12.7 12.4 11.6	 — — — — —		
Signal to Noise plus Distortion	See ENOB		SINAD	SINAD = 6.02 *ENOB +1.76			dB	
Total Harmonic Distortion	16 bit differential mode Avg=32	C	THD	—	-95.8	-90.4	dB	F_{in} = F_{sample}/100
	16 bit single-ended mode Avg=32	D		—	—	—		
Spurious Free Dynamic Range	16 bit differential mode Avg=32	C	SFDR	91.0	96.5	—	dB	F_{in} = F_{sample}/100
	16 bit single-ended mode Avg=32	D		—	—	—		
Input Leakage Error	all modes	D	E_{IL}	I_{In} * R_{AS}			mV	I_{In} = leakage current (refer to DC characteristics)
Temp Sensor Slope	-40 °C– 25 °C	D	m	—	1.646	—	mV/°C	
	25 °C– 125 °C			—	1.769	—		
Temp Sensor Voltage	25 °C	D	V_{TEMP25}	—	701.2	—	mV	

[1] All accuracy numbers assume the ADC is calibrated with V_{REFH}=V_{DDA}

2 Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 2.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

3 1 LSB = $(V_{REFH} - V_{REFL})/2^N$

3.13 VREF Specifications

Table 20. VREF Electrical Specifications

Num	Characteristic	Symbol	Min	Max	Unit
1	Supply voltage	V_{DD}	1.80	3.60	V
2	Operating temperature range	T_{op}	–40	105	C
3	Maximum Load	—	—	10	mA
Operation across Temperature					
4	V Room Temp	V Room Temp	1.135	1.165	V
5	Untrimmed –40 °C	Untrimmed –40 °C	–2 to –6 from Room Temp Voltage		mV
6	Trimmed –40 °C	Trimmed –40 °C	± 1 from Room Temp Voltage		mV
7	Untrimmed 0 °C	Untrimmed 0 °C	+1 to –2 from Room Temp Voltage		mV
	Trimmed 0 °C	Trimmed 0 °C	± 0.5 from Room Temp Voltage		mV
8	Untrimmed 50 °C	Untrimmed 50 °C	+1 to –2 from Room Temp Voltage		mV
9	Trimmed 50 °C	Trimmed 50 °C	± 0.5 from Room Temp Voltage		mV
10	Untrimmed 85 °C	Untrimmed 85 °C	0 to –4 from Room Temp Voltage		mV
11	Trimmed 85 °C	Trimmed 85 °C	± 0.5 from Room Temp Voltage		mV
12	Untrimmed 125 °C	Untrimmed 125 °C	–2 to –6 from Room Temp Voltage		mV
13	Trimmed 125 °C	Trimmed 125 °C	± 1 from Room Temp Voltage		mV
14	Load Bandwidth	—	—	—	—
15	Load Regulation Mode = 10 at 1mA load	Mode = 10	20	100	µV/mA
16	Line Regulation (Power Supply Rejection)	DC	± 0.1 from Room Temp Voltage		mV
		AC	–60		dB
Power Consumption					
17	Powered down Current (Stop Mode, VREFEN = 0, VRSTEN = 0)	I	—	.100	µA
18	Bandgap only (Mode[1:0] 00)	I	—	75	µA
19	Low-Power buffer (Mode[1:0] 01)	I	—	125	µA
20	Tight-Regulation buffer (Mode[1:0] 10)	I	—	1.1	mA
21	Reserved (Mode[1:0] 11)	—	—	—	—

3.14 LCD Specifications

Table 21. LCD Electricals, 3-V Glass

#	C	Characteristic	Symbol	Min	Typ	Max	Unit
1	D	LCD Supply Voltage	V_{LCD}	0.9	1.5	1.8	V
2	D	LCD Frame Frequency	f_{Frame}	28	30	58	Hz
3	D	LCD Charge Pump Capacitance	C_{LCD}	—	100	100	nF
4	D	LCD Bypass Capacitance	C_{BYLCD}	—	100	100	nF
5	D	LCD Glass Capacitance	C_{glass}	—	2000	8000	pF
6	D	V_{IREG} HRefSel = 0	V_{IREG}	0.89	1.00	1.15	V
7		V_{IREG} HRefSel = 1		1.49	1.67	1.85[1]	
8	D	V_{IREG} TRIM Resolution	Δ_{RTRIM}	1.5	—	—	% V_{IREG}
9	D	V_{IREG} Ripple HRefSel = 0	—	—	—	0.1	V
10		HRefSel = 1	—	—	—	0.15	
11	D	V_{LCD} Buffered Adder[2]	I_{Buff}	—	1		µA

1 V_{IREG} Max can not exceed V_{DD} – 0.15 V

2 VSUPPLY = 10, BYPASS = 0

3.15 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the flash memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see the Memory section of the reference manual.

Table 22. Flash Characteristics

#	C	Characteristic	Symbol	Min	Typical	Max	Unit
1	D	Supply voltage for program/erase –40 °C to 85 °C	$V_{prog/erase}$	1.8	—	3.6	V
2	D	Supply voltage for read operation	V_{Read}	1.8	—	3.6	V
3	D	Internal FCLK frequency[1]	f_{FCLK}	150	—	200	kHz
4	D	Internal FCLK period (1/FCLK)	t_{Fcyc}	5	—	6.67	µs
5	P	Byte program time (random location)[2]	t_{prog}	9			t_{Fcyc}
6	P	Byte program time (burst mode)[2]	t_{Burst}	4			t_{Fcyc}
7	P	Page erase time[2]	t_{Page}	4000			t_{Fcyc}
8	P	Mass erase time[2]	t_{Mass}	20,000			t_{Fcyc}
9	D	Byte program current[3]	R_{IDDBP}	—	4	—	mA

1 The frequency of this clock is controlled by a software setting.

2 These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

3 The program and erase currents are additional to the standard run I_{DD}. These values are measured at room temperatures with V_{DD} = 3.0 V, bus frequency = 4.0 MHz.

3.16 EMC Performance

Electromagnetic compatibility (EMC) performance is highly dependent on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation all play a significant role in EMC performance. The system designer should consult Freescale applications notes such as AN2321, AN1050, AN1263, AN2764, and AN1259 available on www.freescale.com for advice and guidance specifically targeted at optimizing EMC performance.

3.16.1 Radiated Emissions

Microcontroller radiated RF emissions are measured from 150 kHz to 1 GHz using the TEM/GTEM Cell method in accordance with the IEC 61967-2 and SAE J1752/3 standards. The measurement is performed with the microcontroller installed on a custom EMC evaluation board while running specialized EMC test software. The radiated emissions from the microcontroller are measured in a TEM cell in two package orientations (North and East).

4 Ordering Information

This appendix contains ordering information for the device numbering system.

Table 23. Device Numbering System

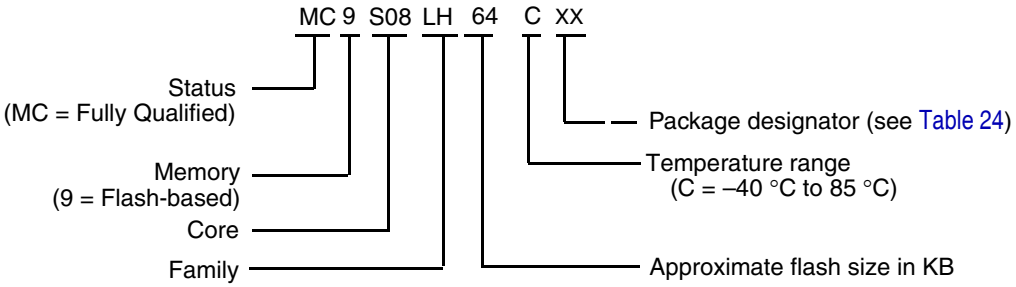
Device Number[1]	Memory		Available Packages[2]
	Flash	RAM	
MC9S08LH64	64 KB	4000	80-pin LQFP
	64 KB	4000	64-pin LQFP
MC9S08LH36	36 KB	4000	80-pin LQFP
	36 KB	4000	64-pin LQFP

1 See Table 1 for a complete description of modules included on each device.

2 See Table 24 for package information.

4.1 Device Numbering System

Example of the device numbering system:



4.2 Package Information

Table 24. Package Descriptions

Pin Count	Package Type	Abbreviation	Designator	Case No.	Document No.
80	Low Quad Flat Package	LQFP	LK	917A	98ASS23237W
64	Low Quad Flat Package	LQFP	LH	840F	98ASS23234W

4.3 Mechanical Drawings

Table 24 provides the available package types and their document numbers. The latest package outline/mechanical drawings are available on the MC9S08LH64 Series Product Summary pages at http://www.freescale.com.

To view the latest drawing, either:

- Click on the appropriate link in Table 24, or
- Open a browser to the Freescale website (http://www.freescale.com), and enter the appropriate document number (from Table 24) in the “Enter Keyword” search box at the top of the page.

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