IXYS

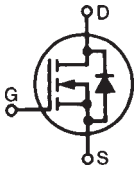
X-Class Power MOSFET

IXTP32N65XM

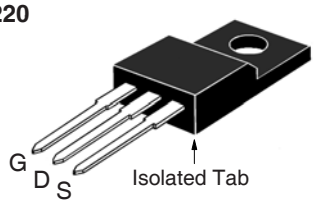
V_{DSS} = 650V
I_{D25} = 32A
$R_{DS(on)}$ ≤ 135mΩ

(Electrically Isolated Tab)

N-Channel Enhancement Mode



OVERMOLDED TO-220



G = Gate D = Drain
S = Source

Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	T_J = 25°C to 150°C	650	V
V_{DGR}	T_J = 25°C to 150°C, R_{GS} = 1MΩ	650	V
V_{GSS}	Continuous	±30	V
V_{GSM}	Transient	±40	V
I_{D25}	T_C = 25°C, Limited by T_{JM}	32	A
I_{DM}	T_C = 25°C, Pulse Width Limited by T_{JM}	64	A
dv/dt	$I_S \le I_{D25}$, $V_{DD} \le V_{DSS}$, $T_J \le 150°C$	30	V/ns
P_D	T_C = 25°C	78	W
T_J		-55 ... +150	°C
T_{JM}		150	°C
T_{stg}		-55 ... +150	°C
T_L	Maximum Lead Temperature for Soldering	300	°C
T_{SOLD}	Plastic Body for 10s	260	°C
V_{ISOL}	50/60 Hz, 1 Minute	2500	V~
M_d	Mounting Torque	1.13 / 10	Nm/lb.in
Weight		2.5	g

Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
BV_{DSS}	V_{GS} = 0V, I_D = 250μA	650			V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250μA	3.0		5.5	V
I_{GSS}	V_{GS} = ±30V, V_{DS} = 0V			±100	nA
I_{DSS}	$V_{DS} = V_{DSS}$, V_{GS} = 0V			5	μA
	T_J = 125°C			50	μA
$R_{DS(on)}$	V_{GS} = 10V, I_D = 16A, Note 1			135	mΩ

Features

- International Standard Package
- Plastic Overmolded Tab
- Low $R_{DS(ON)}$ and Q_G
- Avalanche Rated
- 2500V~ Electrical Isolation
- Low Package Inductance

Advantages

- High Power Density
- Easy to Mount
- Space Savings

Applications

- Switch-Mode and Resonant-Mode Power Supplies
- DC-DC Converters
- PFC Circuits
- AC and DC Motor Drives
- Robotics and Servo Controls

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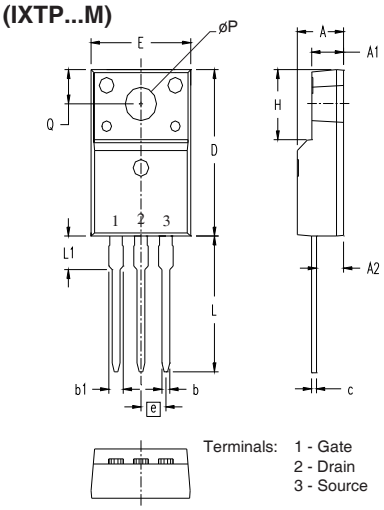
Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max	
g_{fs}	V_{DS} = 10V, I_D = 16A, Note 1	13	22		S
R_{Gi}	Gate Input Resistance		2.6		Ω
C_{iss}	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz		2205		pF
C_{oss}			1600		pF
C_{rss}			30		pF
	Effective Output Capacitance				
$C_{o(er)}$	Energy related; V_{GS} = 0V, V_{DS} = 0.8 • V_{DSS}		111		pF
$C_{o(tr)}$	Time related; V_{GS} = 0V, V_{DS} = 0.8 • V_{DSS}		349		pF
$t_{d(on)}$	**Resistive Switching Times**		23		ns
t_r	V_{GS} = 10V, V_{DS} = 0.5 • V_{DSS}, I_D = 16A		49		ns
$t_{d(off)}$	R_G = 5Ω (External)		58		ns
t_f			28		ns
$Q_{g(on)}$	V_{GS} = 10V, V_{DS} = 0.5 • V_{DSS}, I_D = 16A		54		nC
Q_{gs}			12		nC
Q_{gd}			29		nC
R_{thJC}				1.6	°C/W

Source-Drain Diode

Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max	
I_S	V_{GS} = 0V, Note1			32	A
I_{SM}	Repetitive, pulse Width Limited by T_{JM}			128	A
V_{SD}	I_F = I_S, V_{GS} = 0V, Note 1			1.4	V
t_{rr}	I_F = 16A, -di/dt = 100A/μs		400		ns
Q_{RM}	V_R = 100V		6.1		μC
I_{RM}			31		A

Note 1. Pulse test, t ≤ 300μs, duty cycle, d ≤ 2%.

OVERMOLDED TO-220 (IXTP...M)



SYM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.177	.193	4.50	4.90
A1	.092	.108	2.34	2.74
A2	.101	.117	2.56	2.96
b	.028	.035	0.70	0.90
b1	.050	.058	1.27	1.47
c	.018	.024	0.45	0.60
D	.617	.633	15.67	16.07
E	.392	.408	9.96	10.36
e	.100 BSC		2.54 BSC	
H	.255	.271	6.48	6.88
L	.499	.523	12.68	13.28
L1	.119	.135	3.03	3.43
ØP	.121	.129	3.08	3.28
Q	.126	.134	3.20	3.40

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IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents: 4,835,592 4,860,072 4,881,106 4,931,844 5,017,508 5,034,796 5,049,961 5,063,307 5,187,117 5,237,481 5,381,025 5,486,715 6,162,665 6,259,123B1 6,306,728B1 6,404,065B1 6,534,343 6,583,505 6,683,344 6,710,405B2 6,710,463 6,727,585 6,759,692 6,771,478B2 7,005,734B2 7,063,975B2 7,071,537 7,157,338B2

Fig. 1. Output Characteristics @ T_J = 25°C

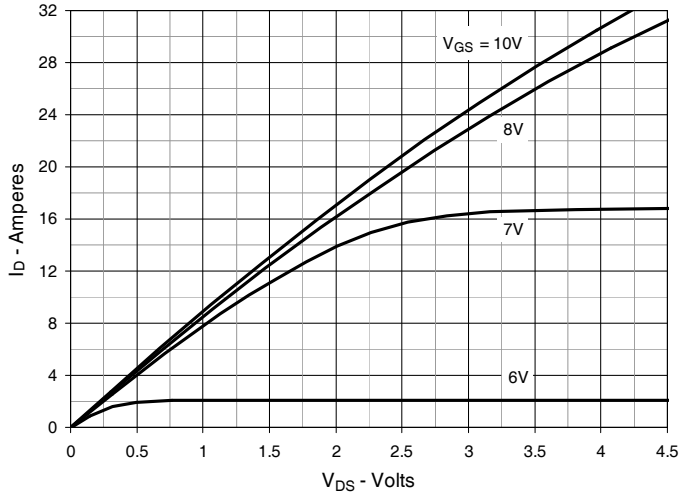


Fig. 2. Extended Output Characteristics @ T_J = 25°C

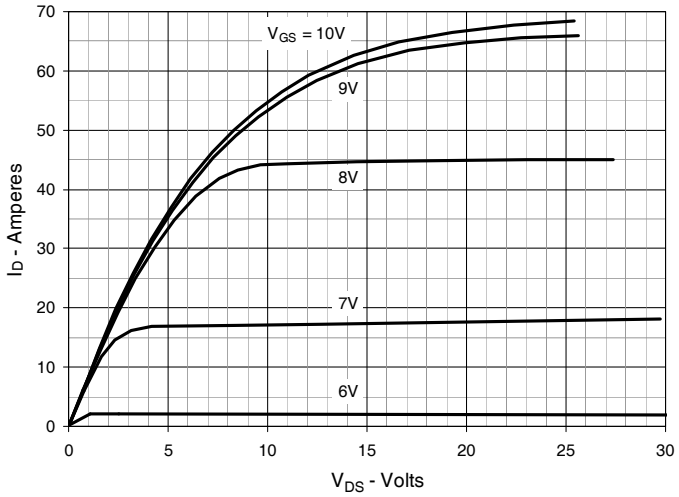


Fig. 3. Output Characteristics @ T_J = 125°C

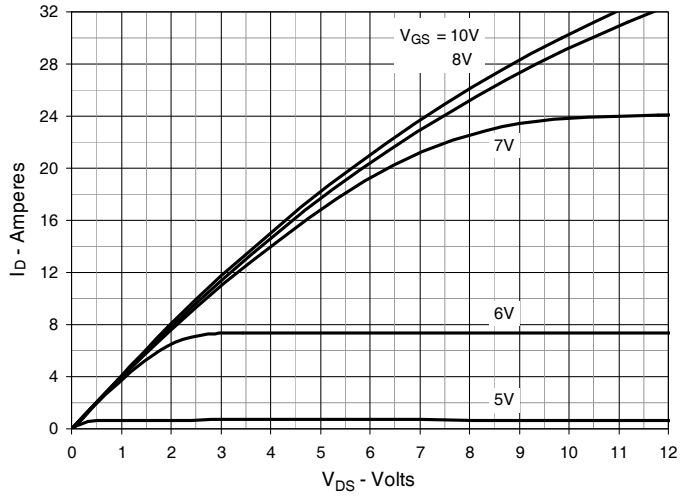


Fig. 4. $R_{DS(on)}$ Normalized to I_D = 16A Value vs. Junction Temperature

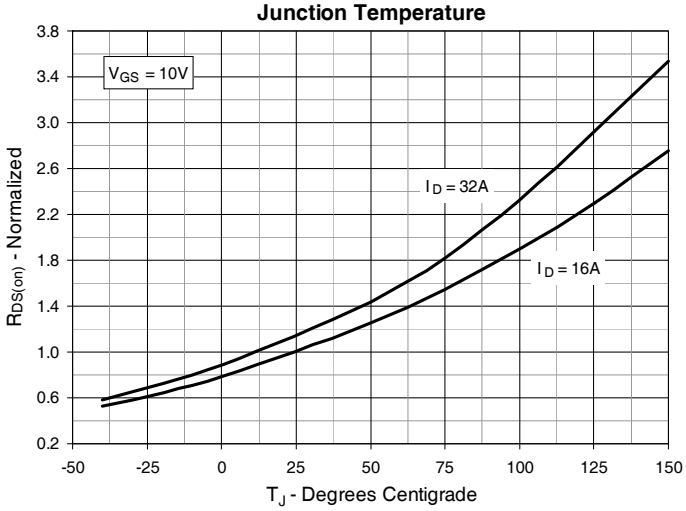


Fig. 5. $R_{DS(on)}$ Normalized to I_D = 16A Value vs. Drain Current

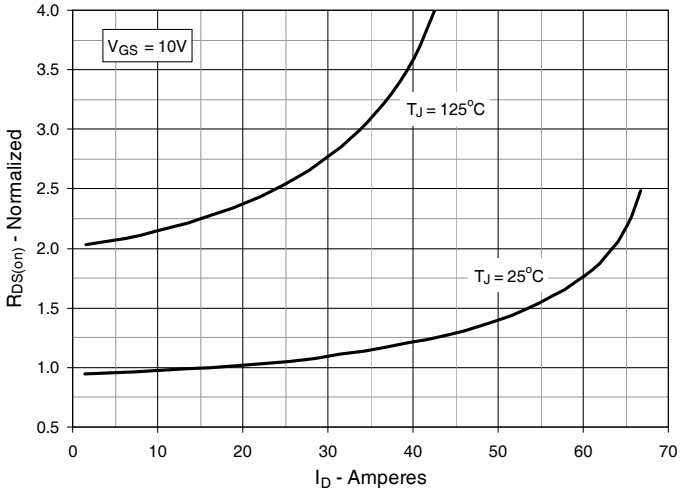
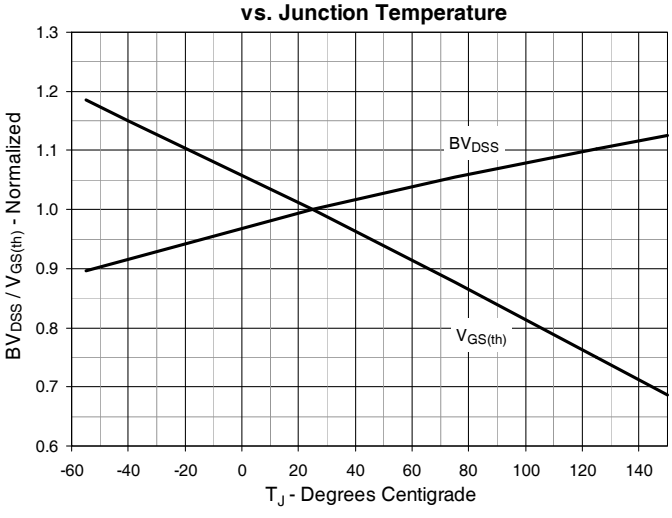


Fig. 6. Normalized Breakdown & Threshold Voltages vs. Junction Temperature



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Fig. 7. Input Admittance

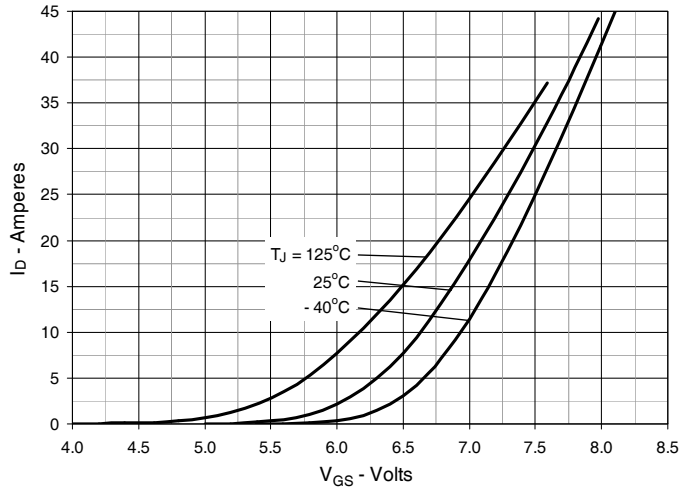


Fig.8. Transconductance

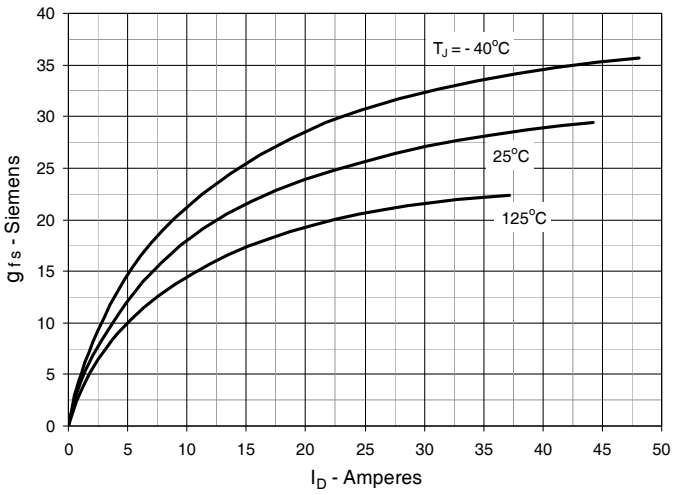


Fig. 9. Forward Voltage Drop of Intrinsic Diode

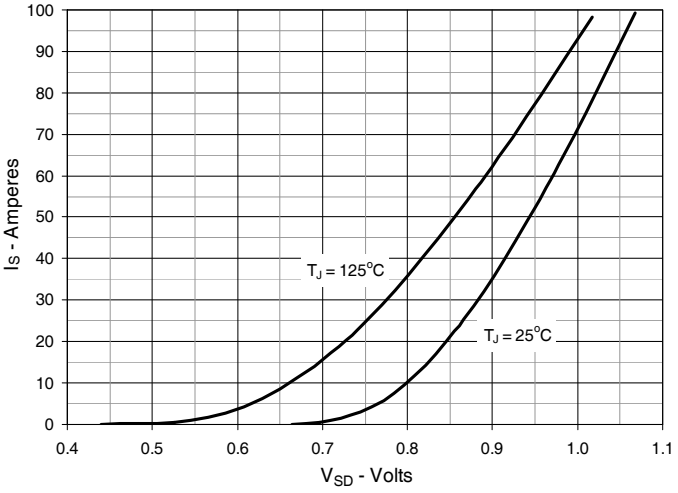


Fig. 10. Gate Charge

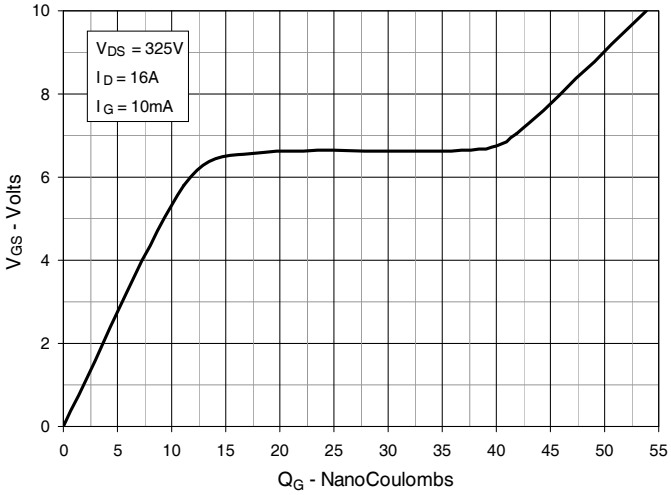


Fig. 11. Capacitance

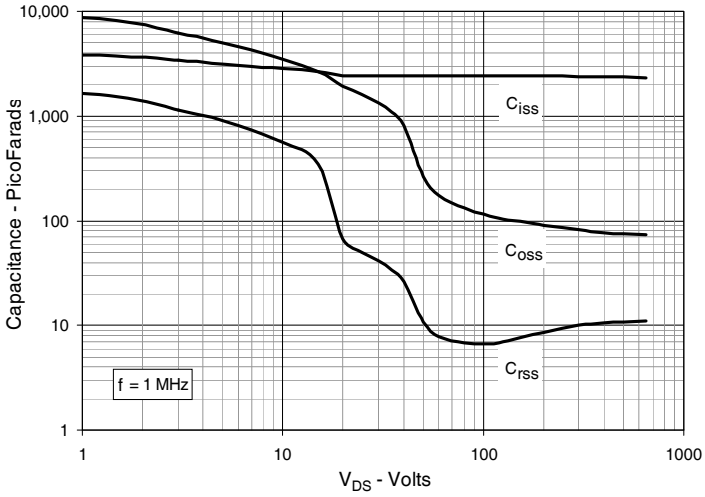
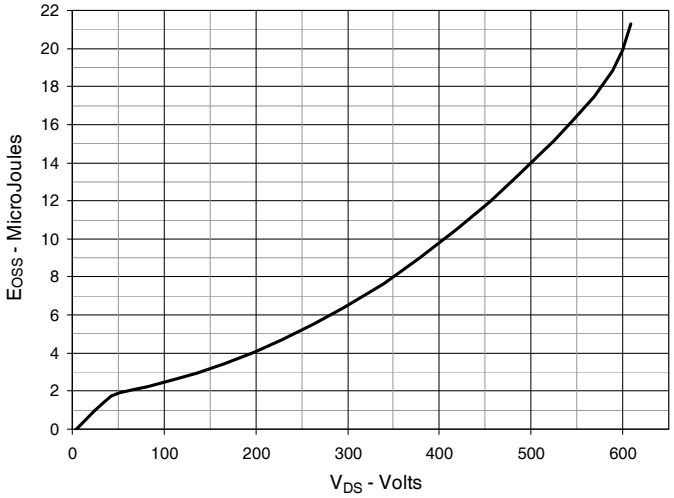


Fig. 12. Output Capacitance Stored Energy



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Fig. 13. Forward-Bias Safe Operating Area

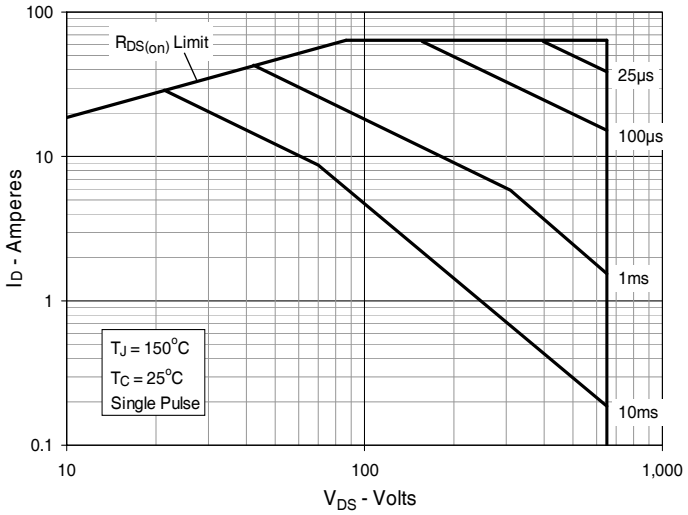
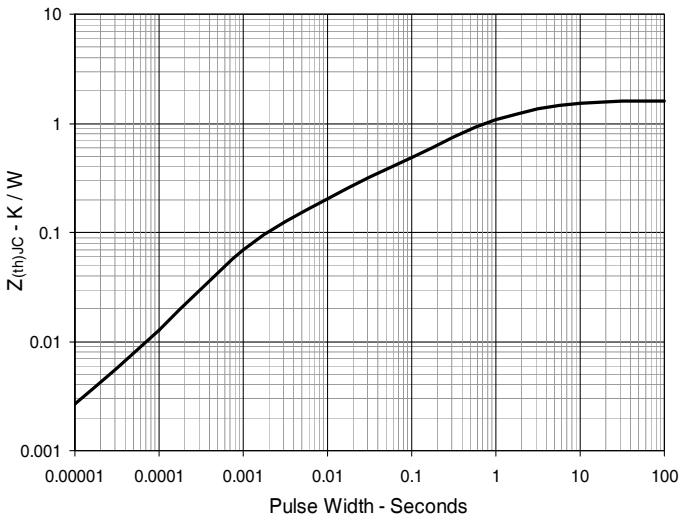


Fig. 14. Maximum Transient Thermal Impedance



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