



Quad LVDS Line Receiver with Flow-Through Pinout and "In-Path" Fail-Safe

General Description

The MAX9173 quad low-voltage differential signaling (LVDS) line receiver is ideal for applications requiring high data rates, low power, and low noise. The MAX9173 is guaranteed to receive data at speeds up to 500Mbps (250MHz) over controlled-impedance media of approximately 100Ω. The transmission media can be printed circuit (PC) board traces or cables.

The MAX9173 accepts four LVDS differential inputs and translates them to LVCMOS/LVTTL outputs. The MAX9173 inputs are high impedance and require an external termination resistor when used in a point-to-point connection.

The device supports a wide common-mode input range of 0.05V to $V_{CC} - 0.05V$, allowing for ground potential differences and common-mode noise between the driver and the receiver. A fail-safe feature sets the output high when the inputs are open, or when the inputs are undriven and shorted or undriven and parallel terminated. The EN and $\overline{EN}$ inputs control the high-impedance outputs. The enables are common to all four receivers. Inputs conform to the ANSI TIA/EIA-644 LVDS standard. The flow-through pinout simplifies board layout and reduces crosstalk by separating the LVDS inputs and LVCMOS/LVTTL outputs. The MAX9173 operates from a single 3.3V supply, and is specified for operation from -40°C to +85°C. Refer to the MAX9121/MAX9122 data sheet for lower jitter quad LVDS receivers with parallel fail-safe. Refer to the MAX9123 data sheet for a quad LVDS line driver with flow-through pinout.

The device is available in 16-pin TSSOP, SO, and space-saving thin QFN packages.

Applications

Digital Copiers
Laser Printers
Cellular Phone Base Stations
Network Switches/Routers
Backplane Interconnect
Clock Distribution
LCD Displays
Telecom Switching Equipment

Pin Configurations and Functional Diagram appear at end of data sheet.

Features

- ◆ Accepts LVDS and LVPECL Inputs
- ◆ Fully Compatible with DS90LV048A
- ◆ Low 1.0mA (max) Disable Supply Current
- ◆ In-Path Fail-Safe Circuitry
- ◆ Flow-Through Pinout
Simplifies PC Board Layout
Reduces Crosstalk
- ◆ Guaranteed 500Mbps Data Rate
- ◆ 400ps Pulse Skew (max)
- ◆ Conforms to ANSI TIA/EIA-644 LVDS Standard
- ◆ High-Impedance LVDS Inputs when Powered-Off
- ◆ Available in Tiny 3mm x 3mm QFN Package

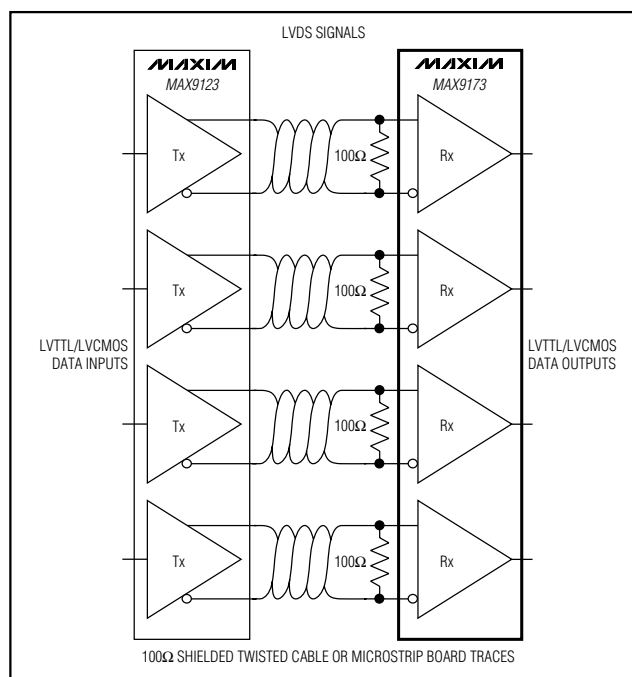
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX9173EUE	-40°C to +85°C	16 TSSOP
MAX9173ESE	-40°C to +85°C	16 SO
MAX9173ETE*	-40°C to +85°C	16 Thin QFN-EP**

*Future product. Contact factory for availability.

**EP = Exposed pad.

Typical Operating Circuit



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ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND-0.3V to +4.0V
 IN₊, IN₋ to GND-0.3V to +4.0V
 OUT₋, EN, $\overline{\text{EN}}$ to GND-0.3V to (V_{CC} + 0.3V)
 Continuous Power Dissipation (T_A = +70°C)
 16-Pin TSSOP (derate 9.4mW/°C above T_A = +70°C) ..755mW
 16-Pin SO (derate 8.7mW/°C above T_A = +70°C)696mW
 16-Pin QFN (derate 14.7mW/°C above T_A = +70°C)..1177mW

Junction Temperature+150°C
 Storage Temperature Range-65°C to +150°C
 ESD Protection (Human Body Model, IN₊, IN₋)±7.0kV
 Lead Temperature (soldering, 10s)+300°C

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.0V to 3.6V, differential input voltage |V_{ID}| = 0.1V to 1.2V, common-mode input voltage V_{CM} = |V_{ID}|/2 to V_{CC} - |V_{ID}|/2, outputs enabled, and T_A = -40°C to +85°C. Typical values are at V_{CC} = 3.3V, V_{CM} = 1.2V, |V_{ID}| = 0.2V, and T_A = +25°C, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LVDS INPUTS (IN₊, IN₋)						
Differential Input High Threshold	V _{TH}			-45	0	mV
Differential Input Low Threshold	V _{TL}		-100	-45		mV
Input Current (Noninverting Input)	I _{IN+}	Figure 1	+0.5	-2.5	-5	μA
Power-Off Input Current (Noninverting Input)	I _{IN+OFF}	V _{IN+} = 0 to 3.6V, V _{IN-} = 0 to 3.6V, V _{CC} = 0 or open (Figure 1)	-0.5	0	+0.5	μA
Input Current (Inverting Input)	I _{IN-}	Figure 1	-0.5	+5.0	+10	μA
Power-Off Input Current (Inverting Input)	I _{IN-OFF}	V _{IN+} = 0 to 3.6V, V _{IN-} = 0 to 3.6V, V _{CC} = 0 or open, Figure 1	-0.5	0	+0.5	μA
LVCMOS/LVTTL OUTPUTS (OUT₋)						
Output High Voltage (Table 1)	V _{OH}	I _{OH} = -4.0mA	2.7	3.2		V
		Open, undriven short, or undriven parallel termination V _{ID} = 0	2.7	3.2		
Output Low Voltage	V _{OL}	I _{OL} = +4.0mA, V _{ID} = -100mV		0.1	0.25	V
Output Short-Circuit Current	I _{OS}	V _{OUT-} = 0 (Note 3)	-45	-77	-120	mA
Output High-Impedance Current	I _{OZ}	Disabled, V _{OUT-} = 0 or V _{CC}	-1		+1	μA
LOGIC INPUTS (EN, $\overline{\text{EN}}$)						
Input High Voltage	V _{IH}		2.0		V _{CC}	V
Input Low Voltage	V _{IL}		0		0.8	V
Input Current	I _{IN}	V _{IN} = high or low	-15		+15	μA
Input Clamp Voltage	V _{CL}	I _{CL} = -18mA		-0.88	-1.5	V
POWER SUPPLY						
Supply Current	I _{CC}	Inputs open		12	15	mA
Disabled Supply Current	I _{CCZ}	Disabled, inputs open		0.56	1.0	mA

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AC ELECTRICAL CHARACTERISTICS

($V_{CC} = 3.0V$ to $3.6V$, $C_L = 15pF$, $|V_{ID}| = 0.2V$, $V_{CM} = 1.2V$, and $T_A = -40^{\circ}C$ to $+85^{\circ}C$. Typical values are at $V_{CC} = 3.3V$ and $T_A = +25^{\circ}C$, unless otherwise noted.) (Notes 4–7)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Propagation Delay High to Low	t_{PHLD}	Figures 2 and 3	1.2	2.01	2.7	ns
Differential Propagation Delay Low to High	t_{PLHD}	Figures 2 and 3	1.2	2.07	2.7	ns
Differential Pulse Skew $ t_{PHLD} - t_{PLHD} $	t_{SKD1}	Figures 2 and 3 (Note 8)		60	400	ps
Differential Channel-to-Channel Skew	t_{SKD2}	Figures 2 and 3 (Note 9)		100	500	ps
Differential Part-to-Part Skew	t_{SKD3}	Figures 2 and 3 (Note 10)			1	ns
	t_{SKD4}	Figures 2 and 3 (Note 11)			1.5	
Rise Time	t_{TLH}	Figures 2 and 3		0.66	1.0	ns
Fall Time	t_{THL}	Figures 2 and 3		0.62	1.0	ns
Disable Time High to Z	t_{PHZ}	$R_L = 2k\Omega$, Figures 4 and 5		9.5	14	ns
Disable Time Low to Z	t_{PLZ}	$R_L = 2k\Omega$, Figures 4 and 5		9.5	14	ns
Enable Time Z to High	t_{PZH}	$R_L = 2k\Omega$, Figures 4 and 5		3	14	ns
Enable Time Z to Low	t_{PZL}	$R_L = 2k\Omega$, Figures 4 and 5		3	14	ns
Maximum Operating Frequency	f_{MAX}	All channels switching (Note 12)	250			MHz

Note 1: Current into a pin is defined as positive. Current out of a pin is defined as negative. All voltages are referenced to ground except V_{TH} , V_{TL} , and V_{ID} .

Note 2: Devices are 100% production tested at $T_A = +25^{\circ}C$ and are guaranteed by design for $T_A = -40^{\circ}C$ to $+85^{\circ}C$ as specified.

Note 3: Short only one output at a time. Do not exceed the absolute maximum junction temperature specification.

Note 4: AC parameters are guaranteed by design and characterization.

Note 5: C_L includes scope probe and test jig capacitance.

Note 6: Pulse generator output conditions: $t_R = t_F < 1ns$ (0% to 100%), frequency = 250MHz, 50% duty cycle, $V_{OH} = 1.3V$, $V_{OL} = 1.1V$. High-impedance delay pulse generator output conditions: $t_R = t_F < 3ns$ (0% to 100%), frequency = 1MHz, 50% duty cycle, $V_{OH} = 3V$ and $V_{OL} = 0$.

Note 7: Propagation delay and differential pulse skew decrease when $|V_{ID}|$ is increased from 200mV to 400mV. Skew specifications apply for $200mV \leq |V_{ID}| \leq 1.2V$ over the common-mode range $V_{CM} = |V_{ID}|/2$ to $V_{CC} - |V_{ID}|/2$.

Note 8: t_{SKD1} is the magnitude of the difference of differential propagation delays in a channel. $t_{SKD1} = |t_{PHLD} - t_{PLHD}|$.

Note 9: t_{SKD2} is the magnitude of the difference of the t_{PLHD} or t_{PHLD} of one channel and the t_{PLHD} or t_{PHLD} of any other channel on the same part.

Note 10: t_{SKD3} is the magnitude of the difference of any differential propagation delays between parts operating over rated conditions at the same V_{CC} and within $5^{\circ}C$ of each other.

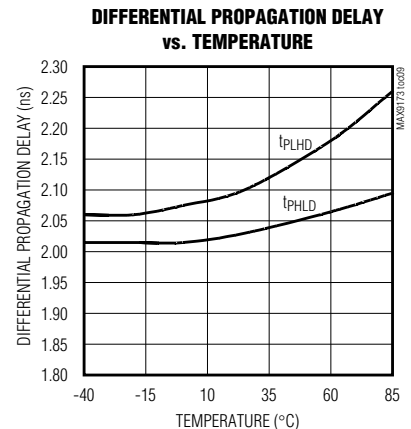
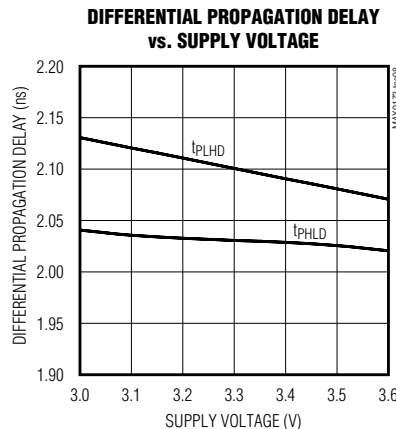
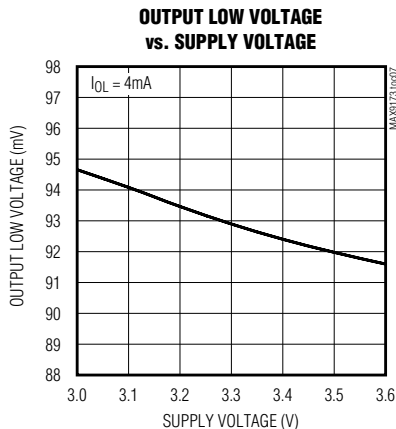
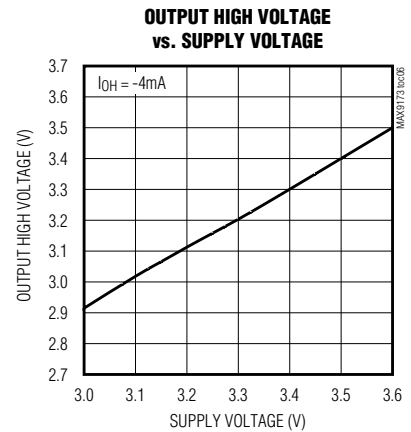
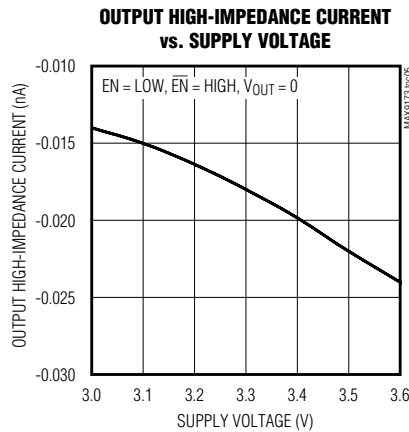
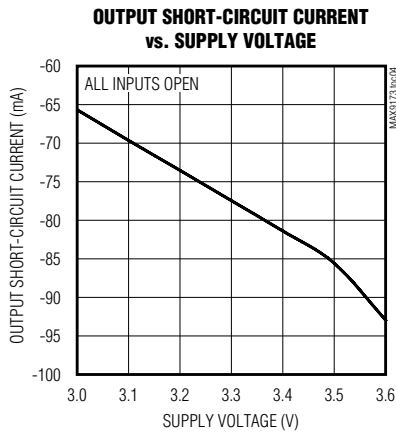
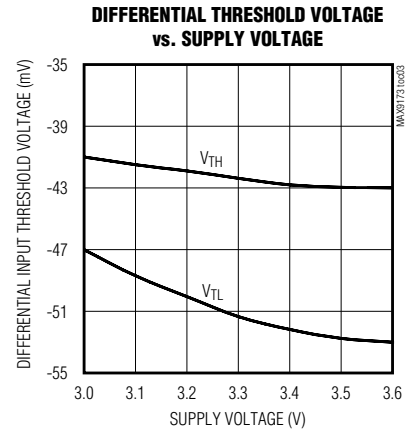
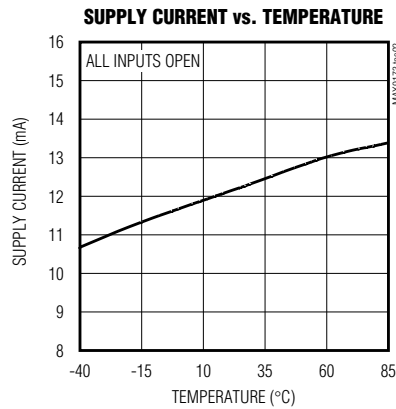
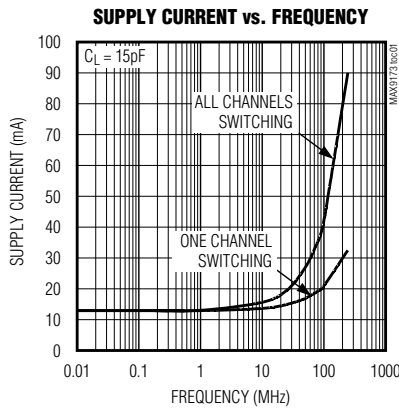
Note 11: t_{SKD4} is the magnitude of the difference of any differential propagation delays between parts operating over rated conditions.

Note 12: 60% to 40% duty cycle, $V_{OL} = 0.4V$ (max), $V_{OH} = 2.7V$ (min), load = 15pF.

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Typical Operating Characteristics

($V_{CC} = 3.3V$, $V_{CM} = 1.2V$, $|V_{ID}| = 0.2V$, $f = 100MHz$, input rise and fall time = 1ns (0% to 100%), $C_L = 15pF$, and $T_A = +25^\circ C$, unless otherwise noted.) (Figures 2 and 3)

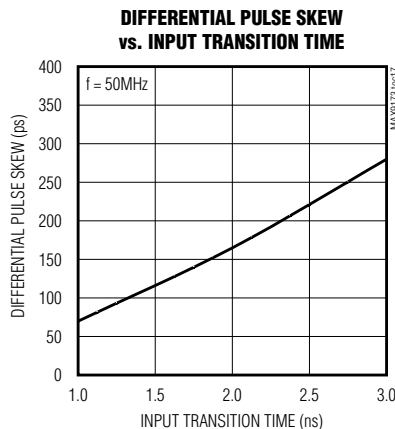
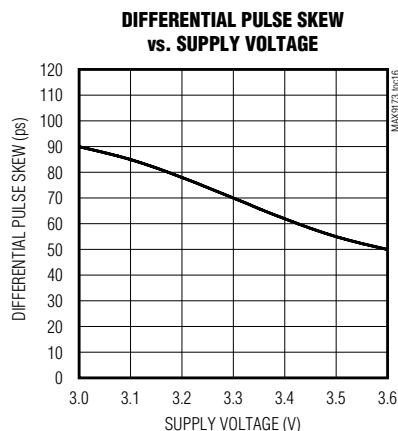
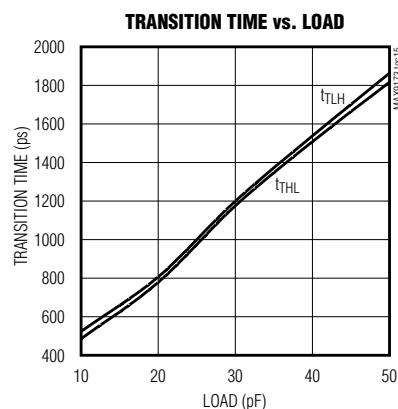
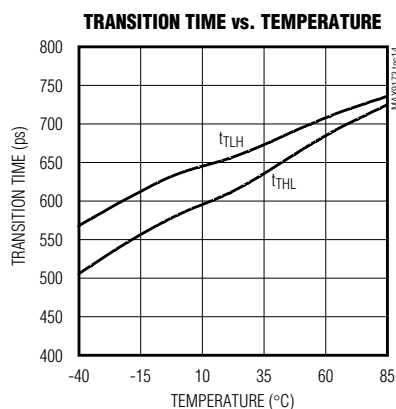
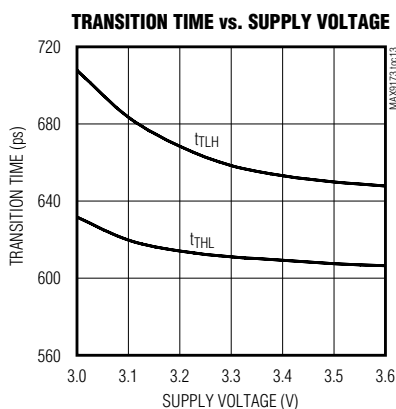
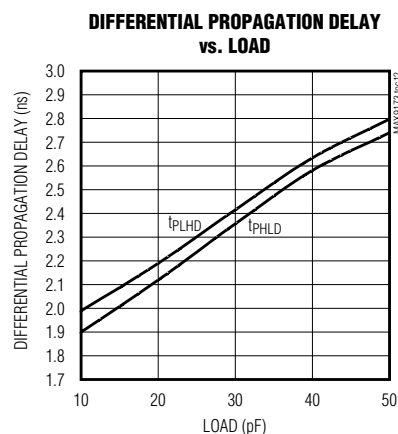
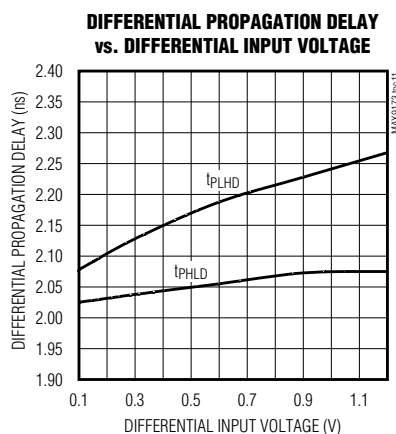
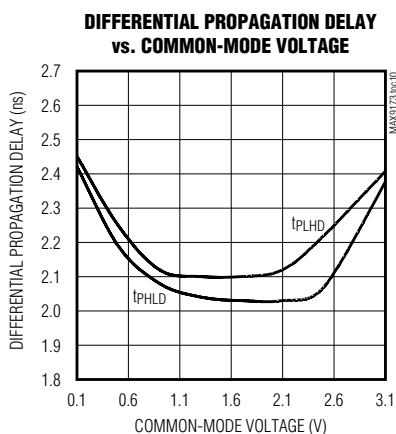


Quad LVDS Line Receiver with Flow-Through Pinout and “In-Path” Fail-Safe

Typical Operating Characteristics (continued)

($V_{CC} = 3.3V$, $V_{CM} = 1.2V$, $|V_{ID}| = 0.2V$, $f = 100MHz$, input rise and fall time = 1ns (0% to 100%), $C_L = 15pF$, and $T_A = +25^\circ C$, unless otherwise noted.) (Figures 2 and 3)

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Pin Description

PIN		NAME	FUNCTION
TSSOP/SO	QFN		
1	15	IN1-	Inverting Differential Receiver Input for Receiver 1
2	16	IN1+	Noninverting Differential Receiver Input for Receiver 1
3	1	IN2+	Noninverting Differential Receiver Input for Receiver 2
4	2	IN2-	Inverting Differential Receiver Input for Receiver 2
5	3	IN3-	Inverting Differential Receiver Input for Receiver 3
6	4	IN3+	Noninverting Differential Receiver Input for Receiver 3
7	5	IN4+	Noninverting Differential Receiver Input for Receiver 4
8	6	IN4-	Inverting Differential Receiver Input for Receiver 4
9, 16	7, 14	$\overline{\text{EN}}$, EN	Receiver Enable Inputs. When EN = high and $\overline{\text{EN}}$ = low or open, the outputs are active. For other combinations of EN and $\overline{\text{EN}}$, the outputs are disabled and in high impedance.
10	8	OUT4	LVC MOS/LVTTL Receiver Output for Receiver 4
11	9	OUT3	LVC MOS/LVTTL Receiver Output for Receiver 3
12	10	GND	Ground
13	11	VCC	Power-Supply Input. Bypass VCC to GND with 0.1 μ F and 0.001 μ F ceramic capacitors. Place the smaller value cap as close to the pin as possible.
14	12	OUT2	LVC MOS/LVTTL Receiver Output for Receiver 2
15	13	OUT1	LVC MOS/LVTTL Receiver Output for Receiver 1
—	Exposed Pad	EP	Exposed Pad. Solder to ground plane for proper heat dissipation.

Table 1. Input/Output Function Table

ENABLES		INPUTS	OUTPUT
EN	$\overline{\text{EN}}$	(IN ₊) - (IN ₋)	OUT ₋
H	L or open	V _{ID} ≥ 0	H
		V _{ID} ≤ -100mV	L
		Open, undriven short, or undriven parallel termination	H
All other combinations of ENABLE pins		Don't care	Z

Detailed Description

LVDS is a signaling method intended for point-to-point communication over a controlled-impedance medium as defined by the ANSI TIA/EIA-644 and IEEE 1596.3 standards. LVDS uses a lower voltage swing than other common communication standards, achieving higher data rates with reduced power consumption while reducing EMI and system susceptibility to noise.

The MAX9173 is a 500Mbps, four-channel LVDS receiver intended for high-speed, point-to-point, low-power applications. Each channel accepts an LVDS input and

translates it to an LVTTL/LVC MOS output. The receiver is specified to detect differential signals as low as 100mV and as high as 1.2V within an input voltage range of 0 to VCC. The 250mV to 400mV differential output of an LVDS driver is nominally centered around a 1.2V offset. This offset, coupled with the receiver's 0 to VCC input voltage range, allows more than $\pm 1\text{V}$ shift in the signal (as seen by the receiver). This allows for a difference in ground references of the transmitter and the receiver, the common-mode effects of coupled noise, or both.

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Fail-Safe

The MAX9173 fail-safe drives the receiver output high when the differential input is:

- Open
- Undriven and shorted
- Undriven and terminated

Without fail-safe, differential noise at the input may switch the receiver and appear as data to the receiving system. An open input occurs when a cable and termination are disconnected. An undriven, terminated input occurs when a cable is disconnected with the termination still connected across the receiver inputs or when the driver of a receiver is in high impedance. An undriven, shorted input can occur due to a shorted cable.

“In-Path” vs. “Parallel” Fail-Safe

The MAX9173 has in-path fail-safe that is compatible with in-path fail-safe receivers, such as the DS90LV048A. Refer to the MAX9121/MAX9122 data sheet for pin-compatible receivers with parallel fail-safe and lower jitter. Refer to the MAX9130 data sheet for a single LVDS receiver with parallel fail-safe in an SC70 package.

The MAX9173 with in-path fail-safe is designed with a +45mV input offset voltage, a 2.5 μ A current source between V_{CC} and the noninverting input, and a 5 μ A current sink between the inverting input and ground (Figure 1). If the differential input is open, the 2.5 μ A current source pulls the input to approximately V_{CC} - 0.8V and the 5 μ A current sink pulls the inverting input to ground, which drives the receiver output high. If the differential input is shorted or terminated with a typical value termination resistor, the +45mV offset drives the receiver output high. If the input is terminated and floating, the receiver output is driven high by the +45mV offset, and the 2:1 current sink to current source ratio (5 μ A:2.5 μ A) pulls the inputs to ground. This can be an advantage when switching between drivers on a multi-point bus because the change in common-mode voltage from ground to the typical driver offset voltage of 1.2V is not as much as the change from V_{CC} to 1.2V (parallel fail-safe pulls the bus to V_{CC}).

ESD Protection

ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The receiver inputs of the MAX9173 have ± 7.0 kV of protection against static electricity (per Human Body Model).

Figure 6a shows the Human Body Model, and Figure 6b shows the current waveform it generates when discharged into a low-impedance load. This model con-

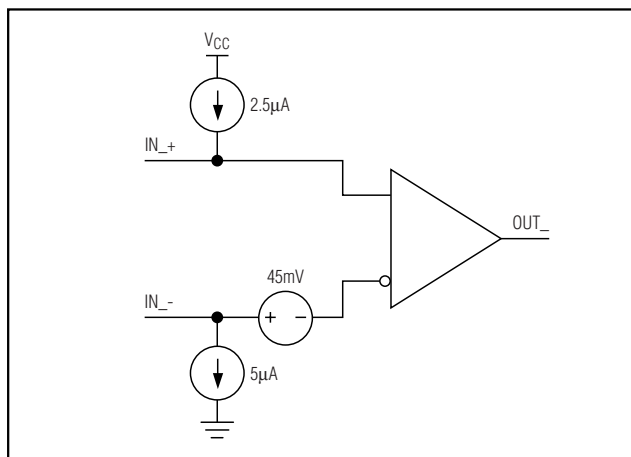


Figure 1. Input with Fail-Safe Network

sists of a 100pF capacitor charged to the ESD test voltage, which is then discharged into the test device through a 1.5k Ω resistor.

Applications Information

Differential Traces

Input trace characteristics affect the performance of the MAX9173. Use controlled-impedance board traces. For point-to-point connections, match the receiver input termination resistor to the differential characteristic impedance of the board traces.

Eliminate reflections and ensure that noise couples as common mode by running the differential traces close together. Reduce skew by matching the electrical length of the traces. Excessive skew can result in a degradation of magnetic field cancellation.

Each channel's differential signals should be routed close to each other to cancel their external magnetic field. Maintain a constant distance between the differential traces to avoid discontinuities in differential impedance. Minimize the number of vias to further prevent impedance discontinuities.

Cables and Connectors

LVDS transmission media typically have controlled differential impedance of 100 Ω . Use cables and connectors that have matched differential impedance to minimize impedance discontinuities.

Avoid the use of unbalanced cables such as coaxial cable. Balanced cables such as twisted pair offer superior signal quality and tend to generate less EMI due to magnetic field canceling effects. Balanced cables pick up noise as common mode, which is rejected by the LVDS receiver.

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Termination

The MAX9173 requires an external termination resistor. The termination resistor should match the differential impedance of the transmission line. Termination resistance values may range between 90Ω to 132Ω , depending on the characteristic impedance of the transmission medium.

When using the MAX9173, minimize the distance between the input termination resistors and the MAX9173 receiver inputs. Use 1% surface-mount resistors.

Board Layout

In general, separate the LVDS inputs from single-ended outputs to reduce crosstalk. Take special care when routing traces with the QFN package. Ideally, the LVDS

inputs should be separated by 180° from the LVTTTL/LVCMOS outputs to reduce crosstalk.

For LVDS applications, a four-layer PC board that provides separate layers of power, ground, LVDS inputs, and output signals is recommended. When using the QFN package, solder the exposed pad (EP) to the ground plane using an array of vias for proper heat dissipation.

Chip Information

TRANSISTOR COUNT: 1462

PROCESS: CMOS

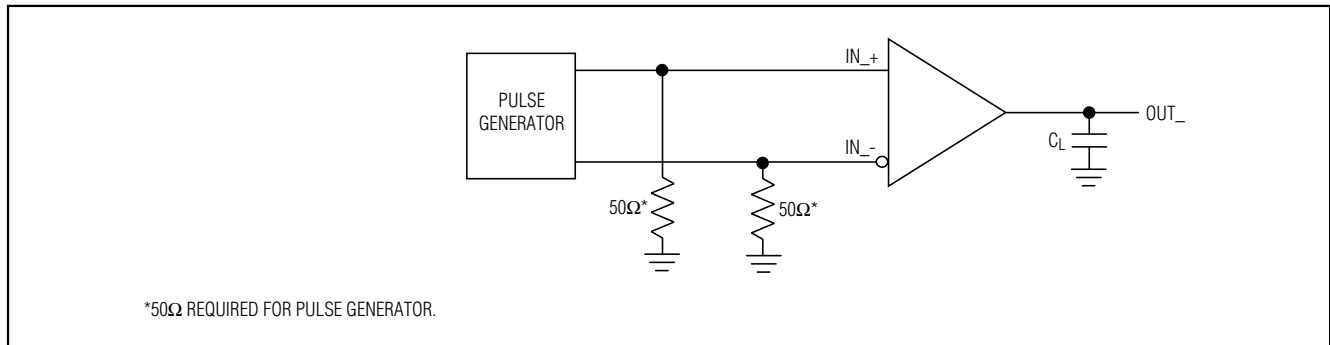


Figure 2. Propagation Delay and Transition Time Test Circuit

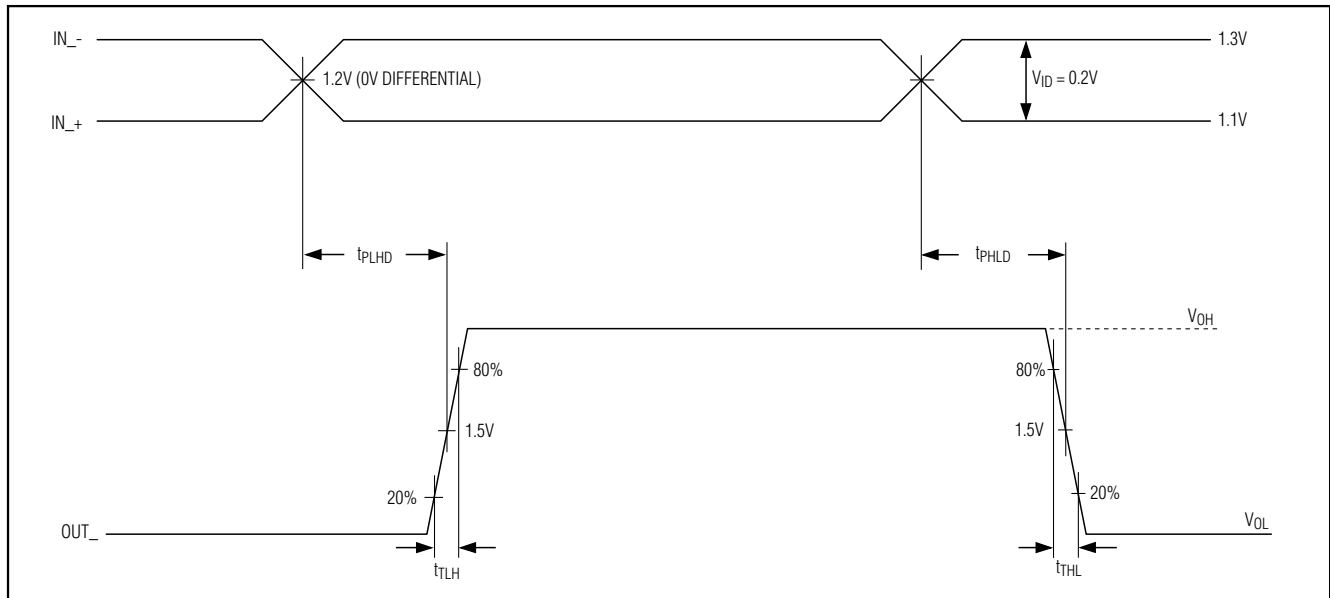


Figure 3. Propagation Delay and Transition Time Test Waveforms

Quad LVDS Line Receiver with Flow-Through Pinout and “In-Path” Fail-Safe

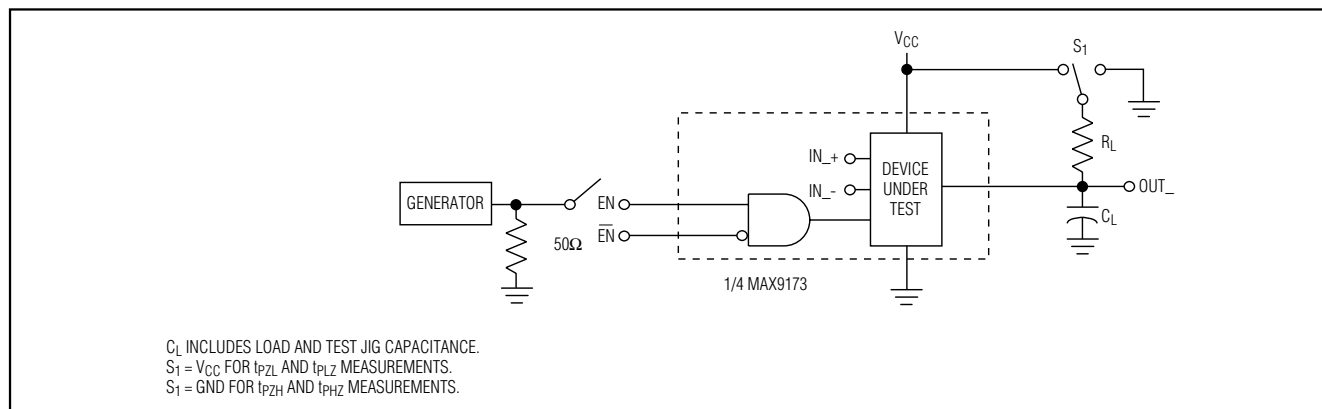


Figure 4. High-Impedance Delay Test Circuit

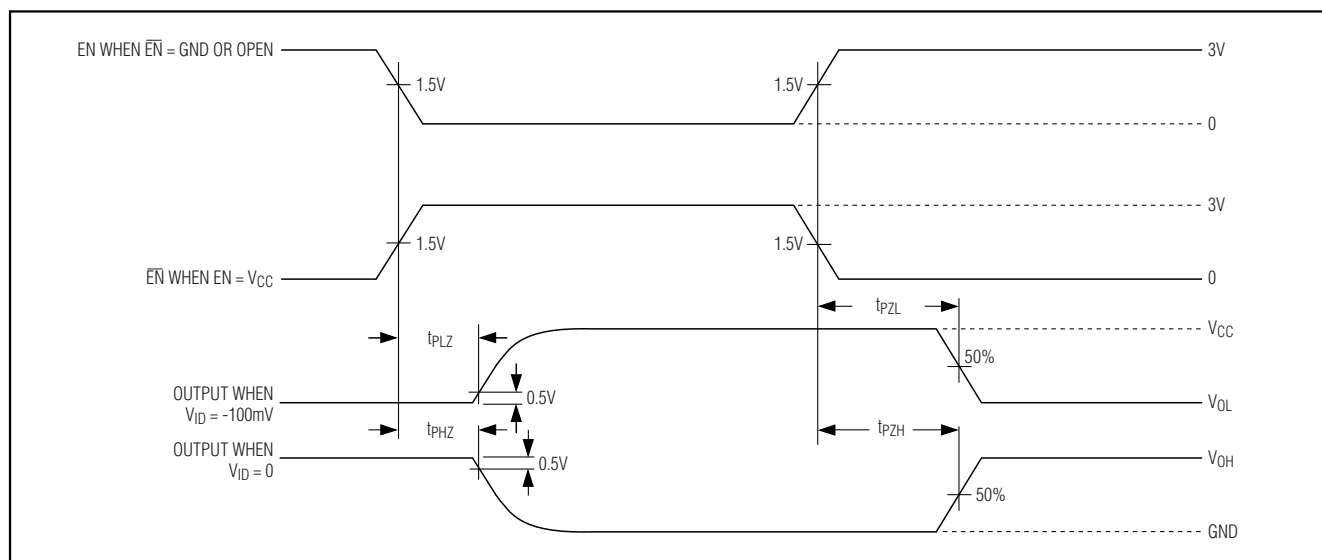


Figure 5. High-Impedance Delay Waveforms

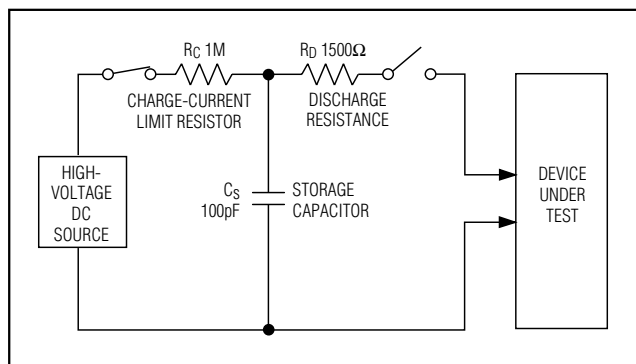


Figure 6a. Human Body ESD Test Modules

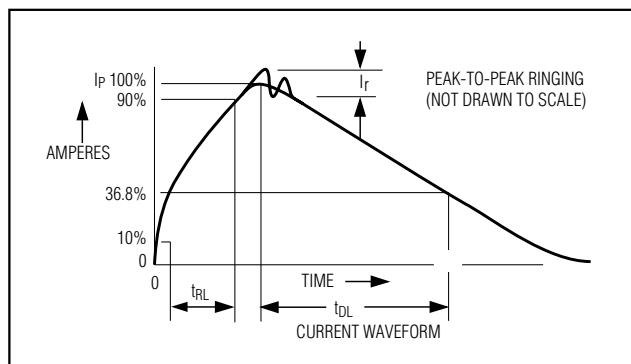
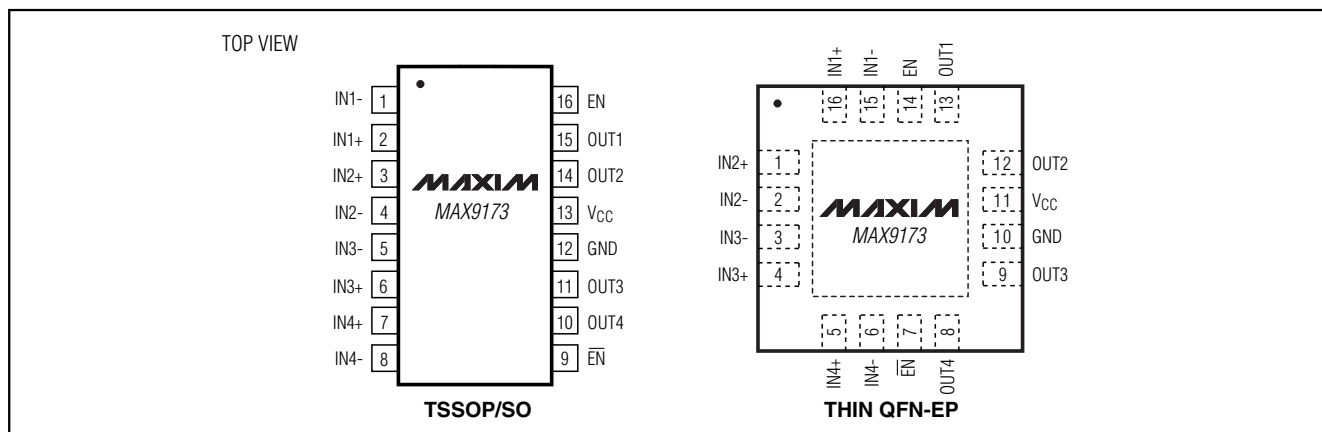


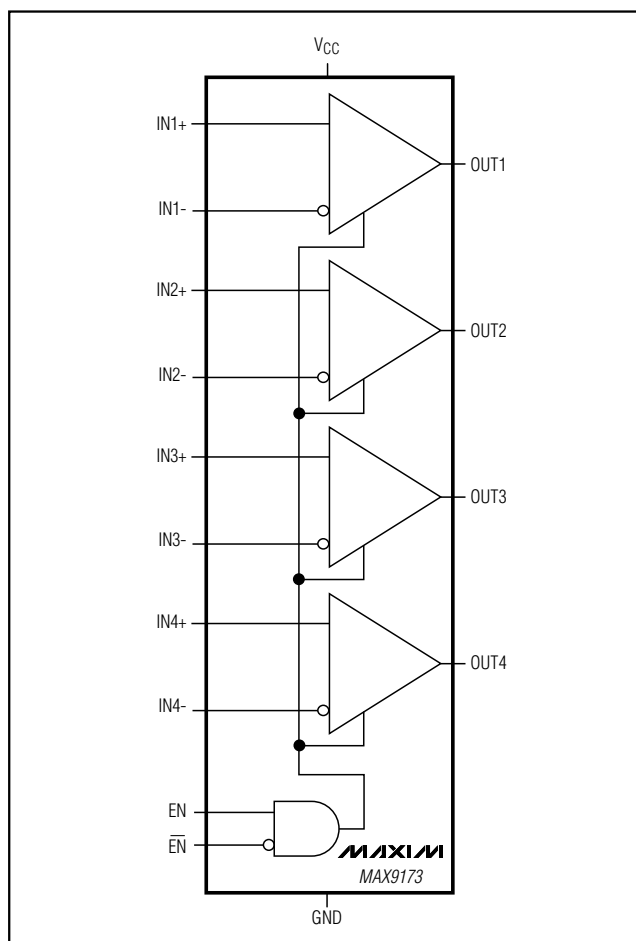
Figure 6b. Human Body Current Waveform

Quad LVDS Line Receiver with Flow-Through Pinout and “In-Path” Fail-Safe

Pin Configurations



Functional Diagram



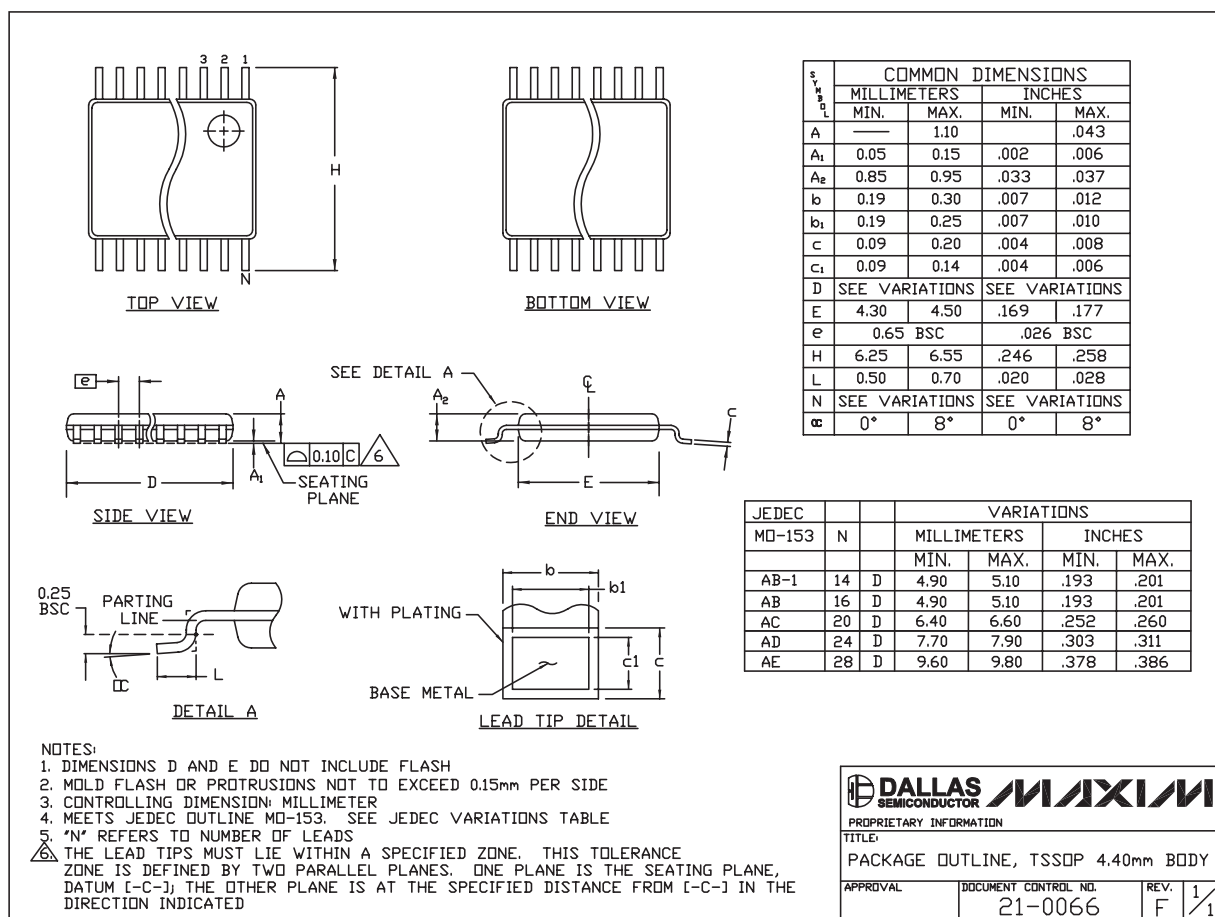
Quad LVDS Line Receiver with Flow-Through Pinout and "In-Path" Fail-Safe

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)

MAX9173

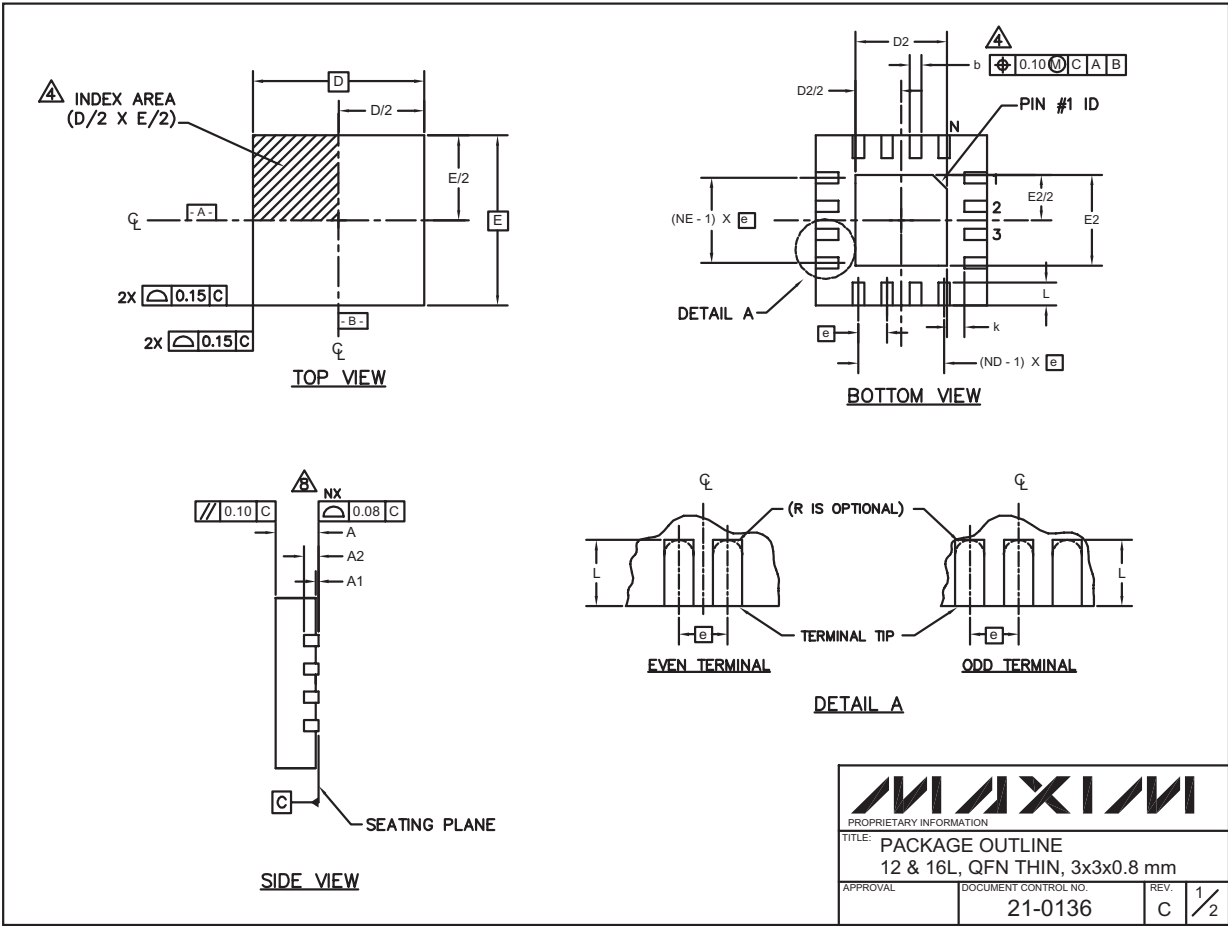
TSSOP4, 4.0mm, EPS



Quad LVDS Line Receiver with Flow-Through Pinout and “In-Path” Fail-Safe

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)



Quad LVDS Line Receiver with Flow-Through Pinout and “In-Path” Fail-Safe

Package Information (continued)

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MAX9173

PKG REF.	12L 3x3			16L 3x3		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80
b	0.20	0.25	0.30	0.20	0.25	0.30
D	2.90	3.00	3.10	2.90	3.00	3.10
E	2.90	3.00	3.10	2.90	3.00	3.10
e	0.50 BSC.			0.50 BSC.		
L	0.45	0.55	0.65	0.30	0.40	0.50
N	12			16		
ND	3			4		
NE	3			4		
A1	0	0.02	0.05	0	0.02	0.05
A2	0.20 REF			0.20 REF		
k	0.25	-	-	0.25	-	-

EXPOSED PAD VARIATIONS								
PKG CODES	D2			E2			PIN ID	JEDEC
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.		
T1233-1	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1
T1633-1	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2
T1633F-3	0.65	0.80	0.95	0.65	0.80	0.95	0.225 x 45°	-

NOTES:

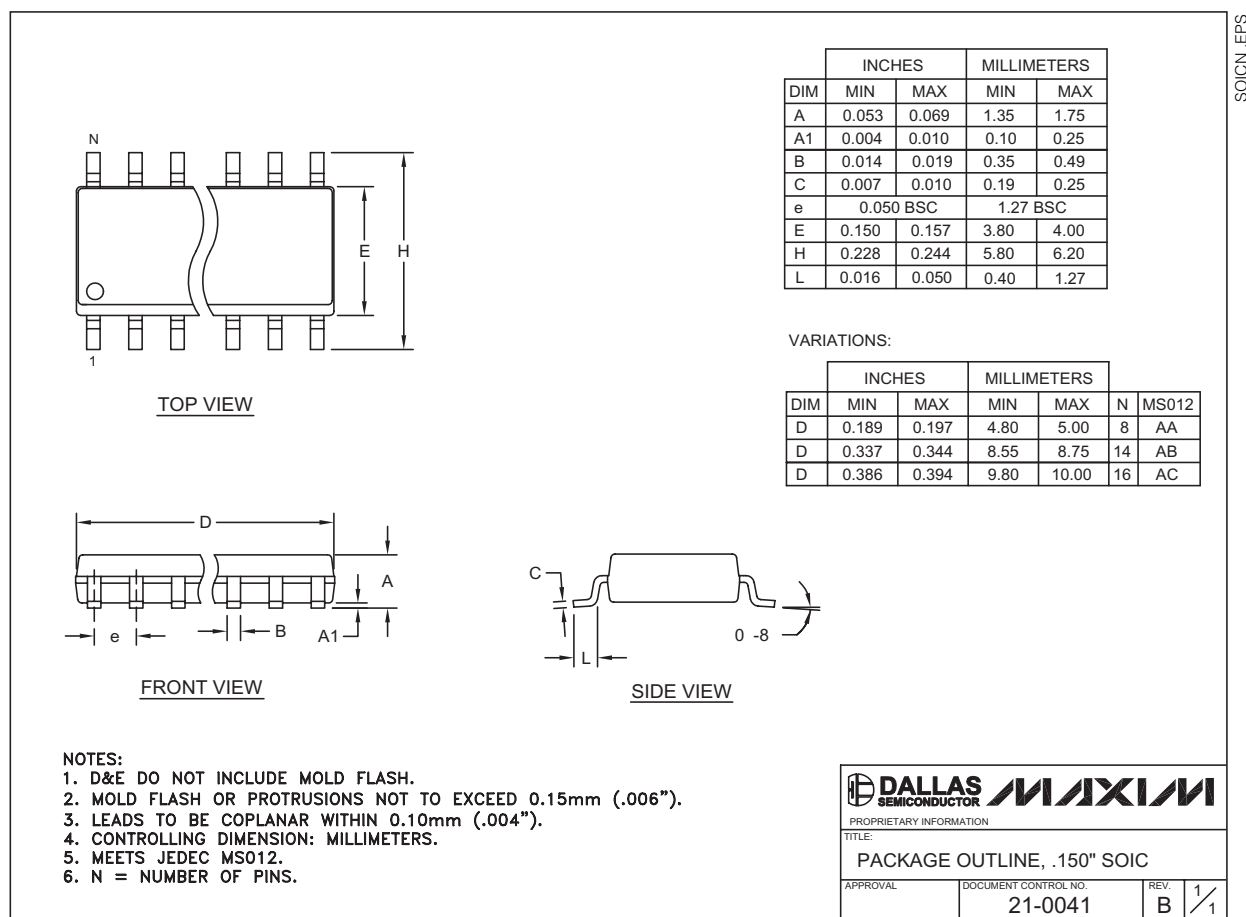
1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.20 mm AND 0.25 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220 REVISION C.

		
PROPRIETARY INFORMATION		
TITLE: PACKAGE OUTLINE		
12 & 16L, QFN THIN, 3x3x0.8 mm		
APPROVAL	DOCUMENT CONTROL NO.	REV.
	21-0136	C 2/2

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Package Information (continued)

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