

AN-1897 LMH6629 LLP-8 Amplifier Evaluation Board

1 General Description

The LMH6629 evaluation board is designed to aid in the characterization of Texas Instruments LMH6629 Low Noise Operational Amplifier.

Use the evaluation board as a guide for high frequency layout and as a tool to aid in device testing and characterization.

2 Basic Operation

The LMH6629 is a voltage feedback operational amplifier with differential inputs and a single output. The LMH6629 Evaluation board will support both inverting and non-inverting configurations. For component locations refer to the schematic in [Figure 1](#).

The evaluation board uses end mounted SMA connectors. On the IN+ input, resistor RIN provides input termination. When using the evaluation board for non-inverting applications, load only resistor RGA. The resistors RGB and RT are for use in the inverting configuration. When using this board for inverting applications, do not load RGA; instead load RGB and an appropriate value of RT.

The LMH6629 amplifier has two digital inputs: One is an enable ($\overline{\text{PD}}$) pin and the other is a compensation switching (COMP) pin. To facilitate high speed testing of device response times, both of these pins have provisions for SMA connectors (EN and COMP) and 50 Ω termination resistors (R1 and RC2). Normally the amplifier will be used with the enable pin disconnected. Left unconnected, the $\overline{\text{PD}}$ pin defaults to a logic 1 state in which the amplifier is enabled. To disable the amplifier and place it into a low power mode, set this pin to the negative supply voltage (V^-). For placing the LMH6629 in disable mode, close the SW1–A switch on the board.

The LMH6629 offers two settings for its internal compensation. For maximum stability and use at gains as low as 4V/V, open the SW1–B switch on the board to float the COMP pin (COMP pin floats to a logic 0 state). To operate the LMH6629 at closed loop gains of +10V/V or higher, close the SW1–B on the board to bring COMP pin to the positive supply voltage (V^+).

To use an external signal generator to drive the $\overline{\text{PD}}$ pin, remove resistor R5 and place a 50 Ω termination resistor at the R1 position (R1 should otherwise be left empty). Likewise, to drive the COMP pin externally, remove resistor RC1 and place a 50 Ω resistor in the RC2 position (RC2 should otherwise be left empty).

This board is configured to drive 50 Ω test equipment and is shipped with a 49.9 Ω ROUT resistor. The board spaces labeled R3 and R2 can be loaded with any desired load components including inductors or capacitors to simulate reactive loads or to accomplish impedance matching. Normal operation with this configuration ($A_v=+10\text{V/V}$) requires SW1–A to be open (enabled operation) and SW1–B to be closed to accommodate this closed loop gain.

If single supply operation is desired, load a low impedance metallic short in the R10 position. When using a single supply it is important to pay attention to DC bias voltages.

3 Bill of Materials

The bill of material (BOM) of the board, as shipped from Texas Instruments, is listed [Table 1](#).

Table 1. Bill of Materials

Reference Designator	Description	Value	Tolerance (%)	Qty
V ⁺ , V ⁻ , GND	Test Point	Digikey 5002K-ND	-	3
C1, C9, C10	0.01uF, 50WV ceramic capacitor, size 0603	0.01 μ F	10	3
C2, C11	0.1uF, 16WV ceramic capacitor, size 0603	0.1 μ F	10	2
C3, C12	Tantalum Chip capacitor, size 3528	10 μ F	10	2
IN ⁺ , IN ⁻ , OUT ⁺	SMA End Launch Jack Receptacle - Round Contact	Digikey J502-ND	-	3
R5, RC1	Thick film chip resistor, size 0603	0	1	2
RIN, ROUT, RT	Thick film chip resistor, size 0603	49.9	1	3
RF	Thick film chip resistor, size 0402	249	1	1
RGA	Thick film chip resistor, size 0603	27.4	1	1
SW1	2 Position Vertical Full Profile Dip Switch	Digikey CKN3001-ND	-	1
U1	IC	LMH6629	-	1

4 Schematic

This board consists of four layers. All four layers are detailed in [Figure 2](#) through [Figure 5](#).

POWER SUPPLY CONNECTIONS

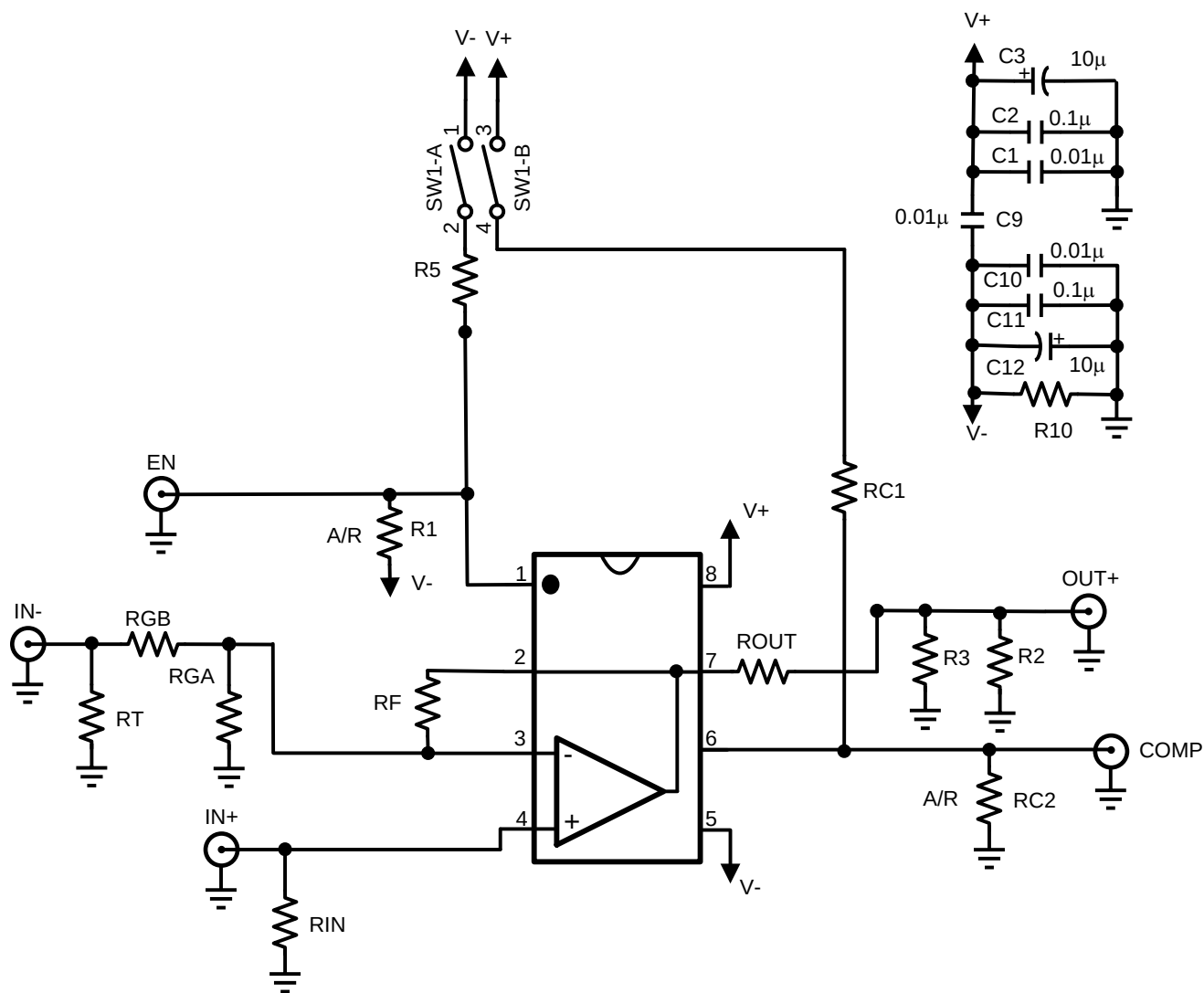


Figure 1. LMH6629 Evaluation Board Schematic

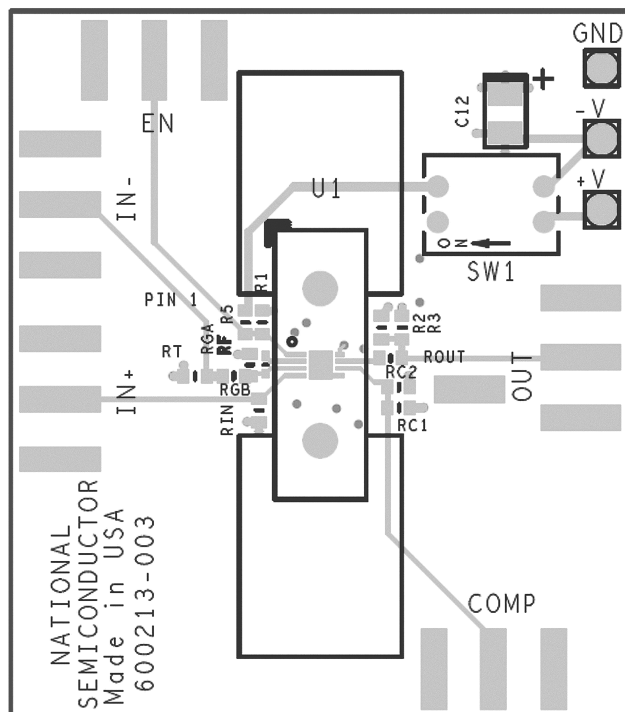


Figure 2. Evaluation Board Top Layer

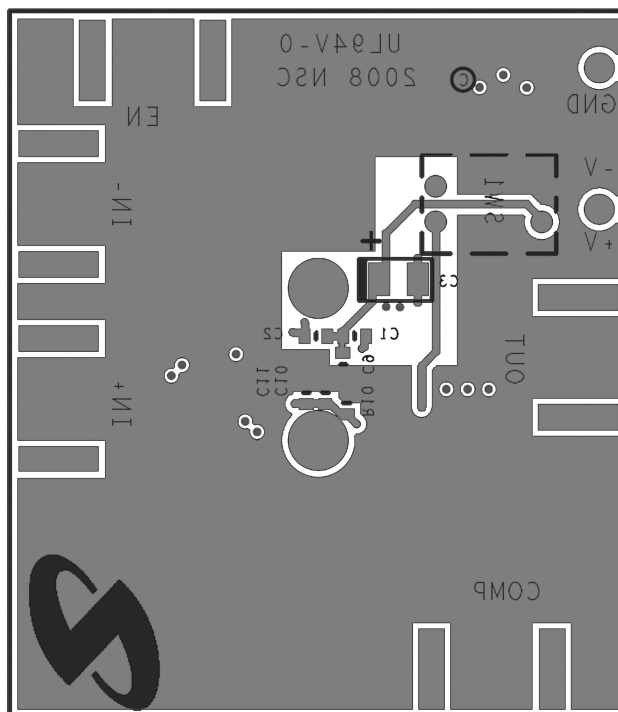


Figure 3. Evaluation Board Bottom Layer

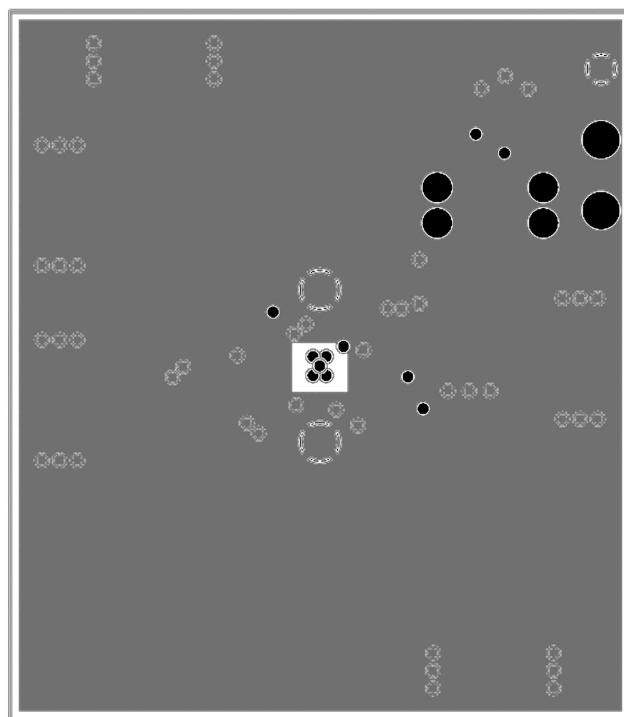


Figure 4. Evaluation Board Layer 2

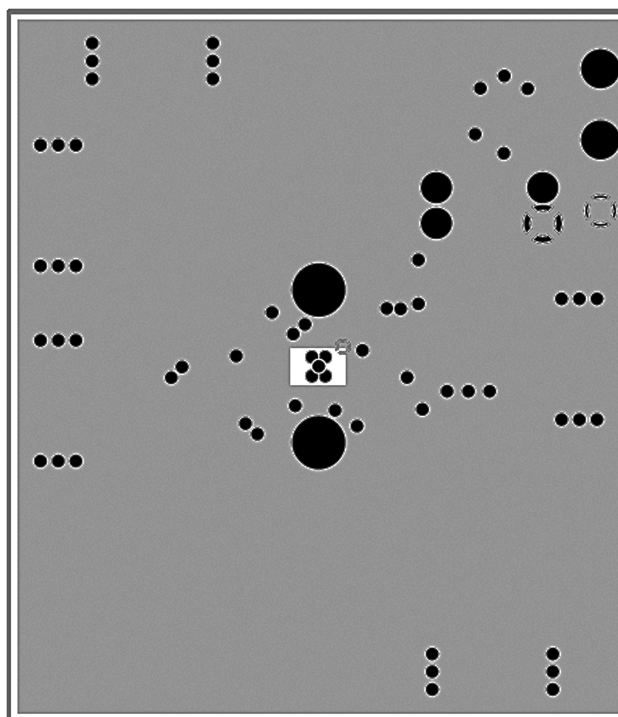


Figure 5. Evaluation Board Layer 3

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