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FAIRCHILD SEMICONDUCTOR®

August 2009

FDMF6704 - XS™ DrMOS

The Xtra Small, High Performance, High Frequency DrMOS Module

Benefits

- Ultra compact size - 6 mm x 6 mm MLP, 44 % space saving compared to conventional MLP 8 mm x 8 mm DrMOS packages.
- Fully optimized system efficiency.
- Clean voltage waveforms with reduced ringing.
- High frequency operation.
- Compatible with a wide variety of PWM controllers in the market.

Features

- Ultra- compact thermally enhanced 6 mm x 6 mm MLP package 84 % smaller than conventional discrete solutions.
- Synchronous driver plus FET multichip module.
- High current handling of 35 A.
- Over 93 % peak efficiency.
- Tri-State PWM input.
- Fairchild's PowerTrench® 5 technology MOSFETs for clean voltage waveforms and reduced ringing.
- Optimized for high switching frequencies of up to 1 MHz.
- Skip mode SMOD [low side gate turn off] input.
- Fairchild SyncFET™ [integrated Schottky diode] technology in the low side MOSFET.
- Integrated bootstrap Schottky diode.
- Adaptive gate drive timing for shoot-through protection.
- Driver output disable function [DISB# pin].
- Undervoltage lockout (UVLO).
- Fairchild Green Packaging and RoHS compliant. Low profile SMD package.

General Description

The XS™ DrMOS family is Fairchild's next-generation fully-optimized, ultra-compact, integrated MOSFET plus driver power stage solutions for high current, high frequency synchronous buck DC-DC applications. The FDMF6704 XS™ DrMOS integrates a driver IC, two power MOSFETs and a bootstrap Schottky diode into a thermally enhanced, ultra compact 6 mm x 6 mm MLP package. With an integrated approach, the complete switching power stage is optimized with regards to driver and MOSFET dynamic performance, system inductance and $R_{DS(ON)}$. This greatly reduces the package parasitics and layout challenges associated with conventional discrete solutions. XS™ DrMOS uses Fairchild's high performance PowerTrench™ 5 MOSFET technology, which dramatically reduces ringing in synchronous buck converter applications. PowerTrench™ 5 can eliminate the need for a snubber circuit in buck converter applications. The driver IC incorporates advanced features such as SMOD for improved light load efficiency and a Tri-State PWM input for compatibility with a wide range of PWM controllers. A 5 V gate drive and an improved PCB interface optimized for a maximum low side FET exposed pad area, ensure higher performance. This product is compatible with the new Intel 6 mm x 6 mm DrMOS specification.

Applications

- Compact blade servers V-core, non V-core and VTT DC-DC converters.
- Desktop computers V-core, non V-core and VTT DC-DC converters.
- Workstations V-core, non V-core and VTT DC-DC converters.
- Gaming Motherboards V-core, non V-core and VTT DC-DC converters.
- Gaming consoles.
- High-current DC-DC Point of Load (POL) converters.
- Networking and telecom microprocessor voltage regulators.

Power Train Application Circuit

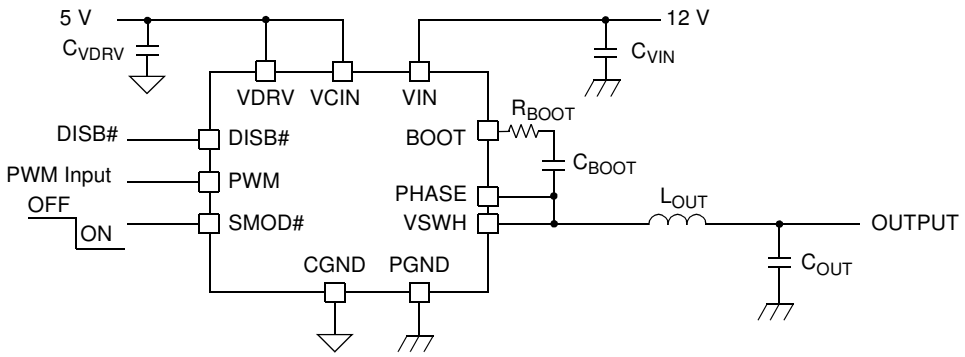


Figure 1. Power Train Application Circuit

Ordering Information

Order Number	Marking	Temperature Range	Device Package	Packing Method	Quantity
FDMF6704	FDMF6704_1	-55 °C to 150 °C	40 Pin, 3 DAP, MLP 6x6 mm	Tape and Reel	3000

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Functional Block Diagram

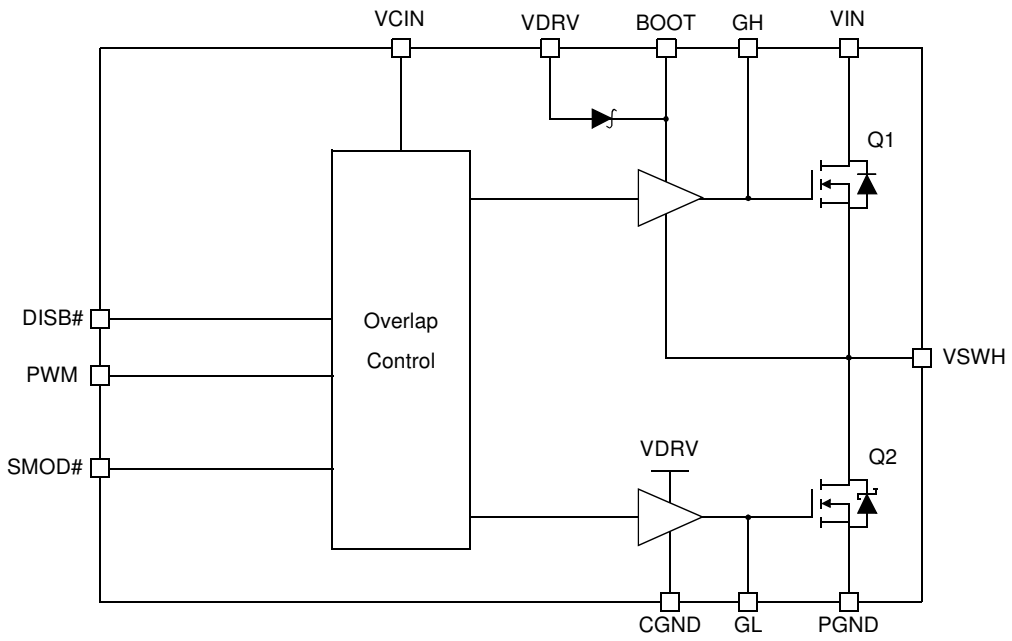
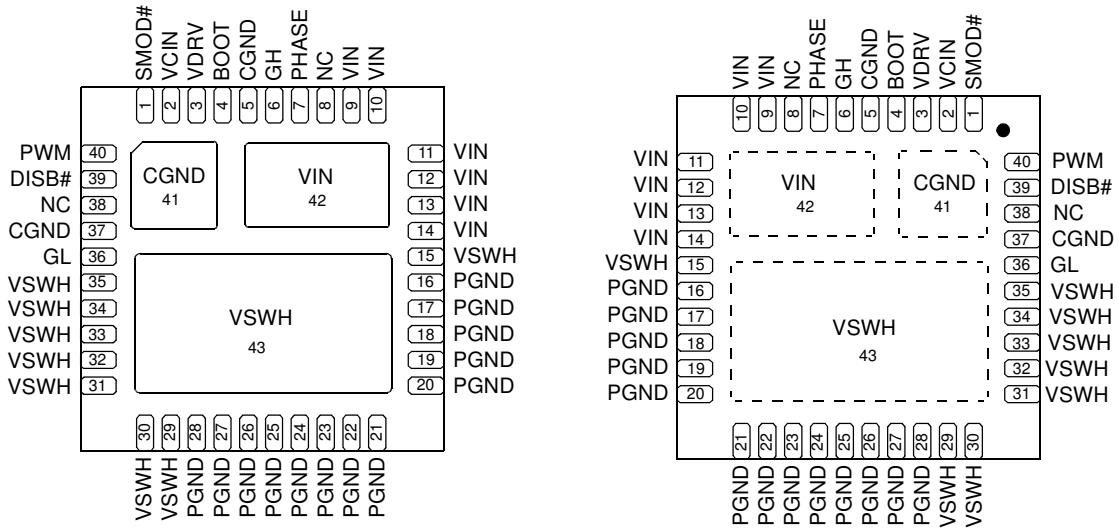


Figure 2. Functional Block Diagram

Pin Configuration



Bottom View

Top View

Figure 3. 6mm x 6mm, 40L MLP

Pin Description

Pin	Name	Function
1	SMOD#	When SMOD# = HI, low side driver is inverse of PWM input. When SMOD# = Low, low side driver is disabled. This pin has no internal pullup or pulldown. It should not be left floating. Do not add noise filter cap.
2	VCIN	IC bias supply. Minimum 1 µF ceramic capacitor is recommended from this pin to CGND.
3	VDRV	Power for low side driver. Minimum 1 µF ceramic capacitor is recommended to be connected as close as possible from this pin to CGND.
4	BOOT	Bootstrap supply input. Provides voltage supply to high-side MOSFET driver. Connect bootstrap capacitor from this pin to PHASE.
5, 37, 41	CGND	IC ground. Ground return for driver IC.
6	GH	For manufacturing test only. This pin must be floated. Must not be connected to any pin.
7	PHASE	Switch node pin for easy bootstrap capacitor routing. Electrically shorted to VSWH pin.
8, 38	NC	No connect.
9-14, 42	VIN	Power input. Output stage supply voltage.
15, 29-35, 43	VSWH	Switch node input. Provides return for high-side bootstrapped driver and acts as a sense point for the adaptive shoot-thru protection.
16-28	PGND	Power ground. Output stage ground. Source pin of low side MOSFET(s).
36	GL	For manufacturing test only. This pin must be floated. Must not be connected to any pin.
39	DISB#	Output disable. When low, this pin disable FET switching (GH and GL are held low). This pin has no internal pullup or pulldown. It should not be left floating. Do not add noise filter cap.
40	PWM	PWM Signal Input. This pin accepts a Tri-state logic-level PWM signal from the controller. Do not add noise filter cap.

Absolute Maximum Rating

Parameter			Min	Max	Units
VCIN, VDRV, DISB#, PWM, SMOD#, GL to CGND				6	V
VIN to PGND, CGND				27	V
BOOT, GH to VSWH, PHASE				6	V
BOOT, VSWH, PHASE, GH to GND				27	V
BOOT to VDRV				22	V
$I_{O(AV)}$*	V_{IN} = 12 V, V_O = 1.3 V	f_{SW} = 350 kHz		35	A
		f_{SW} = 1 MHz		32	A
$I_{O(peak)}$*				80	A
$R_{\theta JPCB}$	Junction to PCB Thermal Resistance			3.75	°C/W
Operating and Storage Junction Temperature Range			-55	150	°C

* $I_{O(AV)}$ and $I_{O(peak)}$ are measured in FCS evaluation board. These ratings can be changed with different application setting.

Recommended Operating Range

Parameter		Min	Typ	Max	Units
V_{CIN}	Control Circuit Supply Voltage	4.5	5	5.5	V
V_{IN}	Output Stage Supply Voltage	3*	12	14	V

* May be operated at lower input voltage. See figure 10.

Electrical Characteristics

V_{IN} = 12 V, T_A = 25 °C unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Operating Quiescent Current	IQ	PWM = GND			2	mA
		PWM = V_{CIN}			2	
VCIN UVLO						
UVLO Threshold			3.0	3.2	3.4	V
UVLO COMP Hysteresis				0.2		V
PWM Input						
Sink Impedance				10		kΩ
Source Impedance				10		kΩ
Tri-State Rising Threshold		V_{CIN} = 5 V	3.2	3.4	3.6	V
Hysteresis				100		mV
Tri-State Falling Threshold		V_{CIN} = 5 V	1.2	1.4	1.6	V
Hysteresis				100		mV
Tri-State Pin Open				2.5		V
Tri-State Shut Off Time				100		ns
SMOD# and DISB# Input						
High Level Input Voltage			2			V
Low Level Input Voltage					0.8	V
Input Bias Current			-2		2	µA
Propagation Delay Time		PWM = GND, delay between SMOD# or DISB# from HI to LO to GL from HI to LO.		15		ns
High Side Driver						
Rise Time		10 % to 90 %		25		ns
Fall Time		90 % to 10 %		20		ns
Deadband Time	t_{DTHH}	GL going LO to GH going HI, 10 % to 10 %		25		ns
Propagation Delay	t_{PDHL}	PMW going LO to GH going LO		10		ns
Low Side Driver						
Rise Time		10 % to 90 %		25		ns
Fall Time		90 % to 10 %		20		ns
Deadband Time	t_{DTLH}	VSWH going LO to GL going HI, 10 % to 10 %		20		ns
Propagation Delay	t_{PDLL}	PWM going HI to GL going LO		10		ns
250 ns Time Out Circuit						
250 ns Time Delay		Delay between GH from HI to LO and GL from LO to HI.		250		ns

Description of Operation

Circuit Description

The FDMF6704 is a driver plus FET module optimized for synchronous buck converter topology. A single PWM input signal is all that is required to properly drive the high-side and the low-side MOSFETs. Each part is capable of driving speeds up to 1 MHz.

PWM

When the PWM input goes high, the high side MOSFET turns on. When it goes low, the low side MOSFET turns on. When it is open, both the low side and high side MOFET will turn off.

The DISB# input is combined with the PWM signal to control the driver output. In a typical multiphase design, DISB# will be a shared signal used to turn on all phases. The individual PWM signals from the controller will be used to dynamically enable or disable individual phases.

Low-Side Driver

The low-side driver (GL) is designed to drive a ground referenced low $R_{DS(ON)}$ N-channel MOSFET. The bias for GL is internally connected between VDRV and CGND. When the driver is enabled, the driver's output is 180° out of phase with the PWM input. When the driver is disabled (DISB# = 0 V), GL is held low.

High-Side Driver

The high-side driver (GH) is designed to drive a floating N-channel MOSFET. The bias voltage for the high-side driver is developed by a bootstrap supply circuit, consisting of the internal diode and external bootstrap capacitor (C_{BOOT}). During start-up, VSWH is held at PGND, allowing C_{BOOT} to charge to V_{DRV} through the internal diode. When the PWM input goes high, GH will begin to charge the high-side MOSFET's gate (Q1). During this transition, charge is removed from C_{BOOT} and delivered to Q1's gate. As Q1 turns on, VSWH rises to V_{IN}, forcing the BOOT pin to V_{IN} +$V_{C(BOOT)}$, which provides sufficient VGS enhancement for Q1. To complete the switching cycle, Q1 is turned off by pulling GH to VSWH. C_{BOOT} is then recharged to VDRV when VSWH falls to PGND. GH output is in phase with the PWM input. When the driver is disabled, the high-side gate is held low.

SMOD

The SMOD (Skip Mode) function allows for higher converter efficiency under light load conditions. During SMOD, the LS FET is disabled and it prevents discharging of output caps. When the SMOD# pin is pulled high, the sync buck converter will work in synchronous mode. When the SMOD# pin is pulled low, the LS FET is turned off. The SMOD function does not have internal current sensing. This SMOD# pin is connected to a PWM controller which enables or disables the SMOD automatically when the controller detects light load condition. Normally this pin is Active Low.

Adaptive Gate Drive Circuit

The driver IC embodies an advanced design that ensures minimum MOSFET dead-time while eliminating potential shoot-through (cross-conduction) currents. It senses the state of the MOSFETs and adjusts the gate drive, adaptively, to ensure they do not conduct simultaneously. Refer to Figure 4 for the relevant timing waveforms.

To prevent overlap during the low-to-high switching transition (Q2 OFF to Q1 ON), the adaptive circuitry monitors the voltage at the GL pin. When the PWM signal goes HIGH, Q2 will begin to turn OFF after some propagation delay (t_{PDLL}). Once the GL pin is discharged below 1 V, Q1 begins to turn ON after adaptive delay t_{DTHH}.

To preclude overlap during the high-to-low transition (Q1 OFF to Q2 ON), the adaptive circuitry monitors the voltage at the VSWH pin. When the PWM signal goes LOW, Q1 will begin to turn OFF after some propagation delay (t_{PDHL}). Once the VSWH pin falls below 1 V, Q2 begins to turn ON after adaptive delay t_{DTLH}.

Additionally, V_{GS} of Q1 is monitored. When $V_{GS(Q1)}$ is discharged low, a secondary adaptive delay is initiated, which results in Q2 being driven ON after 250 ns, regardless of VSWH state. This function is implemented to ensure C_{BOOT} is recharged each switching cycle, particularly for cases where the power convertor is sinking current and VSWH voltage does not fall below the 1 V adaptive threshold. The 250 ns secondary delay is longer than t_{DTLH}.

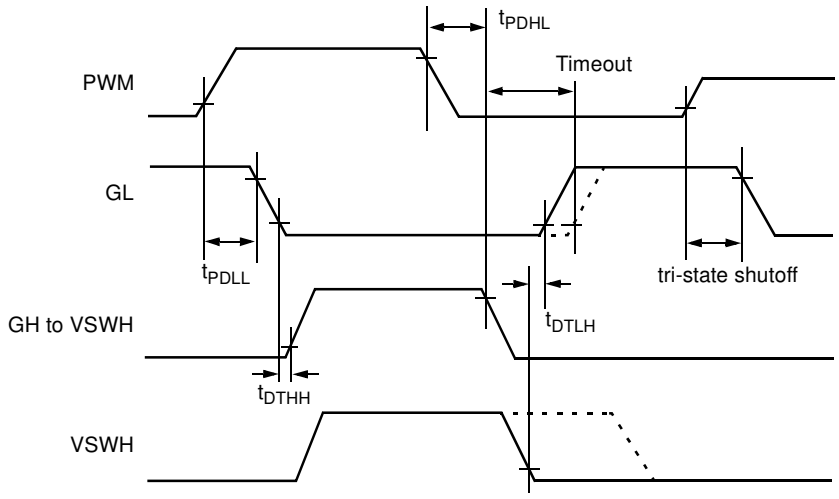


Figure 4. Timing Diagram

Switch Node Ringing Suppression

Fairchild's DrMOS products have proprietary feature* that minimizes the peak overshoot and ringing voltage on the switch node (VSWH) output, without the need of external snubbers. The following pictures show the waveforms of an FDMF6704 DrMOS part and a competitor's part tested without snubbing. The tests were done in the same test circuit, under the same operating conditions.

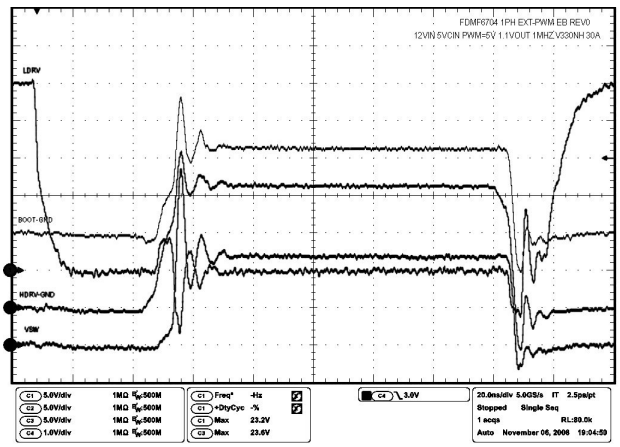


Figure 5. FDMF6704

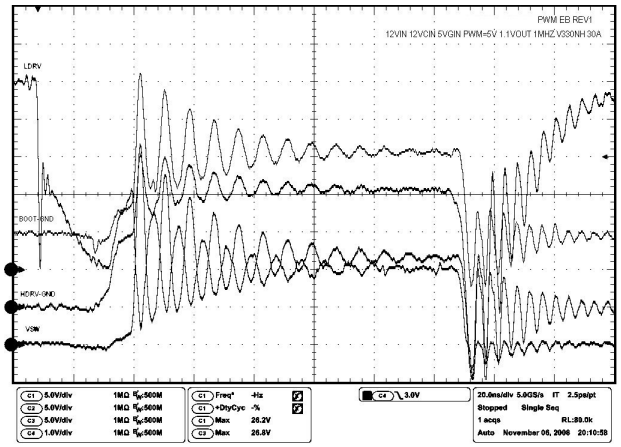


Figure 6. Competitor Part

* Patent Pending

Typical Characteristics

V_{IN} = 12V, V_{CIN} = 5V, T_A = 25°C unless otherwise noted.

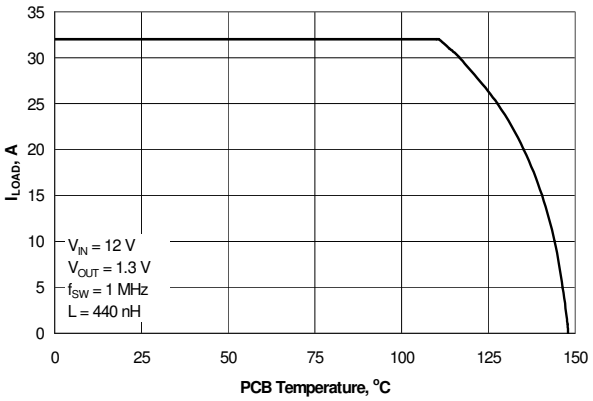


Figure 7. Safe Operating Area

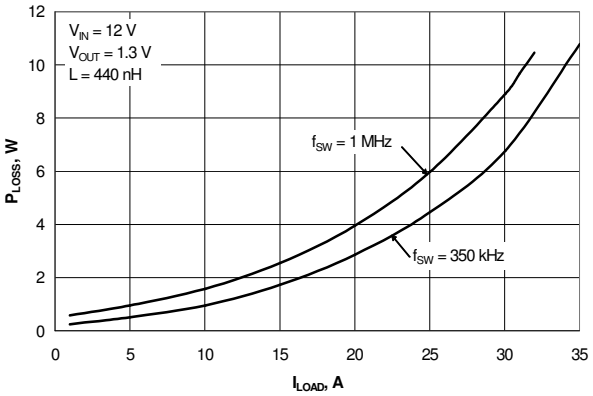


Figure 8. Module Power Loss vs. Output Current

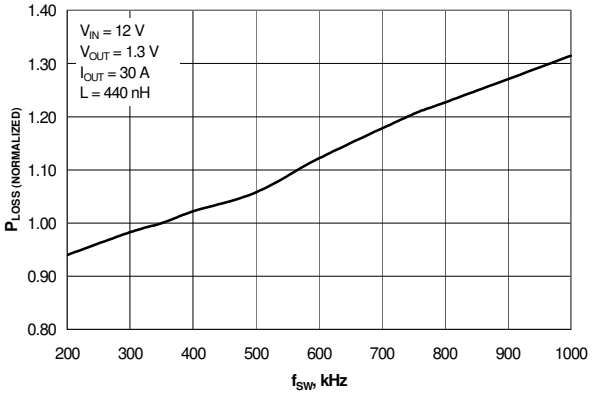


Figure 9. Power Loss vs. Switching Frequency

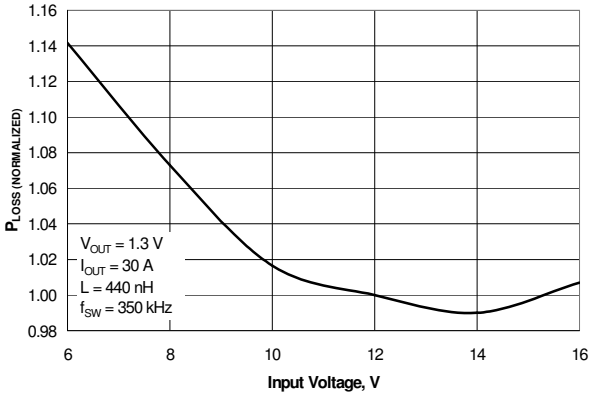


Figure 10. Power Loss vs. Input Voltage

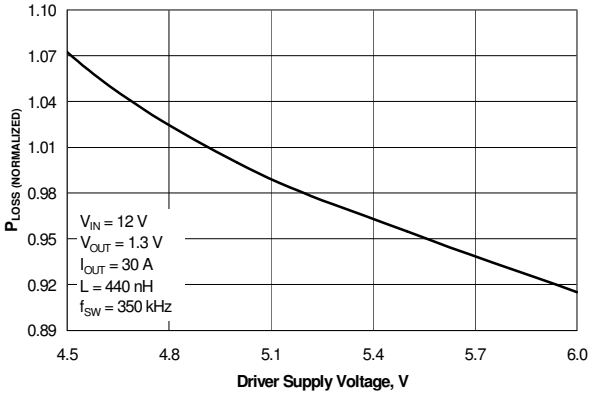


Figure 11. Power Loss vs. Driver Supply Voltage

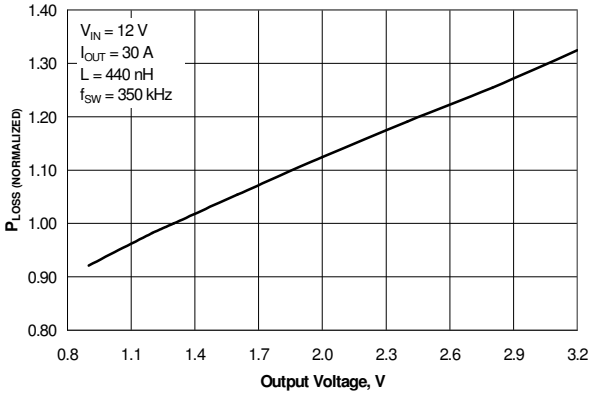


Figure 12. Power Loss vs. Output Voltage

Typical Characteristics

V_{IN} = 12V, V_{CIN} = 5V, T_A = 25°C unless otherwise noted.

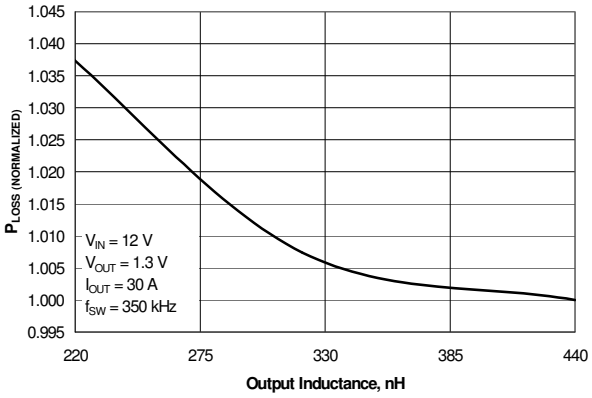


Figure 13. Power Loss vs. Output Inductance

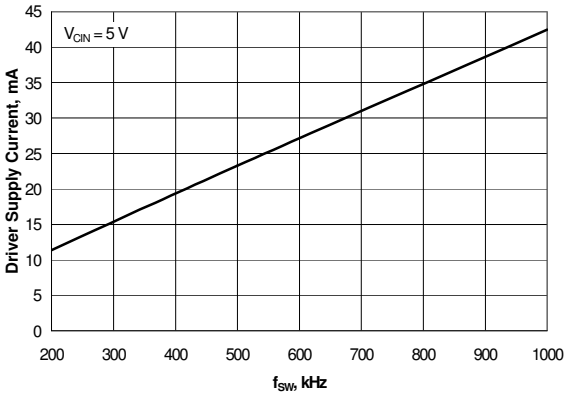


Figure 14. Driver Supply Current vs. Frequency

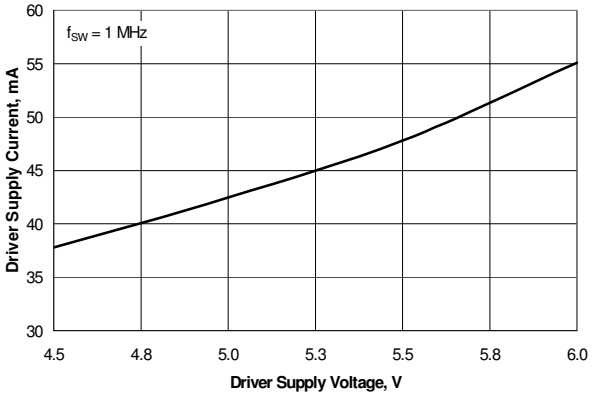


Figure 15. Driver Supply Current vs. Drive Supply Voltage

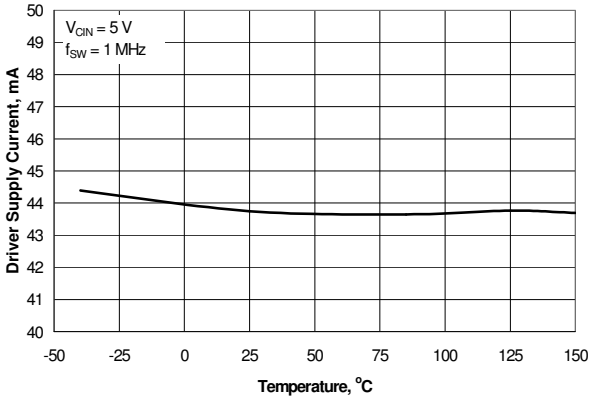


Figure 16. Driver Supply Current vs. Temperature

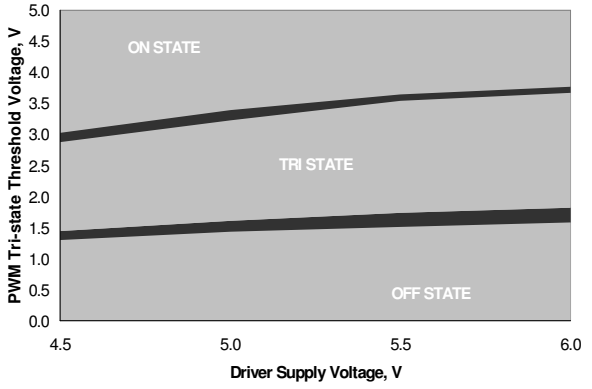


Figure 17. PWM Tri-state Threshold Voltage vs. Driver Supply Voltage

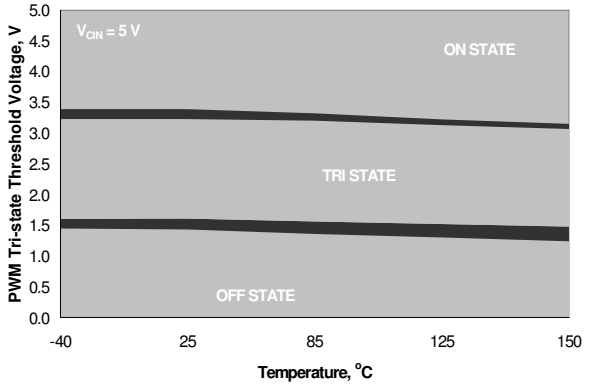


Figure 18. PWM Tri-state Threshold Voltage vs. Temperature

Typical Characteristics

V_{IN} = 12V, V_{CIN} = 5V, T_A = 25°C unless otherwise noted.

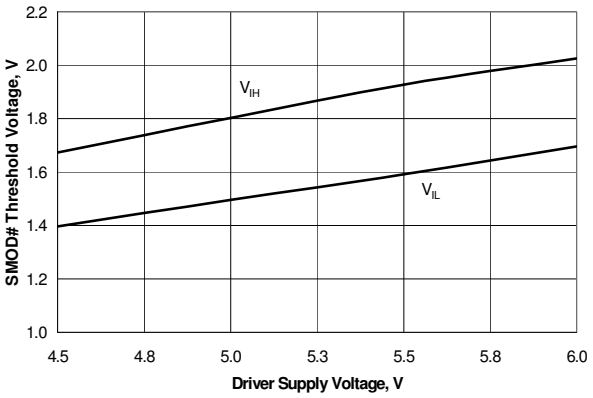


Figure 19. SMOD# Threshold Voltage vs. Driver Supply Voltage

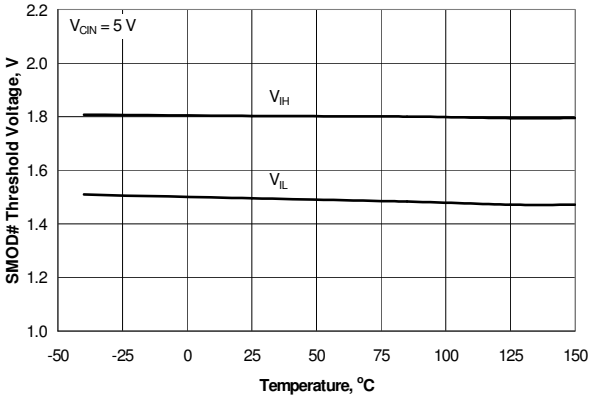


Figure 20. SMOD# Threshold Voltage vs. Temperature

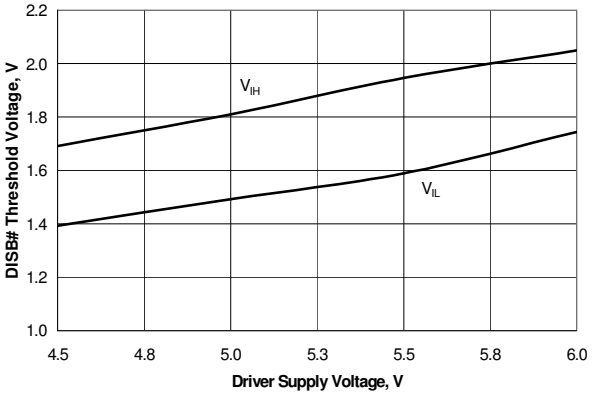


Figure 21. DISB# Threshold Voltage vs. Driver Supply Voltage

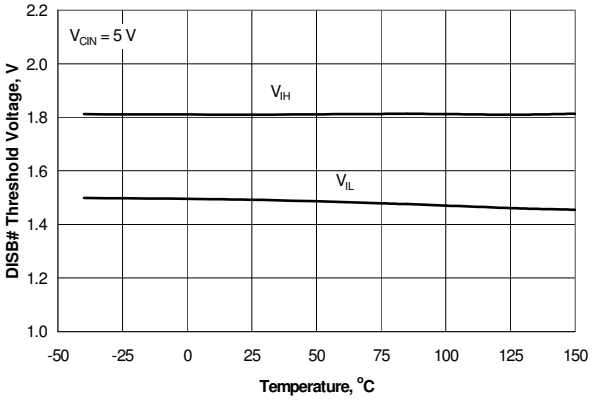


Figure 22. DISB# Threshold Voltage vs. Temperature

Application Information

Supply Capacitor Selection

For the supply input (VCIN) of the FDMF6704, a local ceramic bypass capacitor is recommended to reduce the noise and to supply the peak current. Use at least a 1µF, X7R or X5R capacitor. Keep this capacitor close to the FDMF6704 VCIN and PGND pins.

Bootstrap Circuit

The bootstrap circuit uses a charge storage capacitor (C_{BOOT}), as shown in Figure 23. A bootstrap capacitance of 100nF, X7R or X5R capacitor is adequate. A series bootstrap resistor would be needed for specific application in order to improve switching noise immunity

VCIN Filter

The VDRV pin provides power to the gate drive of the high side and low side power FET. In most cases, it can be connected directly to VCIN, the pin that provides power to the logic section of the driver. For additional noise immunity, an RC filter can be inserted between VDRV and VCIN. Recommended values would be 10 Ohms and 1µF.

Typical Application

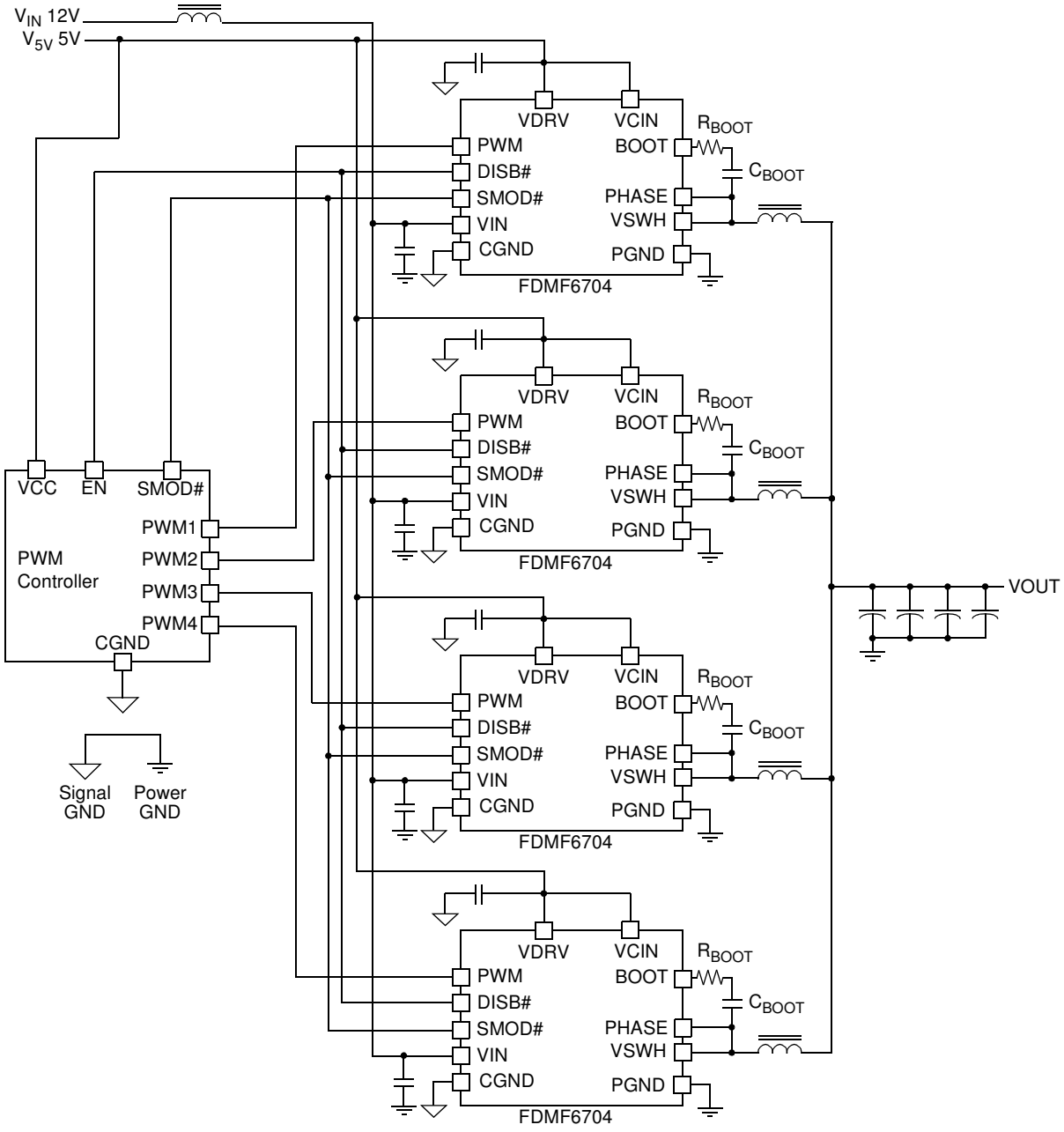


Figure 23. Typical Application

Power Loss and Efficiency Measurement and Calculation

Refer to Figure 24 for power loss testing method. Power loss calculation are as follows:

(a) P_{IN}	= (V_{IN} x I_{IN}) + (V_{5V} x I_{5V})	(W)
(b) P_{SW}	= V_{SW} x I_{OUT}	(W)
(c) P_{OUT}	= V_{OUT} x I_{OUT}	(W)
(d) P_{LOSS_MODULE}	= P_{IN} - P_{SW}	(W)
(e) P_{LOSS_BOARD}	= P_{IN} - P_{OUT}	(W)
(f) EFF_{MODULE}	= 100 x P_{SW}/P_{IN}	(%)
(g) EFF_{BOARD}	= 100 x P_{OUT}/P_{IN}	(%)

PCB Layout Guideline

Figure 25 shows a proper layout example of FDMF6704 and critical parts. All of high current flow path, such as VIN, VSWH, V_{OUT} and GND copper, should be short and wide for better and stable current flow, heat radiation and system performance.

Following is a guideline which the PCB designer should consider:

1. Input ceramic bypass capacitors must be close to VIN and PGND pin of FDMF6704 to help reduce the input current ripple component induced by switching operation.

2. The VSWH copper trace serves two purposes. In addition to being the high frequency current path from the DrMOS package to the output inductor, it also serves as heatsink for the lower FET in the DrMOS package. The trace should be short and wide enough to present a low impedance path for the high frequency, high current flow between the DrMOS and inductor in order to minimize losses and temperature rise. Please note that the VSWH node is a high voltage and high frequency switching node with high noise potential. Care should be taken to minimize coupling to adjacent traces. Additionally, since this copper trace also acts as heatsink for the lower FET, tradeoff must be made to use the largest area possible to improve DrMOS cooling while maintaining acceptable noise emission.

3. Output inductor location should be as close as possible to the FDMF6704 for lower power loss due to copper trace. Care should be taken so that inductor dissipation does not heat the DrMOS.

4. The PowerTrench® 5 MOSFETs used in the output stage are very effective at minimizing ringing. In most cases, no snubber will be required. If a snubber is used, it should be placed near the FDMF6704. The resistor and capacitor need to be of proper size for the power dissipation.

5. Place ceramic bypass capacitor and BOOT capacitor as close as possible to the VCIN and BOOT pins of the FDMF6704 to ensure clean and stable power. Routing width and length should be considered as well.

6. Include a trace from PHASE to VSWH in order to improve noise margin. Keep trace as short as possible.

7. The layout should include the option to insert a small value series boot resistor between boot cap and BOOT pin. The boot loop size, including R_{BOOT} and C_{BOOT}, should be as small as possible. The boot resistor is normally not required, but is effective at improving noise operating margin in multi phase designs that may have noise issues due to ground bounce and high negative VSWH ringing. The VIN and PGND pins handle large current transients with frequency components above 100 MHz. If possible, these package pins should be connected directly to the VIN and board GND planes. The use of thermal relief traces in series with these pins is discouraged since this will add inductance to the power path. This added inductance in series with the PGND pin will degrade system noise immunity by increasing negative VSWH ringing.

8. CGND pad and PGND pins should be connected by plane GND copper with multiple vias for stable grounding. Poor grounding can create a noise transient offset voltage level between CGND and PGND. This could lead to fault operation of gate driver and MOSFET.

9. Ringing at the BOOT pin is most effectively controlled by close placement of the boot capacitor. Do not add an additional BOOT to PGND capacitor. This may lead to excess current flow through the BOOT diode.

10. SMOD#, DISB# and PWM pins don't have internal pull up or pull down resistors. They should not be left floating. These pins should not have any noise filter caps.

11. Use multiple vias on each copper area to interconnect top, inner and bottom layers to help smooth current flow and heat conduction. Vias should be relatively large and of reasonable inductance. Critical high frequency components such as R_{BOOT}, C_{BOOT}, the RC snubber and bypass caps should be located close to the DrMOS module and on the same side of the PCB as the module. If not feasible, they should be connected from the backside via a network of low inductance vias.

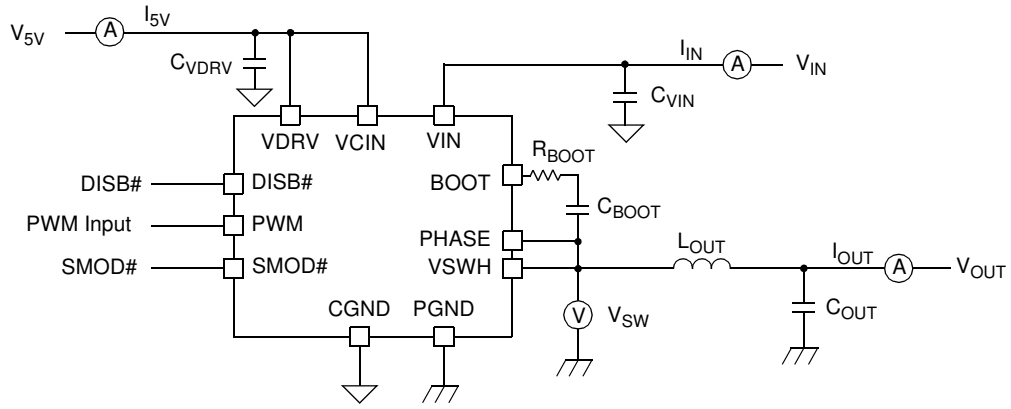
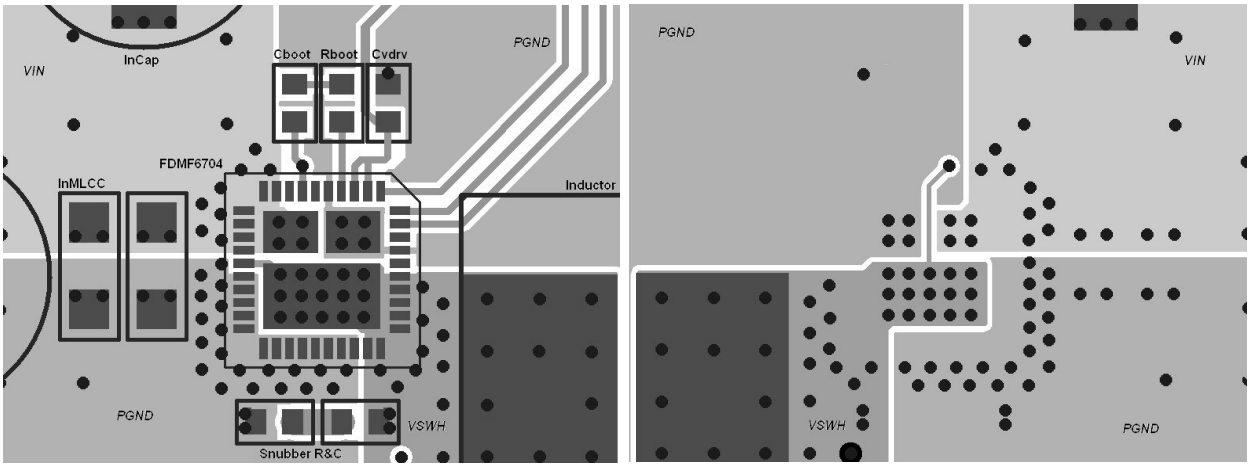


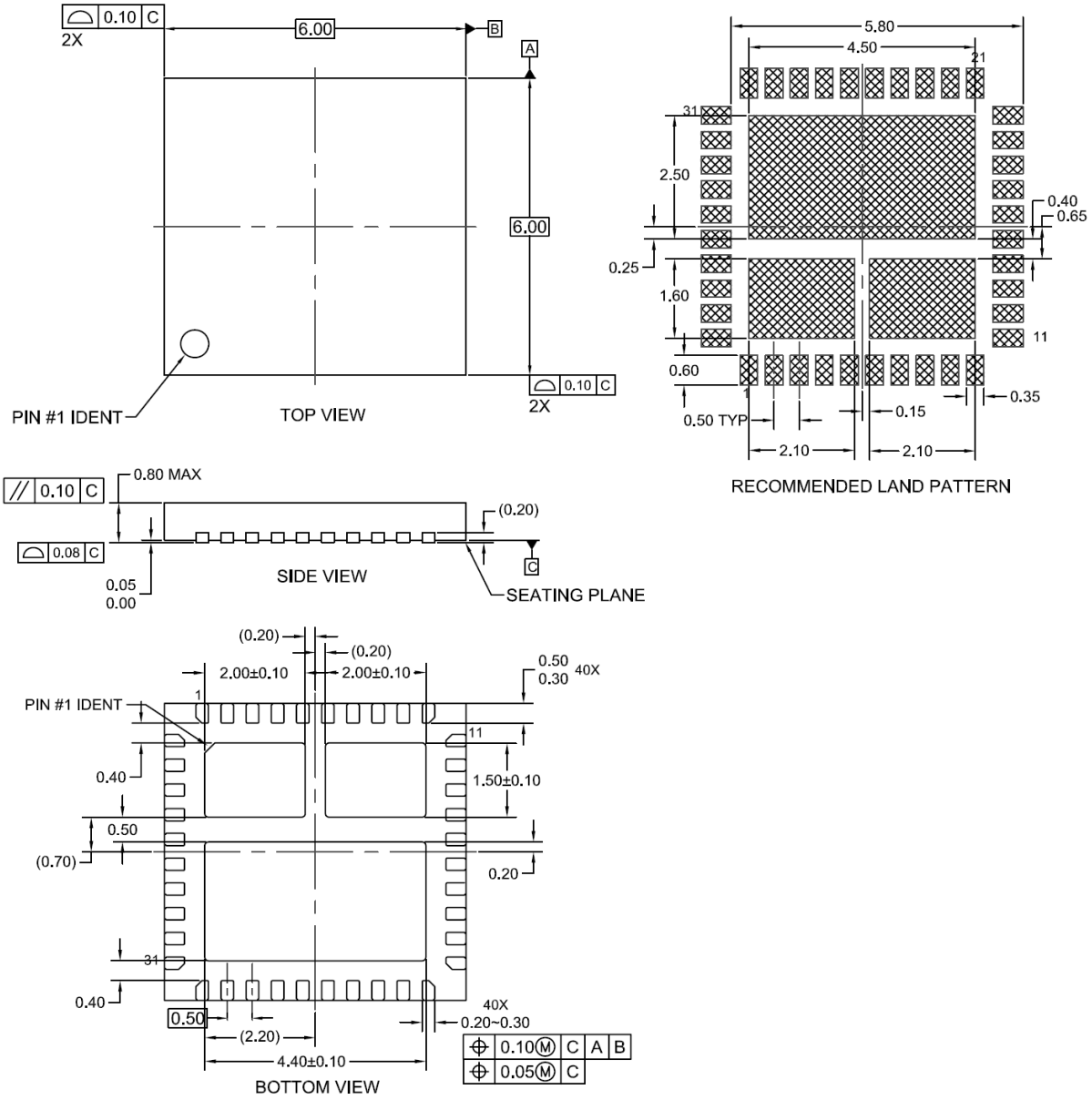
Figure 24. Power Loss Measurement Block Diagram



TOP VIEW BOTTOM VIEW

Figure 25. Typical PCB Layout Example

Dimensional Outline and Pad layout



NOTES:

A. DOES NOT FULLY CONFORM TO JEDEC REGISTRATION, MO-220. DATED MAY/2005.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

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