

## **BUF08832EVM User Guide and Software Tutorial**

This user's guide describes the characteristics, operation, and use of the BUF08832EVM evaluation board. It discusses how to set up and configure the software and hardware, and reviews various aspects of the program operation. Throughout this document, the terms *evaluation board*, *evaluation module*, and *EVM* are synonymous with the BUF08832EVM. This user's guide also includes information regarding operating procedures and input/output connections, an electrical schematic, and a parts list for the EVM.

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## 1 Overview

The BUF08832 is a programmable gamma-voltage generator and  $V_{COM}$  calibrator. This device offers eight programmable gamma channels and one programmable  $V_{COM}$  channel, making it ideal for 10-bit source TFT-LCD reference drivers. The BUF08832EVM is a platform for evaluating the performance of the [BUF08832](#) under various signal, reference, and supply conditions. This document gives a general overview of the BUF08832EVM, and provides a general description of the features and functions to be considered while using this evaluation module.

### 1.1 BUF08832EVM Kit Contents

Contact the Texas Instruments Product Information Center nearest you if any component is missing.

The complete kit includes the following items:

- BUF08832\_Test\_Board PCB
- USB DIG Platform PCB
- USB cable
- Barrel plug cable assembly (part # 10-01935 - Tensility International Corporation) for external power supply
- CD-ROM that contains this user's guide, product software, and related documentation

Check the TI web site at <http://www.ti.com> to verify that you have the latest versions of the related software.

### 1.2 Related Documentation from Texas Instruments

The following documents provide information regarding Texas Instruments' integrated circuits used in the assembly of the BUF08832EVM. This user's guide is available from the TI web site under literature number **SBOU081**. Any letter appended to the literature number corresponds to the document revision that is current at the time of the writing of this document. Newer revisions may be available from the [TI web site](#), or call the Texas Instruments' Literature Response Center at (800) 477-8924 or the Product Information Center at (972) 644- 5580. When ordering, identify the document by both title and literature number.

#### Related Documentation

| Document                                     | Literature Number       |
|----------------------------------------------|-------------------------|
| <a href="#">BUF08832 Product Data Sheet</a>  | <a href="#">SBOS476</a> |
| <a href="#">USB DIG Platform Users Guide</a> | <a href="#">SBOU058</a> |

## 2 BUF08832EVM Hardware Setup

Figure 1 shows the system setup for the BUF08832EVM. The PC runs software that communicates with the USB DIG Platform. The USB DIG Platform generates the analog and digital signals used to communicate with the BUF08832\_Test\_Board. Connectors on the BUF08832\_Test\_Board allow the user to connect to the device under test (DUT), in order to monitor the power, current, and voltage of the BUF08832 DUT.

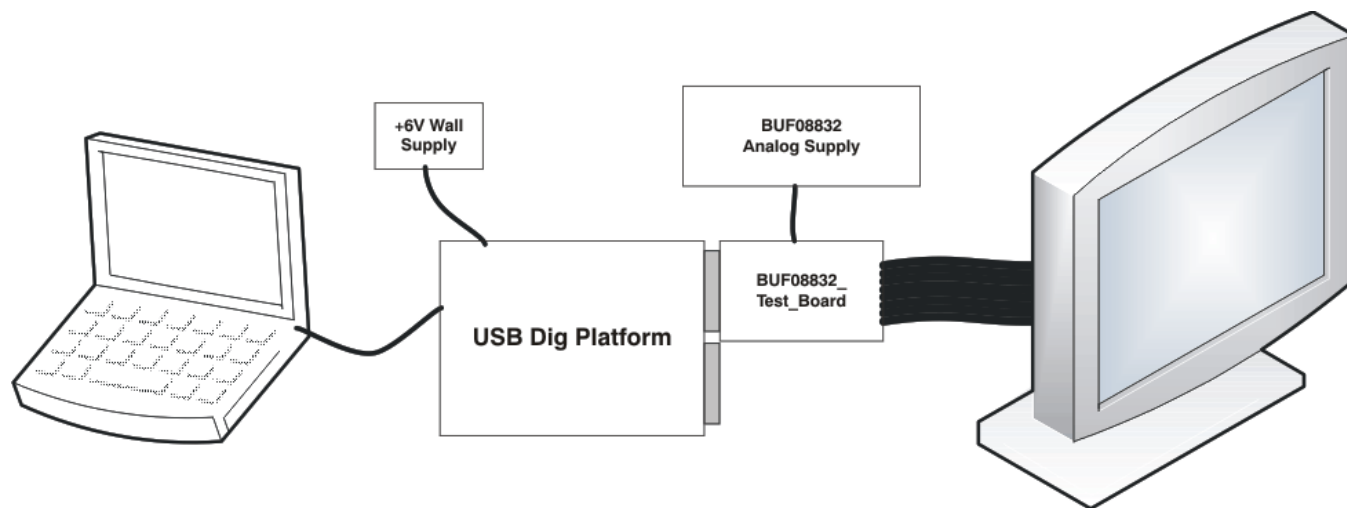


Figure 1. BUF08832EVM Hardware Setup

### 2.1 Theory of Operation for BUF08832\_Test\_Board Hardware

Figure 2 presents a block diagram of the BUF08832\_Test\_Board. The functionality of this PCB is relatively simple. It provides connections to the I<sup>2</sup>C interface and general-purpose input/outputs (GPIO) on the USB DIG Platform board. It also provides connection points for external connections of the shunt voltage, bus voltage, and GND.

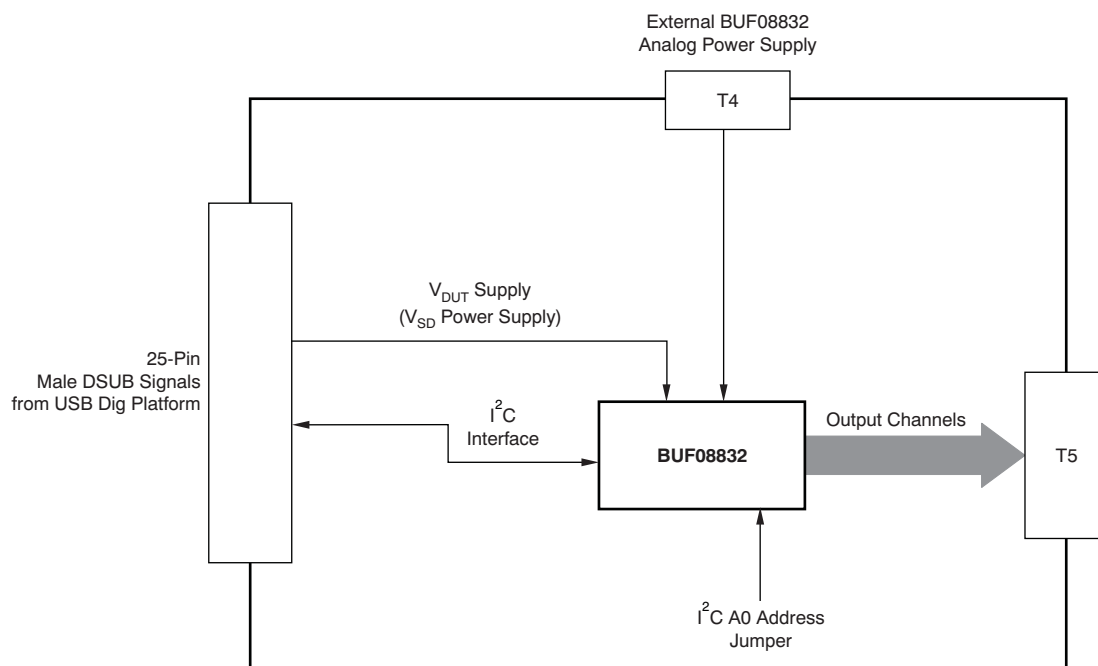


Figure 2. BUF08832\_Test\_Board Block Diagram

## 2.2 Signal Definitions of J1 (25-Pin Male DSUB)

Table 1 lists the different signals connected to J1 on the BUF08832\_Test\_Board. Table 1 also identifies signals connected to pins on J1 that are not used on the BUF08832\_Test\_Board.

**Table 1. Signal Definition of J1 (25-Pin Male DSUB) on BUF08832\_Test\_Board**

| PIN On J1 | Signal                   | BUF08832 Pin                                                                                         |
|-----------|--------------------------|------------------------------------------------------------------------------------------------------|
| 1         | NC                       | No connection                                                                                        |
| 2         | NC                       | No connection                                                                                        |
| 3         | NC                       | No connection                                                                                        |
| 4         | NC                       | No connection                                                                                        |
| 5         | NC                       | No connection                                                                                        |
| 6         | NC                       | No connection                                                                                        |
| 7         | NC                       | No connection                                                                                        |
| 8         | NC                       | No connection                                                                                        |
| 9         | I <sup>2</sup> C_SCK     | No connection                                                                                        |
| 10        | I <sup>2</sup> C_SDA2    | No connection                                                                                        |
| 11        | NC                       | No connection                                                                                        |
| 12        | I <sup>2</sup> C_SCK_ISO | I <sup>2</sup> C clock signal (SCL) channel 1; can be disconnected using a switch                    |
| 13        | I <sup>2</sup> C_SDA_ISO | I <sup>2</sup> C data signal (SDA) channel 1; can be disconnected using a switch                     |
| 14        | NC                       | No connection                                                                                        |
| 15        | NC                       | No connection                                                                                        |
| 16        | NC                       | No connection                                                                                        |
| 17        | V <sub>DUT</sub>         | Switched 3V or 5V power. Note that when power is switched off, the digital I/O is also switched off. |
| 18        | V <sub>CC</sub>          | No connection                                                                                        |
| 19        | NC                       | No connection                                                                                        |
| 20        | NC                       | No connection                                                                                        |
| 21        | GND                      | Common or ground connection for power.                                                               |
| 22        | SPI_SCK                  | No connection                                                                                        |
| 23        | SPI_CS1                  | No connection                                                                                        |
| 24        | SPI_DOUT                 | No connection                                                                                        |
| 25        | SPI_DIN1                 | No connection                                                                                        |

## 2.3 Theory of Operation for USB\_DIG\_Platform

Figure 3 shows the block diagram for the USB DIG Platform. This platform is a general-purpose data acquisition system that is used on several different Texas Instruments evaluation modules. The details of its operation are included in a separate document, [SBOU058](#) (available for download at [www.ti.com](#)). The block diagram shown in Figure 3 gives a brief overview of the platform. The primary control device on the USB DIG Platform is the [TUSB3210](#).

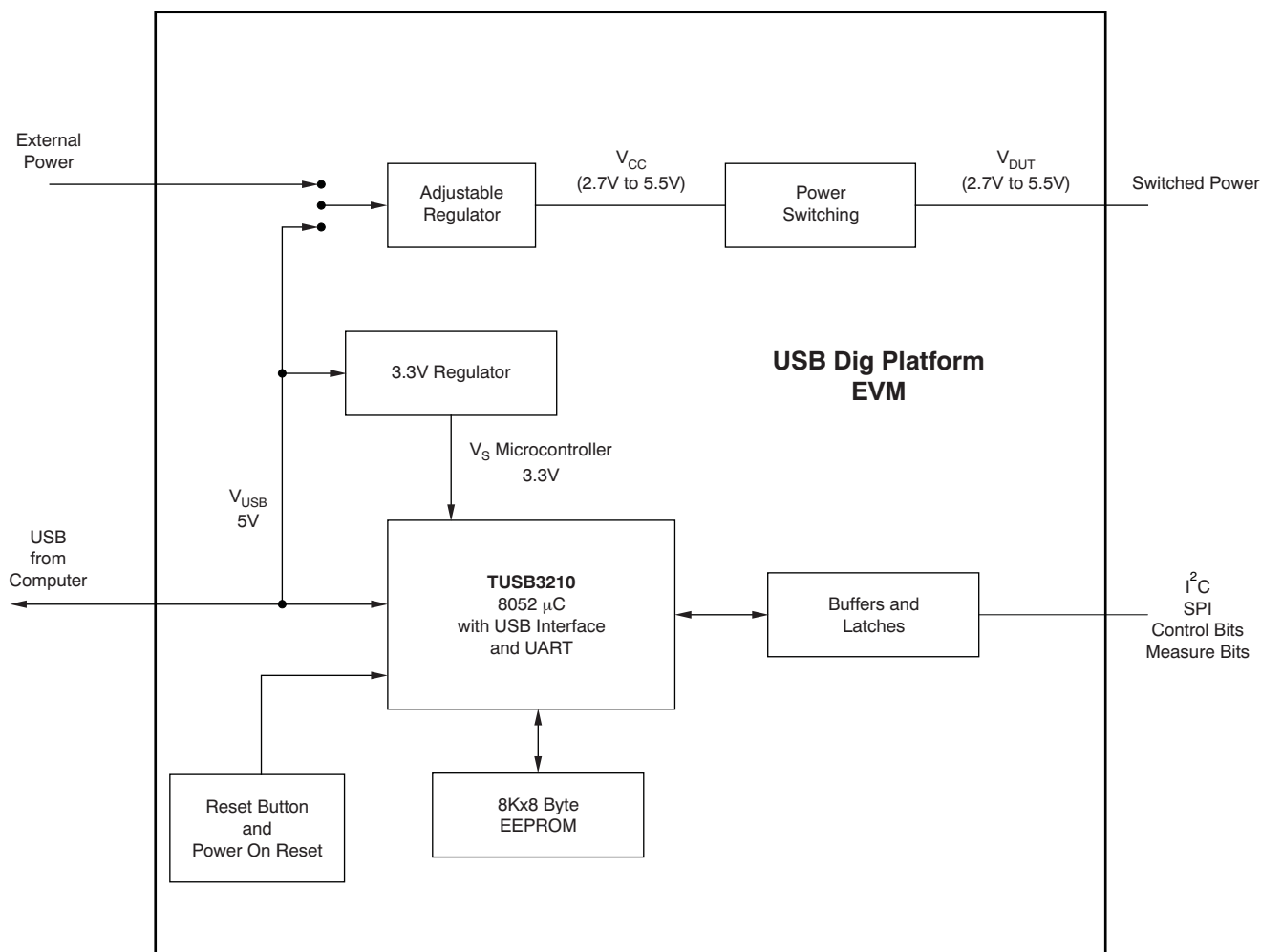


Figure 3. USB\_DIG\_Platform Theory of Operation

### 3 BUF08832EVM Hardware Overview

The BUF08832EVM hardware overview involves connecting the two PCBs of the EVM together, applying power, connecting the USB cable, and setting the jumpers. This section presents the details of this procedure.

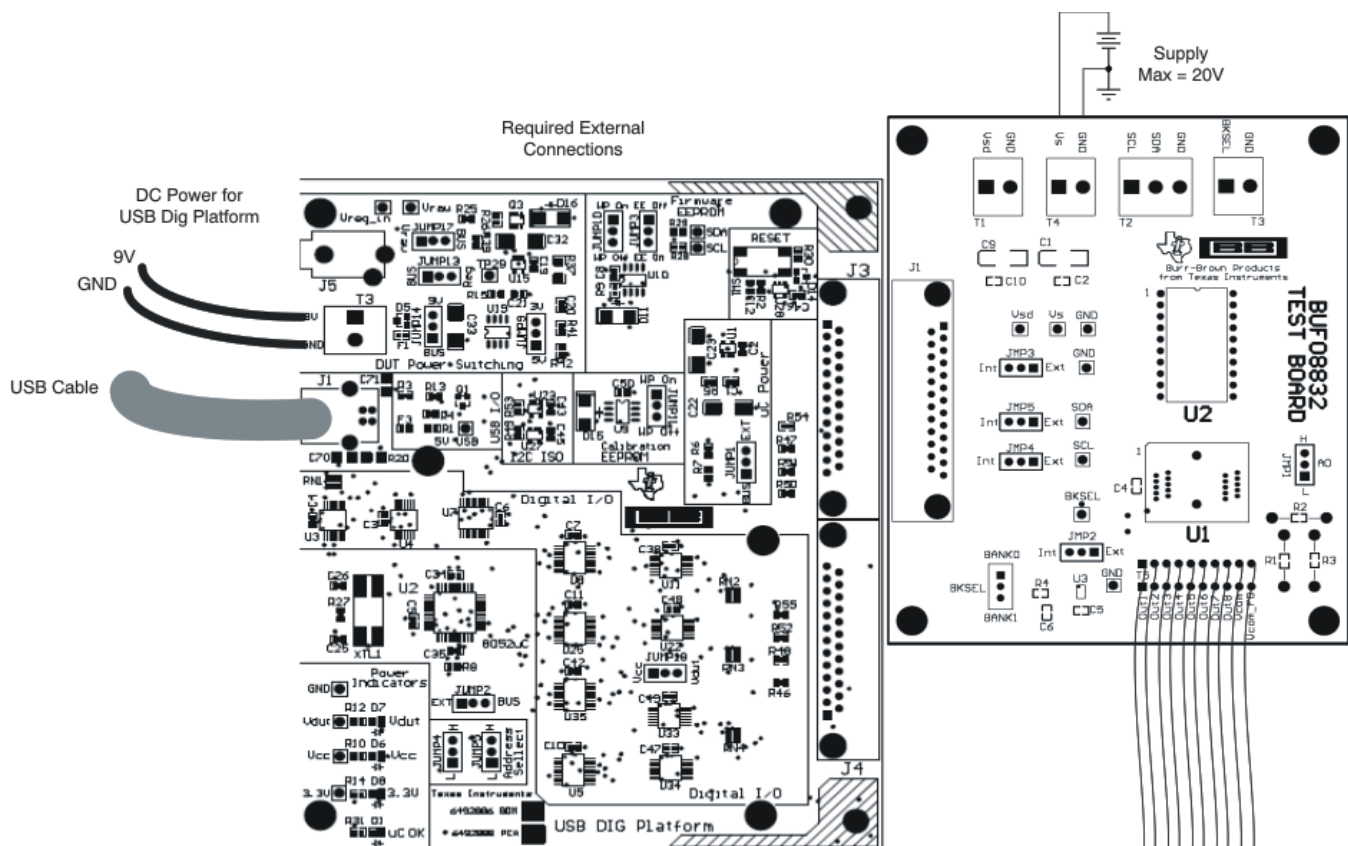
#### 3.1 Electrostatic Discharge Warning

##### CAUTION

Many of the components on the BUF08832EVM are susceptible to damage by electrostatic discharge (ESD). Customers are advised to observe proper ESD handling precautions when unpacking and handling the EVM, including the use of a grounded wrist strap at an approved ESD workstation.

#### 3.2 Typical Hardware Connections

To set up the BUF08832EVM hardware, connect the two PCBs of the EVM together, and apply a power source to the BUF08832 Test Board. The external connections may be the real-world system that the BUF08832 will be incorporated into. Figure 4 illustrates the typical hardware connections.





### 3.3 Connecting the Hardware

To connect the two PCBs of the BUF08832EVM together, gently push on both sides of the DSUB connectors (as shown in [Figure 5](#)). Make sure that the two connectors are completely pushed together; loose connections may cause intermittent operation.

### 3.4 Connecting Power

After the two parts of the BUF08832EVM are connected, as [Figure 5](#) shows, connect the power to the EVM. Always connect power before connecting the USB cable. If you connect the USB cable before connecting the power, the computer will attempt to communicate with an unpowered device that will not be able to respond.

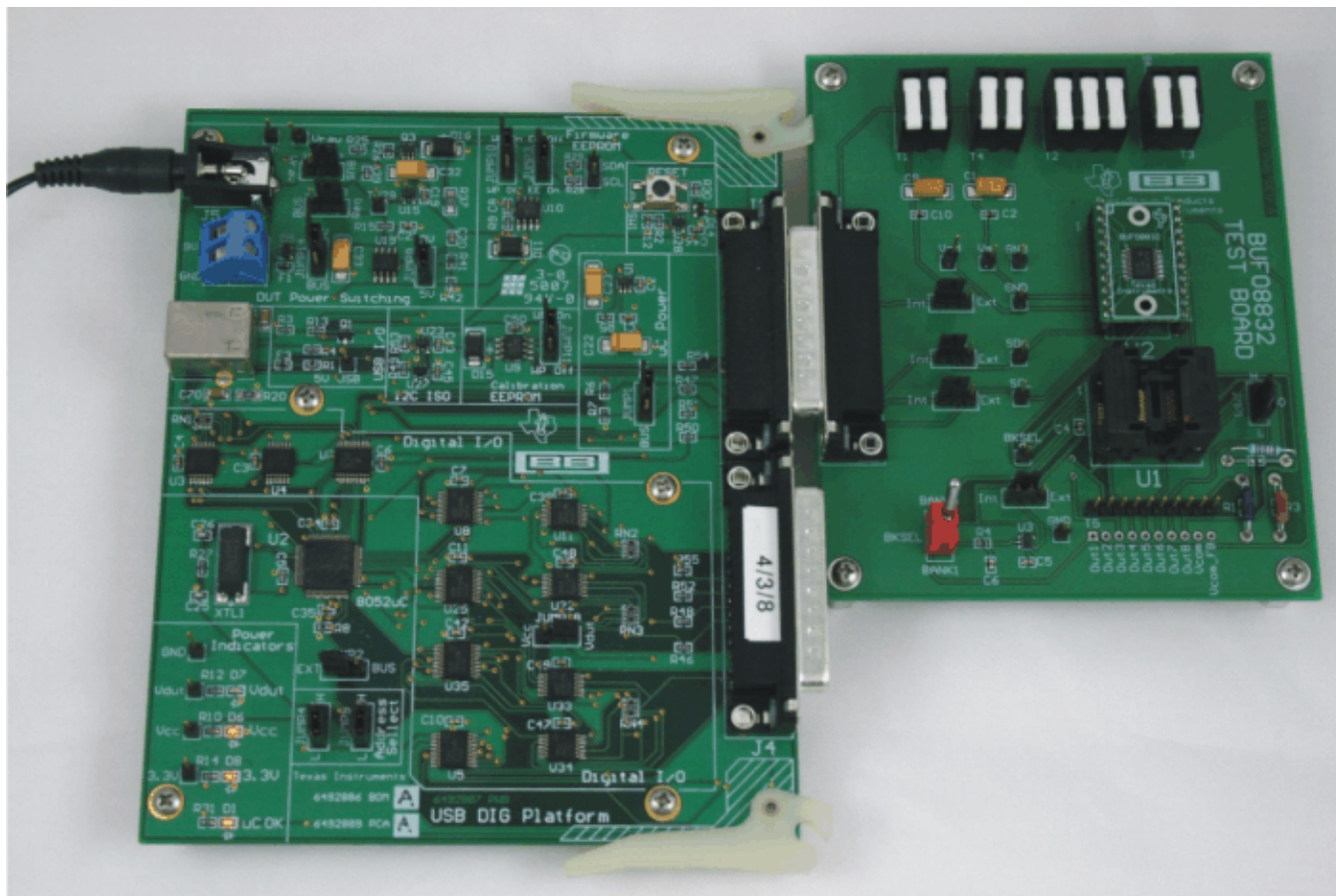


Figure 5. Connecting Power to the EVM

### 3.5 Connecting the USB Cable to the BUF08832EVM

Figure 6 shows the typical response to connecting the USB DIG Platform board to a PC USB port for the first time. Note that the EVM must be powered on before connecting the USB cable. Typically, the computer will respond with a *Found New Hardware, USB Device* pop-up dialog. The pop-up window typically changes to *Found New Hardware, USB Human Interface Device*. This pop-up indicates that the device is ready to be used. The USB DIG Platform uses the human interface device drivers that are part of the Microsoft® Windows® operating system.

In some cases, the Windows *Add Hardware Wizard* will pop up. If this prompt occurs, allow the system device manager to install the human interface drivers by clicking **Yes** when requested to install drivers.

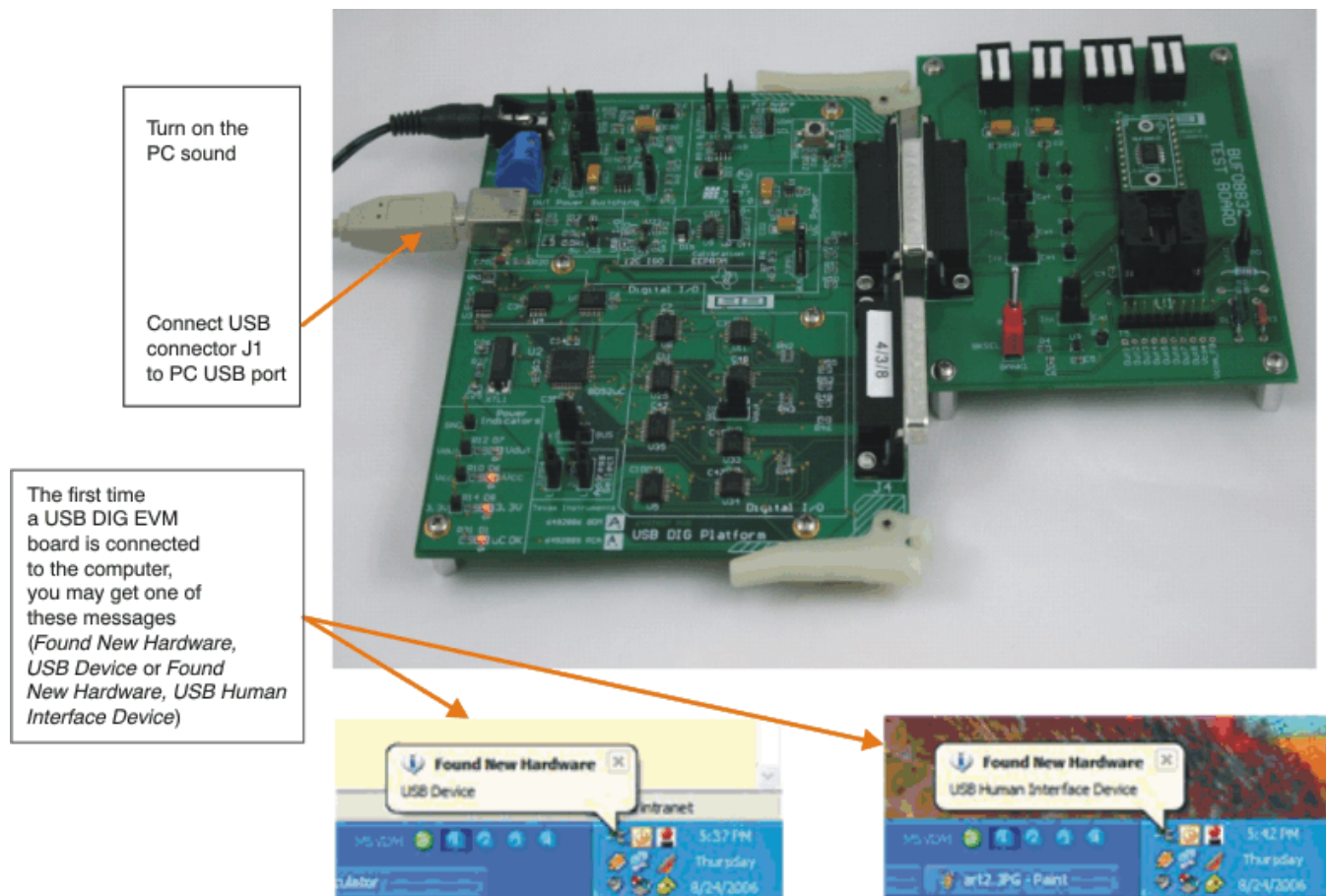


Figure 6. Connecting the USB Cable



### 3.6 BUF08832EVM Default Jumper Settings

Figure 7 shows the default jumpers configuration for the BUF08832EVM. In general, the jumper settings of the USB DIG Platform will not need to be changed. You may want to change some of the jumpers on the BUF08832\_Test\_Board to match your specific configuration. For instance, you may wish to set a specific I<sup>2</sup>C address on the DUT.

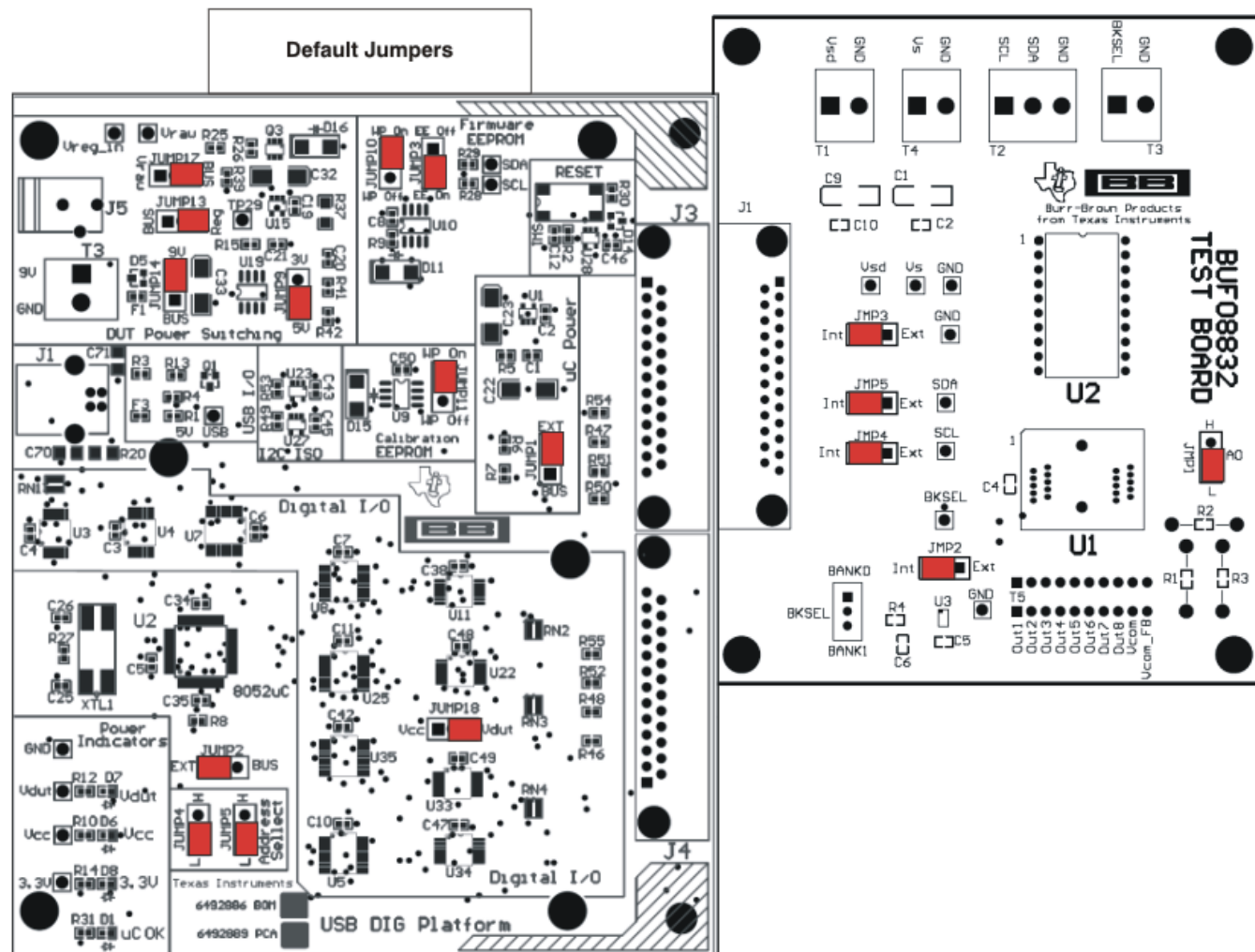


Figure 7. BUF08832EVM Default Jumper Settings

Jumpers 2 through 5 on the BUF08832\_Test\_Board are all typically set to the same position. When set to the INT position, the signals for digital supply, bank select and the digital communication lines are generated and controlled from the USB\_DIG\_Platform or by the onboard bank select switch. When these jumpers are set to the EXT position, the previously described signals connect to the terminal strips T1, T2, and T3. Jumper 1 controls the I<sup>2</sup>C address pin for the BUF08832. This jumper can set the address for A0 to either high or low.

**Table 2** summarizes the function of the BUF08832\_Test\_Board jumpers. For most applications, Jumpers 2 through 5 are all set to either the INT or the EXT position.

**Table 2. BUF08832\_Test\_Board Jumper Functions**

| Jumper | Default | Purpose                                                                                                                                                                                                                                                                                                                                                                      |
|--------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| JMP1   | L       | This jumper selects I <sup>2</sup> C AO address selection. Two separate I <sup>2</sup> C addresses can be selected, depending on whether JMP1 is set to high or low.                                                                                                                                                                                                         |
| JMP2   | INT     | This jumper selects whether the BKSEL pin on the BUF08832 is controlled by the manual switch located on the BUF08832_Test_Board or whether the BKSEL can be controlled by an external source connected to terminal T3. The default INT position allows the BKSEL pin to be controlled by the manual switch.                                                                  |
| JMP3   | INT     | This jumper selects whether the VSD pin on the BUF08832 is connected to the VDUT signal generated from the USB_DIG_Platform or whether digital supply pin is connected to terminal T1, allowing for an external supply to power the digital circuitry. The default INT position connects the VSD pin to the VDUT control signal.                                             |
| JMP4,  | INT     | This jumper selects whether the SCL pin on the BUF08832 is connected to the I <sup>2</sup> C_SCK_ISO signal generated from the USB_DIG_Platform or whether the SCL pin is connected to terminal T2 allowing for an external source to control the I <sup>2</sup> C clock line. The default INT position connects the SCL pin to the I <sup>2</sup> C_SCK_ISO control signal. |
| JMP5   | INT     | This jumper selects whether the SDA pin on the BUF08832 is connected to the I <sup>2</sup> C_SDA_ISO signal generated from the USB_DIG_Platform or whether the SDA pin is connected to terminal T2 allowing for an external source to control the I <sup>2</sup> C data line. The default INT position connects the SDA pin to the I <sup>2</sup> C_SDA_ISO control signal.  |

**Table 3** summarizes the function of the USB DIG Platform jumpers. For most applications, the default jumper position should be used. A separate document ([SBOU058](#)) gives details regarding the operation and design of the USB DIG Platform.

**Table 3. USB DIG Platform Jumper Functions**

| Jumper       | Default   | Purpose                                                                                                                                                                                                                                         |
|--------------|-----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| JUMP1        | EXT       | This jumper selects external power or bus power. External power is applied on J5 or T3 (9V dc). Bus power is 5V from the USB bus. External power is typically used because the USB Bus power is noisy.                                          |
| JUMP2        | EXT       | Same as JUMP1.                                                                                                                                                                                                                                  |
| JUMP3        | EE ON     | This jumper determines where the TUSB3210 will load the USB DIG Platform firmware upon power-up or reset. The <i>EE Off</i> position is used for development for development or firmware update.                                                |
| JUMP4, JUMP5 | L, L      | This jumper sets the address for the USB board. The only reason to change from the default setting is if multiple boards are being used.                                                                                                        |
| JUMP9        | 5V        | This jumper selects the voltage of the device under test supply ( $V_{DUT} = 5V$ or $3V$ ). This jumper is typically the only jumper that is changed for most applications.                                                                     |
| JUMP10       | WP ON     | This write protects the firmware EEPROM.                                                                                                                                                                                                        |
| JUMP11       | WP ON     | This write protects the calibration EEPROM                                                                                                                                                                                                      |
| JUMP13       | REG       | Uses the regulator output to generate the $V_{DUT}$ supply. The USB bus can be used as the $V_{DUT}$ supply.                                                                                                                                    |
| JUMP14       | 9V        | Uses the external power (9V as opposed to the bus)                                                                                                                                                                                              |
| JUMP17       | BUS       | While in the BUS position $V_{DUT}$ operation is normal. While in the V <sub>raw</sub> position the $V_{DUT}$ supply is connected to an external source. This configuration allows for any value of $V_{DUT}$ between 3V and 5V. <sup>(1)</sup> |
| JUMP18       | $V_{DUT}$ | Connects the pull-up on GPIO to the $V_{DUT}$ supply or the $V_{CC}$ supply.                                                                                                                                                                    |

<sup>(1)</sup> **CAUTION:** Adjusting outside of this range will damage the EVM.

### 3.7 BUF08832\_Test\_Board Features

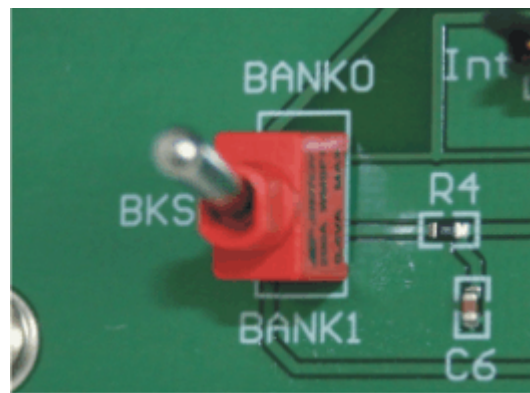
This section describes some of the hardware features present on the BUF08832\_Test\_Board.

#### 3.7.1 JMP1: I<sup>2</sup>C Address Hardware Setting

Jumper JMP1 is used to set the hardware setting for the A0 I<sup>2</sup>C address pin on the BUF08832. Using JMP1, the A0 address can be set to either a logic '1' or a logic '0' to allow for two unique I<sup>2</sup>C addresses. See [Section 5.2.1](#) for more details about how to configure the BUF08832EVM software to match the JMP1 hardware setting.

#### 3.7.2 BKSEL: OTP Bank Selection

The BKSEL switch (illustrated in [Figure 8](#)) located on the BUF08832\_Test\_Board selects the memory bank to be used when operating the EVM. Bank 0 selects the gamma curve that is stored in Bank\_0 of the BUF08832. Bank 1 selects the gamma curve that is stored in Bank\_1 of the BUF08832.



**Figure 8. BKSEL Switch**

#### 3.7.3 JMP2: BKSEL Control Setting

Jumper JMP2 determines how the OTP memory bank selection is controlled. There are two settings JMP2 can be set to. Position INT specifies that control of the BKSEL pin is handled on the BUF08832EVM. For this jumper setting, the BKSEL switch controls whether Bank 0 or Bank 1 OTP is selected.

The EXT position for JMP2 allows for an external control signal connected to terminal T3 to determine the selection of which OTP bank to be used.

#### 3.7.4 JMP3: VSD Control Setting

Jumper JMP3 selects where the BUF08832 digital supply pin is connected. If JMP3 is set in the INT position, the V<sub>SD</sub> pin is connected to the switchable V<sub>DUT</sub> signal generated from the USB\_DIG\_Platform. This voltage can be set to either 3.3V or 5V depending on how JUMP9 on the USB\_DIG\_Platform is set. While JMP3 is set to the INT position, the V<sub>SD</sub> Power button on the BUF08832 software is able to control whether the V<sub>DUT</sub> supply voltage is turned on or off.

When JMP3 is set in the EXT position, an external supply connected to terminal T1 can be used to provide the digital supply voltage for the BUF08832.

#### 3.7.5 JMP4: I<sup>2</sup>C SCK Control Setting

Jumper JMP4 selects where the BUF08832 I<sup>2</sup>C SCL pin is connected. If JMP4 is set in the INT position, the I<sup>2</sup>C clock signal is generated from the I<sup>2</sup>C\_SCK\_ISO signal from the USB\_DIG\_Platform.

When JMP4 is set in the EXT position, an external source connected to SCL pin of terminal T2 can be used to provide the I<sup>2</sup>C SCK signal for the BUF08832.

### 3.7.6 JMP5: I<sup>2</sup>C SDA Control Setting

Jumper JMP5 selects where the BUF08832 I<sup>2</sup>C SDA pin is connected. If JMP5 is set in the INT position, the I<sup>2</sup>C data signal is generated from the I<sup>2</sup>C\_SDA\_ISO signal from the USB\_DIG\_Platform.

When JMP4 is set in the EXT position, an external source connected to SDA pin of terminal T2 can be used to provide the I<sup>2</sup>C SDA signal for the BUF08832.

### 3.7.7 BUF08832 Device Placement

The BUF08832\_Test\_Board allows the user two separate locations on the board where the BUF08832 test device can be installed. The U1 location on the BUF08832\_Test\_Board is a ZIF socket that allows the user to evaluate and program many devices very quickly. One drawback to this socket is that there is no connection to the PowerPAD™ thermal pad of the BUF08832. Because of this drawback, while in this socket, the BUF08832 cannot be operated to its full output capability as a result of thermal dissipation limitations.

The U2 location allows for a BUF08832 device that is soldered down on a DIP adaptor board to be installed on the BUF08832\_Test\_Board. The output capability of the BUF08832 that is soldered to this adaptor board can be fully evaluated. The thermal pad of this soldered BUF08832 is connected correctly allowing the device to dissipate the necessary power while being evaluated. One populated BUF08832 DIP adaptor board is provided with the EVM.

#### CAUTION

Only one location should be populated at a time. The use of both locations simultaneously will likely damage one or both of the devices being tested.

### 3.7.8 Terminal Strip T5

Terminal strip T5 provides the individual channel output signals on a single row of headers as well as a row of vias. This footprint provides the user with multiple options on how to interface the output signals of the BUF08832 with the appropriate display panel or evaluation system. Users can develop a custom cable to connect the headers directly to their panels or solder directly to the individual vias.

## 4 BUF08832EVM Software Setup

This section discusses how to install the BUF08832 software.

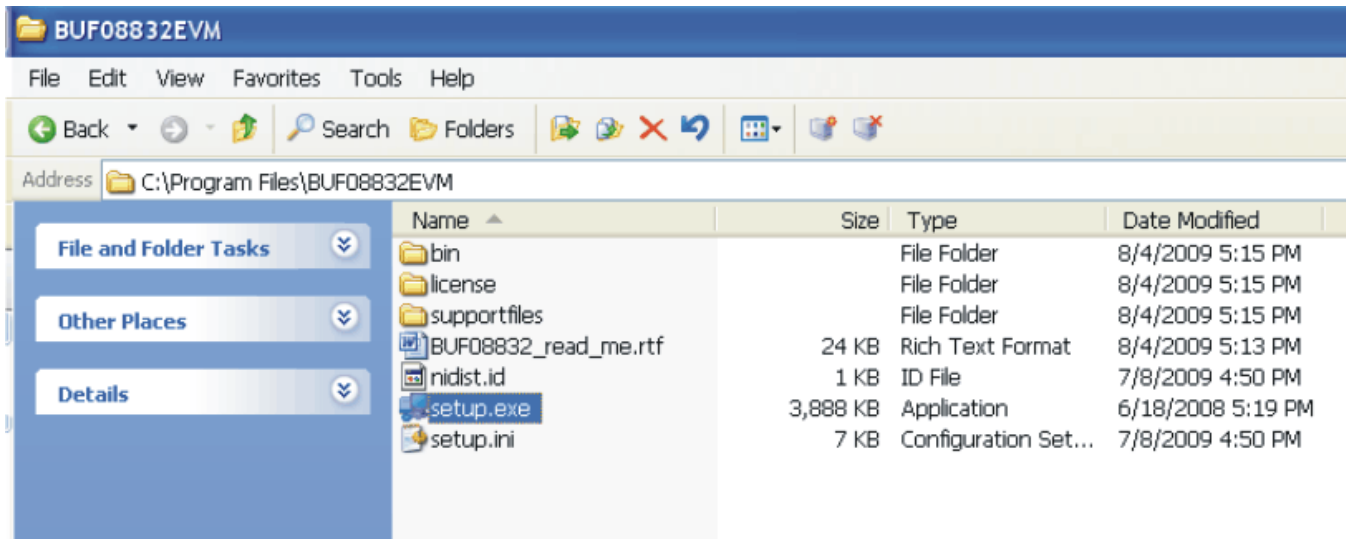
### 4.1 Operating Systems for BUF08832 Software

The BUF08832EVM software has been tested on the Microsoft Windows XP operating system (OS) with United States and European regional settings. The software should also function on other Windows operating systems.

### 4.2 BUF08832EVM Software Installation

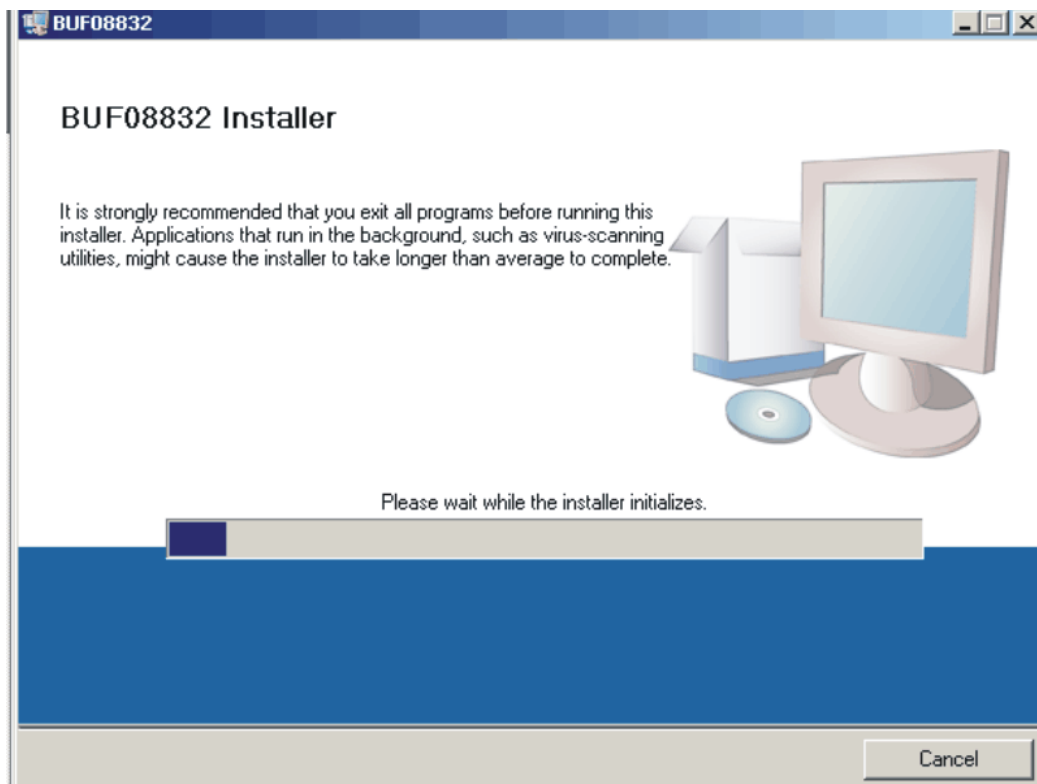
The BUF08832EVM software is included on the CD that is shipped with the EVM kit. It is also available through the [BUF08832EVM product folder](#) on the TI web site. To download the software to your system, insert the disc into an available CD-ROM drive. Navigate to the drive contents and open the BUF08832EVM software folder. Locate the compressed file (*BUF08832EVM.zip*) and open it. Using WinZIP® or a similar file compression program, extract the BUF08832EVM files into a specific BUF08832 folder (for example, C:\BUF08832) on your hard drive.

Once the files are extracted, navigate to the BUF08832 folder that you created on your hard drive. Locate the *setup.exe* file; then click the file to start the installation process, as shown in [Figure 9](#).



**Figure 9. BUF08832EVM Software Installation**

The BUF08832 software installer file then opens to begin the installation process, as [Figure 10](#) shows.



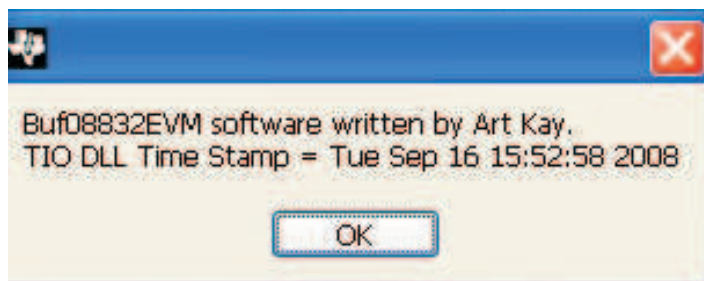
**Figure 10. BUF08832EVM Software Install Window**



After the installer has begun, the user is given the choice of where to install the program on the PC. Following this option, two license agreements are presented that must be accepted. After accepting the Texas Instruments and National Instruments license agreements, the progress bar opens and shows the installation of the software. At the completion of the software installation, a *Read Me* file opens, showing the hardware that is provided with the BUF08832EVM kit. Click the **Finish** button to complete the installation procedure.

### 4.3 Software Description and Set-Up

The BUF08832EVM software allows the user to read and write to all registers in the BUF08832 gamma correction buffer. Furthermore, it allows programming of the OTP register on the BUF08832. The software also permits the user to select either I<sup>2</sup>C address. Press the **About** button as shown in [Figure 11](#) to verify that you have the latest version of the software.



**Figure 11. BUF08832EVM Software About Button**

## 5 BUF08832EVM Software Overview

This section discusses how to install the BUF08832 software.

### 5.1 Starting the BUF08832EVM Software

The BUF08832 software can be operated through the Windows *Start* menu. From *Start*, select *All Programs*; then select the BUF08832EVM program. Figure 12 shows how the software should appear if the EVM is functioning properly.

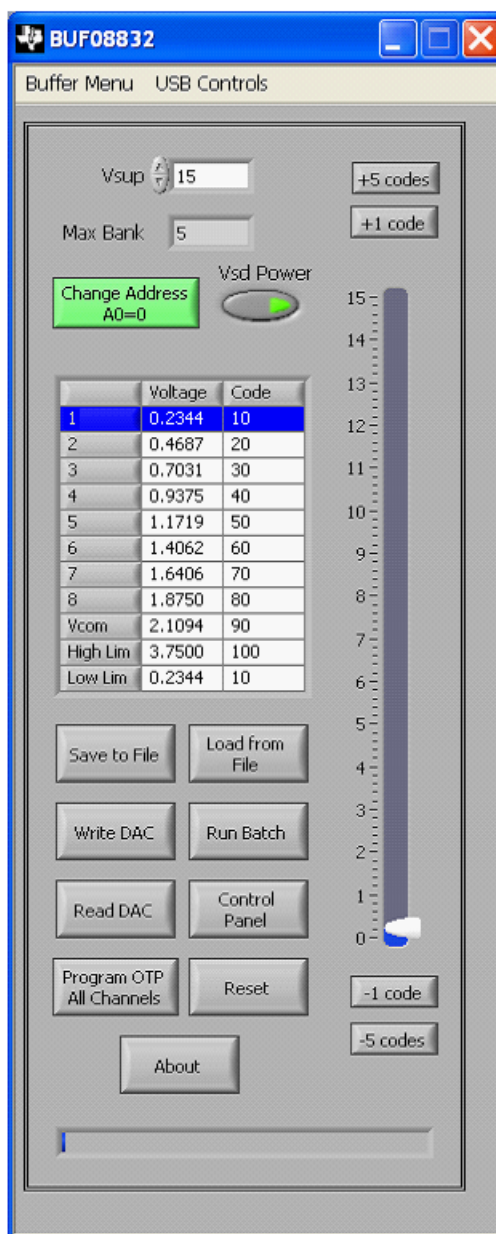
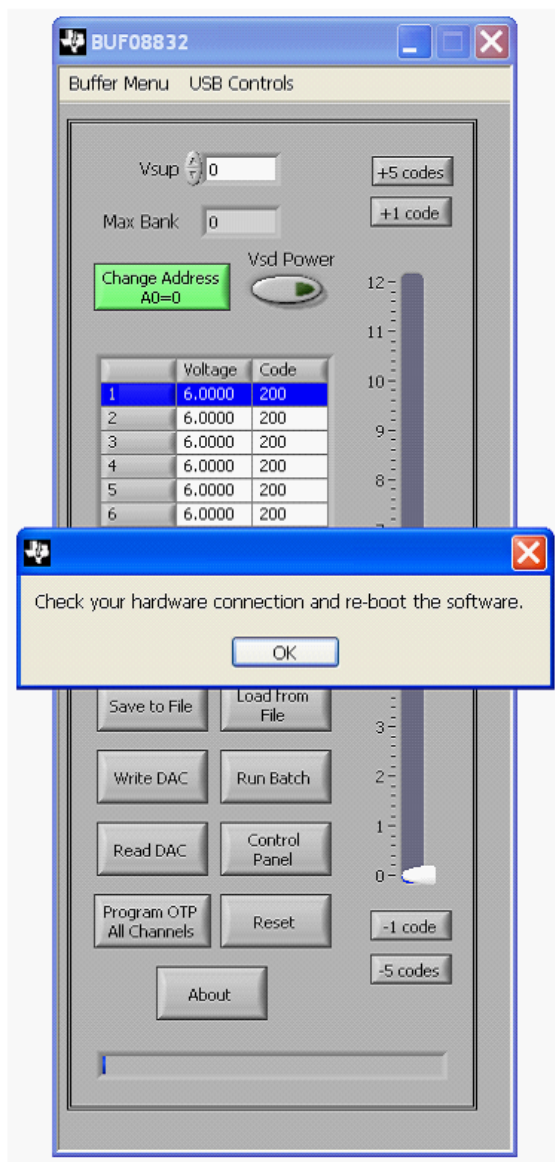


Figure 12. BUF08832EVM Software Functioning Properly

Figure 13 shows an error that pops up if the computer cannot communicate with the EVM. If you receive this error, first check to see that the USB cable is properly connected. This error can also occur if you connect the USB cable before the USB DIG Platform 9V power source. A second possible reason for this problem is that there may be a problem with your computer USB human interface device driver. Make sure that when you plug the in the USB cable, the computer recognizes the device. If the sound is on, you will hear the distinctive sound that you expect when a USB device is properly connected to the PC.

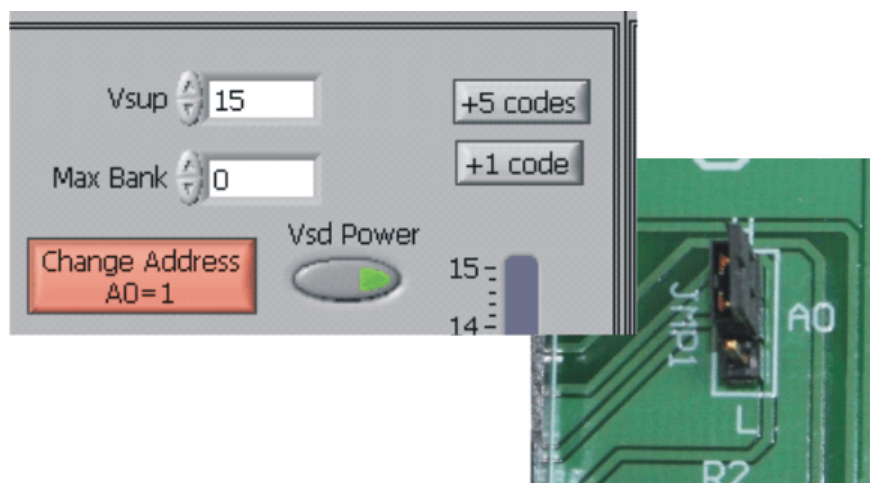


**Figure 13. BUF08832EVM Software: No Communication with the USB\_DIG\_Platform**

## 5.2 Using the BUF08832 Software

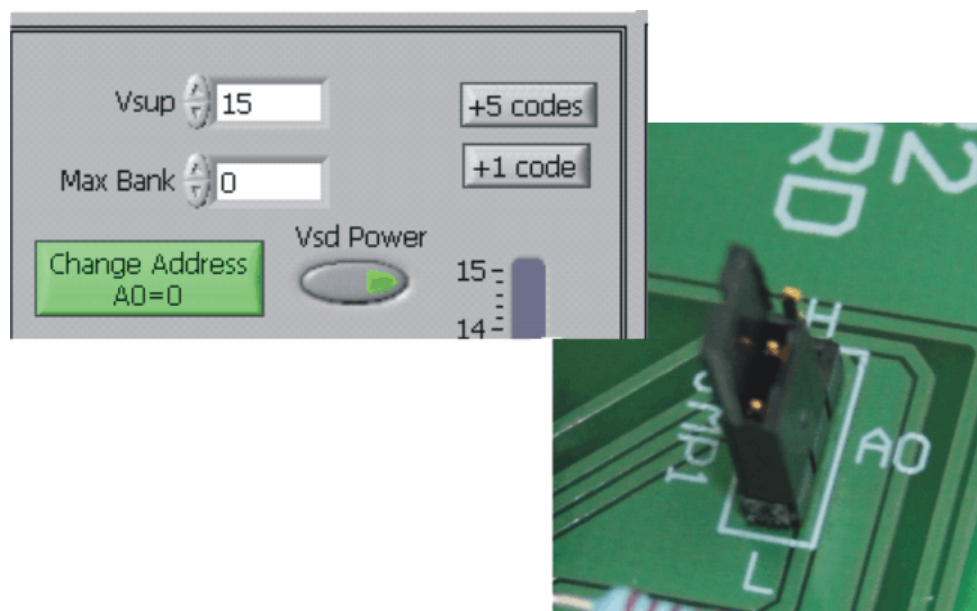
### 5.2.1 I<sup>2</sup>C Address Selection

As mentioned previously in the *BUF08832\_Test\_Board Features* section (see [Section 3.7](#)), jumper JMP1 is used to set the I<sup>2</sup>C address pin of the BUF08832. [Figure 14](#) shows how the hardware and software must both be set to allow for communication between the BUF08832EVM and the software. Without jumper JMP1 and the software address button configured correctly, the software will not be able to communicate with the BUF08832 device.



**Figure 14. BUF08832\_Test\_Board Jumper JMP1 Set For Logic '1'**

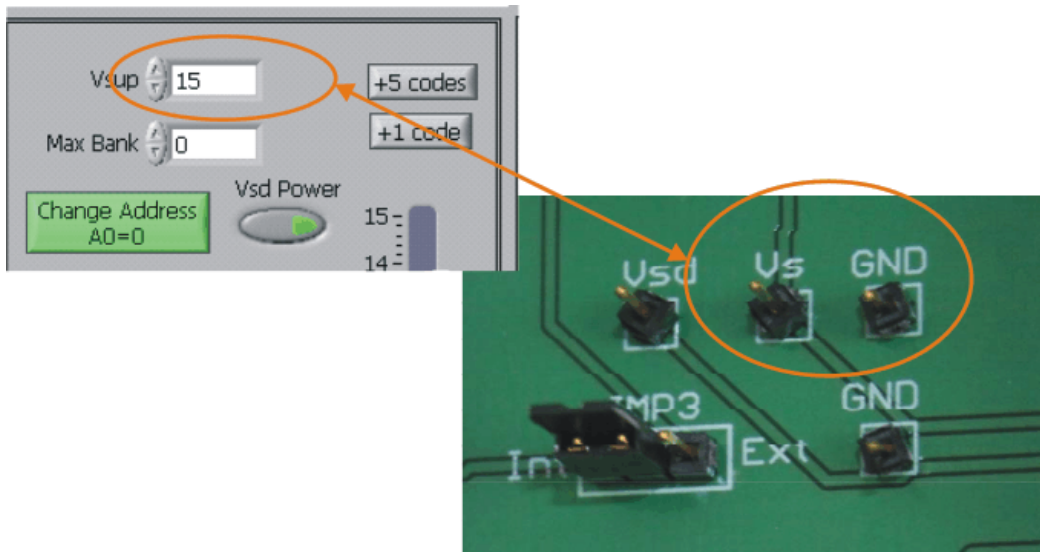
When JMP1 and the software are set as shown in [Figure 15](#), the second I<sup>2</sup>C address can be configured.



**Figure 15. BUF08832\_Test\_Board Jumper JMP1 Set For Logic '0'**

## 5.2.2 Measuring the Power Supply

You must measure the power supply ( $V_S$ ) with respect to the GND on the BUF08832\_Test\_Board and enter it in the  $V_{SUP}$  field located in the top section of the software interface, as shown in Figure 16.



**Figure 16. Measuring and Entering Power-Supply Voltage**

The voltage out of each DAC is calculated according to the  $V_S$  value entered. For example, changing the value in the channel 6 cell as shown below immediately changes the output of channel 6 to 0.996V. The calculation is performed according to Equation 1.

$$V_{DAC\_CHANNEL} = \frac{V_S \times \text{Code\_in\_Decimal}}{1024} \quad (1)$$

### Example 1.

Channel 6: Code 44 (hexadecimal) = 68 (decimal)

$$V_{DAC\_CHANNEL} = \frac{15V \times 68}{1024} = 0.996V$$

### 5.2.3 Read DAC Button

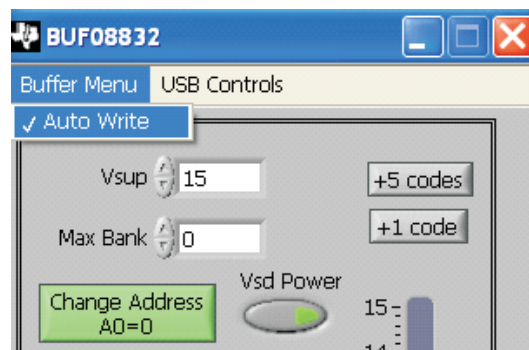
By pressing the **Read DAC** button in the BUF08832EVM software, all of the BUF08832 DAC/V<sub>COM</sub> registers are read to obtain the respective current register contents. Once the read procedure is complete, all of the corresponding text boxes are updated to show the current values present in the DAC/V<sub>COM</sub> registers.

### 5.2.4 Write DAC Button

The method used to write the values in the DAC/V<sub>COM</sub> registers is based on whether or not the Auto Write feature is enabled. The BUF08832 has two methods of writing information into the DAC/V<sub>COM</sub> registers. The first method allows for the output voltage to change immediately after the writing to the DAC register. In the BUF08832EVM software, this mode is configured by enabling the Auto Write feature found in the Buffer Menu dropdown menu. In this mode, as an individual channel is written to, the output voltage changes as soon as the user moves to a different text box in the software. The second method of writing to the DAC/V<sub>COM</sub> registers allows for the user to write multiple channels and then have all of the output voltages change at the same time rather than each channel voltage changing as soon as it is written to.

Disabling the Auto Write feature in the software allows the user to enter all of the values desired for all of the channels and then press the **Write DAC** button to change all of the output voltage of all of the channels at one time. When the Auto Write feature is enabled, no change occurs to the output voltages when the **Write DAC** button is pressed. No change occurs because after the text box for a given channel has been updated, as soon as another item in the software is clicked, the Auto Write feature automatically performs a write command to the updated channel that then updates the output voltage. When in the Auto Write enabled mode, the **Write DAC** button cannot be pressed with different data in the corresponding channel text boxes than the values already stored in the DAC/V<sub>COM</sub> register; thus, no change occurs.

[Figure 17](#) shows the location in the Buffer Menu showing the Auto Write feature enabled. Clicking on the Auto Write feature again enables/disables the feature, depending on its current state.



**Figure 17. Auto Write Feature Enabled**



### 5.2.5 Reset Button

Pressing the **Reset** button in the BUF08832EVM software calls a General-Call Reset for the BUF08832. The status of the DAC/ $V_{COM}$  registers after the General-Call Reset depends on whether the OTP has been programmed or not. If the OTP has been programmed, the channel registers will be loaded with the most recent values programmed into the OTP memory. If the OTP memory has not been programmed, the channel registers will default to 1000000000, or midsupply.

Pressing the **Reset** button does not generate a Read DAC call, so the corresponding channels are not updated. The **Read DAC** button must be pressed in order to update the text boxes to the respective current corresponding values.

### 5.2.6 Save to File Button

The register configurations of the BUF08832 DACs are displayed in both analog voltage and in hexadecimal (see [Figure 12](#)). The DAC codes (that is, gamma voltages) can be saved into a text file using the **Save to File** button.

Pressing the **Save to File** button opens a file-save dialog box similar to that shown in [Figure 18](#). Pressing the folder icon creates a new folder on your PC. It is a good idea to create a directory exclusively for BUF08832 DAC code (that is, gamma voltage) files. Enter a unique file name in the *Filename* field to store your BUF08832 register information. Press the **OK** button to save the file.

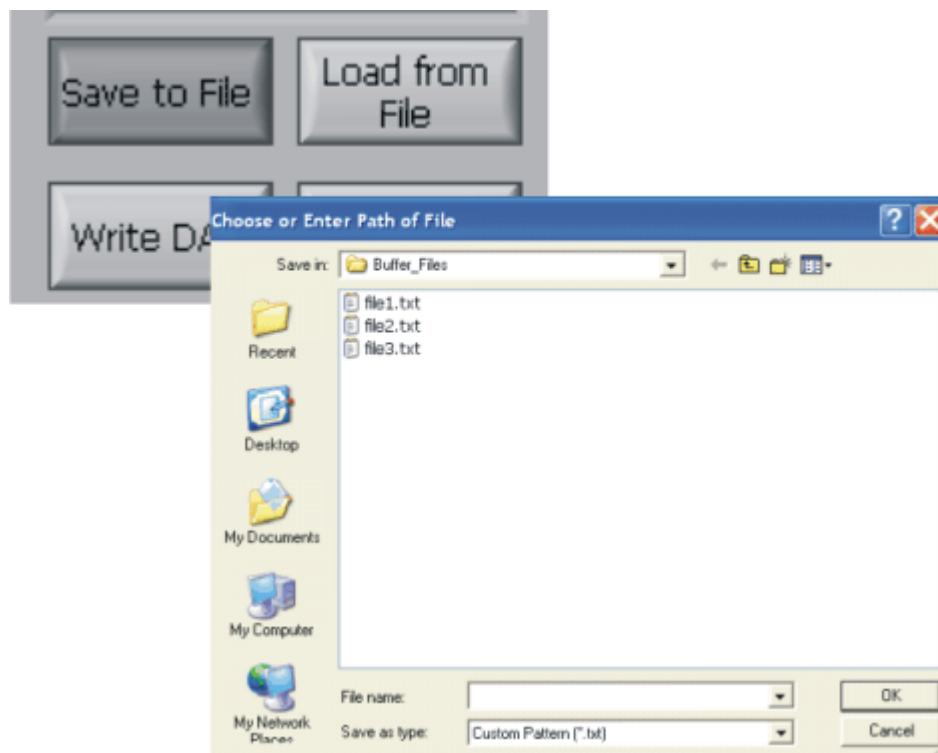


Figure 18. Save to File Dialog Box Button and Window

Saved BUF08832 DAC codes (gamma voltages) exist in a text file that can be opened in a text editor, as [Figure 19](#) illustrates.

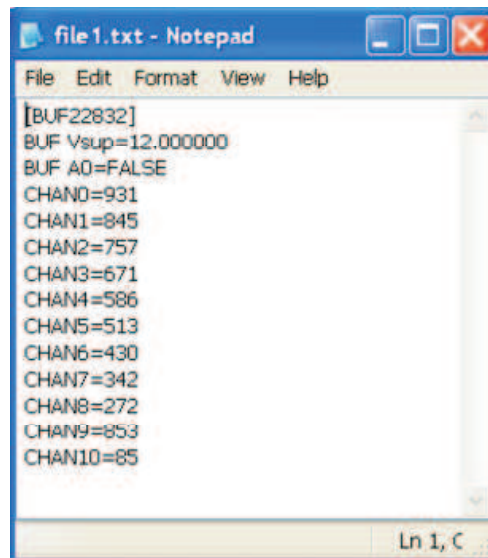


Figure 19. File Format of Saved Data

### 5.2.7 Load From File Button

The BUF08832EVM software is also able to load data saved from previous evaluations. A saved register configuration can be loaded into the BUF08832 using the **Load From File** button, as shown in [Figure 20](#). The program remembers where you saved the last register configuration. Simply select the desired configuration and press *Open*.

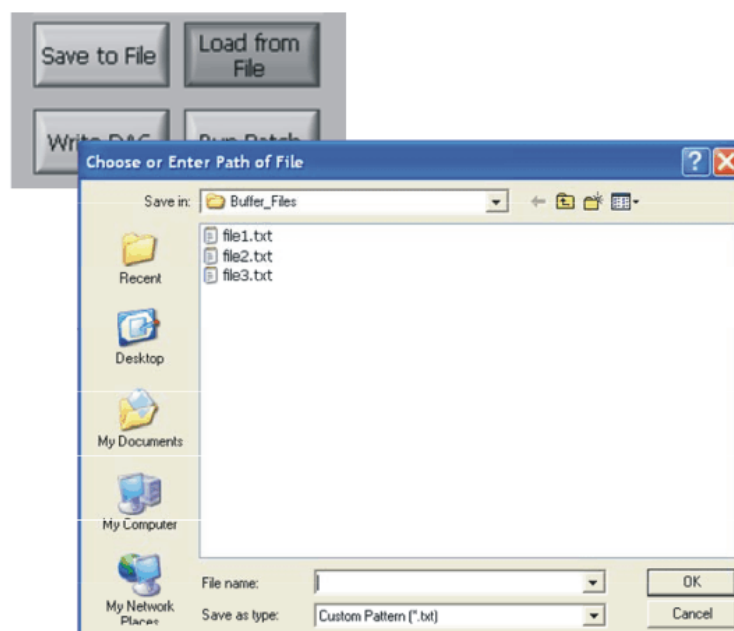


Figure 20. Load From File Button and Window

## 5.2.8 Changing the DAC/V<sub>COM</sub> Analog Voltage

The voltage of any of the DAC or V<sub>COM</sub> channels can be adjusted in several ways. First, you can change the voltage by entering the desired voltage directly in the voltage text box. In order to be able to manually type the voltage into the text box, you must first click on the cell to be edited. Click a second time and the cell turns from blue to black, and allows the user to type the updated voltage in the cell. The hexadecimal DAC codes can be entered in the *Code* column in the same manner.

Another method of changing the voltage of a DAC or V<sub>COM</sub> channel is through the use of the slider on the main software window. There is only a single slider that is used for all channels. In order to use the slider to adjust the voltage of a particular channel, that channel must first be selected. To select a channel, click on either the channel number, voltage, or code of a particular channel. The entire channel row highlights in blue to show the user that the channel is selected. Adjusting the slider bar then only updates the highlighted channel.

The final method to change DAC/V<sub>COM</sub> voltages is through the **±1 Code** and **±5 Code** buttons on the main software window. These buttons allow for fine and coarse adjustments, respectively, to the highlighted channel, giving the user the ability to quickly step the channel output up or down as needed without having to manually enter the changes in the *Code* column.

## 5.2.9 Run Batch Button

The **Run Batch** button (as noted in [Figure 21](#)) enables the user to configure the BUF08832 to cycle through different register configurations in a continuous loop. When connected to the end application, this feature can be used to cycle through different gamma settings to determine what the optimal settings must be for a given application.

When the **Run Batch** button is pressed, a new dialog box displays as [Figure 21](#) shows. The delay time is the amount of time allowed between loading new configurations into the BUF08832 DUT.

Use the **Single Step Up** and **Single Step Down** buttons to step through the selected files manually. The currently selected file name is displayed in the lower left corner area of the dialog box. Double-click on the file names to select them. Once a series of filenames have been selected, the check box turns dark. Double-click on a filename again to unselect it from the batch run.

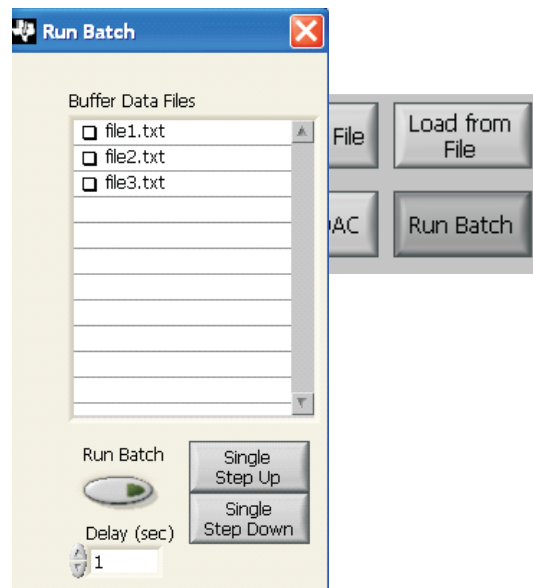


Figure 21. Run Batch Dialog Button and Window

### 5.2.10 Control Panel Button

Pressing the **Control Panel** button brings up a display panel that allows you to adjust each channel using a set of graphical sliders, as shown in [Figure 22](#). Simply drag the slider to adjust the desired channel output. The DAC code and corresponding output value of each channel change automatically. This function is similar to the slider present on the primary BUF08832EVM software window that changes based on the channel that highlighted (as discussed in the [above section](#)).

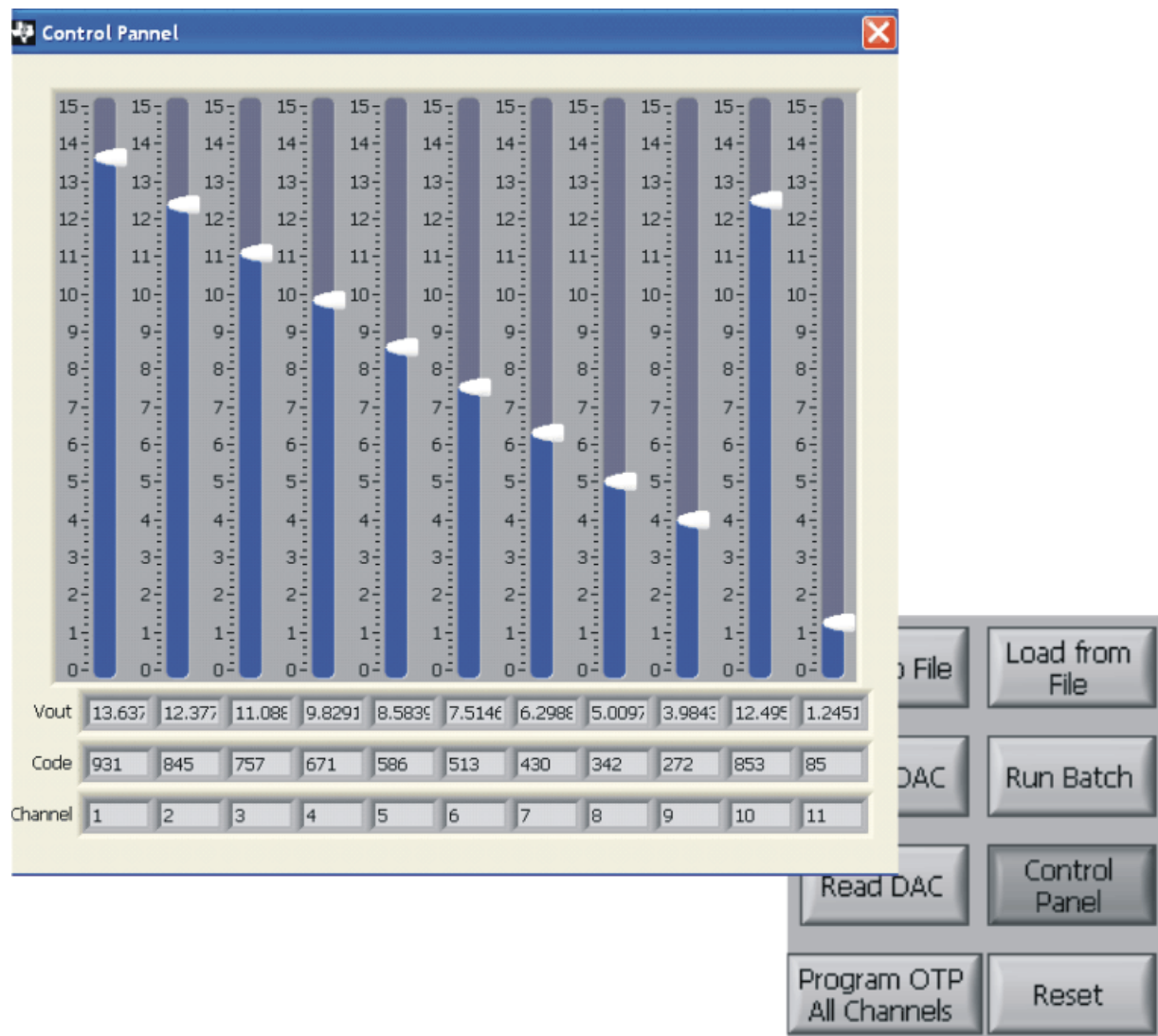


Figure 22. Control Panel Button and Window

## 5.2.11 Program OTP All Channels Button

As Figure 23 shows, pressing the **Program OTP All Channels** button allows you to program a gamma curve into the nonvolatile memory in the BUF08832. All eight channels (including the  $V_{COM}$  channels) are then programmed simultaneously. The values are stored in the memory bank that is selected via the BKSEL switch (see Section 3.7.2).

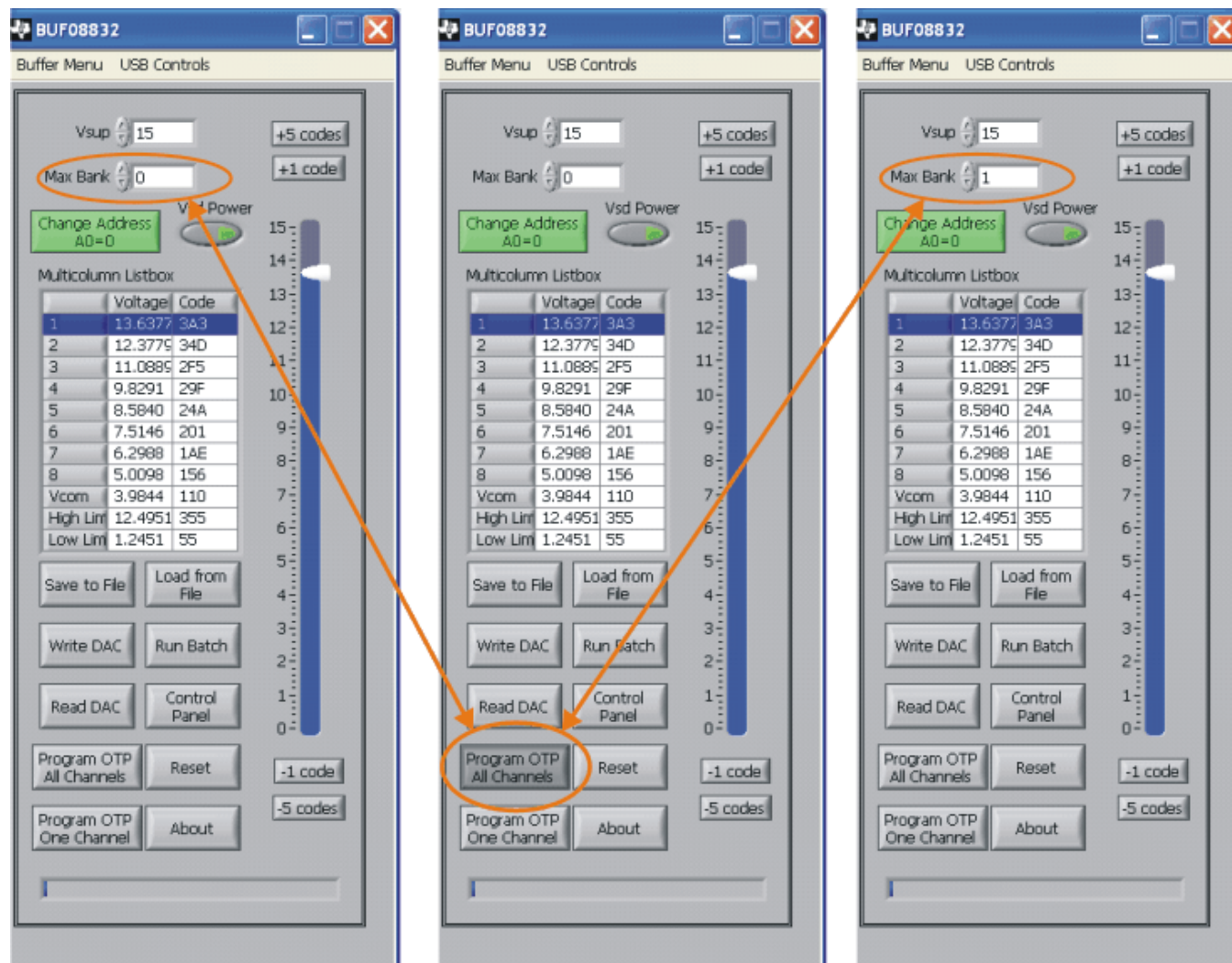
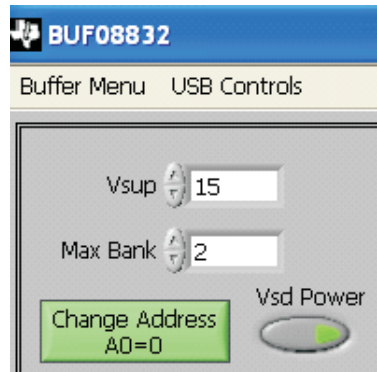


Figure 23. Program OTP All Channels Button

### 5.2.12 Max Bank Field

The Max Bank field at the top of the software interface (as shown in [Figure 24](#)) shows how many times the memory of the most-programmed channel of the selected memory bank has been previously written to.

- None: Max bank shows 0
- Once: Max Bank shows 0
- Twice: Max bank shows 1
- Three times: Max bank shows 2
- 16 times: Max bank shows 15



**Figure 24. Max Bank Field**

## 6 BUF08832EVM Documentation

This section contains the complete bill of materials and schematic diagram for the BUF08832\_Test\_Board. Documentation information for the USB\_DIG\_Platform can be found in the USB\_DIG\_Platform User's Guide, SBOU058, available at the TI web site at <http://www.ti.com>.



## 6.1 BUF08832\_Test\_Board Schematic

Figure 25 shows the schematic for the BUF08832\_Test\_Board.

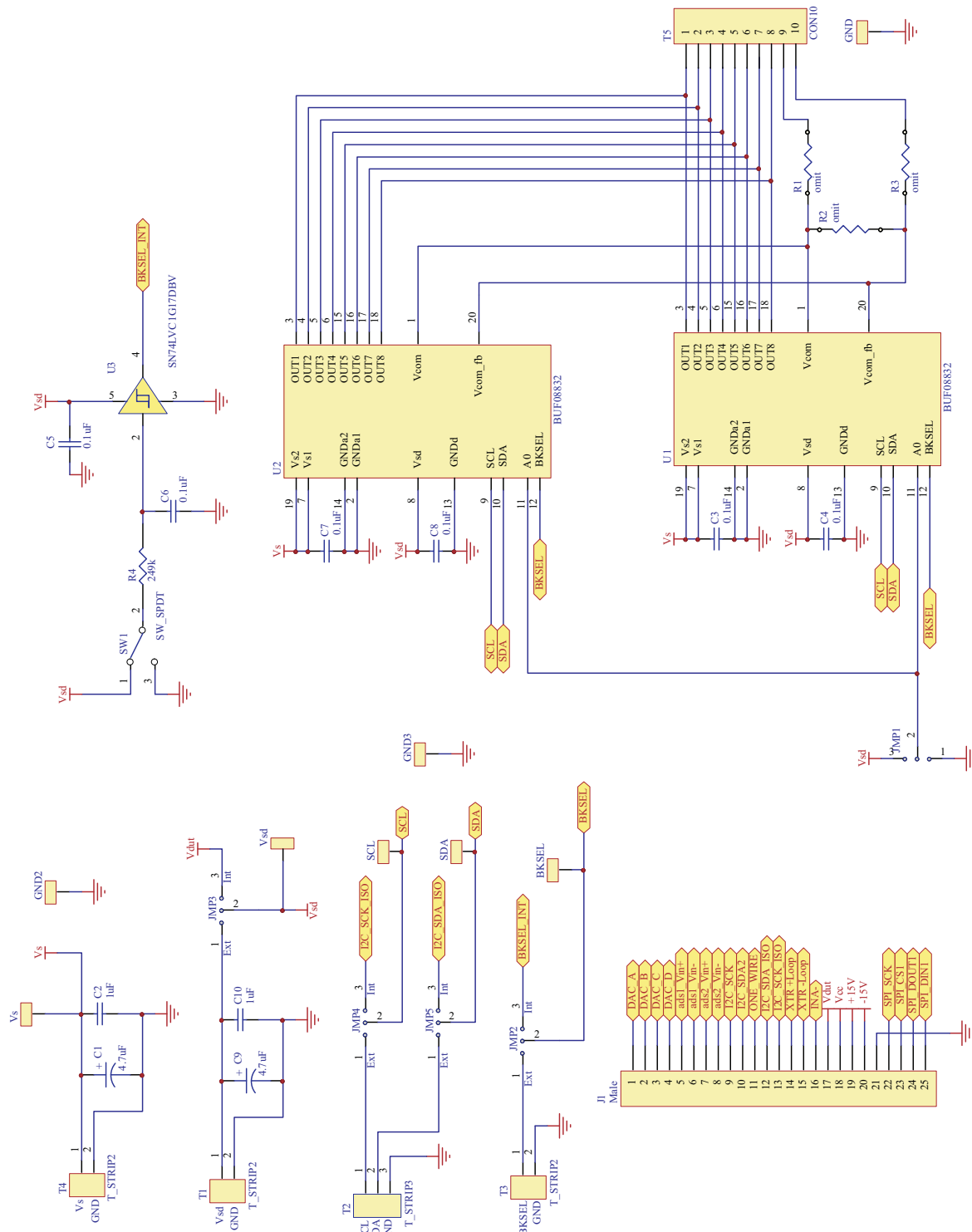


Figure 25. BUF08832\_Test\_Board Schematic

## 6.2 BUF08832\_Test\_Board Bill of Materials

Table 4 lists the bill of materials for this EVM.

**Table 4. BUF08832\_Test\_Board Bill of Materials**

| No. | Qty | Value             | Ref Des          | Description                                                                       | Vendor                           | Part number        |
|-----|-----|-------------------|------------------|-----------------------------------------------------------------------------------|----------------------------------|--------------------|
| 1   | 1   | 34Ω               | R1               | RES 34.0Ω 1% 50PPM 1/4W See Assembly Drawing                                      | Vishay/Dale                      | CMF5034R000FHEB    |
| 2   | 1   | 1.2kΩ             | R2               | RES 1.21kΩ 1% 50PPM 1/4W See Assembly Drawing                                     | Vishay/Dale                      | CMF501K2100FHEB    |
| 3   | 1   | 150Ω              | R3               | RES 150Ω 1% 50PPM 1/4W See Assembly Drawing                                       | Vishay/Dale                      | CMF50150R00FHEB    |
| 4   | 1   | 249kΩ             | R4               | RES 249kΩ 1/16W .5% 0603 SMD                                                      | Susumu Co Ltd                    | RR0816P-2493-D-39D |
| 5   | 2   | 4.7μF             | C1, C9           | CAP TANT 4.7μF 35V 10% SMD                                                        | Vishay/Sprague                   | 293D475X9035C2TE3  |
| 6   | 2   | 1μF               | C2, C10          | CAP CER 1 μF 25V Y5V 0603                                                         | Murata Electronics North America | GRM188F51E105ZA12D |
| 7   | 6   | 0.1μF             | C3-C8            | CAP .10μF 25V CERAMIC Y5V 0603                                                    | Kemet                            | C0603C104Z3VACTU   |
| 8   | 1   |                   | U1               | Socket, TSSOP 28-Pin ZIF                                                          | ENPLAS                           | OTS-20(28)-0.65-01 |
| 9   | 2   |                   | U2               | CONN RCPT .100" 10POS GOLD T/H                                                    | Samtec Inc                       | SS-110-G-2         |
| 10  | 1   |                   | U3               | IC BUFFER SCHMIT TRIG SOT235                                                      | Texas Instruments                | SN74LVC1G17DBVR    |
| 11  | 1   | DSUB25M           | J1               | CONN D-SUB PLUG R/A 25POS 30GOLD (With Threaded Inserts and Board locks)          | AMP/Tyco Electronics             | 5747842-4          |
| 12  | 1   |                   | S1               | SWITCH TOGGLE SPDT .4VA PC MNT                                                    | E-Switch                         | 200AWMSP1T1A1M2RE  |
| 13  | 3   |                   | T1, T3, T4       | TERM BLOCK .2 IN 2 POS PCB                                                        | Tyco Electronics                 | 1437671-1          |
| 14  | 1   |                   | T2               | TERM BLOCK 3POS 5.08MM SCREWLESS                                                  | Tyco Electronics                 | 1437671-4          |
| 15  | 1   | T5 Cut to size    | T5               | CONN HEADER 10POS .100" SGL GOLD                                                  | Samtec                           | TSW-132-07-G-S     |
| 16  | 6   |                   | Pin Socket (U1)  | Pin SOCKET RCPT .014-.026 30AU (R1,R2,R3)                                         | AMP                              | 5050863-5          |
| 17  | 8   | TP cut to size    | Test Points, All | CONN HEADER 1POS .100" SGL GOLD                                                   | Samtec                           | TSW-132-07-G-S     |
| 18  | 4   | Standoff          | —                | Standoffs, Hex , 4-40 Threaded, 0.500" length, 0.250" OD, Aluminum Iridite Finish | Keystone                         | 2203               |
| 19  | 4   | Screw             | —                | SCREW MACHINE PHIL 4-40X1/4 SS                                                    | Building Fasteners               | PMSSS 440 0025 PH  |
| 20  | 5   | JUMP3 cut to size | JMP1-JMP5        | CONN HEADER 3POS .100" SGL GOLD                                                   | Samtec                           | TSW-132-07-G-S     |
| 21  | 5   |                   | N/A              | SHUNT LP W/HANDLE 2 POS 30AU                                                      | AMP/Tyco Electronics             | 881545-2           |
| 22  | 1   | BUF08832          | U1               | IC CURR/PWR MON BI-DIR MSOP-10                                                    | Texas Instruments                | BUF08832AIDGS      |

### Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Original (November 2009) to A Revision                         | Page |
|-----------------------------------------------------------------------------|------|
| • Changed power supply in the <i>BUF08832EVM Kit Contents</i> section. .... | 2    |

## STANDARD TERMS AND CONDITIONS FOR EVALUATION MODULES

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- 3 *Regulatory Notices:*

- 3.1 *United States*

### 3.1.1 *Notice applicable to EVMs not FCC-Approved:*

This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

### 3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

#### **CAUTION**

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

#### **FCC Interference Statement for Class A EVM devices**

*NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.*

## FCC Interference Statement for Class B EVM devices

*NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:*

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

## 3.2 Canada

### 3.2.1 For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210

#### Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

#### Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

#### Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

#### Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

## 3.3 Japan

3.3.1 *Notice for EVMs delivered in Japan:* Please see [http://www.tij.co.jp/llds/ti\\_ja/general/eStore/notice\\_01.page](http://www.tij.co.jp/llds/ti_ja/general/eStore/notice_01.page) 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。  
[http://www.tij.co.jp/llds/ti\\_ja/general/eStore/notice\\_01.page](http://www.tij.co.jp/llds/ti_ja/general/eStore/notice_01.page)

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required by Radio Law of Japan to follow the instructions below with respect to EVMs:

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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#### 4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

##### 4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

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