



TMP144 Low-Power, Digital Temperature Sensor With SMAART Wire™ / UART Interface

1 Features

- Multiple Device Access (MDA):
 - Global Read/Write Operations
- SMAART Wire™ / UART interface
- Resolution: 12-Bit or 0.0625°C
- ±1°C Maximum (–10°C to +100°C)
- ±2°C Maximum (–40°C to +125°C)
- Low Quiescent Current:
 - 3-μA Active I_Q at 0.25 Hz
 - 1-μA Shutdown
- Supply Range: 1.4 V to 3.6 V
- Push-Pull Digital Output
- Package: 0.76 mm × 0.96 mm (±0.03 mm) 4-Ball YFF (DSBGA)

2 Applications

- Handsets
- Smartphones
- Tablets
- LED Backlighting
- HDTVs
- Enterprise Servers
- Notebooks
- Medical

3 Description

The TMP144 digital output temperature sensor can read temperatures to a resolution of 0.0625°C.

The device has a SMAART wire™ / UART interface that supports daisy-chain configurations. The interface also supports multiple device access (MDA) commands that let the master communicate with multiple devices on the bus simultaneously. MDA commands are used as an alternative to sending individual commands to each device on the bus. Up to 16 TMP144 devices can be attached together in parallel and can be easily read by the host computer.

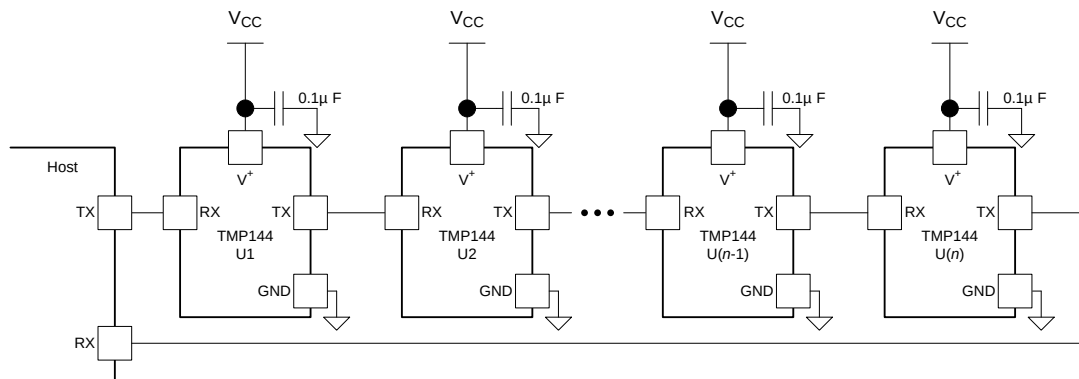
The TMP144 device is designed for space-constrained, power-sensitive applications with multiple temperature measurement zones that must be monitored. The device is specified for operation over a temperature range of –40°C to 125°C and is available in a four-ball wafer chip-scale package (DSBGA).

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TMP144	DSBGA (4)	0.76 mm x 0.96 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Application



Up to 16 TMP144 devices can be configured as a daisy-chain. (See also [Device Nomenclature](#))



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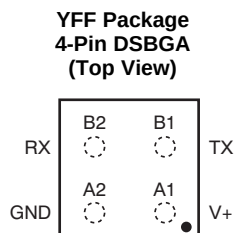
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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
October 2018	*	Initial release.

5 Pin Configuration and Functions



Pin Functions

PIN		I/O ⁽¹⁾	DESCRIPTION
NAME	NO.		
GND	A2	G	Ground
RX	B2	I	Serial data input pin
TX	B1	O	Serial data output pin (push-pull output)
V+	A1	I	Supply voltage 1.4 V to 3.6 V

(1) I = Input, O = Output, G = Ground

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

	MIN	MAX	UNIT
Supply voltage	−0.3	3.6	V
Input voltage	−0.3	(V+) + 0.3	V
Operating junction temperature, T _J	−55	150	°C
Storage temperature, T _{stg}	−60	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD) Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage, V+	1.4	3.3	3.6	V
Operating temperature, T _A	−40		125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TMP144	UNIT
		YFF (DSBGA)	
		4 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	188.5	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	2.1	°C/W
R _{θJB}	Junction-to-board thermal resistance	35.1	°C/W
ψ _{JT}	Junction-to-top characterization parameter	10.6	°C/W
ψ _{JB}	Junction-to-board characterization parameter	35.1	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

$T_A = -40^{\circ}\text{C}$ to 125°C and $V_+ = +1.4\text{ V}$ to $+3.6\text{ V}$ (unless otherwise noted). Typical values at $T_A = 25^{\circ}\text{C}$ and $V_+ = 3.3\text{ V}$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TEMPERATURE INPUT						
Temperature accuracy (error)		$V_+ = 3.3\text{ V}, -10^{\circ}\text{C} \leq T_A \leq 100^{\circ}\text{C}$		± 0.5	± 1	$^{\circ}\text{C}$
		$V_+ = 1.4\text{ V to } 3.6\text{ V}, -40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$		± 1	± 2.0	$^{\circ}\text{C}$
Temperature resolution (LSB)				0.0625		$^{\circ}\text{C}$
DC power-supply sensitivity				± 0.2	± 0.5	$^{\circ}\text{C/V}$
DIGITAL INPUT/OUTPUT						
V_{IH}	Input logic levels		$0.7 \times (V_+)$	$(V_+) + 0.3$		V
V_{IL}			-0.5	$0.3 \times (V_+)$		V
I_{IN}	Input current	$0 \leq V_{IN} \leq V_{(V_+)} + 0.3\text{ V}$	-1		1	μA
V_{OL}	Output logic levels	$V_+ > 2\text{ V}, I_{OL} = 1\text{ mA}$	0		0.4	V
		$V_+ < 2\text{ V}, I_{OL} = 1\text{ mA}$	0		$0.2 \times V_+$	V
V_{OH}		$V_+ > 2\text{ V}, I_{OH} = 1\text{ mA}$	$(V_+) - 0.4$		V_+	V
		$V_+ < 2\text{ V}, I_{OH} = 1\text{ mA}$	$0.8 \times V_+$		V_+	V
ADC Resolution				12		Bit
Conversion time				26	35	ms
Conversion modes		CR1 = 0, CR0 = 0 (default)		0.25		Conv/s
		CR1 = 0, CR0 = 1		1		Conv/s
		CR1 = 1, CR0 = 0		4		Conv/s
		CR1 = 1, CR0 = 1		8		Conv/s
Timeout time		Interface		28	38	ms
SMAART wire™ / UART interface		Serial baud rate	4.8		114	kbps
POWER SUPPLY						
Operating supply range			1.4		3.6	V
I_Q	Quiescent current	Serial bus inactive, CR1 = 0, CR0 = 0 (default), $V_+ = 3.3\text{ V}$		3	10	μA
		Serial bus active, CR1 = 0, CR0 = 0, $V_+ = 3.3\text{ V}$		53		μA
I_{SD}	Shutdown current	Serial bus inactive, $V_+ = 3.3\text{ V}$		0.6	5	μA
Power-on reset voltage		Supply voltage rising		0.9		V
Power supply ramp		Power-on time			1	ms

6.6 Timing Requirements

		MIN	NOM	MAX	UNIT
Baud rate		4.8		114	kbps
t_R	Clock/data rise time			0.5%	Baud
t_F	Clock/data fall time			0.5%	Baud
Jitter				± 1	Baud



Figure 1. SMAART wire™ / UART Interface Timing Diagram

6.7 Typical Characteristics

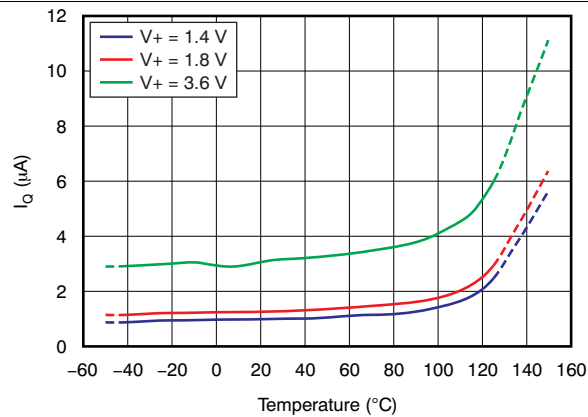


Figure 2. Quiescent Current vs Temperature

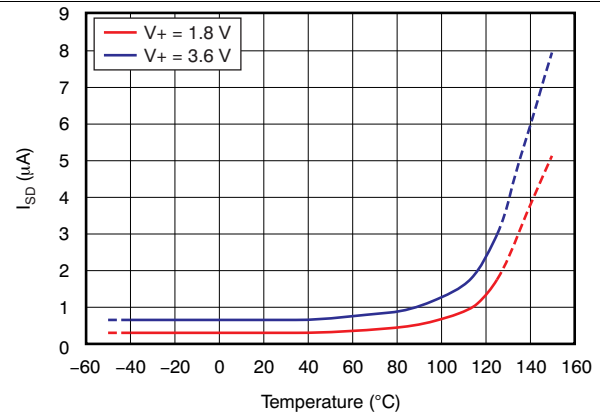


Figure 3. Shutdown Current vs Temperature

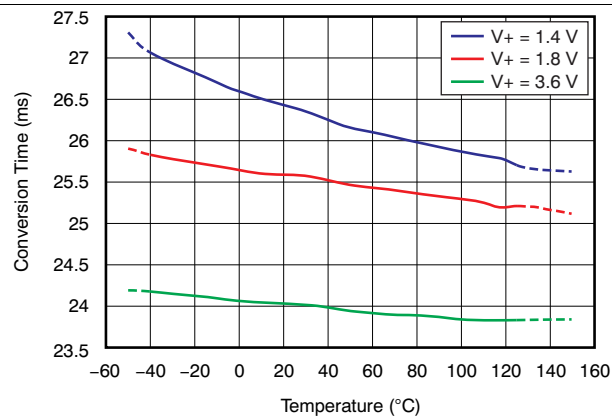


Figure 4. Conversion Time vs Temperature

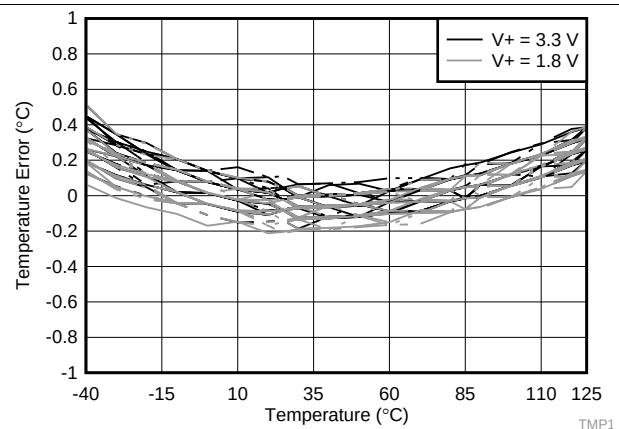


Figure 5. Temperature Error vs Temperature

7 Detailed Description

7.1 Overview

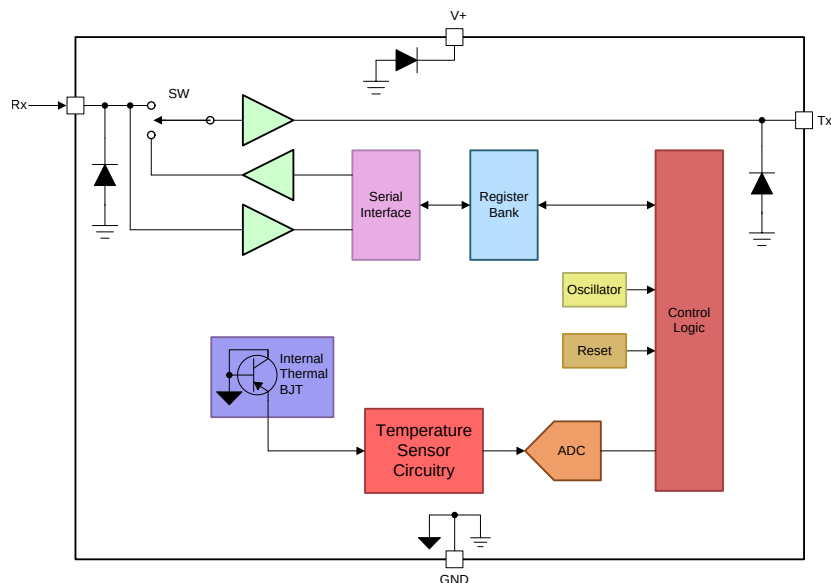
The TMP144 is a digital output temperature sensor in a wafer chip-scale package (WCSP) that is designed for thermal management and thermal profiling. The TMP144 includes a SMAART wire™ / UART interface that can communicate in a daisy-chain with up to 16 devices on a single bus. The interface requires two pins from the host: the first device in the daisy-chain receives data from the host and the last device in the daisy-chain returns data to the host. In addition, the TMP144 can do multiple device access (MDA) commands that allow multiple TMP144 devices to respond to a single global bus command. MDA commands reduce communication time and power in a bus that contains multiple TMP144 devices. The TMP144 is specified over a temperature range of -40°C to 125°C .

The TMP144 can also configure the bus in a transparent mode, where the input from the host is sent directly to the next device in the chain without delay. Additionally, the TMP144 can disconnect the chain and create a serial communication controlled by each TMP144 on the bus, thereby allowing each device to have configurable addressing and interrupt capabilities. The input pin, RX, is a high-impedance node. The output pin, TX, has an internal push-pull output stage that can drive the host to GND or V+.

After an initialization sequence, each device on the bus is programmed with its own interface address that allows it to respond to its own address. The devices can also respond to general commands that permit the user to read or write to all devices on the bus without the need to send individual addresses and commands to each device.

The temperature sensor in the TMP144 is the chip itself. Thermal paths run through the package bumps as well as the package. The lower thermal resistance of metal causes the bumps to provide the primary thermal path. To maintain accuracy in applications that require air or surface temperature measurement, care should be taken to isolate the package from ambient air temperature. A thermally-conductive adhesive can help to achieve accurate surface temperature measurement.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Communication Protocol

Each communication of the SMAART wire™ / UART protocol consists of 12-bit word, transferred least significant bit (LSB) first. Each 12-bit word begins with a *Start* bit that is logic low, and ends with a *Stop* bit that is logic high. By using a Start bit and Stop bit for each 12-bit word, the TMP144 can calibrate each word and keep synchronous communication throughout the process.

Feature Description (continued)

The steps for the SMAART wire™ / UART communication protocol are:

1. The host sends a Start bit to start the communication process.
2. The host sends the calibration byte (55h) to allows the TMP144 to sync to the baud rate of the host.
3. The host sends a Stop bit after the calibration byte.
4. The host sends a second Start bit, followed by the command register byte and a Stop bit.
5. The host sends a third Start bit, followed by the data byte.
6. The master will either send the data byte if the instruction is a write command, or the TMP144 will break the chain and send the data byte if the instruction is a read command.
7. The host sends a Stop bit to finish the process.

The sequence is shown in [Table 1](#) and [Figure 6](#).

Table 1. Communication Format

Start bit	Calibration	Stop bit	Start bit	Command byte	Stop bit	Start bit	Data byte	Stop bit
-----------	-------------	----------	-----------	--------------	----------	-----------	-----------	----------

When the ETM bit is set to 0, any writes to the EM bit will be ignored. Reads from the EM bit will always reflect the value of the EM bit regardless of the ETM bit condition.

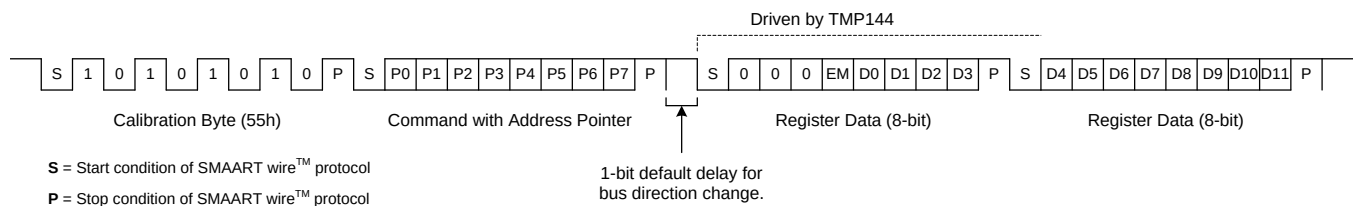


Figure 6. Generic Communication Bitstream

The TMP144 has two dedicated pins for communication: TX and RX. Usually, these two pins are connected internally and the signal on the RX propagates to the TX (that is, the TMP144 works in a transparent mode). The TMP144 breaks this buffer configuration only when the device must send data on the bus or during address assignment and alert procedures.

The TMP144 supports unique *address assignment* and *alert interrupt* procedures. There are general-call read and write commands that allow simultaneous reads or writes to all devices in the daisy-chain. The interface has built-in time outs (typically 28 ms) that return the interface to a known state if communication is disrupted.

7.3.2 Global Initialization and Address Assignment Sequence

At device power-up, every TMP144 in the daisy-chain is connected in transparent mode, as shown in [Figure 7](#). The host must send the initialization command (P7-P0 = 10001100) for the bus to program its internal address, depending on the number of devices on the bus.

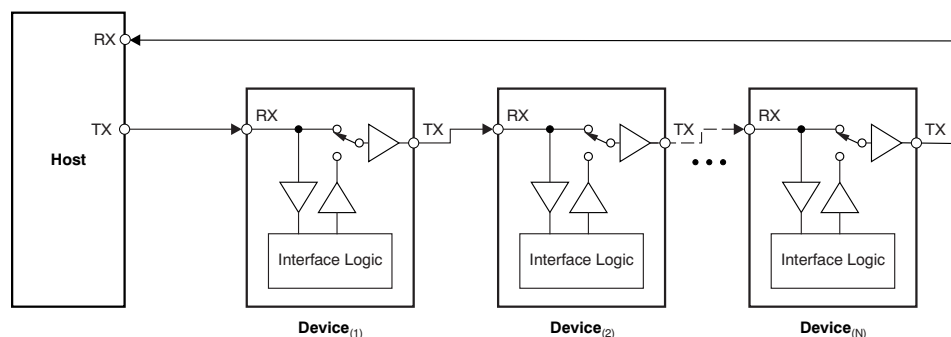


Figure 7. TMP144 Daisy-Chain: Bus Status at Start of Global Initialization

Each TMP144 in the chain interprets the initialization command byte and disconnects the chain, as shown in Figure 8. The host must then send the address assignment command, consisting of P7-P4 = 1001 and P3-P0 = 0000, where P3-P0 represents the address of the first device in the chain. This word is stored internally as its device ID. The first device increments the unit in the device address and then reconnects the bus, as shown in Figure 9. This address is then sent to the next device in the chain. After all devices on the chain have received the respective addresses, the host receives the last programmed address on the chain + 1. The host can use this information to determine the total number of devices in the chain and the respective address of each device.

After the initialization sequence, every device can be addressed individually or through global commands. This global initialization sequence is a requirement and must be performed before any other communication.

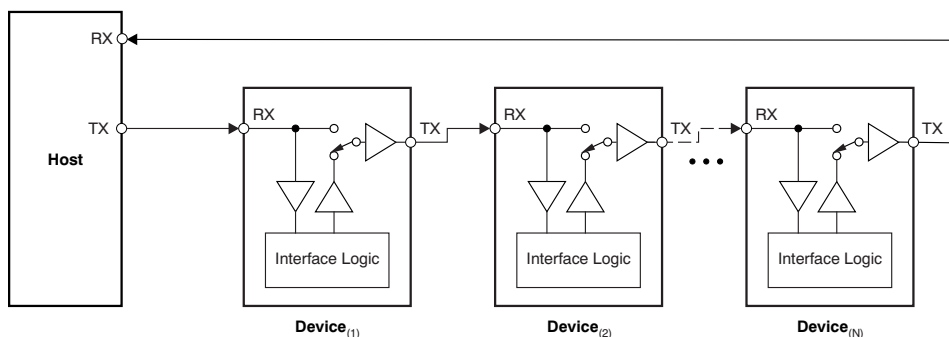


Figure 8. TMP144 Daisy-Chain: Bus Status at Start of Address Assignment

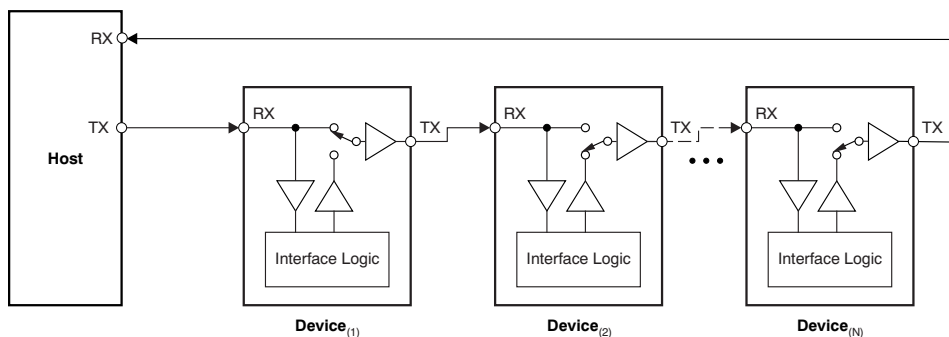


Figure 9. TMP144 Daisy-Chain: Bus Status After First Device Address Assignment

7.3.3 Global Clear Interrupt

The host can initiate a global clear interrupt command (P7-P0 = 10101001) to all TMP144 devices in the daisy-chain. Upon receiving this command, the TMP144 disables future interrupts (D7 in the Configuration Register is set to 0). If a TMP144 previously broke the bus connection and sent an interrupt (logic low on the bus), the device now stops holding the bus low. The device sends the baud rate calibration command and clear interrupt command to the next TMP144 in the chain, then reconnects the bus. In the case of multiple devices having active interrupts, the clear interrupt command propagates through the daisy-chain, disables all interrupts, and reconnects the bus across all devices.

7.3.4 Global Software Reset

The host can initiate a global software reset command (P7-P0 = 10110100) to all TMP144 devices in the daisy-chain. Upon receiving this command, the TMP144 resets all of its internal registers except for the device ID and reconnects the bus. If the bus is broken before the initiation of this command, all TMP144 devices before the broken bus point receive the command. If the host intends to initiate a global software reset across all TMP144 devices in the chain, this command must be transmitted multiple times until it echoes back to the host.

7.3.5 Individual Read and Write

The host can initiate an individual read and write command to a particular TMP144 device in the daisy-chain by sending the read/write command. The read/write command consists of these parameters:

- P7 = 0
- P6-P3 = the device ID
- P2-P1 = the data register pointer; see [Table 3](#)
- P0 = indicates read/write control

P0 = 0 indicates an individual write command. The host must transfer one more byte of data for the register indicated by bits P2-P1. The TMP144 in the daisy-chain that corresponds to the device ID noted by bits P6-P3 then updates the appropriate register. P0 = 1 indicates an individual read command. As shown in [Figure 10](#), the TMP144 in the daisy-chain that corresponds to the device ID pointed by bits P6-P3 then breaks the bus, transmits the data from the register pointed by bits P2-P1, and reconnects the bus.

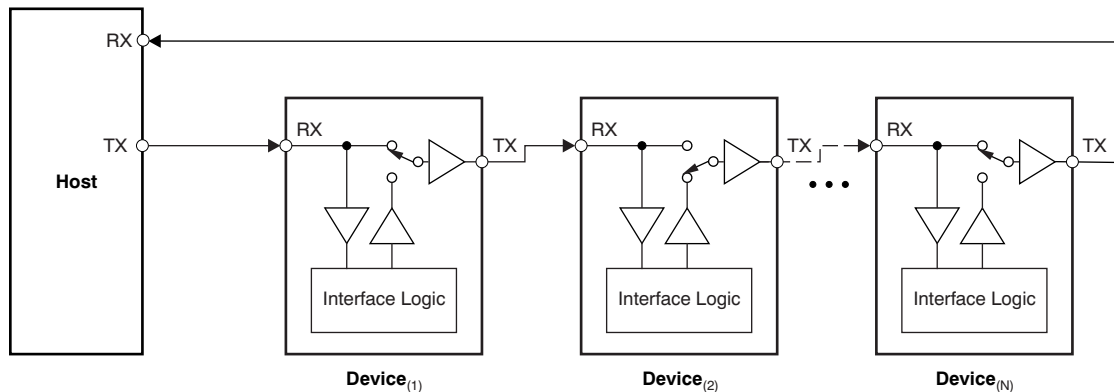


Figure 10. TMP144 Daisy-Chain: Bus Status During Individual Read Operation of Second Device

7.3.6 Timeout Function

A timeout mechanism is implemented on the TMP144 to allow for re-synchronization of the SMAART wire interface if synchronization between the host and the TMP144 is lost for 28 ms (typical). If the timeout period expires between the calibration byte and the command byte, between the command byte and a data byte, or between any data bytes, the TMP144 resets the SMAART wire interface circuitry and waits for the baud rate calibration command to restart. Every time a byte is transmitted on the SMAART wire interface, this timeout period restarts.

7.3.7 SMAART wire™ / UART Interface Timing Specifications

[Figure 1](#) shows the key timing and jitter considerations for the SMAART wire™ / UART interface, and the [Timing Requirements](#) section contains the timing specifications for proper operation. During a transaction, the baud rate must remain within $\pm 1\%$ of its initialization byte value. The baud rate, however, can change from transaction to transaction. There is an allowed delay between each byte transfer of less than 28 ms, which is the bus inactivity timeout check for the TMP144 SMAART wire interface (see [Figure 1](#) and the [Timing Requirements](#) section).

7.4 Device Functional Modes

7.4.1 Shutdown Mode (M1 = 0, M0 = 0)

Shutdown mode saves maximum power by shutting down all device circuitry other than the serial interface, reducing the current consumption to typically less than 0.5 μA . Shutdown mode is enabled when bits M1 and M0 (in the [Configuration Register](#)) read 00. The device shuts down when the current conversion is complete.

Device Functional Modes (continued)

7.4.2 One-Shot Mode (M1 = 0, M0 = 1)

The TMP144 features a One-Shot Temperature Measurement mode. When the device is in Shutdown mode, writing 01 to bits M1 and M0 starts a single temperature conversion. During the conversion, bits M1 and M0 read 01. The device returns to the shutdown state at the completion of the single conversion. After the conversion, bits M1 and M0 read 00. This feature is useful for reducing power consumption in the TMP144 when continuous temperature monitoring is not required.

As a result of the short conversion time, the TMP144 can achieve a higher conversion rate. A single conversion typically takes 26 ms and an individual read can take place in less than 300 μ s. When using One-Shot mode, 30 or more conversions per second are possible.

7.4.3 Continuous Conversion Mode (M1 = 1)

When the TMP144 is in Continuous Conversion mode (M1 = 1), continuous conversions are performed at a rate determined by the conversion rate bits, CR1 and CR0 (in the [Conversion Rate \(CR1, CR0\)](#)). The TMP144 performs a single conversion, then powers down and waits for the appropriate delay set by CR1 and CR0. See [Table 5](#) for CR1 and CR0 settings.

7.4.4 Extended Temperature Mode (ETM = 1)

When the TMP144 is in Extended Temperature mode (ETM = 1), the temperature result and temperature limit registers will be 13-bit instead of 12-bit. This extra bit increases the range of the measurement. For example, with a 12-bit temperature, the maximum value is 7FFh or 127.9°C. With a 13-bit temperature value, however, the maximum value is FFFh or 255.9°C.

The EM bit for the T_{HIGH} and T_{LOW} registers is not cleared when the user changes ETM from 1 to 0. Additionally, when enabling ETM, TI recommends that the user update the T_{HIGH} and T_{LOW} register limits because the added bit will effectively left shift and double the register value. This will double the corresponding temperature limit. Conversely, when exiting Extended Temperature Mode by setting ETM to 0, the limit will be right-shifted by 1 bit and halved unless the register value is updated.

The ETM bit value is considered at the end of every conversion cycle, but the T_{HIGH} and T_{LOW} registers can be updated immediately after setting the bit to 1.

7.5 Register Maps

7.5.1 Command Register

Figure 11 shows the internal register structure of the TMP144. Communications between the registers are transferred through the interface in LSB-first order. The 8-bit Command Register, as shown in Table 2, is used to determine the type of instruction being addressed. These eight bits could either interpret a global instruction or an individual instruction, which is determined by the value of P7. When P7 = 0, the command byte interprets an individual instruction; when P7 = 1, the command byte interprets a global instruction.

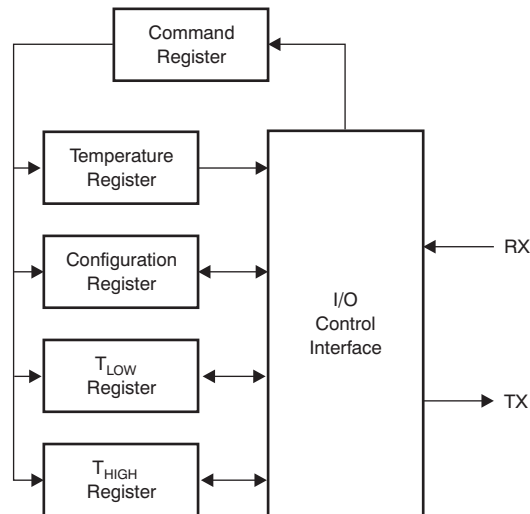


Figure 11. Internal Register Structure

Table 2. Command Register Byte

P7	P6	P5	P4	P3	P2	P1	P0
GLB	IN3/ID3	IN2/ID2	IN1/ID1	IN0/ID0	P1	P0	R/W

7.5.2 Global Read and Write

The host can initiate a global read or write command to all TMP144s in the daisy-chain by sending the read/write command, consisting of P7-P3 = 11110. P2-P1 indicate the data register pointer, as shown in Table 3, and P0 indicates read/write control. P0 = 0 indicates a global write command. The host must transfer one more byte of data for the register (indicated by bits P2-P1), and every TMP144 in the daisy-chain updates the appropriate register. P0 = 1 indicates a global read command. The TMP144 with the device ID of 0000 then breaks the bus connection, transmits the data from the register indicated by bits P2-P1, and then reconnects the bus. The TMP144 with the device ID of 0001 then repeats the same sequence, followed by the rest of the TMP144 devices in the daisy-chain.

Table 3. Pointer Addresses

P1	P0	REGISTER
0	0	Temperature register (read-only)
0	1	Configuration register (read/write)
1	0	T _{LOW} register (read/write)
1	1	T _{HIGH} register (read/write)

7.5.3 Configuration Register

The Configuration Register is a 12-bit read/write register used to store bits that control the operational modes of the temperature sensor. Read/write operations are performed LSB first. The format and power-up/reset value of the Configuration Register is shown in Table 4.

Table 4. Configuration and Power-Up/Reset Format

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
INT_EN	CR1	CR0	FH	FL	LC	M1	M0	ETM	Reserved		
0	0	0	0	0	0	1	0	0	0	0	0

7.5.3.1 Temperature Watchdog Function (FH, FL)

The TMP144 contains a watchdog function that monitors the device temperature and compares the result to the values stored in the temperature limit registers (T_{HIGH} and T_{LOW}) to determine if the device temperature is within these set limits. If the temperature of the TMP144 becomes greater than the value in the T_{HIGH} register, then the flag-high bit (FH) in the Configuration Register is set to 1. If the temperature falls below value in the T_{LOW} register, then the flag-low bit (FL) is set to 1. If both flag bits remain 0, then the temperature is within the temperature window set by the temperature limit registers as shown in Figure 12.

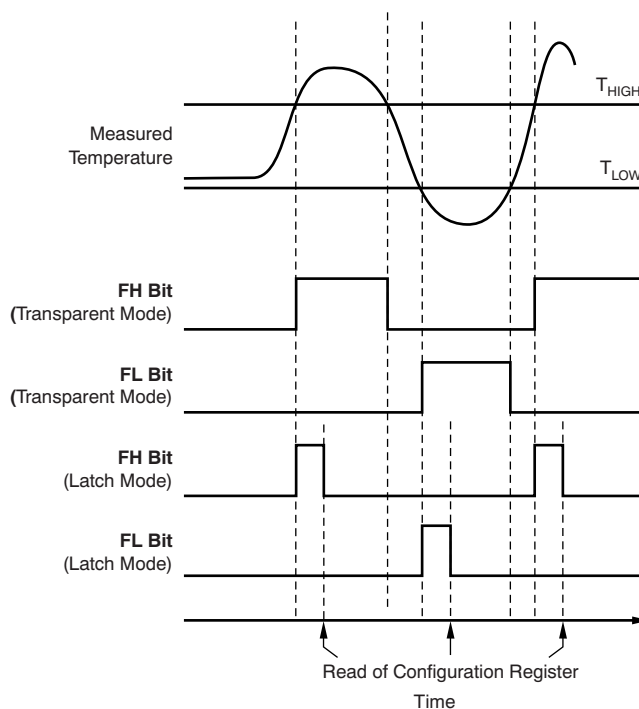


Figure 12. Temperature Flag Functional Diagram

The latch bit (LC) in the Configuration Register is used to latch the value of the flag bits (FH and FL) until the master issues a read command to the Configuration Register. The flag bits are set to 0 if a read command is received by the TMP144, or if $LC = 0$ and the temperature is within the temperature limits. The power-on default values for these bits are $FH = 0$, $FL = 0$, and $LC = 0$.

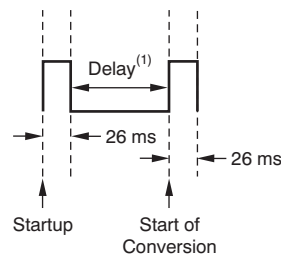
7.5.3.2 Conversion Rate (CR1, CR0)

The conversion rate bits (CR1 and CR0), located in the Configuration Register, configure the TMP144 for conversion rates of 8 Hz, 4 Hz, 1 Hz, or 0.25 Hz (default). The TMP144 has a typical conversion time of 26 ms. To achieve different conversion rates, the TMP144 performs a single conversion and then powers down and waits for the appropriate delay set by CR1 and CR0. [Table 5](#) shows the settings for CR1 and CR0.

Table 5. Conversion Rate Settings

CR1	CR0	CONVERSION RATE
0	0	0.25 Hz (default)
0	1	1 Hz
1	0	4 Hz
1	1	8 Hz

After power-up or general-call reset, the TMP144 immediately starts a conversion as shown in [Figure 13](#). The first result is available after 26 ms (typical). The active quiescent current during conversion is 40 μ A (typical at +25°C, V+ = 1.8 V). The quiescent current during delay is 1.0 μ A (typical at +25°C, V+ = 1.8 V).



(1) Delay is set by CR1 and CR0.

Figure 13. Conversion Start

7.5.3.3 Interrupt Functionality (INT_EN)

The TMP144 interrupts the host by disconnecting the bus and issuing an interrupt request by holding the bus low if all of these conditions are met (as shown in Figure 14):

- INT_EN in the Configuration Register is set to 1;
- The temperature result is higher than the value in the T_{HIGH} register or lower than the value in the T_{LOW} register (as indicated by a 1 in either FL or FH);
- The bus is logic high and idle for more than 28 ms.

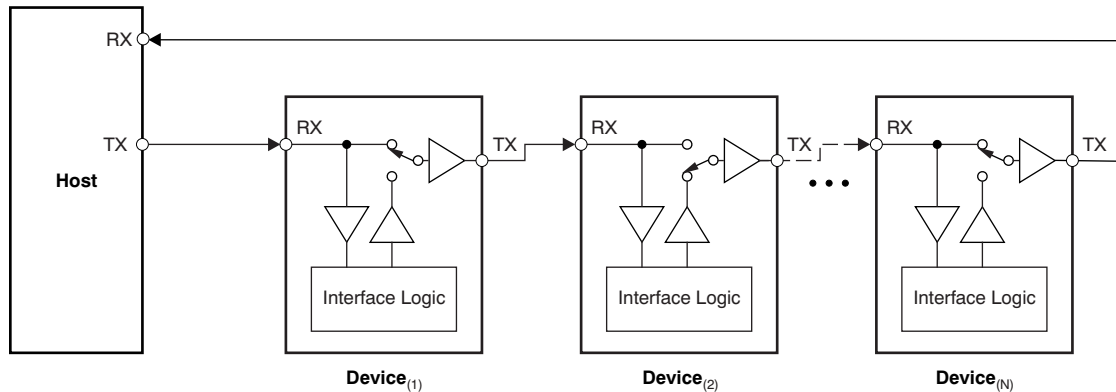


**Figure 14. TMP144 Daisy-Chain:
Bus Status During an Interrupt Request (Logic Low) From Second Device**

The interrupt on the bus is latched regardless of the status of LC. Writing a 1 to INT_EN automatically sets the LC bit. The TMP144 holds the bus low until one of the following events happen:

- Global Interrupt Clear command is received.
- Global Software Reset command is received.
- A power-on reset event occurs.

Each of these events clears the INT_EN. The TMP144 does not issue future interrupts until the host writes 1 to bit D7 in the Configuration Register to re-enable future interrupts.

In a system with enabled interrupts, it is possible for a TMP144 on the bus to issue an interrupt at the same time that the host starts a communication sequence. To avoid this scenario, TI recommends that the host should check the status on the receiving side of the bus after transmitting the calibration byte. If it is 1, then the host can continue with the communication. If it is 0, one of the TMP144 devices on the bus is issuing an alert and the host must transmit a Global Interrupt Clear command.

7.5.3.4 Extended Temperature Mode (ETM)

The ETM bit of the configuration enables the extended temperature mode the TMP144. In this mode, the T_{HIGH} and T_{LOW} temperature registers will be 13-bit instead of the default 12-bit. The LSB resolution will remain at 0.0625°C per LSB in this mode, but the maximum temperature value of the registers is moved from 127.9375°C to 255.9375°C.

7.5.4 Temperature Register

The Temperature Register stores the results of the conversion in 12-bit or 13-bit format, depending on the status of the ETM bit in the configuration register. Negative numbers are represented in binary twos complement format. Following power-up or reset, the Temperature Register reads 0°C until the first conversion is complete.

7.5.4.1 Temperature Register With ETM = 0

With the ETM bit = 0, the temperature register of the TMP144 is configured as a 12-bit, read-only register that stores the output of the most recent conversion. Two bytes must be read to obtain data, and is described in Table 6. The data format for temperature with ETM = 0 is summarized in Table 7. One LSB equals 0.0625°C.

With ETM = 0, the maximum temperature value represented will be 127.9375°C.

Table 6. Temperature Register With ETM = 0

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	EM
T11	T10	T9	T8	T7	T6	T5	T4	T3	T2	T1	T0	0

Negative numbers are represented in binary twos complement format.

Table 7. 12-Bit Temperature Data Format With ETM = 0⁽¹⁾

TEMPERATURE (°C)	DIGITAL OUTPUT	
	BINARY (T11 - T0)	HEX
+127.9375	0111 1111 1111	7FF
+125	0111 1101 0000	7D0
+100	0110 0100 0000	640
+80	0101 0000 0000	500
+75	0100 1011 0000	4B0
+50	0011 0010 0000	320
+25	0001 1001 0000	190
+0.0625	0000 0000 0001	001
0	0000 0000 0000	000
-0.0625	1111 1111 1111	FFF
-25	1110 0111 0000	E70
-40	1101 1000 0000	D80
-128	1000 0000 0000	800

(1) The resolution for the analog-to-digital converter (ADC) is 0.0625°C/count, where *count* is equal to the digital output of the ADC.

For positive temperatures (for example, +50°C):

Twos complement is not performed on positive numbers. Therefore, simply convert the number to binary code, left-justified format. Denote a positive number with most significant bit (MSB) = 0.

Example: (+50°C)/(0.0625°C/count) = 800 = 320h = 0011 0010 0000

For negative temperatures (for example, -25°C):

Generate the twos complement of a negative number by complementing the absolute value binary number and adding 1. Denote a negative number with MSB = 1.

Example: (|-25°C|)/(0.0625°C/count) = 400 = 190h = 0001 1001 0000

Twos complement format: 1110 0110 1111 + 1 = 1110 0111 0000 = E70h

7.5.4.2 Temperature Register With ETM = 1

With the ETM bit = 1, the temperature register of the TMP144 is configured as an 13-bit, read-only register that stores the output of the most recent conversion. Two bytes must be read to obtain data, and is described in [Table 8](#). The data format for temperature with ETM = 1 is summarized in [Table 9](#). One LSB equals 0.0625°C.

With ETM = 0, the maximum temperature value represented will be 255.9375°C.

Table 8. Temperature Register With ETM = 1

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	EM
T12	T11	T10	T9	T8	T7	T6	T5	T4	T3	T2	T1	T0

Negative numbers are represented in binary twos complement format.

Table 9. 13-Bit Temperature Data Format With ETM = 1⁽¹⁾

TEMPERATURE (°C)	DIGITAL OUTPUT	
	BINARY (T12 - T0)	HEX
+255.9375	0 1111 1111 1111	0FFF
+125	0 0111 1101 0000	07D0
+100	0 0110 0100 0000	0640
+80	0 0101 0000 0000	0500
+75	0 0100 1011 0000	04B0
+50	0 0011 0010 0000	0320
+25	0 0001 1001 0000	0190
+0.0625	0 0000 0000 0001	0001
0	0 0000 0000 0000	0000
-0.0625	1 1111 1111 1111	1FFF
-25	1 1110 0111 0000	1E70
-40	1 1101 1000 0000	1D80
-256	1 0000 0000 0000	1000

(1) The resolution for the analog-to-digital converter (ADC) is 0.0625°C/count, where *count* is equal to the digital output of the ADC.

For positive temperatures (for example, +50°C):

Twos complement is not performed on positive numbers. Therefore, simply convert the number to binary code, left-justified format. Denote a positive number with most significant bit (MSB) = 0.

Example: (+50°C)/(0.0625°C/count) = 800 = 0320h = 0 0011 0010 0000

For negative temperatures (for example, -25°C):

Generate the twos complement of a negative number by complementing the absolute value binary number and adding 1. Denote a negative number with MSB = 1.

Example: (|-25°C|)/(0.0625°C/count) = 400 = 0190h = 0 0001 1001 0000

Twos complement format: 1 1110 0110 1111 + 1 = 1 1110 0111 0000 = 1E70h

7.5.5 Temperature Limit Registers

The T_{HIGH} and T_{LOW} registers are used to store the temperature limit thresholds for the TMP144 watchdog function. At the end of each temperature measurement, the TMP144 compares the temperature results to each of these limits. If the temperature result is greater than the T_{HIGH} limit, then the FH bit in the Configuration Register is set to 1. If the temperature result is less than the T_{LOW} limit, then the FL bit in the Configuration Register is set to 1. See [Figure 12](#).

[Table 10](#) and [Table 11](#) describe the format for the T_{HIGH} and T_{LOW} registers with ETM = 0. Power-up reset values for T_{HIGH} and T_{LOW} are: $T_{HIGH} = +60^{\circ}\text{C}$ and $T_{LOW} = -10^{\circ}\text{C}$. The format of the data for T_{HIGH} and T_{LOW} is the same as for the Temperature Register. One LSB equals 0.0625°C .

TI recommends that the user update the T_{HIGH} and T_{LOW} registers upon changing the ETM bit in the configuration register.

Table 10. T_{HIGH} Register With ETM = 0

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	EM
H11	H10	H9	H8	H7	H6	H5	H4	H3	H2	H1	H0	X

Table 11. T_{LOW} Register With ETM = 0

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	EM
L11	L10	L9	L8	L7	L6	L5	L4	L3	L2	L1	L0	X

[Table 12](#) and [Table 13](#) describe the format for the T_{HIGH} and T_{LOW} registers with ETM = 1. One LSB equals 0.0625°C .

Table 12. T_{HIGH} Register With ETM = 1

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	EM
H12	H11	H10	H9	H8	H7	H6	H5	H4	H3	H2	H1	H0

Table 13. T_{LOW} Register with ETM = 1

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	EM
L12	L11	L10	L9	L8	L7	L6	L5	L4	L3	L2	L1	L0

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TMP144 devices are typically used to for thermal management of multiple hotspots. The MDA commands make it easy to manage multiple devices at the same time, which reduces communication time and power. The WCSP package enables the device to be placed in space-constrained designs and allows the device to have a fast thermal response.

8.2 Typical Application

Figure 15 shows typical connections for TMP144 devices in a daisy-chain configuration.

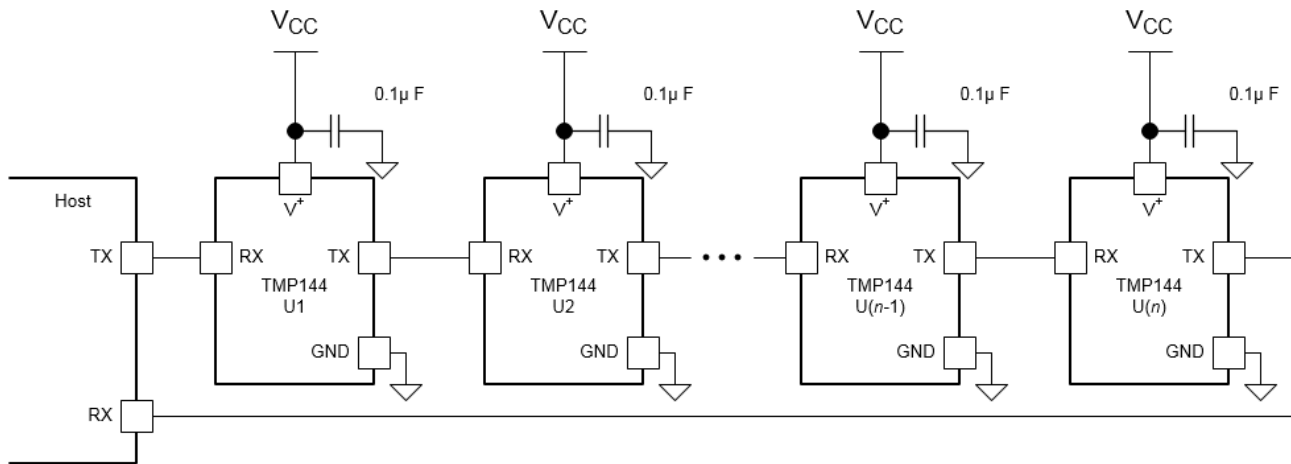


Figure 15. Typical Application With Multiple Devices

8.2.1 Design Requirements

Multiple devices are connected in this typical application. The key design requirements are discussed in the following sections.

8.2.2 Detailed Design Procedure

8.2.2.1 Trace Length

The maximum trace or cable length between two TMP144 devices can vary because of the effective resistance and capacitance of the type of cable used in a customer application. Design the trace or cable such that timing specifications in [Timing Requirements](#) can be satisfied for each TMP144 device in the daisy-chain.

8.2.2.2 Voltage Drop Effect

Take into account the voltage drop that occurs along the supply and ground lines as a result of the currents of all the devices on the line. This voltage drop occurs as a result of multiple devices simultaneously consuming current through the combined resistance of the common wire, connectors, and solder contacts. Make sure that the supply on the last device does not fall below the minimum operating supply of 1.4 V.

Typical Application (continued)

8.2.2.3 Power Supply Noise Filtering

To reduce power supply noise, a 0.1- μ F bypass capacitor is used for each TMP144 device. Depending on the environment, additional bypass capacitors (for example, 1 nF) may be required.

8.2.3 Application Curves

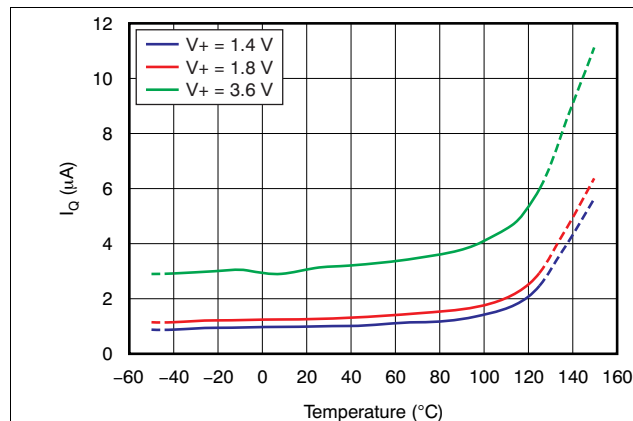


Figure 16. Typical Quiescent Current vs Temperature

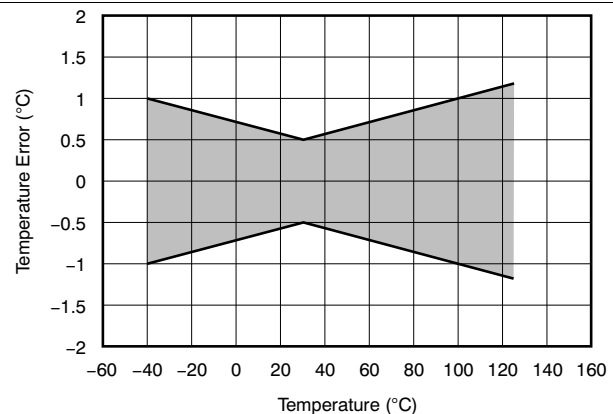


Figure 17. Temperature Error vs Temperature

9 Power Supply Recommendations

The TMP144 operates on a power-supply range from 1.4 V to 3.6 V. The device is trimmed for operation at a 3.3-V supply, but the TMP144 can measure temperature accurately in the full supply range.

The TMP144 is a very low-power device and generates very low noise on the supply bus. Applying a bypass capacitor to the V₊ pin of the TMP144 can further reduce any noise the TMP144 might propagate to other components. Use a C_F capacitor with a value greater than 0.1 μ F as shown in Figure 18. Place the bypass capacitor as close to the supply and ground pins of the device as possible for best results.

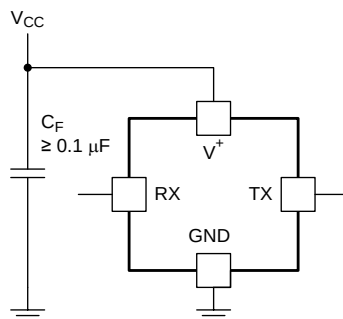


Figure 18. Power Supply Noise Reduction With a Bypass Capacitor

10 Layout

10.1 Layout Guidelines

Mount the TMP144 to a PCB as shown in [Figure 19](#). Obtaining acceptable performance with alternate layout schemes is possible, however this layout produces good results and is intended as a guideline:

- Bypass the V+ pin to ground with a low-ESR ceramic bypass-capacitor. The typical recommended bypass capacitance is a 0.1- μ F ceramic capacitor with a X5R or X7R dielectric. The optimum placement is closest to the V+ and GND pins of the device. Take care to minimize the loop area formed by the bypass-capacitor connection, the V+ pin, and the GND pin of the IC. Alternatively, the bypass capacitor can also be grounded through a via connected to the GND plane.
- Use larger copper area pads to reduce self-heating and lower thermal resistance to the environment.
- If possible, use PCB boards with thick copper layers.
- If possible, do not use stain to protect the IC because stain can increase thermal resistance.

10.2 Layout Example

-  VIA to power plane
-  VIA to ground plane

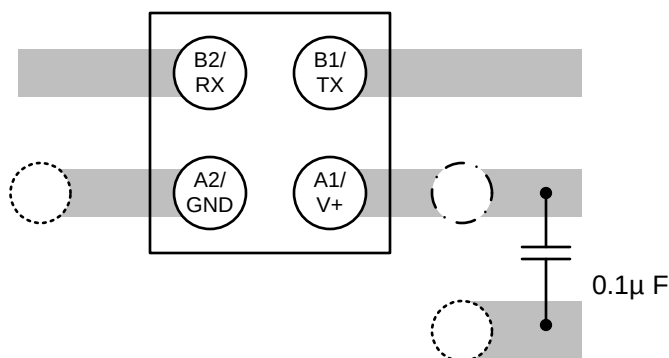


Figure 19. Layout Example

11 Device and Documentation Support

11.1 Device Support

11.1.1 Device Nomenclature

daisy-chain A method of propagating signals along a bus in which the devices are connected in series and the signal passed from one device to the next. The daisy-chain scheme permits assignment of device priorities based on the electrical position of the device on the bus.

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

SMAART wire, E2E are trademarks of Texas Instruments.
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11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMP144YFFR	ACTIVE	DSBGA	YFF	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	C2	Samples
TMP144YFFT	ACTIVE	DSBGA	YFF	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	C2	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

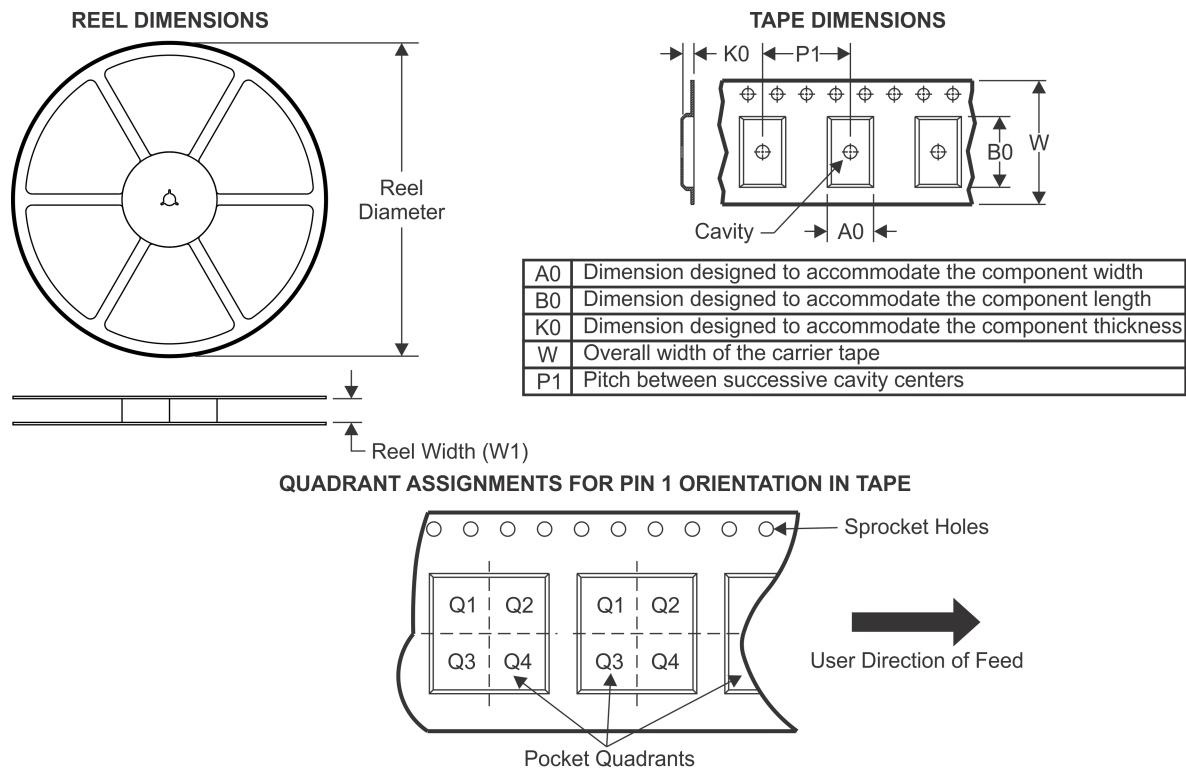
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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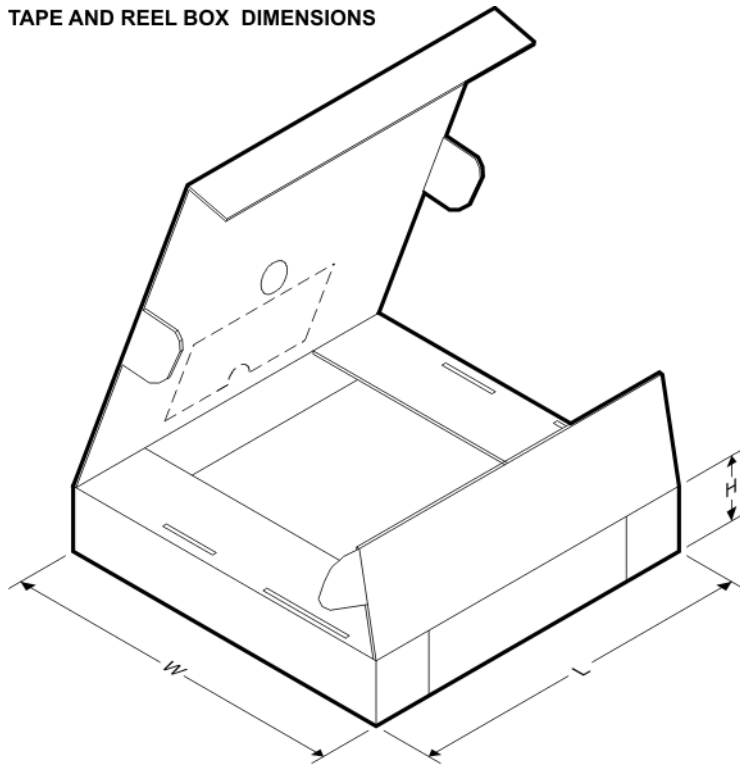
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

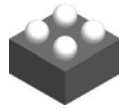
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMP144YFFR	DSBGA	YFF	4	3000	180.0	8.4	0.86	1.06	0.69	4.0	8.0	Q1
TMP144YFFT	DSBGA	YFF	4	250	180.0	8.4	0.86	1.06	0.69	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMP144YFFR	DSBGA	YFF	4	3000	182.0	182.0	20.0
TMP144YFFT	DSBGA	YFF	4	250	182.0	182.0	20.0

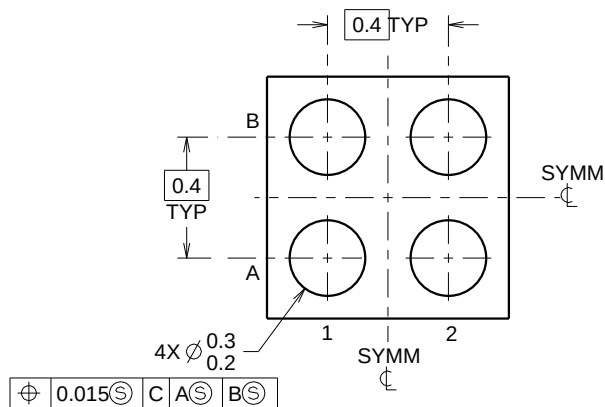
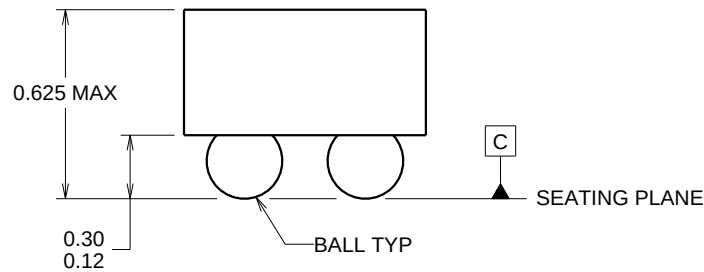
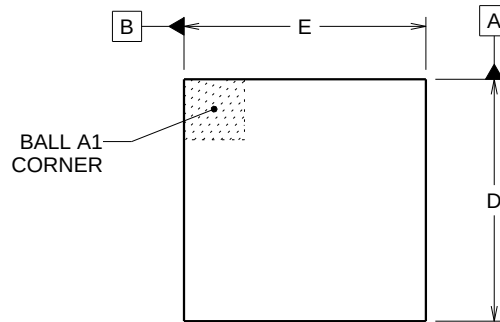


YFF0004

PACKAGE OUTLINE

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



D: Max = 0.99 mm, Min = 0.93 mm

E: Max = 0.79 mm, Min = 0.73 mm

4219460/A 02/2014

NOTES:

NanoFree Is a trademark of Texas Instruments.

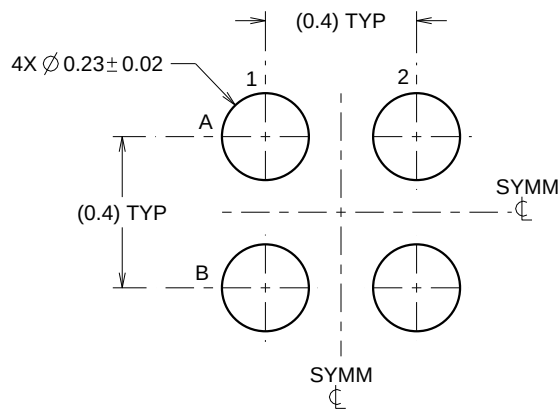
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.

EXAMPLE BOARD LAYOUT

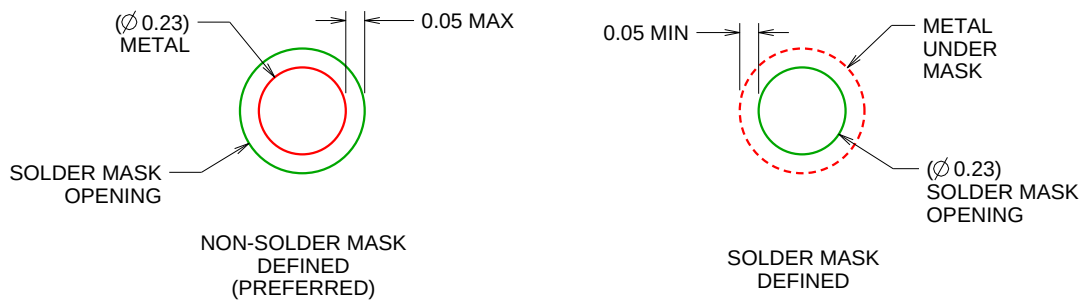
YFF0004

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:50X



SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

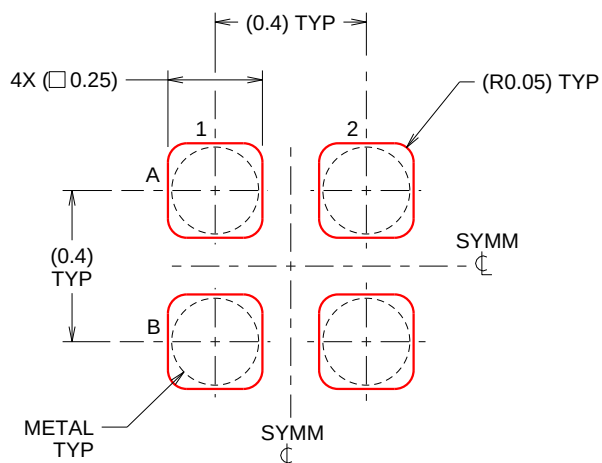
4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).

EXAMPLE STENCIL DESIGN

YFF0004

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:50X

4219460/A 02/2014

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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