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March 2015

MM74HC02
Quad 2-Input NOR Gate

Features

- Typical Propagation Delay: 8 ns
- Wide Power Supply Range: 2 V to 6 V
- Low Quiescent Supply Current: 20 µA Maximum (74HC Series)
- Moisture Level Sensitivity 1
- Low Input Current: 1 µA Maximum
- High Output Current: 4 mA Minimum

General Description

The MM74HC02 NOR gates utilize advanced silicon-gate CMOS technology to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. All gates have buffered outputs, providing high noise immunity and the ability to drive 10 LS-TTL loads. The 74HC logic family is functionally as well as pin-out compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

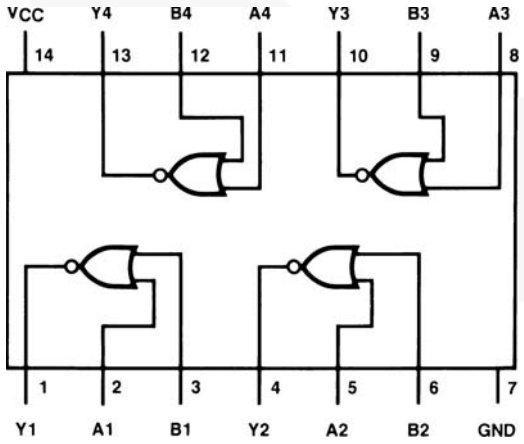
Ordering Information

Part Number	Top Mark	Package	Packing Method
MM74HC02M	MM74HC02M	SOIC 14L	Rail
MM74HC02MX	MM74HC02M	SOIC 14L	Tape and Reel
MM74HC02MTC	HC02	TSSOP 14L	Rail
MM74HC02MTCX	HC02	TSSOP 14L	Tape and Reel

All packages are lead free per JEDEC: J-STD-020B standard.

Connection Diagram

Pin Assignment for SOIC, TSSOP



Top View

Logic Diagram



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Absolute Maximum Ratings(1)

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		-0.5 to +7.0	V
V_{IN}	DC Input Voltage		-1.5 to V_{CC}+1.5	V
V_{OUT}	DC Output Voltage		-0.5 to V_{CC}+0.5	V
I_{IK}, I_{OK}	Clamp Diode Current		±20	mA
I_{OUT}	DC Output Current, per pin		±25	mA
I_{CC}	DC V_{CC} or GND Current, per pin		±50	mA
T_{STG}	Storage Temperature Range		-65 to +150	°C
P_D	Power Dissipation	(2)	600	mW
		S.O. Package only	500	
T_L	Lead Temperature (Soldering 10 seconds)		260	°C

Notes:

1. Unless otherwise specified all voltages are referenced to ground.
2. Power dissipation temperature derating - plastic “N” package: -12 mW/°C from 65°C to 85°C.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter		Min.	Max.	Unit
V_{CC}	Supply Voltage		2	6	V
V_{IN}, V_{OUT}	DC Input or Output Voltage		0	V_{CC}	V
T_A	Operating Temperature Range		-40	85	°C
t_r, t_f	Input Rise or Fall Times	V_{CC} = 2.0 V		1000	ns
		V_{CC} = 4.5 V		500	
		V_{CC} = 6.0 V		400	

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DC Electrical Characteristics[3]

Symbol	Parameter	V_{CC} (V)	Conditions	T_A = 25°C		T_A =-40 to 85°C	T_A =-55 to 125°C	Unit
				Typ.	Guaranteed Limits			
V_{IH}	Minimum HIGH Level Input Voltage	2.0			1.50	1.50	1.50	V
		4.5			3.15	3.15	3.15	
		6.0			4.20	4.20	4.20	
V_{IL}	Maximum LOW Level Input Voltage	2.0			0.50	0.50	0.50	V
		4.5			1.35	1.35	1.35	
		6.0			1.80	1.80	1.80	
V_{OH}	Minimum HIGH Level Output Voltage	2.0	$V_{IN} = V_{IL}$, $\|I_{OUT}\| \le 20\ \mu A$	2.0	1.9	1.9	1.9	V
		4.5		4.5	4.4	4.4	4.4	
		6.0		6.0	5.9	5.9	5.9	
		4.5	$V_{IN} = V_{IL}$, $\|I_{OUT}\| \le 4.0$ mA	4.20	3.98	3.84	3.70	
		6.0	$V_{IN} = V_{IL}$, $\|I_{OUT}\| \le 5.2$ mA	5.70	5.48	5.34	5.20	
V_{OL}	Minimum LOW Level Output Voltage	2.0	$V_{IN} = V_{IH}$ or V_{IL}, $\|I_{OUT}\| \le 20\ \mu A$	0	0.1	0.1	0.1	V
		4.5		0	0.1	0.1	0.1	
		6.0		0	0.1	0.1	0.1	
		4.5	$V_{IN} = V_{IH}$ or V_{IL}, $\|I_{OUT}\| \le 4.0$ mA	0.20	0.26	0.33	0.40	
		6.0	$V_{IN} = V_{IH}$ or V_{IL}, $\|I_{OUT}\| \le 5.2$ mA	0.20	0.26	0.33	0.40	
I_{IN}	Maximum Input Current	6.0	$V_{IN} = V_{CC}$ or GND		±0.1	±0.1	±0.1	µA
I_{CC}	Maximum Quiescent Supply Current	6.0	$V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0\ \mu A$		2.0	20	40	µA

Note:

3. For a power supply of 5 V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5 V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5 V and 4.5 V respectively. (The V_{IH} value at 5.5 V is 3.85 V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0 V values should be used.

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AC Electrical Characteristics

V_{CC} = 5 V, T_A = 25°C, C_L = 15 pF, $t_r = t_f$ = 6 ns

Symbol	Parameter	Conditions	Typ.	Guaranteed Limit	Unit
t_{PHL}, t_{PLH}	Maximum Propagation Delay		8	15	ns

AC Electrical Characteristics

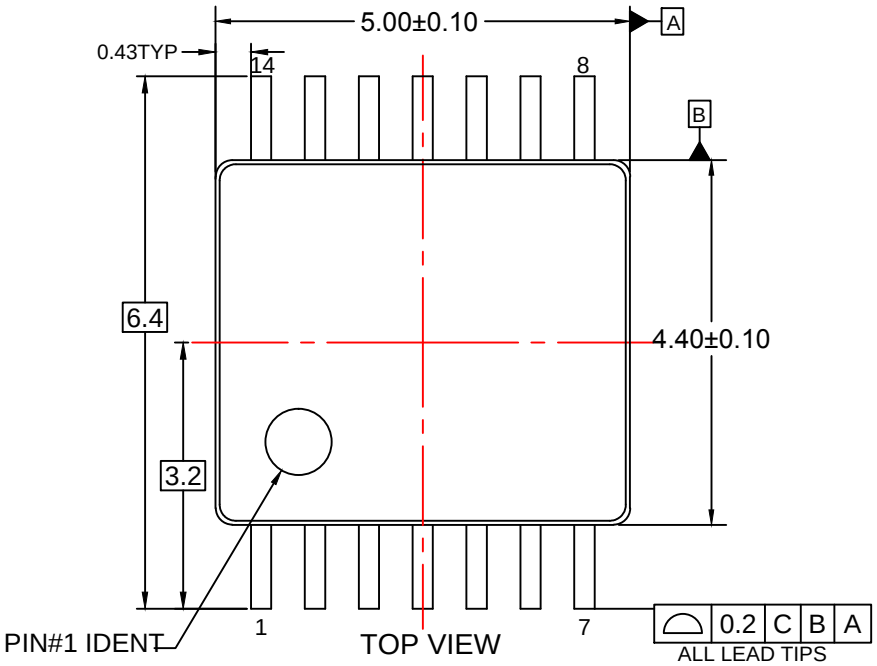
V_{CC} = 2.0 V to 6.0 V, C_L = 50 pF, $t_r = t_f$ = 6 ns (unless otherwise specified)

Symbol	Parameter	V_{CC} (V)	Conditions	T_A = 25°C		T_A =-40 to 85°C	T_A =-55 to 125°C	Unit
				Typ.	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay	2.0		45	90	113	134	ns
		4.5		9	18	23	27	
		6.0		8	15	19	23	
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time	2.0		30	75	95	110	ns
		4.5		8	15	19	22	
		6.0		7	13	16	19	
C_{PD}	Power Dissipation Capacitance(4)		(per gate)	20				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

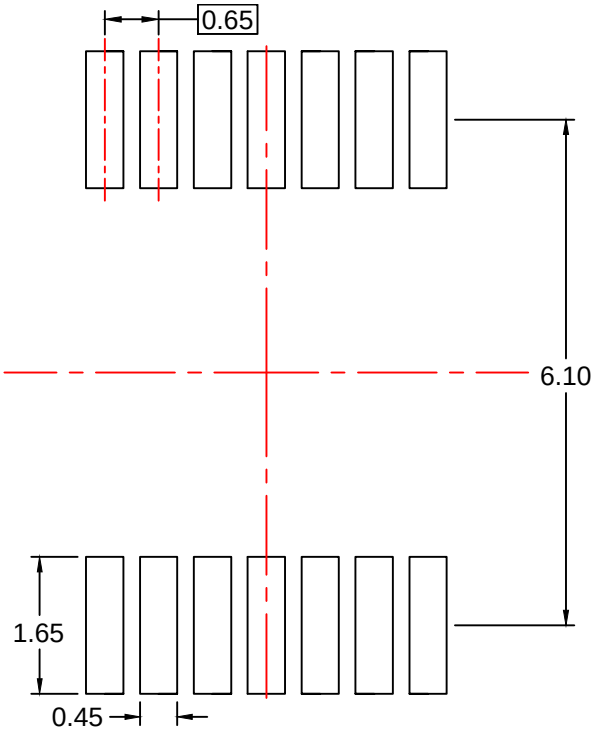
Note:

4. C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

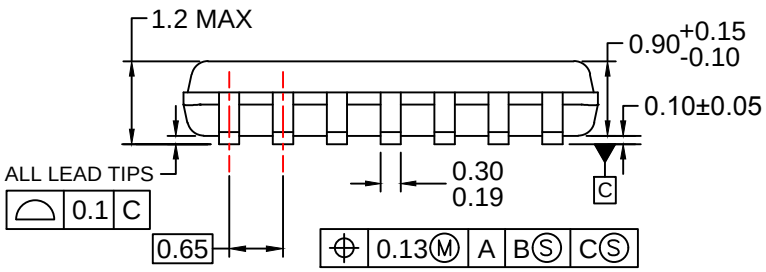
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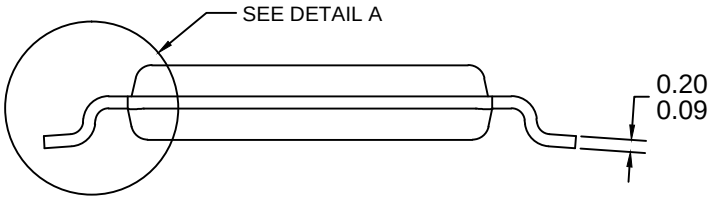
TOP VIEW

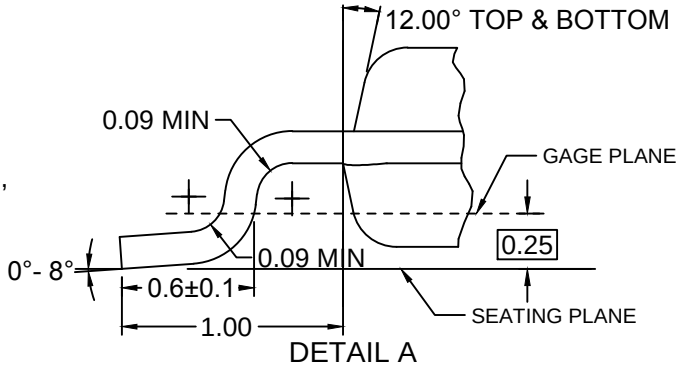


RECOMMENDED LAND PATTERN



FRONT VIEW





DETAIL A

NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6

B. DIMENSIONS ARE IN MILLIMETERS.

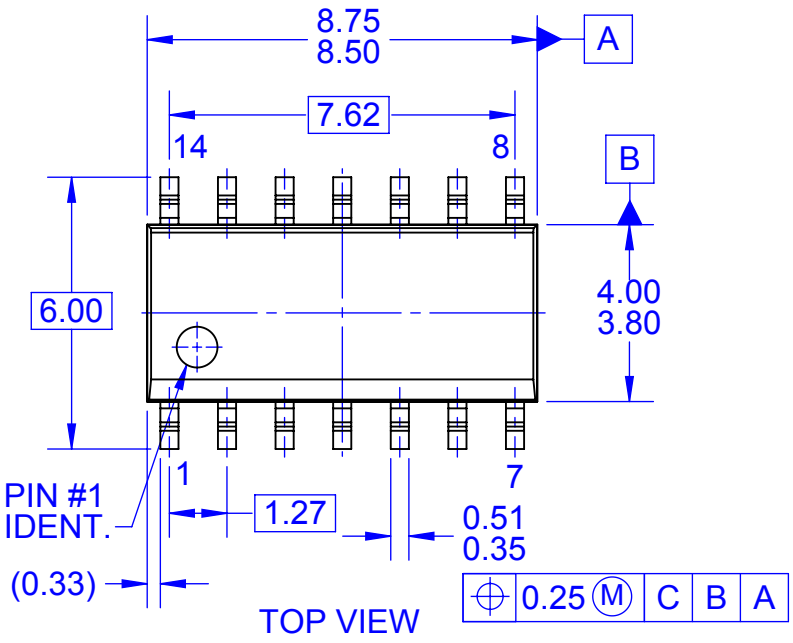
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS

D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 2009.

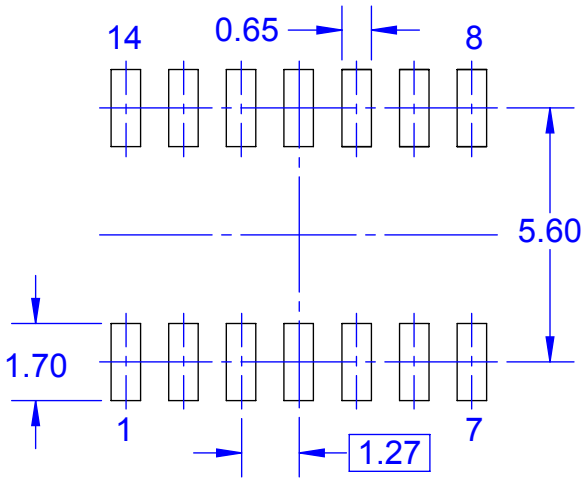
E. LANDPATTERN STANDARD: SOP65P640X110-14M.

F. DRAWING FILE NAME: MKT-MTC14rev7.

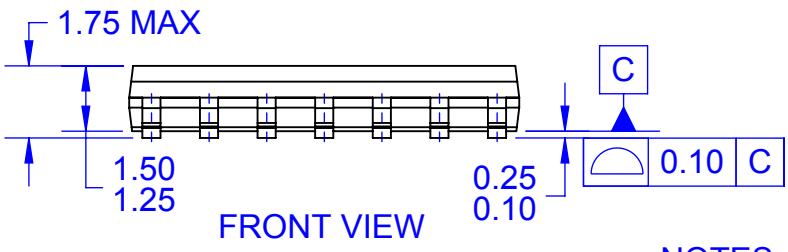
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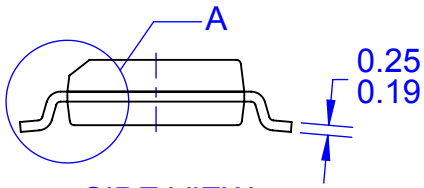
TOP VIEW



LAND PATTERN RECOMMENDATION



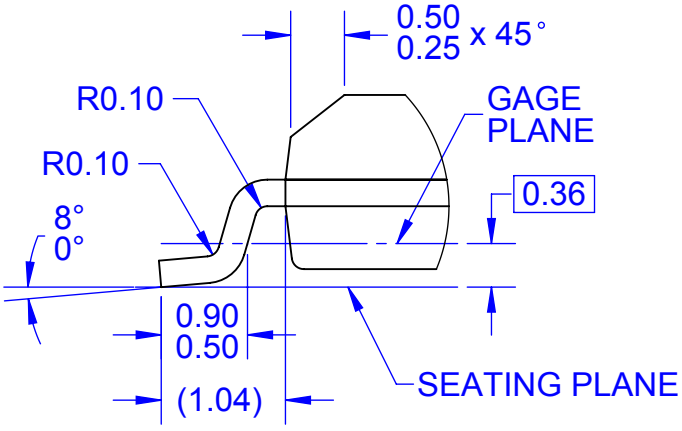
FRONT VIEW



SIDE VIEW

NOTES:

A. CONFORMS TO JEDEC MS-012, VARIATION AB, ISSUE C
B. ALL DIMENSIONS ARE IN MILLIMETERS
C. DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS
D. LAND PATTERN STANDARD: SOIC127P600X145-14M
E. CONFORMS TO ASME Y14.5M, 2009
D. DRAWING FILENAME: MKT-M14Arev14



DETAIL A
SCALE 16 : 1

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