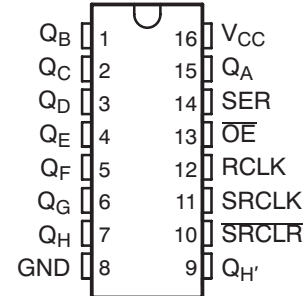


8-BIT SHIFT REGISTER WITH 3-STATE OUTPUT REGISTERS

Check for Samples: [SN74LV595A-Q1](#)

FEATURES

- Qualified for Automotive Applications
- Customer-Specific Configuration Control Can Be Supported Along With Major-Change Approval
- 2-V to 5.5-V V_{CC} Operation
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2.3 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Supports Mixed-Mode Voltage Operation on All Ports
- 8-Bit Serial-In, Parallel-Out Shift
- I_{off} Supports Partial-Power-Down Mode Operation
- Shift Register Has Direct Clear



DESCRIPTION

The SN74LV595A is an 8-bit shift register designed for 2-V to 5.5-V V_{CC} operation.

This device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-state outputs. Separate clocks are provided for both the shift and storage register. The shift register has a direct overriding clear ($\overline{SRCLR}$) input, serial (SER) input, and a serial output for cascading. When the output-enable ($\overline{OE}$) input is high, all outputs except $Q_{H'}$ are in the high-impedance state.

Both the shift register clock (SRCLK) and storage register clock (RCLK) are positive-edge triggered. If both clocks are connected together, the shift register always is one clock pulse ahead of the storage register.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION⁽¹⁾

T_A	PACKAGE ⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	TSSOP – PW	Reel of 2000	SN74LV595AIPWRQ1	LV595AI
-40°C to 125°C	TSSOP – PW	Reel of 2000	SN74LV595AQPWRQ1	LV595AQ

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

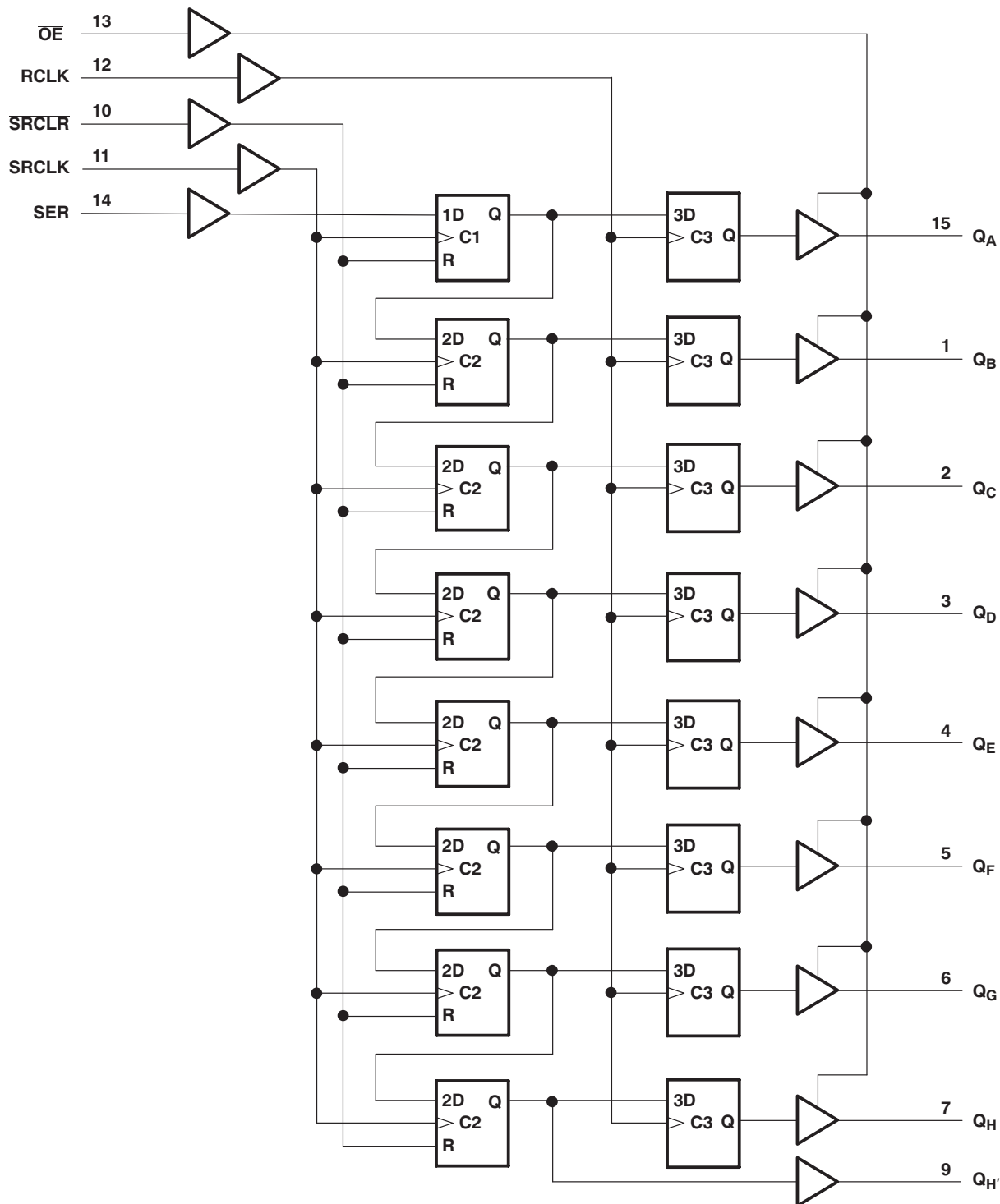


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

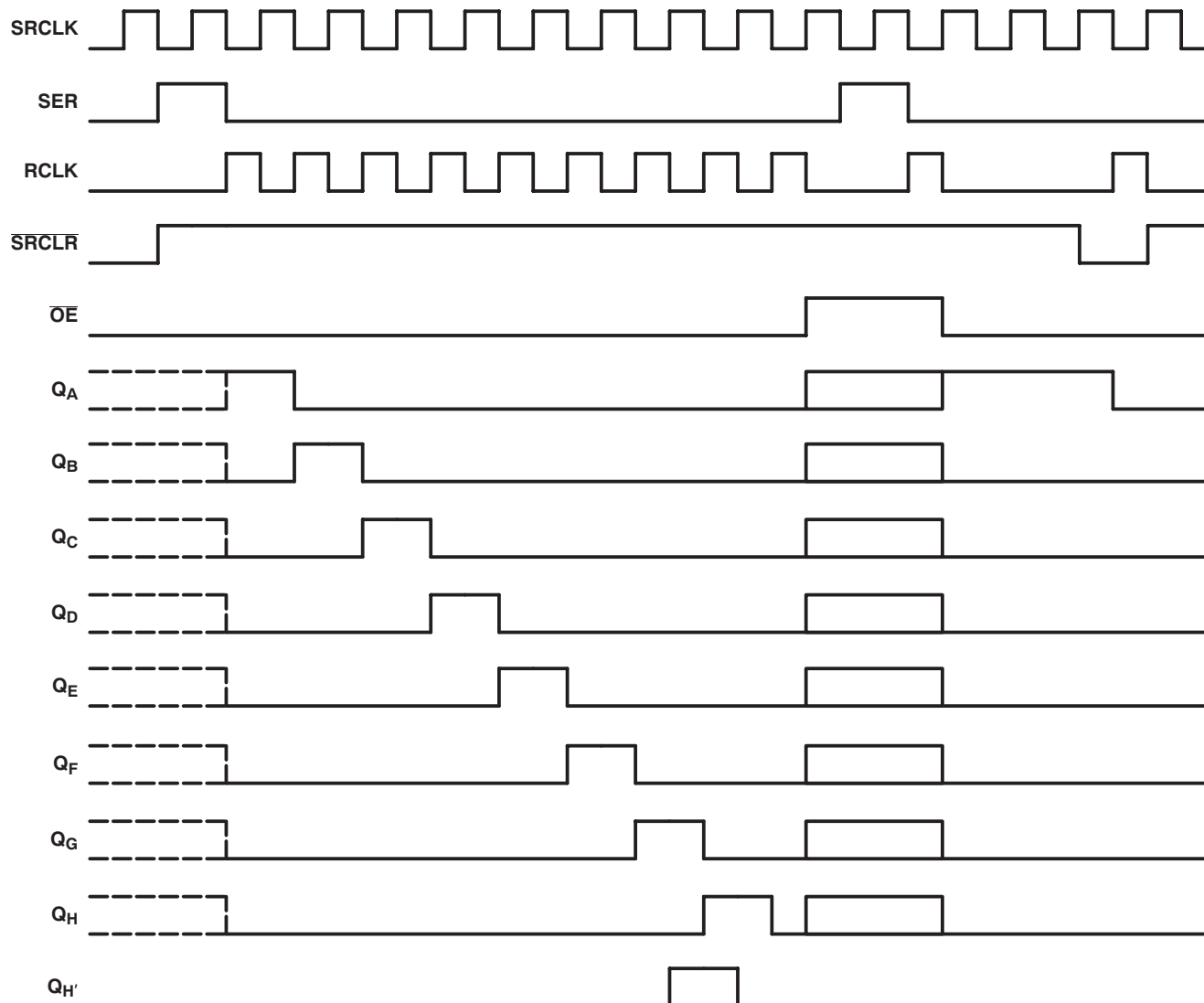
Table 1. FUNCTION TABLE

INPUTS					FUNCTION
SER	SRCLK	$\overline{\text{SRCLR}}$	RCLK	$\overline{\text{OE}}$	
X	X	X	X	H	Outputs Q_A – Q_H are disabled.
X	X	X	X	L	Outputs Q_A – Q_H are enabled.
X	X	L	X	X	Shift register is cleared.
L	↑	H	X	X	First stage of the shift register goes low. Other stages store the data of previous stage, respectively.
H	↑	H	X	X	First stage of the shift register goes high. Other stages store the data of previous stage, respectively.
X	X	X	↑	X	Shift-register data is stored in the storage register.

LOGIC DIAGRAM (POSITIVE LOGIC)



TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

V_{CC}	Supply voltage range		–0.5 V to 7 V
V_I	Input voltage range ⁽²⁾		–0.5 V to 7 V
V_O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾		–0.5 V to 7 V
V_O	Output voltage range applied in the high or low state ^{(2) (3)}		–0.5 V to $V_{CC} + 0.5$ V
I_{IK}	Input clamp current ⁽²⁾	$V_I < 0$	–20 mA
I_{OK}	Output clamp current ⁽²⁾	$V_O < 0$	–50 mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}	±35 mA
	Continuous current through V_{CC} or GND		±70 mA
θ_{JA}	Package thermal impedance ⁽⁴⁾		108°C/W
T_{stg}	Storage temperature range		–65°C to 150°C
ESD	Electrostatic discharge rating	Human-body model (HBM)	2000 V
		Machine model (MM)	200 V
		Charged-device model (CDM)	1000 V

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 5.5 V maximum.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS⁽¹⁾

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 2$ V	1.5		V
		$V_{CC} = 2.3$ V to 2.7 V	$V_{CC} \times 0.7$		
		$V_{CC} = 3$ V to 3.6 V	$V_{CC} \times 0.7$		
		$V_{CC} = 4.5$ V to 5.5 V	$V_{CC} \times 0.7$		
V_{IL}	Low-level input voltage	$V_{CC} = 2$ V		0.5	V
		$V_{CC} = 2.3$ V to 2.7 V		$V_{CC} \times 0.3$	
		$V_{CC} = 3$ V to 3.6 V		$V_{CC} \times 0.3$	
		$V_{CC} = 4.5$ V to 5.5 V		$V_{CC} \times 0.3$	
V_I	Input voltage		0	5.5	V
V_O	Output voltage	High or low state	0	V_{CC}	V
		3-state	0	5.5	
I_{OH}	High level output current	$V_{CC} = 2$ V		–50	mA
		$V_{CC} = 2.3$ V to 2.7 V		–2	
		$V_{CC} = 3$ V to 3.6 V		–8	
		$V_{CC} = 4.5$ V to 5.5 V		–16	
I_{OL}	Low level output current	$V_{CC} = 2$ V		50	mA
		$V_{CC} = 2.3$ V to 2.7 V		2	
		$V_{CC} = 3$ V to 3.6 V		8	
		$V_{CC} = 4.5$ V to 5.5 V		16	
$\Delta t/\Delta v$	Input transition rise/fall time	$V_{CC} = 2.3$ V to 2.7 V		200	ns/V
		$V_{CC} = 3$ V to 3.6 V		100	
		$V_{CC} = 4.5$ V to 5.5 V		20	
T_A	Operating free-air temperature	SN74LV595AIPWRQ1	–40	85	°C
		SN74LV595AQPWRQ1	–40	125	

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	T _A = -40°C TO 85°C			T _A = -40°C TO 125°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V _{OH}		I _{OH} = -50 μA	2 V to 5.5 V	V _{CC} - 0.1			V _{CC} - 0.1			V
		I _{OH} = -2 mA	2.3 V	2			2			
	Q _{H'}	I _{OH} = -6 mA	3 V	2.48			2.45			
	Q _A -Q _H	I _{OH} = -8 mA		2.48			2.45			
	Q _{H'}	I _{OH} = -12 mA	4.5 V	3.8			3.7			
	Q _A -Q _H	I _{OH} = -16 mA		3.8			3.7			
V _{OL}		I _{OL} = 50 μA	2 V to 5.5 V				0.1			V
		I _{OH} = 2 mA	2.3 V				0.45			
	Q _{H'}	I _{OH} = 6 mA	3 V				0.5			
	Q _A -Q _H	I _{OH} = 8 mA					0.5			
	Q _{H'}	I _{OH} = 12 mA	4.5 V				0.65			
	Q _A -Q _H	I _{OH} = 16 mA					0.65			
I _I		V _I = 5.5 V or GND	0 V to 5.5 V				±1			nA
I _{OZ}	Q _A -Q _H	V _O = V _{CC} or GND	5.5 V				±10			μA
I _{CC}		V _I = V _{CC} or GND, I _O = 0	5.5 V				40			μA
I _{off}		V _I or V _O = 0 to 5.5 V	0				5 ⁽¹⁾			μA
C _i		V _I = V _{CC} or GND	3.3 V	3.5			3.5			pF

(1) I_{off} does not apply to pin 9.

TIMING REQUIREMENTS

over operating free-air temperature range, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted)

		T _A = 25°C		T _A = -40°C TO 85°C		T _A = -40°C TO 125°C		UNIT		
		MIN	MAX	MIN	MAX	MIN	MAX			
t _w	Pulse duration	SRCLK high or low		7		7.5		8.5		ns
		RCLK high or low		7		7.5		8.5		
		SRCLR low		6		6.5		7.5		
t _{su}	Setup time	SER before SRCLK↑		5.5		5.5		6.5		ns
		SRCLK↑ before RCLK↑ ⁽¹⁾		8		9		10		
		SRCLR low before RCLK↑		8.5		9.5		10.5		
		SRCLR high (inactive) before SRCLK↑		4		4		5		
t _h	Hold time	SER after SRCLK↑		1.5		1.5		2.5		ns

- (1) This setup time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.

TIMING REQUIREMENTS

over operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted)

		T _A = 25°C		T _A = -40°C TO 85°C		T _A = -40°C TO 125°C		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration	SRCLK high or low		5.5		5.5		ns
		RCLK high or low		5.5		5.5		
		SRCLR low		5		5		
t _{su}	Setup time	SER before SRCLK↑		3.5		3.5		ns
		SRCLK↑ before RCLK↑ ⁽¹⁾		8		8.5		
		SRCLR low before RCLK↑		8		9		
		SRCLR high (inactive) before SRCLK↑		3		3		
t _h	Hold time	SER after SRCLK↑		1.5		1.5		ns

- (1) This setup time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.

TIMING REQUIREMENTS

over operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted)

		T _A = 25°C		T _A = -40°C TO 85°C		T _A = -40°C TO 125°C		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration	SRCLK high or low		5		5		ns
		RCLK high or low		5		6		
		SRCLR low		5.2		5.2		
t _{su}	Setup time	SER before SRCLK↑		3		3		ns
		SRCLK↑ before RCLK↑ ⁽¹⁾		5		5		
		SRCLR low before RCLK↑		5		5		
		SRCLR high (inactive) before SRCLK↑		2.5		2.5		
t _h	Hold time	SER after SRCLK↑		2		2		ns

- (1) This setup time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$, $C_L = 50\text{ pF}$ (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ TO 85°C		$T_A = -40^\circ\text{C}$ TO 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{\max}$			60	70		40		30		MHz
t_{PLH}	RCLK	Q_A-Q_H		11.2	17.2	1	19.3	1	22.3	ns
t_{PHL}				11.2	17.2	1	19.3	1	22.3	ns
t_{PLH}	SRCLK	$Q_{H'}$		13.1	22.5	1	25.5	1	28.5	ns
t_{PHL}				13.1	22.5	1	25.5	1	28.5	ns
t_{PHL}	$\overline{\text{SRCLR}}$	$Q_{H'}$		12.4	18.8	1	21.1	1	24.1	ns
t_{PZH}	$\overline{\text{OE}}$	Q_A-Q_H		10.8	17	1	18.3	1	21.3	ns
t_{PZL}				13.4	21	1	23	1	26	ns
t_{PHZ}	$\overline{\text{OE}}$	Q_A-Q_H		12.2	18.3	1	19.5	1	22.5	ns
t_{PLZ}				14	20.9	1	22.6	1	25.6	ns

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$, $C_L = 50\text{ pF}$ (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ TO 85°C		$T_A = -40^\circ\text{C}$ TO 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{\max}$			55	105		50		40		MHz
t_{PLH}	RCLK	Q_A-Q_H		7.9	15.4	1	17	1	20	ns
t_{PHL}				7.9	15.4	1	17	1	20	ns
t_{PLH}	SRCLK	$Q_{H'}$		9.2	16.5	1	18.5	1	21.5	ns
t_{PHL}				9.2	16.5	1	18.5	1	21.5	ns
t_{PHL}	$\overline{\text{SRCLR}}$	$Q_{H'}$		9	16.3	1	17.2	1	20.2	ns
t_{PZH}	$\overline{\text{OE}}$	Q_A-Q_H		7.8	15	1	17	1	20	ns
t_{PZL}				9.6	15	1	17	1	20	ns
t_{PHZ}	$\overline{\text{OE}}$	Q_A-Q_H		8.1	15.7	1	16.2	1	19.2	ns
t_{PLZ}				9.3	15.7	1	16.2	1	19.2	ns

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$, $C_L = 50\text{ pF}$ (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ TO 85°C		$T_A = -40^\circ\text{C}$ TO 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{\max}$			95	140		85		75		MHz
t_{PLH}	RCLK	Q_A-Q_H		5.6	9.4	1	10.5	1	13.5	ns
t_{PHL}				5.6	9.4	1	10.5	1	13.5	ns
t_{PLH}	SRCLK	$Q_{H'}$		6.4	10.2	1	11.4	1	14.4	ns
t_{PHL}				6.4	10.2	1	11.4	1	14.4	ns
t_{PHL}	$\overline{\text{SRCLR}}$	$Q_{H'}$		6.4	10	1	11.1	1	14.1	ns
t_{PZH}	$\overline{\text{OE}}$	Q_A-Q_H		5.7	10.6	1	12	1	15	ns
t_{PZL}				6.8	10.6	1	12	1	15	ns
t_{PHZ}	$\overline{\text{OE}}$	Q_A-Q_H		3.5	10.3	1	11	1	14	ns
t_{PLZ}				3.4	10.3	1	11	1	14	ns

NOISE CHARACTERISTICS⁽¹⁾

 $V_{CC} = 3.3\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$

PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.3		V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.2		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		2.8		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

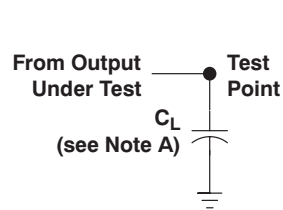
(1) Characteristics are for surface-mount packages only.

OPERATING CHARACTERISTICS

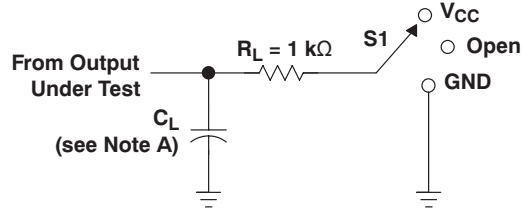
 $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	$C_L = 50\text{ pF}$, $f = 10\text{ MHz}$	$V_{CC} = 3.3\text{ V}$	111	pF
			$V_{CC} = 5\text{ V}$	114	

PARAMETER MEASUREMENT INFORMATION

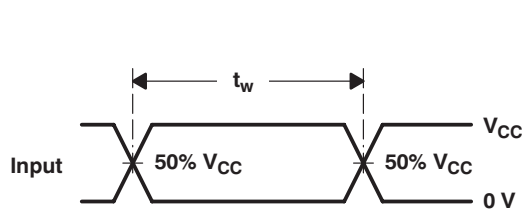


**LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS**

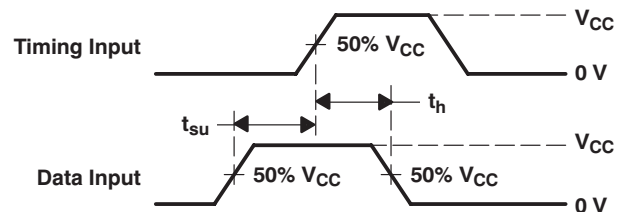


**LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS**

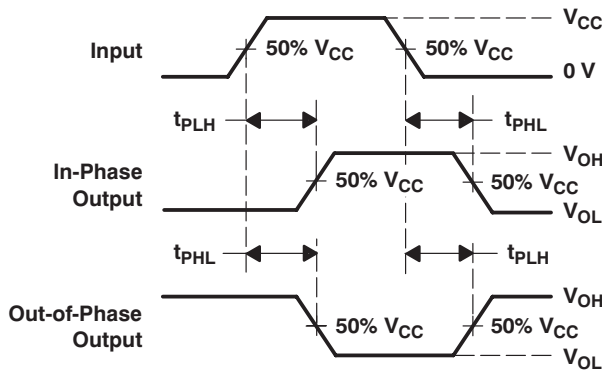
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}



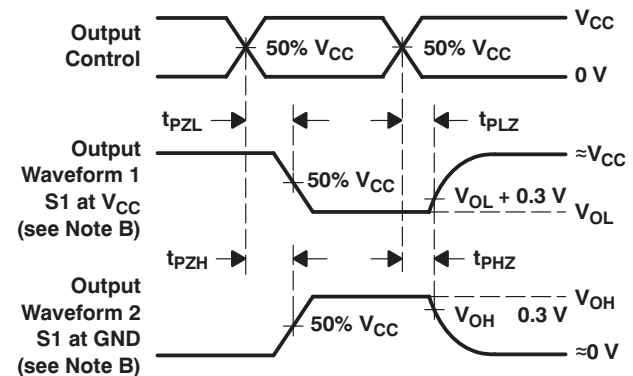
**VOLTAGE WAVEFORMS
PULSE DURATION**



**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS**



**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING**

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 - The outputs are measured one at a time, with one input transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PHL} and t_{PLH} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV595AIPWRG4Q1	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV595AI	Samples
SN74LV595AIPWRQ1	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 85	LV595AI	Samples
SN74LV595AQWRQ1	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV595AQ	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LV595A-Q1 :

- Catalog: [SN74LV595A](#)
- Enhanced Product: [SN74LV595A-EP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION


*All dimensions are nominal

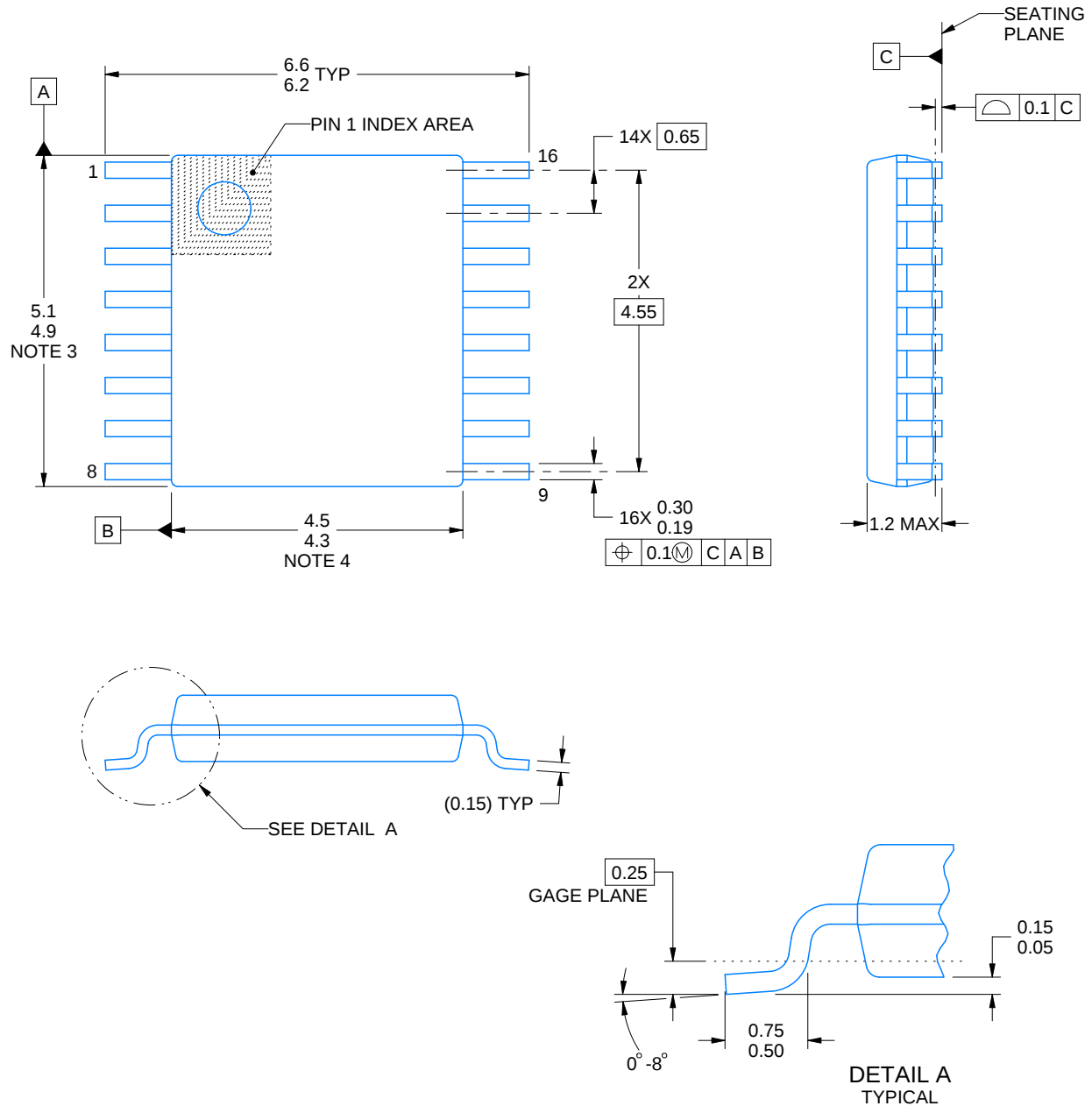
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV595AIPWRG4Q1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV595AIPWRQ1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV595AQPWRQ1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV595AIPWRG4Q1	TSSOP	PW	16	2000	367.0	367.0	35.0
SN74LV595AIPWRQ1	TSSOP	PW	16	2000	367.0	367.0	35.0
SN74LV595AQPWRQ1	TSSOP	PW	16	2000	367.0	367.0	35.0



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NOTES:

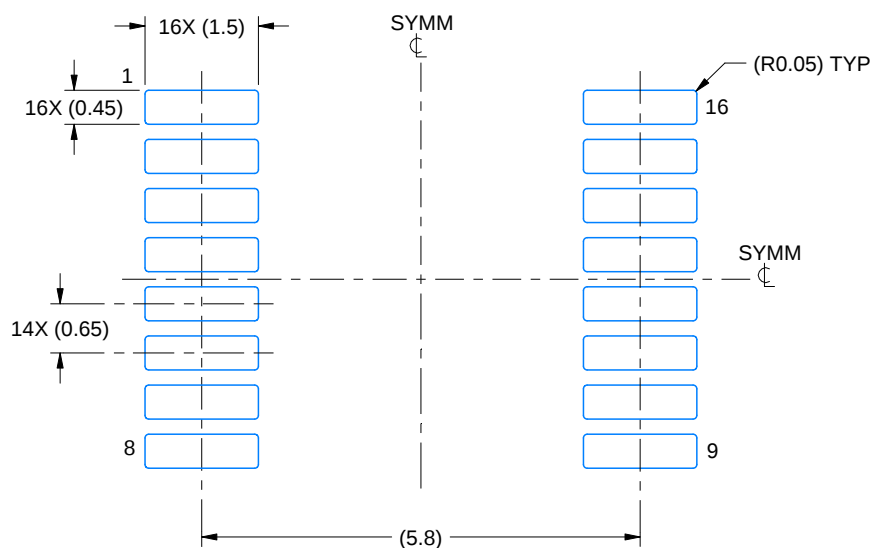
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

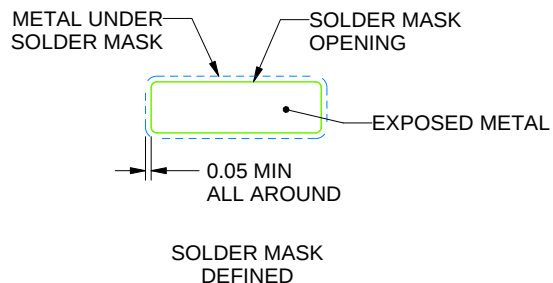
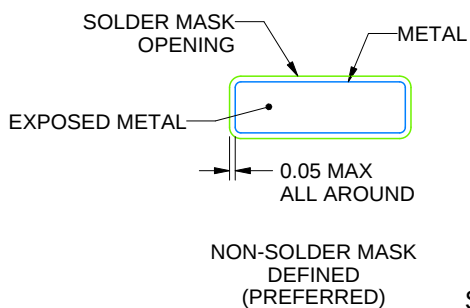
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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