DS91M040
125 MHz Quad M-LVDS Transceiver Evaluation Kit

USER MANUAL

Part Number: DS91M040EVK NOPB

For the latest documents concerning these products and evaluation kit, visit lvds.national.com. Schematics and gerber files are also available at lvds.national.com

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Overview

The purpose of this document is to familiarize you with the DS91M040 evaluation board, suggest the test setup procedures and instrumentation, and to guide you through some typical measurements that will demonstrate the performance of the device.

The primary function of the board is to assist system designers in development and analysis of M-LVDS clock distribution networks in ATCA backplanes. The board also enables the user to examine performance and all functions of the DS91M040 as a standalone device or in a point-to-point configuration.

The DS91M040 is a high-speed quad M-LVDS differential transceiver designed for multipoint applications with multiple drivers or receivers. The device conforms to TIA/EIA-899 standard. It utilizes M-LVDS technology for low power, high-speed and superior noise immunity.

Description

Figure 1 below represents the top layer drawing of the board with the silkscreen annotations. It is a 4 x 3 inch 10 layer printed circuit board (PCB) that features two DS91M040 (U1-U2) devices.

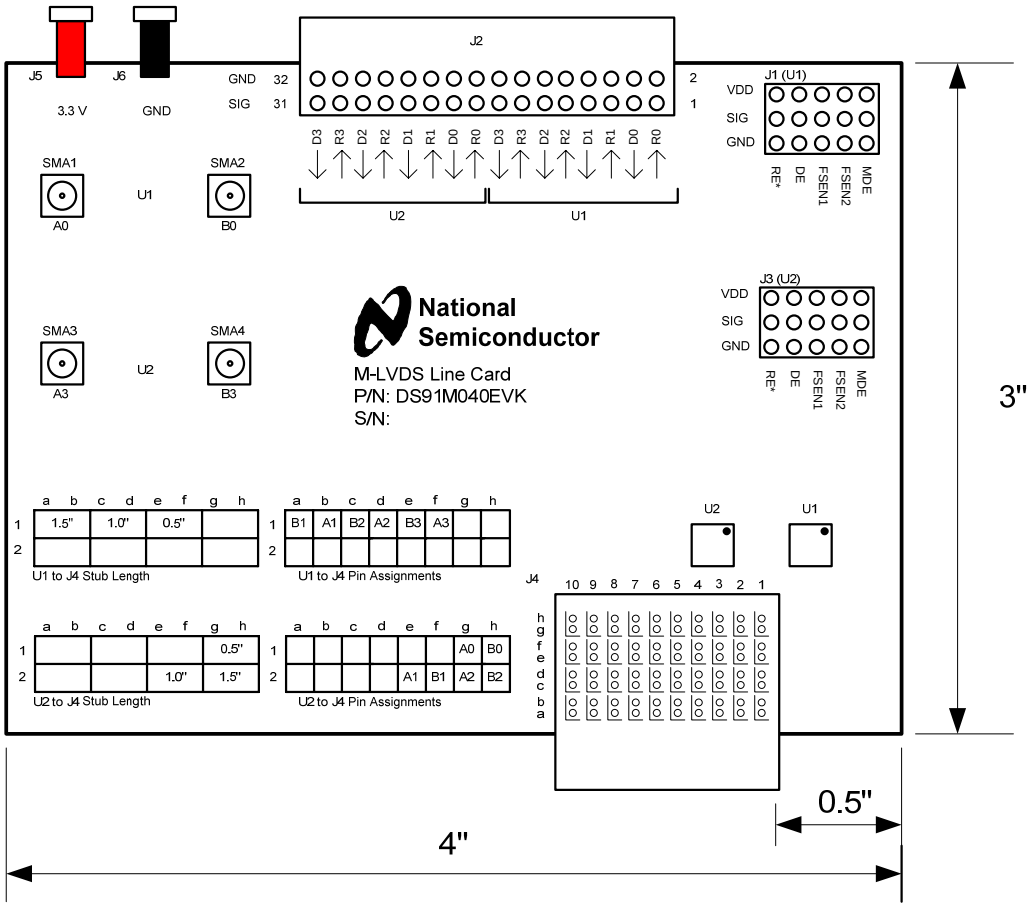


Figure 1 - DS91M040EVK Top View Drawing

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Each device (U1 or U2) has four channels. The three M-LVDS channels of each device directly connect to the first two rows of J4, which is an ADF (Advanced Differential Fabric) connector. When J4 is inserted into any ATCA backplane slot (location J20/P20 for those of you familiar with ATCA backplanes), the M-LVDS I/O pins of each device electrically connect to one of the clock busses (there are six clock busses in an ATCA backplane – See Figure 2).

The remaining M-LVDS channel of each device connects to the SMA connectors for device standalone evaluation or evaluation in point-to-point links.

Table 1 provides M-LVDS I/O pin to J4 pin (and stub length) or SMA connector mapping and LVCMOS pins to J2 pin mapping.

Device	M-LVDS Pins	J4 Pins / SMA Connector	Stub Length	LVCMOS Pins	J2 Pins
U1	A0 B0	SMA1 SMA2	NA	R0 D0	1 3
U1	A1 B1	B1 A1	1.50”	R1 D1	5 7
U1	A2 B2	D1 C1	1.00”	R2 D2	9 11
U1	A3 B3	F1 E1	0.50”	R3 D3	13 15
U2	A0 B0	G1 H1	0.50”	R0 D0	17 19
U2	A1 B1	E2 F2	1.00”	R1 D1	21 23
U2	A2 B2	G2 H2	1.50”	R2 D2	25 27
U2	A3 B3	SMA3 SMA4	NA	R3 D3	29 31

Table 1 - U1 and U2 Pin to Connector Pin Mapping

J1 provides easy connection to U1 control pins. Refer to the DS91M040 datasheet for the device pin descriptions.

J3 provides easy connection to U2 control pins. Refer to the DS91M040 datasheet for the device pin descriptions.

J5 and J6 are power and ground connections.

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DS91M040 Evaluation in an ATCA Backplane

The following is a recommended procedure for building an evaluation M-LVDS clock distribution network with DS91M040EVK evaluation boards. The assumption is that the user already has an ATCA backplane. Figure 2 depicts configuration of a generic M-LVDS clock network in an ATCA backplane.

1. Use two or more DS91M040 evaluation boards and install them at backplane location J20/P20, in the desired slots.

2. Apply the power to the boards (3.3V typical) between J5 and J6 banana plug receptacles, observe the value of $I_{CC,}$ and compare it with the expected value (refer to the datasheet) to ensure that the devices are functional.

3. Select the board you want to configure as a clock driver/distributor. This is accomplished by setting DE and RE* pins to VDD (J1 or J3). Set MDE pin to VDD. Connect a clock source to one of the driver inputs (J2).

4. Configure the remaining boards as clock receivers. This is accomplished by setting DE and RE* pins to GND (J1 or J3). Set MDE pin to VDD. Set the receiver to either M-LVDS Type 1 (FSEN pins set to GND) or Type 2 (FSEN pins set to VDD).

5. Observe clock waveforms by either connecting receiver LVCMOS output pins (J2) directly to an oscilloscope or by probing receiver M-LVDS input pins with a differential probe.

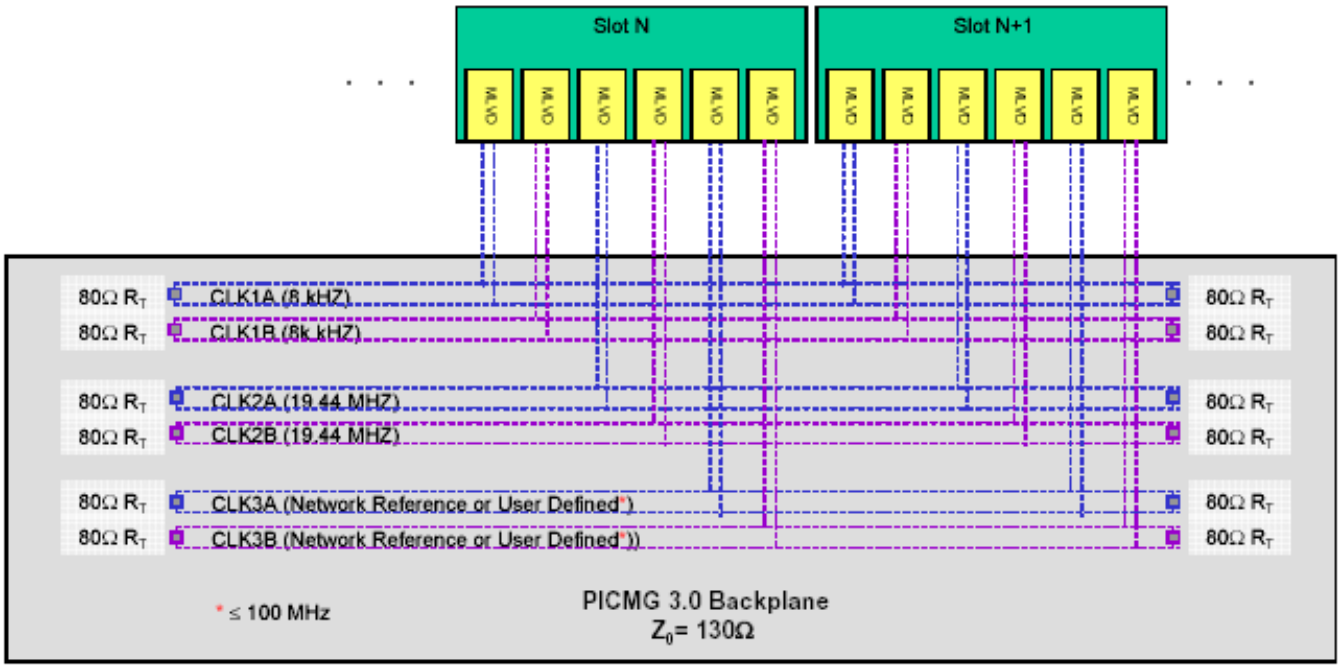


Figure 2 - M-LVDS Clock Distribution Network in an ATCA Backplane

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The block diagram of Figure 2 details a clock distribution network in an ATCA backplane. The clock busses have 130-ohm differential impedance and are doubly terminated with 80 ohms at either end of the backplane. The parallel combination of 80-ohm resistors means that the MLVDS devices will be driving a 40-ohm load termination. The maximum stub length from the backplane is defined in the ATCA standard as 1 inch or 2.54 cm.
Figure 3 shows a picture of a 14-slot ATCA backplane fully populated with DS91M040 evaluation boards.

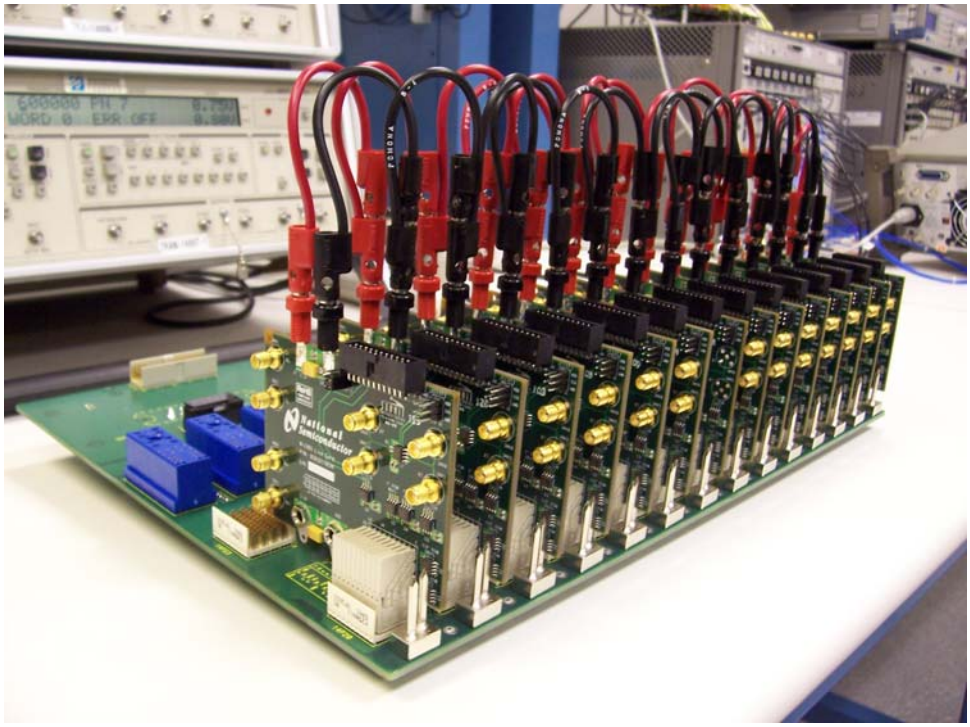


Figure 3 - DS91M040 Evaluation Boards in an ATCA Backplane

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Figure 4 shows 19.44 MHz clock waveforms obtained with a differential probe, Tektronix P6330, on the M-LVDS input pins of the device on a receiver board in slot #8. The14-slot backplane was fully populated. The clock driver/distributor board was in slot #7.

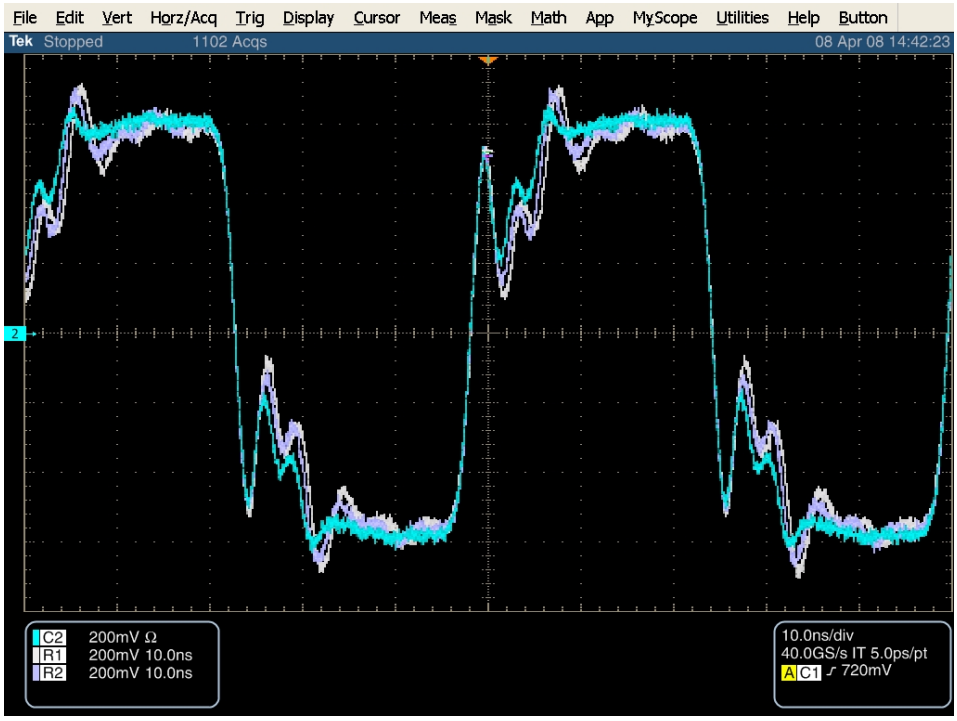


Figure 4 - 19.44 MHz Clock Waveforms Show Stub Length Effects on Signal Integrity

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DS91M040 Evaluation in a Point-to-Point Link

The following is a recommended procedure for building an evaluation M-LVDS point-point network with DS91M040 evaluation boards. Figure 5 depicts a typical setup and instrumentation used for evaluation of a point-to-point link.

1. Use a single DS91M040 evaluation board.

2. Apply the power to the board (3.3 V typical) between J5 and J6 banana plug receptacles, observe the value of $I_{CC,}$ and compare it with the expected value (refer to the datasheet) to ensure that the devices are functional.

3. Configure U1 as a driver. This is accomplished by setting DE and RE* pins to VDD (J1). Connect a signal source to the driver inputs (J2, pin 3).

4. Configure U2 as a receiver. This is accomplished by setting DE and RE* pins to GND (J3).

5. Select a differential interconnect with balanced 100-ohm differential impedance (i.e. UTP cable) and connect the M-LVDS pins of both devices through SMA connectors (SMA1 and SMA2 for U1 driver outputs; SMA3 and SMA4 for U2 receiver inputs ;). You may want to consider developing / obtaining an SMA to RJ45 adapter board for easy interface from SMA connectors to twisted pair cables. See the following link: http://www.national.com/appinfo/lvds/sma2rj45evk.html.

6. Terminate the interconnect with a matching resistor on the inputs of the U2 receiver (R2).

7. Observe waveforms by either connecting the receiver LVCMOS output pin (J2, pin 29) directly to an oscilloscope or by probing receiver M-LVDS input pins with a differential probe.

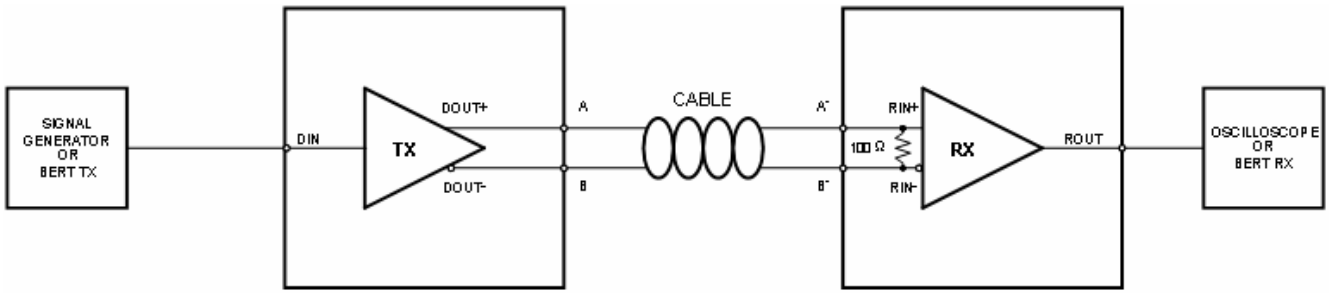


Figure 5 - M-LVDS Point-to-Point Link with DS91M040 Boards and UTP Cable

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Figure 6 shows eye diagrams acquired at the output of the DS91M040 driver loaded with a 100-ohm resistor and after 50 m CAT5e cable terminated with a 100-ohm resistor. The generator connected to the driver input simulated a 100 Mbps PRBS-7 NRZ.

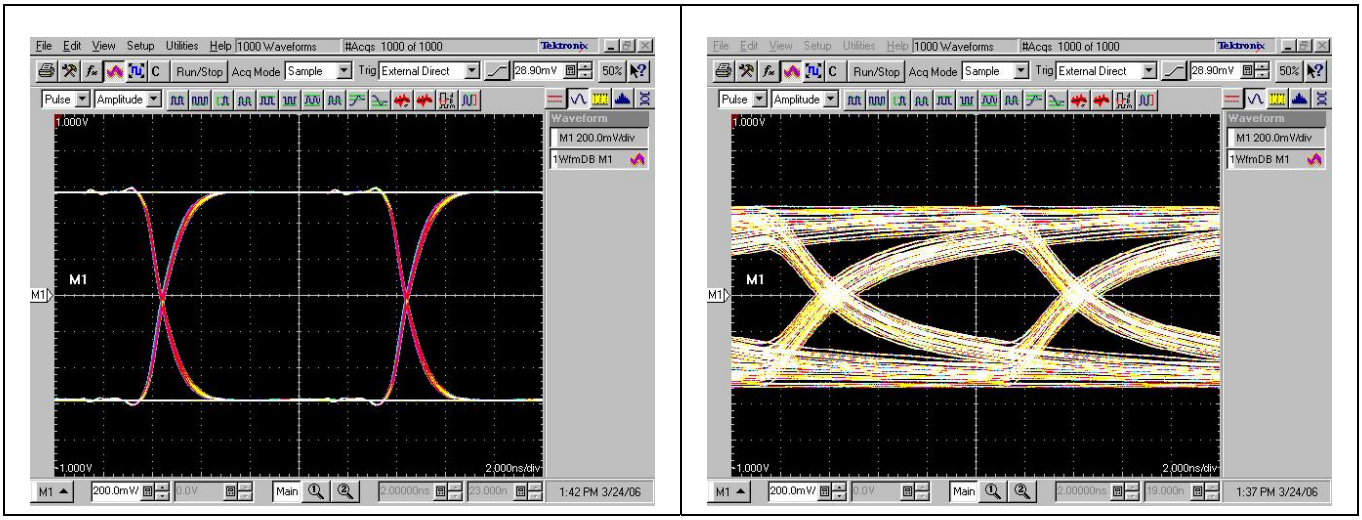


Figure 6 - Eye Diagram Before and After 50m of CAT5e

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