OMAP3530 and OMAP3525 Applications Processors

Check for Samples: OMAP3530, OMAP3525

1 OMAP3530 and OMAP3525 Applications Processors

1.1 Features

- OMAP3530 and OMAP3525 Devices:
  - OMAP™ 3 Architecture
  - MPU Subsystem
    - Up to 720-MHz ARM® Cortex™-A8 Core
    - NEON™ SIMD Coprocessor
  - High-Performance Image, Video, Audio (IVA2.2™) Accelerator Subsystem
    - Up to 520-MHz TMS320C64x+™ DSP Core
    - Enhanced Direct Memory Access (EDMA) Controller (128 Independent Channels)
    - Video Hardware Accelerators
  - PowerVR® SGX™ Graphics Accelerator (OMAP3530 Device Only)
    - Tile-Based Architecture Delivering up to 10 MPoly/sec
    - Universal Scalable Shader Engine: Multi-threaded Engine Incorporating Pixel and Vertex Shader Functionality
    - Industry Standard API Support: OpenGLES 1.1 and 2.0, OpenVG1.0
    - Fine-Grained Task Switching, Load Balancing, and Power Management
    - Programmable High-Quality Image Anti-Aliasing
  - Fully Software-Compatible with C64x and ARM9™
  - Commercial and Extended Temperature Grades
- Advanced Very-Long-Instruction-Word (VLIW) TMS320C64x+ DSP Core
  - Eight Highly Independent Functional Units
    - Six ALUs (32- and 40-Bit), Each Supports Single 32-Bit, Dual 16-Bit, or Quad 8-Bit Arithmetic per Clock Cycle
    - Two Multipliers Support Four 16 x 16-Bit Multiplies (32-Bit Results) per Clock Cycle or Eight 8 x 8-Bit Multiplies (16-Bit Results) per Clock Cycle
  - Load-Store Architecture with Nonaligned Support
  - 64 32-Bit General-Purpose Registers
  - Instruction Packing Reduces Code Size
  - All Instructions Conditional
  - Additional C64x+ Enhancements
    - Protected Mode Operation
    - Exceptions Support for Error Detection and Program Redirection
    - Hardware Support for Modulo Loop Operation
- C64x+ L1 and L2 Memory Architecture
  - 32KB of L1P Program RAM and Cache (Direct Mapped)
  - 80KB of L1D Data RAM and Cache (2-Way Set-Associative)
  - 64KB of L2 Unified Mapped RAM and Cache (4-Way Set-Associative)
  - 32KB of L2 Shared SRAM and 16KB of L2 ROM
- C64x+ Instruction Set Features
  - Byte-Addressable (8-, 16-, 32-, and 64-Bit Data)
  - 8-Bit Overflow Protection
  - Bit Field Extract, Set, Clear
  - Normalization, Saturation, Bit-Counting
  - Compact 16-Bit Instructions
  - Additional Instructions to Support Complex Multiplies
- ARM Cortex-A8 Core
  - ARMv7 Architecture
    - TrustZone®
    - Thumb®-2
    - MMU Enhancements
  - In-Order, Dual-Issue, Superscalar Microprocessor Core
  - NEON Multimedia Architecture
  - Over 2x Performance of ARMv6 SIMD
  - Supports Both Integer and Floating-Point SIMD
  - Jazelle® RCT Execution Environment Architecture
  - Dynamic Branch Prediction with Branch Target Address Cache, Global History Buffer, and 8-Entry Return Stack
  - Embedded Trace Macrocell (ETM) Support for Noninvasive Debug
- ARM Cortex-A8 Memory Architecture:
  - 16-KB Instruction Cache (4-Way Set-

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Associative)
  - 16-KB Data Cache (4-Way Set-Associative)
  - 256-KB L2 Cache
- 112KB of ROM
- 64KB of Shared SRAM
- Endianess:
  - ARM Instructions – Little Endian
  - ARM Data – Configurable
  - DSP Instruction and Data - Little Endian
- External Memory Interfaces:
  - SDRAM Controller (SDRC)
    - 16- and 32-Bit Memory Controller with 1GB of Total Address Space
    - Interfaces to Low-Power Double Data Rate (LPDDR) SDRAM
    - SDRAM Memory Scheduler (SMS) and Rotation Engine
  - General Purpose Memory Controller (GPMC)
    - 16-Bit-Wide Multiplexed Address and Data Bus
    - Up to 8 Chip-Select Pins with 128-MB Address Space per Chip-Select Pin
    - Glueless Interface to NOR Flash, NAND Flash (with ECC Hamming Code Calculation), SRAM, and Pseudo-SRAM
    - Flexible Asynchronous Protocol Control for Interface to Custom Logic (FPGA, CPLD, ASICs, and so forth)
    - Nonmultiplexed Address and Data Mode (Limited 2-KB Address Space)
- System Direct Memory Access (sDMA) Controller (32 Logical Channels with Configurable Priority)
- Camera Image Signal Processor (ISP)
  - CCD and CMOS Imager Interface
  - Memory Data Input
  - BT.601 (8-Bit) and BT.656 (10-Bit) Digital YCbCr 4:2:2 Interface
  - Glueless Interface to Common Video Decoders
  - Resize Engine
    - Resize Images From 1/4x to 4x
    - Separate Horizontal and Vertical Control
- Display Subsystem
  - Parallel Digital Output
    - Up to 24-Bit RGB
    - HD Maximum Resolution
    - Supports Up to 2 LCD Panels
    - Support for Remote Frame Buffer Interface (RFBI) LCD Panels
  - 2 10-Bit Digital-to-Analog Converters (DACs) Supporting:
    - Composite NTSC and PAL Video
    - Luma and Chroma Separate Video (S-Video)
  - Rotation 90-, 180-, and 270-Degrees
  - Resize Images From 1/4x to 8x
  - Color Space Converter
  - 8-Bit Alpha Blending
- Serial Communication
  - 5 Multichannel Buffered Serial Ports (McBSPs)
    - 512-Byte Transmit and Receive Buffer (McBSP1, McBSP3, McBSP4, and McBSP5)
    - 5-KB Transmit and Receive Buffer (McBSP2)
    - SIDETONE Core Support (McBSP2 and McBSP3 Only) For Filter, Gain, and Mix Operations
    - Direct Interface to I2S and PCM Device and TDM Buses
    - 128-Channel Transmit and Receive Mode
  - Four Master or Slave Multichannel Serial Port Interface (McSPI) Ports
  - High-, Full-, and Low-Speed USB OTG Subsystem (12- and 8-Pin ULPI Interface)
  - High-, Full-, and Low-Speed Multiport USB Host Subsystem
    - 12- and 8-Pin ULPI Interface or 6-, 4-, and 3-Pin Serial Interface
    - Supports Transceiverless Link Logic (TLL)
  - One HDQ™/1-Wire® Interface
  - Three UARTs (One with Infrared Data Association [IrDA] and Consumer Infrared [CIR] Modes)
  - Three Master and Slave High-Speed Inter-Integrated Circuit (I^2C) Controllers
- Removable Media Interfaces:
  - Three Multimedia Card (MMC)/Secure Digital (SD) with Secure Data I/O (SDIO)
- Comprehensive Power, Reset, and Clock Management
  - SmartReflex™ Technology
  - Dynamic Voltage and Frequency Scaling (DVFS)
- Test Interfaces
  - IEEE 1149.1 (JTAG) Boundary-Scan Compatible
  - ETM Interface
  - Serial Data Transport Interface (SDTI)
- 12 32-Bit General-Purpose Timers
- 2 32-Bit Watchdog Timers
- 1 32-Bit 32-kHz Sync Timer
- Up to 188 General-Purpose I/O (GPIO) Pins (Multiplexed with Other Device Functions)

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- **65-nm CMOS Technologies**
- **Package-On-Package (POP) Implementation for Memory Stacking (Not Available in CUS Package)**
- **Discrete Memory Interface (Not Available in CBC Package)**
- **Packages:**
  - **515-pin s-PBGA Package (CBB Suffix), .5-mm Ball Pitch (Top), .4-mm Ball Pitch (Bottom)**
  - **515-pin s-PBGA Package (CBC Suffix), .65-mm Ball Pitch (Top), .5-mm Ball Pitch (Bottom)**
  - **423-pin s-PBGA Package (CUS Suffix), .65-mm Ball Pitch**
- **1.8-V I/O and 3.0-V (MMC1 Only), 0.985-V to 1.35-V Adaptive Processor Core Voltage 0.985-V to 1.35-V Adaptive Core Logic Voltage Note: These are default Operating Performance Point (OPP) voltages and could be optimized to lower values using SmartReflex AVS.**

1.2 Applications

- **Portable Navigation Devices**
- **Portable Media Player**
- **Digital Video Camera**
- **Portable Data Collection**
- **Point-of-Sale Devices**
- **Gaming**
- **Web Tablet**
- **Smart White Goods**
- **Smart Home Controllers**

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1.3 Description

OMAP3530 and OMAP3525 devices are based on the enhanced OMAP 3 architecture.

The OMAP 3 architecture is designed to provide best-in-class video, image, and graphics processing sufficient to support the following:

- Streaming video
- Video conferencing
- High-resolution still image

The device supports high-level operating systems (HLOSs), such as:

- Linux®
- Windows® CE
- Android™

This OMAP device includes state-of-the-art power-management techniques required for high-performance mobile products.

The following subsystems are part of the device:

- Microprocessor unit (MPU) subsystem based on the ARM Cortex-A8 microprocessor
- IVA2.2 subsystem with a C64x+ digital signal processor (DSP) core
- PowerVR SGX subsystem for 3D graphics acceleration to support display (OMAP3530 device only)
- Camera image signal processor (ISP) that supports multiple formats and interfacing options connected to a wide variety of image sensors
- Display subsystem with a wide variety of features for multiple concurrent image manipulation, and a programmable interface supporting a wide variety of displays. The display subsystem also supports NTSC and PAL video out.
- Level 3 (L3) and level 4 (L4) interconnects that provide high-bandwidth data transfers for multiple initiators to the internal and external memory controllers and to on-chip peripherals

The device also offers:

- A comprehensive power- and clock-management scheme that enables high-performance, low-power operation, and ultralow-power standby features. The device also supports SmartReflex adaptative voltage control. This power-management technique for automatic control of the operating voltage of a module reduces the active power consumption.
- Memory-stacking feature using the package-on-package (POP) implementation (CBB and CBC packages only)

OMAP3530 and OMAP3525 devices are available in a 515-pin s-PBGA package (CBB suffix), 515-pin s-PBGA package (CBC suffix), and a 423-pin s-PBGA package (CUS suffix). Some features of the CBB and CBC packages are not available in the CUS package. (See Table 1-1 for package differences).

This data manual presents the electrical and mechanical specifications for the OMAP3530 and OMAP3525 applications processors. The information in this data manual applies to both the commercial and extended temperature versions of the OMAP3530 and OMAP3525 applications processors unless otherwise indicated. This data manual consists of the following sections:

- Section 2, *Terminal Description*: assignment, electrical characteristics, multiplexing, and functional description
- Section 3, *Electrical Characteristics*: power domains, operating conditions, power consumption, and DC characteristics
- Section 4, *Clock Specifications*: input and output clocks, DPLL and DLL
- Section 5, *Video DAC Specifications*
- Section 6, *Timing Requirements and Switching Characteristics*
- Section 7, *Package Characteristics*: thermal characteristics, device nomenclature, and mechanical data for available packaging

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1.4 Functional Block Diagram

Figure 1-1 shows the functional block diagram of the OMAP3530 and OMAP3525 applications processors.

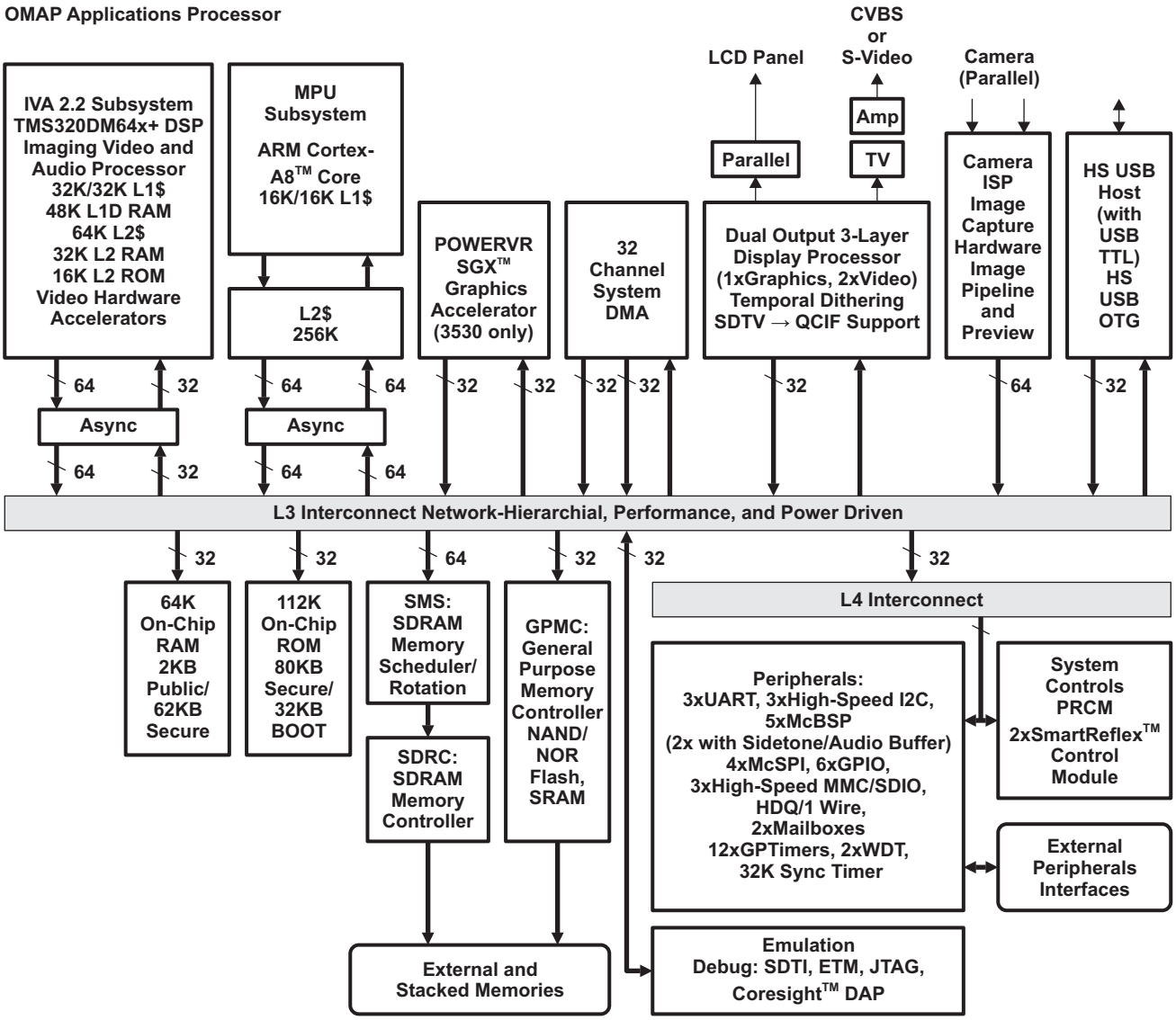

Figure 1-1. OMAP3530 and OMAP3525 Device Functional Block Diagram

Table 1-1. Differences Between CBB, CBC, and CUS Packages

FEATURE	CBB PACKAGE	CBC PACKAGE	CUS PACKAGE
Pin Assignments	For CBB package pin assignments see Table 2-1, *Ball Characteristics (CBB Pkg.)*	For CBC package pin assignments see Table 2-2, *Ball Characteristics (CBC Pkg.)*	For CUS package pin assignments see Table 2-3, *Ball Characteristics (CUS Pkg.)*
Package-On-Package (POP) Interface	POP interface supported	POP interface supported	POP interface not available
Discrete Memory Interface	Discrete Memory Interface supported	Discrete Memory Interface not supported	Discrete Memory Interface supported
GPMC	Eight chip-select pins available	Eight chip-select pins available	Chip-select pins gpmc_ncs1 and gpmc_ncs2 are not available
	Four wait pins available	Four wait pins available	Wait pins gpmc_wait1 and gpmc_wait2 are not available
UART1	CTS signal is available on 3 pins (triple muxed): uart1_cts (AG22 / W8 / T21), uart1_rts (AH22 / AA9), uart1_tx (F28 / Y8 / AE7), uart1_rx (E26 / AA8)	The following signals are either available on two (double muxed) or three pins (triple muxed): uart1_cts (AE21 / T19 / W2), uart1_rts (AE22 / R2), uart1_rx (H3 / H25 / AE4), uart1_tx (L4 / G26)	CTS signal is available on 3 pins (triple muxed): uart1_cts (AC19 / AC2 / AA18), uart1_rts (W6 / AB19), uart1_tx (E23 / V7 / AC3), uart1_rx (D24 / W7)
UART2	The following signals are available on two pins (double muxed): uart2_cts (AF6/AB26), uart2_rts (AE6/AB25), uart2_tx (AF5/AA25), uart2_rx (AE5/AD25)	The following signals are available on two pins (double muxed): uart2_cts (Y24/P3), uart2_rts (AA24/N3), uart2_tx (AD22/U3), uart2_rx (AD21/W3)	The following signals are available on one pin only: uart2_cts (V6), uart2_rts (V5), uart2_tx (W4), uart2_rx (V4)
McBSP3	The following signals are available on three pins (triple muxed): mcbsp3_dx (AF6 / AB26 / V21), mcbsp3_dr (AE6 / AB25 / U21), mcbsp3_clkx (AF5 / AA25 / W21), and mcbsp3_fsx (AE5 / AD25 / K26)	The following signals are available on two pins (triple muxed): mcbsp3_dx (U17/ Y24/ P3), mcbsp3_dr (T20/ AA24 / N3), mcbsp3_clkx (T17/ AD22 / U3), mcbsp3_fsx (P20/ AD21 / W3)	The following signals are available on two pins only (double muxed): mcbsp3_dx (V6/W18), mcbsp3_dr (V5/Y18), mcbsp3_clkx (W4/V18), and mcbsp3_fsx (V4/AA19)
GP Timer	The following signals are available on three pins (triple muxed): gpt8_pwm_evt (N8 / AD25 / V3), gpt9_pwm_evt (T8 / AB26 / Y2), gpt10_pwm_evt (R8 / AB25 / Y3), and gpt11_pwm_evt (P8 / AA25 / Y4)	The following signals are available on three pins (triple muxed): gpt8_pwm_evt (C5/AD21/V9), gpt9_pwm_evt (B4/W8/Y24), gpt10_pwm_evt(C4/U8/AA24), gpt11_pwm_evt(B5/V8/AD22)	The following signals are available on two pins only (double muxed): gpt8_pwm_evt (G4/M4), gpt9_pwm_evt (F4/N4), gpt10_pwm_evt (G5/N3), and gpt11_pwm_evt (F3/M5)
McBSP4	The following signals are available on two pins (double muxed): mcbsp4_clkx (T8/AE1), mcbsp4_dr (R8/AD1), mcbsp4_dx (P8/AD2), mcbsp4_fsx (N8/AC1)	The following signals are available on two pins (double muxed): mcbsp4_clkx (B4 / V3), mcbsp4_dr (C4 / U4), mcbsp4_dx (B5 / R3), mcbsp4_fsx (C5 / T3)	The following signals are available on one pin only: mcbsp4_clkx (F4), mcbsp4_dr (G5), mcbsp4_dx (F3), mcbsp4_fsx (G4)
HSUSB3_TLL	Supported	Supported	Not supported
MM_FSUSB3	Supported	Supported	Not supported
McSPI1	Four chip-select pins are available	Four chip-select pins are available	Chip-select pins mcspi1_cs1 and mcspi_cs2 are not available
MMC3	The following signals are available on two pins (double muxed): mmc3_cmd (AC3 / AE10), and mmc3_clk (AB1 / AF10)	The following signals are available on two pins (double muxed): mmc3_cmd (R8 / AB3), mmc3_clk (R9 / AB2)	The following signals are available on one pin only: mmc3_cmd (AD3), and mmc3_clk (AC1)

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Table 1-1. Differences Between CBB, CBC, and CUS Packages (continued)

FEATURE	CBB PACKAGE	CBC PACKAGE	CUS PACKAGE
GPIO	A maximum of 188 GPIO pins are supported.	A maximum of 188 GPIO pins are supported.	A maximum of 170 GPIO pins are supported. The following GPIO pins are not available: gpio_112, gpio_113, gpio_114, gpio_115, gpio_52, gpio_53, gpio_63, gpio_64, gpio_144, gpio_145, gpio_146, gpio_147, gpio_152, gpio_153, gpio_154, gpio_155, gpio_175, and gpio_176. Pin muxing restricts the total number of GPIO pins available at one time. For more details, see Table 2-4, *Multiplexing Characteristics (CUS Pkg.)*.

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

This data manual revision history table highlights the technical changes made to the SPRS507F device-specific data manual to make it an SPRS507H revision.

SEE	ADDITIONS/MODIFICATIONS/DELETIONS
General	• Added Android to list of supported Operating Systems • 3D Mobile Gaming not supported • Updated/Changed incorrect cross-references
Section 1.2 Applications	• Created Applications section • Updated/Changed supported applications
Table 1-1 Differences Between CBB, CBC, and CUS Packages	• Moved table to appear after the Functional Block Diagram • Updated/Changed the GPIO FEATURE row CUS PACKAGE column "For more details, see ..." cross-reference to *Multiplexing Characteristics (CUS Pkg.)* table
Section 3.3 Recommended Operating Conditions	• Added the paragraph, "The information in the notes below....."
Section 6.5.1 Camera Interface	• Updated/Changed the paragraph, "The camera subsystem provides..."

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2 TERMINAL DESCRIPTION

2.1 Terminal Assignment

Figure 2-1 through Figure 2-5 show the ball locations for the 515- and 423- ball plastic ball grid array (s-PBGA) packages. through Table 2-25 indicate the signal names and ball grid numbers for both packages.

Note: There are no balls present on the top of the 423-ball s-PBGA package.

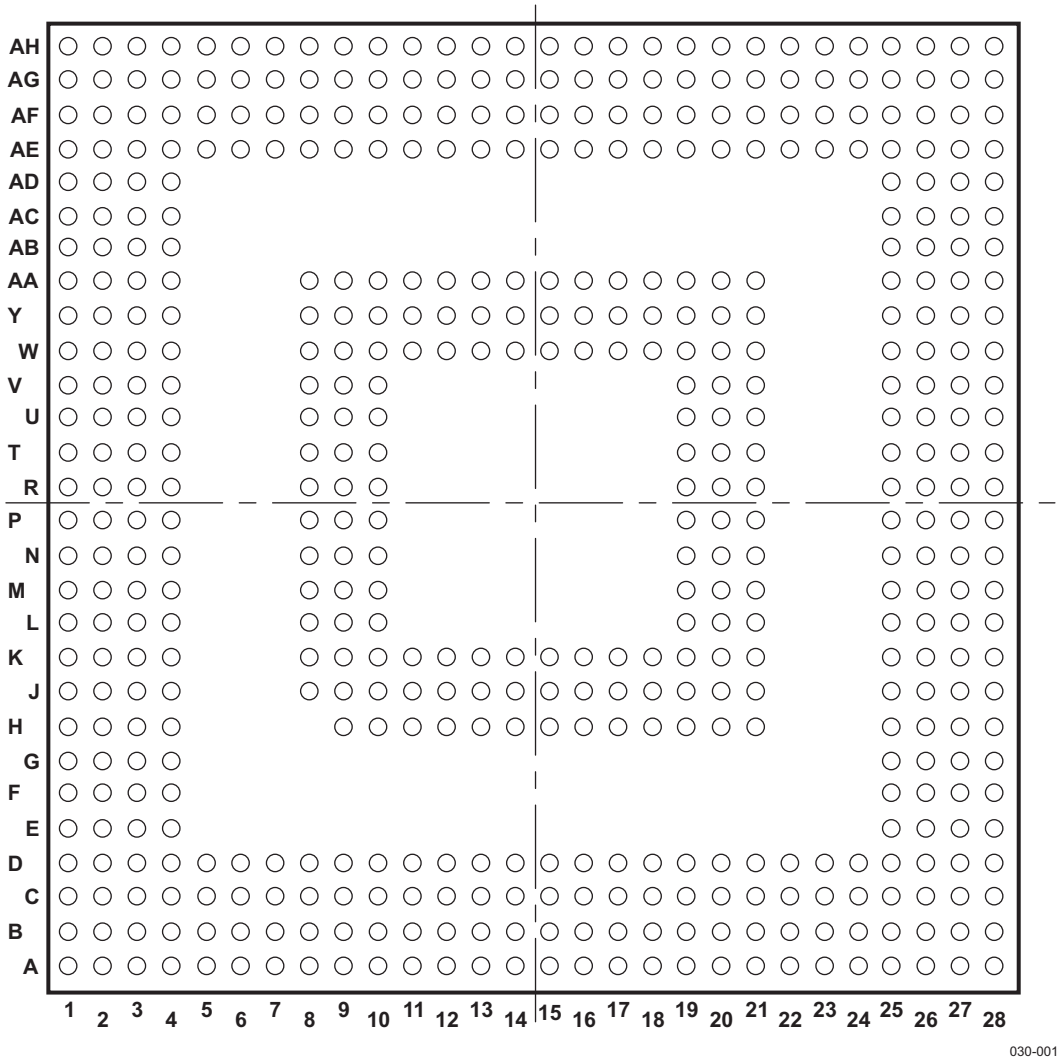

Figure 2-1. OMAP3530/25 Applications Processor CBB s-PBGA-N515 Package (Bottom View)

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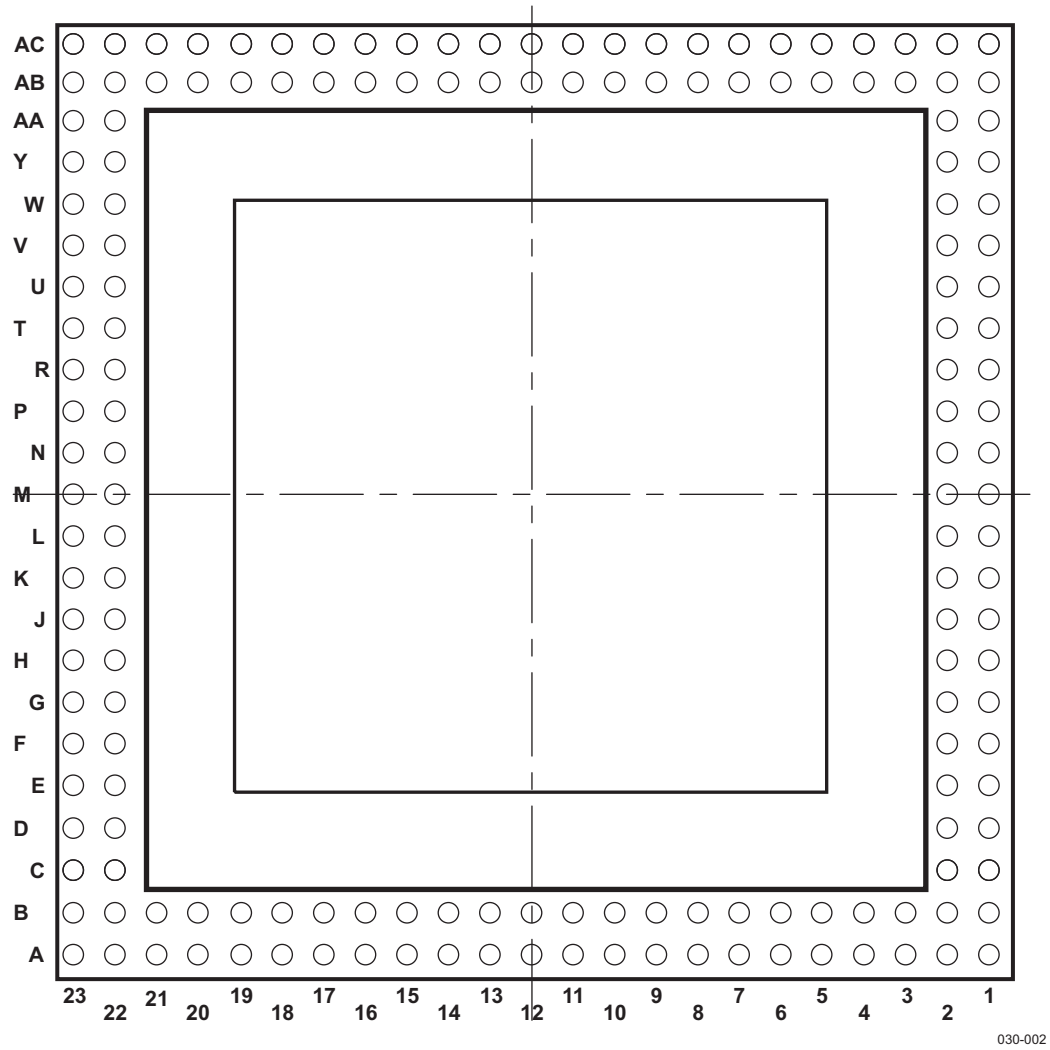

Balls A1, A2, A22, A23, AB1, AB2, AB22, AB23, AC1, AC2, AC22, AC23, B1, B2, B22, and B23 are unused.

Figure 2-2. OMAP3530/25 Applications Processor CBB s-PBGA-N515 Package (Top View)

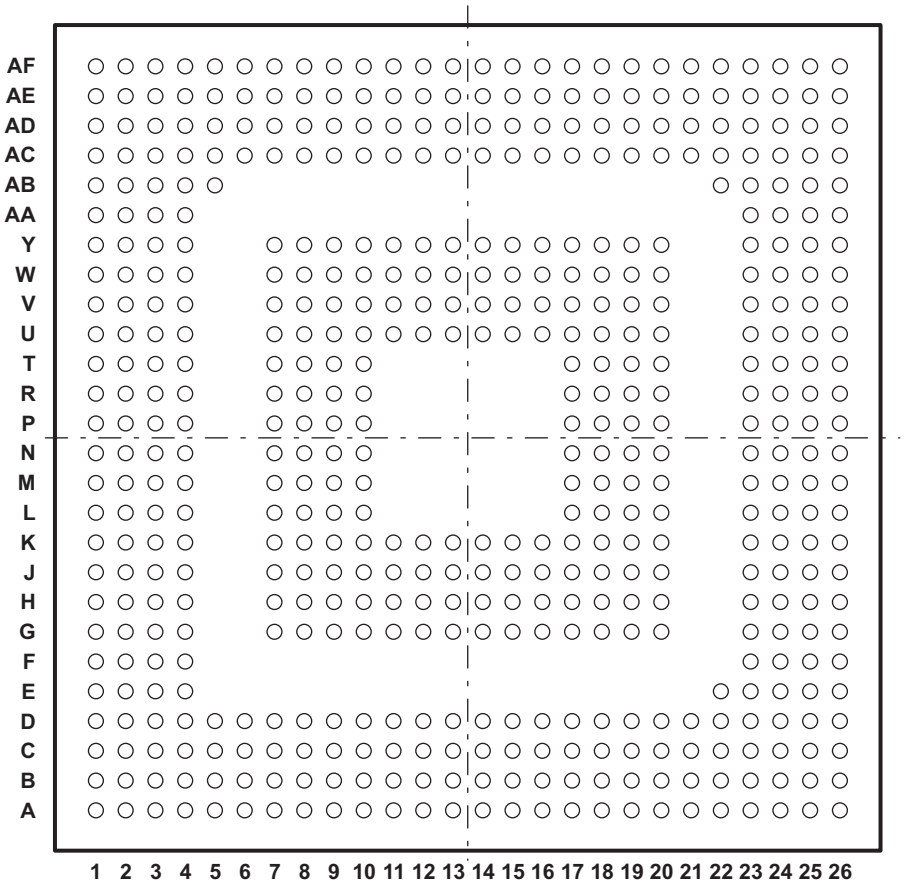

Figure 2-3. OMAP3530/25 Applications Processor CBC s-PBGA-515 Package (Bottom View)

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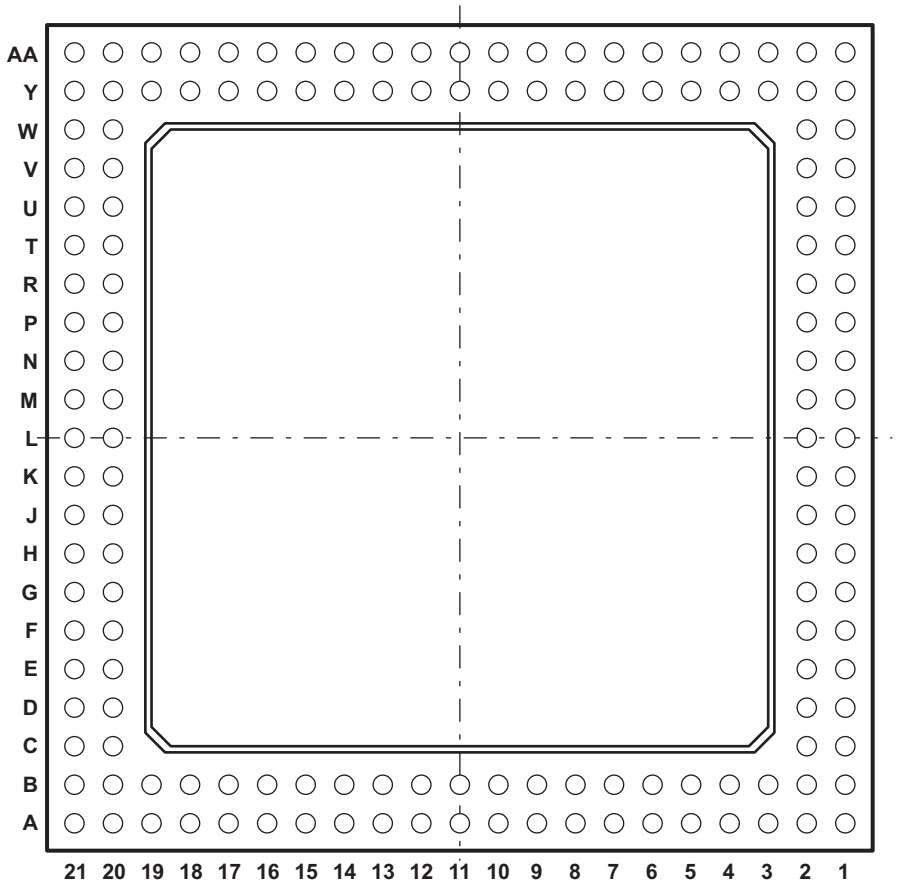

Figure 2-4. OMAP3530/25 Applications Processor CBC s-PBGA-515 Package (Top View)

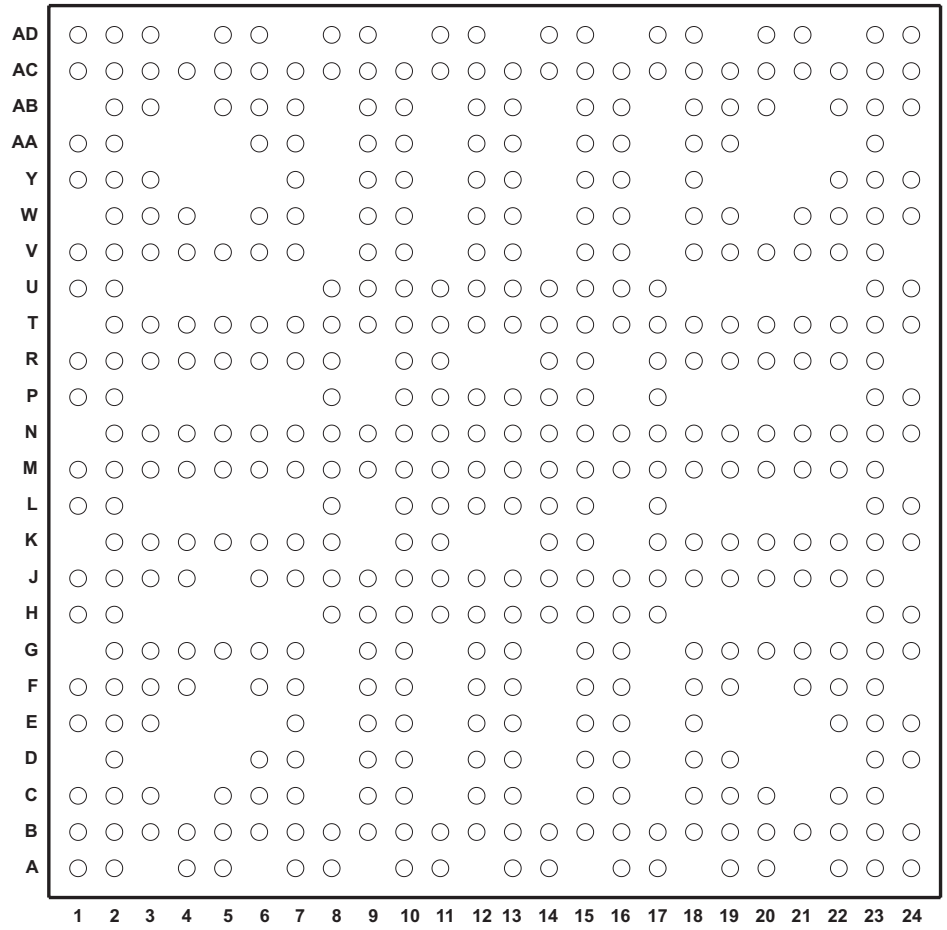

Figure 2-5. OMAP3530/25 Applications Processor CUS s-PBGA-N423 Package (Bottom View)

2.2 Pin Assignments

2.2.1 Pin Map (Top View)

The following pin maps show the top views of the 515-pin sPBGA package **[CBB]**, the 515-pin sPBGA package **[CBC]**, and the 423-pin sPBGA package **[CUS]** pin assignments in four quadrants (A, B, C, and D).

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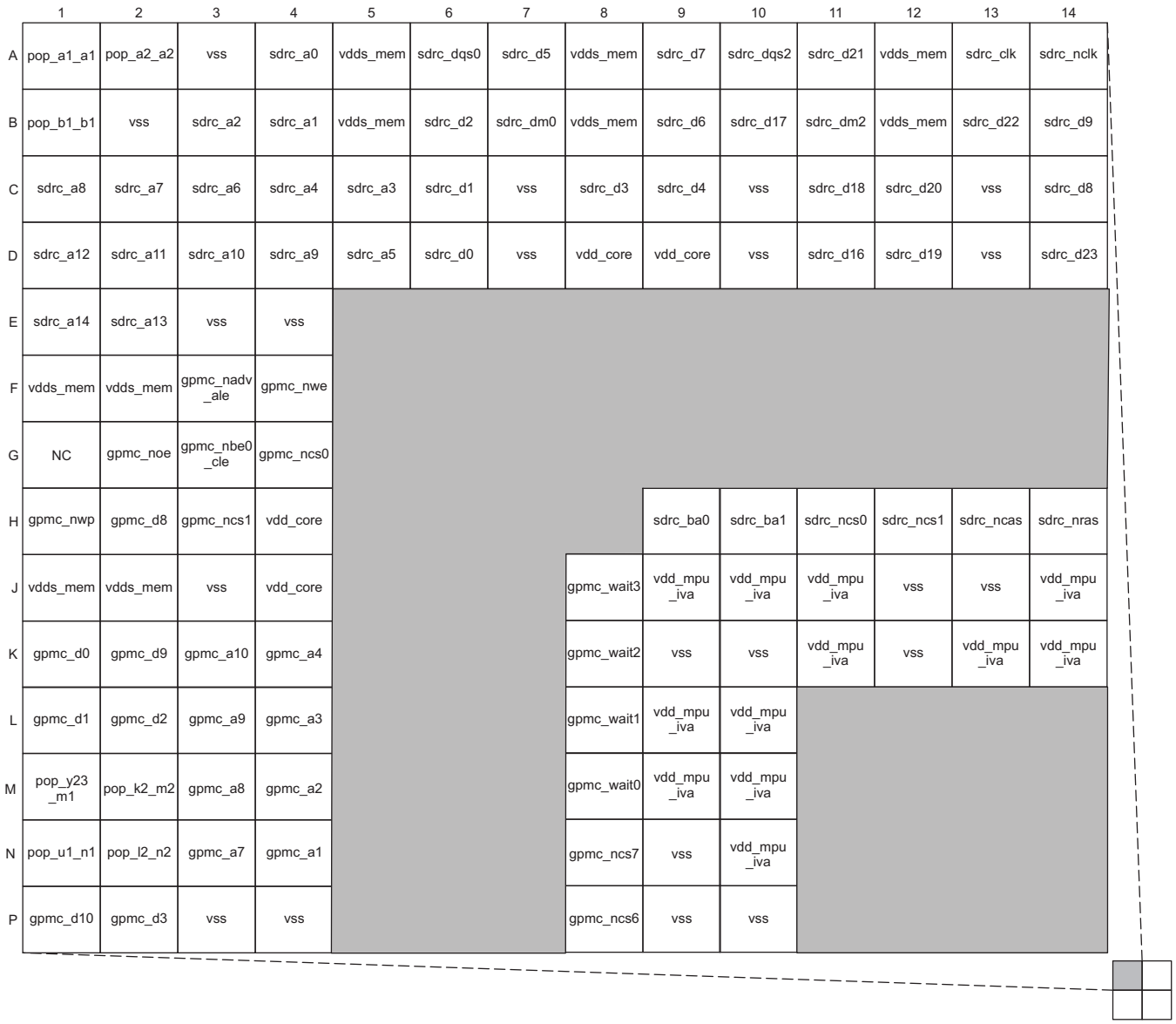
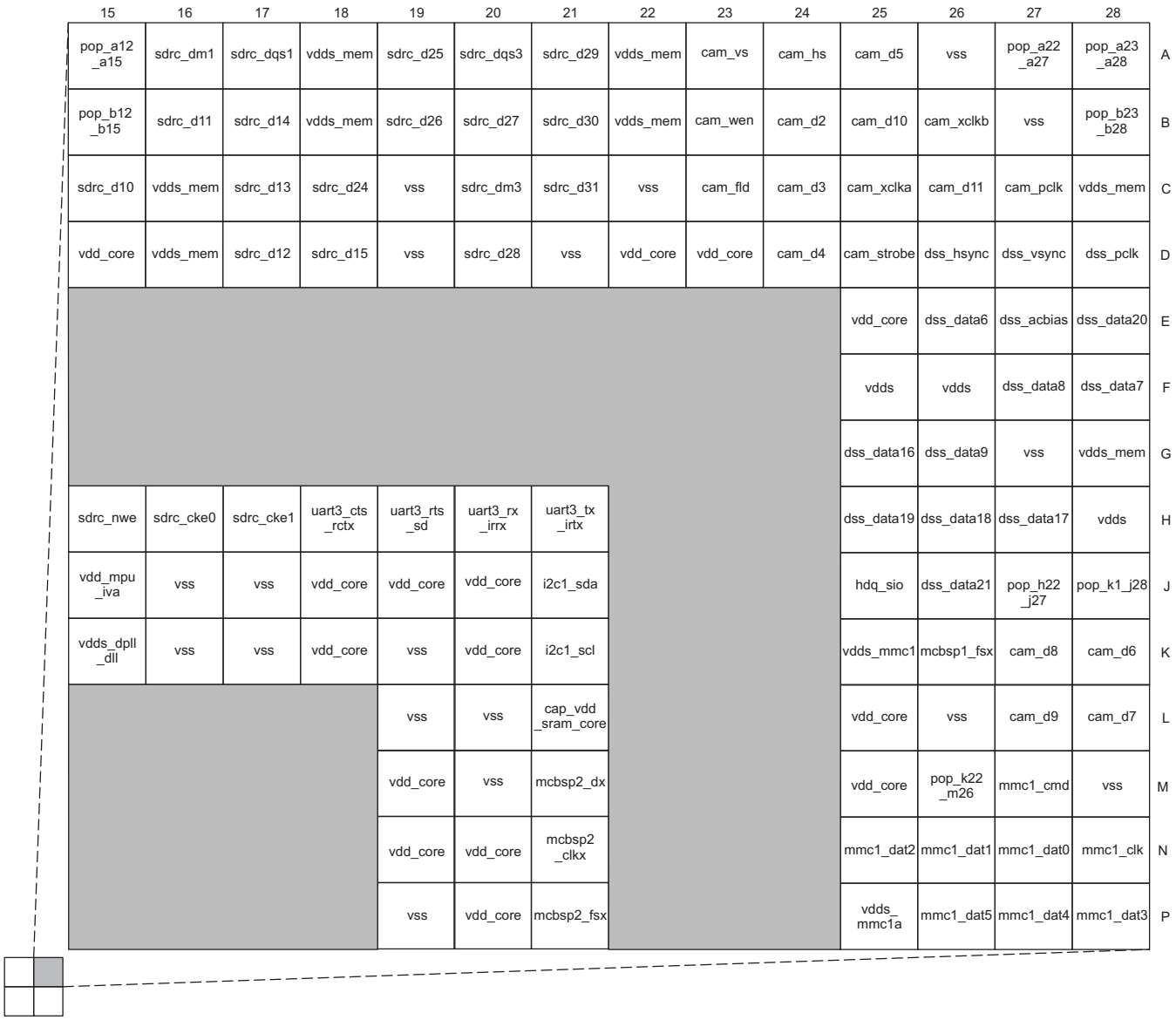


	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	pop_a1_a1	pop_a2_a2	vss	sdrc_a0	vdds_mem	sdrc_dqs0	sdrc_d5	vdds_mem	sdrc_d7	sdrc_dqs2	sdrc_d21	vdds_mem	sdrc_clk	sdrc_nclk
B	pop_b1_b1	vss	sdrc_a2	sdrc_a1	vdds_mem	sdrc_d2	sdrc_dm0	vdds_mem	sdrc_d6	sdrc_d17	sdrc_dm2	vdds_mem	sdrc_d22	sdrc_d9
C	sdrc_a8	sdrc_a7	sdrc_a6	sdrc_a4	sdrc_a3	sdrc_d1	vss	sdrc_d3	sdrc_d4	vss	sdrc_d18	sdrc_d20	vss	sdrc_d8
D	sdrc_a12	sdrc_a11	sdrc_a10	sdrc_a9	sdrc_a5	sdrc_d0	vss	vdd_core	vdd_core	vss	sdrc_d16	sdrc_d19	vss	sdrc_d23
E	sdrc_a14	sdrc_a13	vss	vss										
F	vdds_mem	vdds_mem	gpmc_nadv_ale	gpmc_nwe										
G	NC	gpmc_noe	gpmc_nbe0_cle	gpmc_ncs0										
H	gpmc_nwp	gpmc_d8	gpmc_ncs1	vdd_core					sdrc_ba0	sdrc_ba1	sdrc_ncs0	sdrc_ncs1	sdrc_ncas	sdrc_nras
J	vdds_mem	vdds_mem	vss	vdd_core				gpmc_wait3	vdd_mpu_iva	vdd_mpu_iva	vdd_mpu_iva	vss	vss	vdd_mpu_iva
K	gpmc_d0	gpmc_d9	gpmc_a10	gpmc_a4				gpmc_wait2	vss	vss	vdd_mpu_iva	vss	vdd_mpu_iva	vdd_mpu_iva
L	gpmc_d1	gpmc_d2	gpmc_a9	gpmc_a3				gpmc_wait1	vdd_mpu_iva	vdd_mpu_iva				
M	pop_y23_m1	pop_k2_m2	gpmc_a8	gpmc_a2				gpmc_wait0	vdd_mpu_iva	vdd_mpu_iva				
N	pop_u1_n1	pop_l2_n2	gpmc_a7	gpmc_a1				gpmc_ncs7	vss	vdd_mpu_iva				
P	gpmc_d10	gpmc_d3	vss	vss				gpmc_ncs6	vss	vss				

A. Top Views are provided to assist in hardware debugging efforts.

Figure 2-6. CBB Pin Map [Quadrant A - Top View]



	15	16	17	18	19	20	21	22	23	24	25	26	27	28	
A	pop_a12 _a15	sdrc_dm1	sdrc_dqs1	vdds_mem	sdrc_d25	sdrc_dqs3	sdrc_d29	vdds_mem	cam_vs	cam_hs	cam_d5	vss	pop_a22 _a27	pop_a23 _a28	A
B	pop_b12 _b15	sdrc_d11	sdrc_d14	vdds_mem	sdrc_d26	sdrc_d27	sdrc_d30	vdds_mem	cam_wen	cam_d2	cam_d10	cam_xclkb	vss	pop_b23 _b28	B
C	sdrc_d10	vdds_mem	sdrc_d13	sdrc_d24	vss	sdrc_dm3	sdrc_d31	vss	cam_fld	cam_d3	cam_xclka	cam_d11	cam_pclk	vdds_mem	C
D	vdd_core	vdds_mem	sdrc_d12	sdrc_d15	vss	sdrc_d28	vss	vdd_core	vdd_core	cam_d4	cam_strobe	dss_hsync	dss_vsync	dss_pclk	D
E											vdd_core	dss_data6	dss_acbias	dss_data20	E
F											vdds	vdds	dss_data8	dss_data7	F
G											dss_data16	dss_data9	vss	vdds_mem	G
H	sdrc_nwe	sdrc_cke0	sdrc_cke1	uart3_cts _rctx	uart3_rts _sd	uart3_rx _irrx	uart3_tx _irtx				dss_data19	dss_data18	dss_data17	vdds	H
J	vdd_mpu _iva	vss	vss	vdd_core	vdd_core	vdd_core	i2c1_sda				hdq_sio	dss_data21	pop_h22 _j27	pop_k1_j28	J
K	vdds_dpll _dll	vss	vss	vdd_core	vss	vdd_core	i2c1_scl				vdds_mmc1	mcbsp1_fsx	cam_d8	cam_d6	K
L					vss	vss	cap_vdd _sram_core				vdd_core	vss	cam_d9	cam_d7	L
M					vdd_core	vss	mcbsp2_dx				vdd_core	pop_k22 _m26	mmc1_cmd	vss	M
N					vdd_core	vdd_core	mcbsp2 _clkx				mmc1_dat2	mmc1_dat1	mmc1_dat0	mmc1_clk	N
P					vss	vdd_core	mcbsp2_fsx				vdds_ mmc1a	mmc1_dat5	mmc1_dat4	mmc1_dat3	P

Figure 2-7. CBB Pin Map [Quadrant B - Top View]

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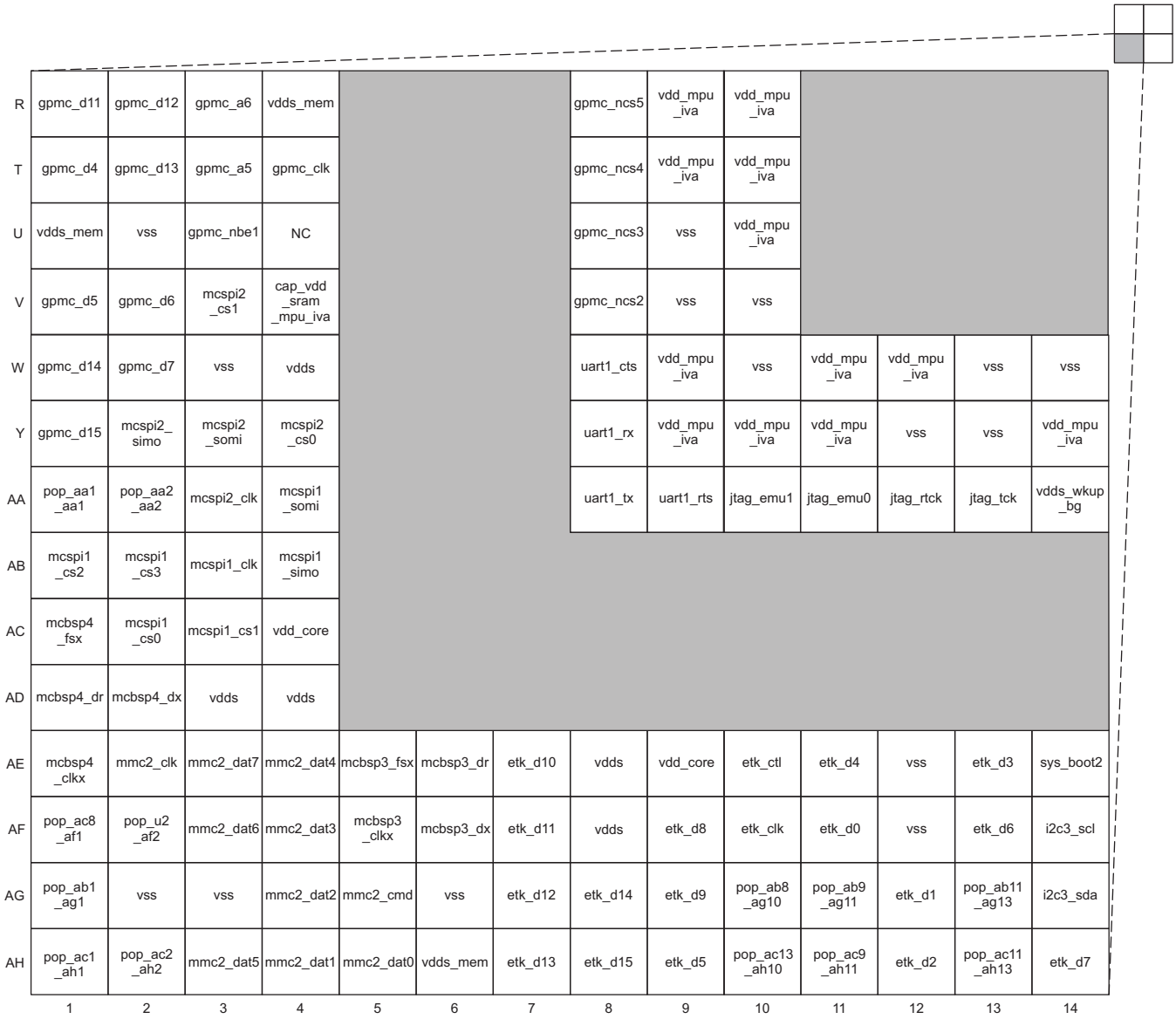
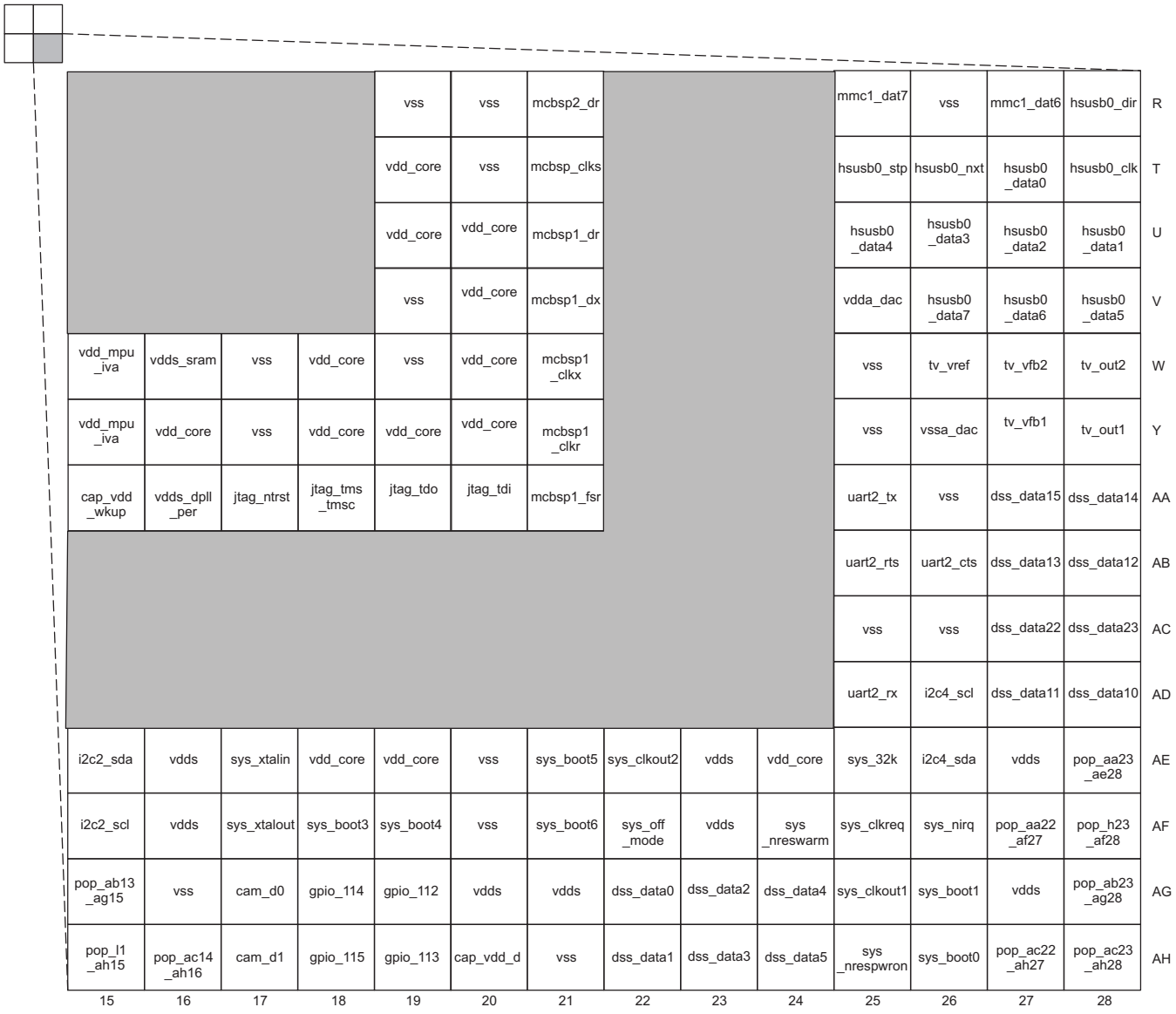


	1	2	3	4	5	6	7	8	9	10	11	12	13	14
R	gpmc_d11	gpmc_d12	gpmc_a6	vdds_mem				gpmc_ncs5	vdd_mpu_iva	vdd_mpu_iva				
T	gpmc_d4	gpmc_d13	gpmc_a5	gpmc_clk				gpmc_ncs4	vdd_mpu_iva	vdd_mpu_iva				
U	vdds_mem	vss	gpmc_nbe1	NC				gpmc_ncs3	vss	vdd_mpu_iva				
V	gpmc_d5	gpmc_d6	mcspi2_cs1	cap_vdd_sram_mpu_iva				gpmc_ncs2	vss	vss				
W	gpmc_d14	gpmc_d7	vss	vdds				uart1_cts	vdd_mpu_iva	vss	vdd_mpu_iva	vdd_mpu_iva	vss	vss
Y	gpmc_d15	mcspi2_simo	mcspi2_somi	mcspi2_cs0				uart1_rx	vdd_mpu_iva	vdd_mpu_iva	vdd_mpu_iva	vss	vss	vdd_mpu_iva
AA	pop_aa1_aa1	pop_aa2_aa2	mcspi2_clk	mcspi1_somi				uart1_tx	uart1_rts	jtag_emu1	jtag_emu0	jtag_rtck	jtag_tck	vdds_wkup_bg
AB	mcspi1_cs2	mcspi1_cs3	mcspi1_clk	mcspi1_simo										
AC	mcbsp4_fsx	mcspi1_cs0	mcspi1_cs1	vdd_core										
AD	mcbsp4_dr	mcbsp4_dx	vdds	vdds										
AE	mcbsp4_clkx	mmc2_clk	mmc2_dat7	mmc2_dat4	mcbsp3_fsx	mcbsp3_dr	etk_d10	vdds	vdd_core	etk_ctl	etk_d4	vss	etk_d3	sys_boot2
AF	pop_ac8_af1	pop_u2_af2	mmc2_dat6	mmc2_dat3	mcbsp3_clkx	mcbsp3_dx	etk_d11	vdds	etk_d8	etk_clk	etk_d0	vss	etk_d6	i2c3_scl
AG	pop_ab1_ag1	vss	vss	mmc2_dat2	mmc2_cmd	vss	etk_d12	etk_d14	etk_d9	pop_ab8_ag10	pop_ab9_ag11	etk_d1	pop_ab11_ag13	i2c3_sda
AH	pop_ac1_ah1	pop_ac2_ah2	mmc2_dat5	mmc2_dat1	mmc2_dat0	vdds_mem	etk_d13	etk_d15	etk_d5	pop_ac13_ah10	pop_ac9_ah11	etk_d2	pop_ac11_ah13	etk_d7

Figure 2-8. CBB Pin Map [Quadrant C - Top View]



	15	16	17	18	19	20	21	22	23	24	25	26	27	28	
R					vss	vss	mcbsp2_dr				mmc1_dat7	vss	mmc1_dat6	hsusb0_dir	R
T					vdd_core	vss	mcbsp_clks				hsusb0_stp	hsusb0_nxt	hsusb0 _data0	hsusb0_clk	T
U					vdd_core	vdd_core	mcbsp1_dr				hsusb0 _data4	hsusb0 _data3	hsusb0 _data2	hsusb0 _data1	U
V					vss	vdd_core	mcbsp1_dx				vdda_dac	hsusb0 _data7	hsusb0 _data6	hsusb0 _data5	V
W	vdd_mpu _iva	vdds_sram	vss	vdd_core	vss	vdd_core	mcbsp1 _clkx				vss	tv_vref	tv_vfb2	tv_out2	W
Y	vdd_mpu _iva	vdd_core	vss	vdd_core	vdd_core	vdd_core	mcbsp1 _clkr				vss	vssa_dac	tv_vfb1	tv_out1	Y
AA	cap_vdd _wkup	vdds_dpll _per	jtag_ntrst	jtag_tms _tmsc	jtag_tdo	jtag_tdi	mcbsp1_fsr				uart2_tx	vss	dss_data15	dss_data14	AA
AB											uart2_rts	uart2_cts	dss_data13	dss_data12	AB
AC											vss	vss	dss_data22	dss_data23	AC
AD											uart2_rx	i2c4_scl	dss_data11	dss_data10	AD
AE	i2c2_sda	vdds	sys_xtalin	vdd_core	vdd_core	vss	sys_boot5	sys_clkout2	vdds	vdd_core	sys_32k	i2c4_sda	vdds	pop_aa23 _ae28	AE
AF	i2c2_scl	vdds	sys_xtalout	sys_boot3	sys_boot4	vss	sys_boot6	sys_off _mode	vdds	sys _nreswarm	sys_clkreq	sys_nirq	pop_aa22 _af27	pop_h23 _af28	AF
AG	pop_ab13 _ag15	vss	cam_d0	gpio_114	gpio_112	vdds	vdds	dss_data0	dss_data2	dss_data4	sys_clkout1	sys_boot1	vdds	pop_ab23 _ag28	AG
AH	pop_l1 _ah15	pop_ac14 _ah16	cam_d1	gpio_115	gpio_113	cap_vdd_d	vss	dss_data1	dss_data3	dss_data5	sys _nrespwron	sys_boot0	pop_ac22 _ah27	pop_ac23 _ah28	AH

Figure 2-9. CBB Pin Map [Quadrant D - Top View]

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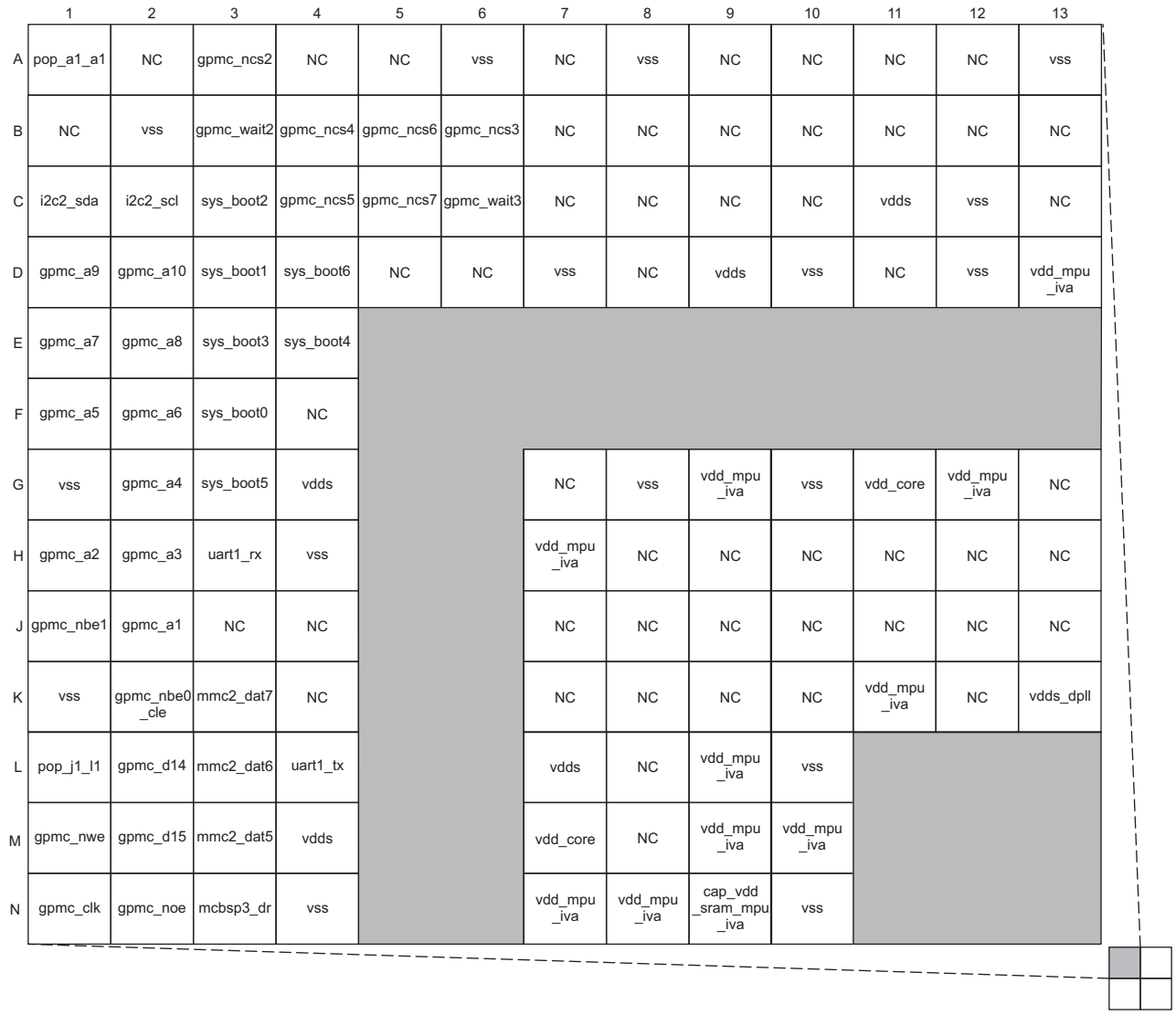
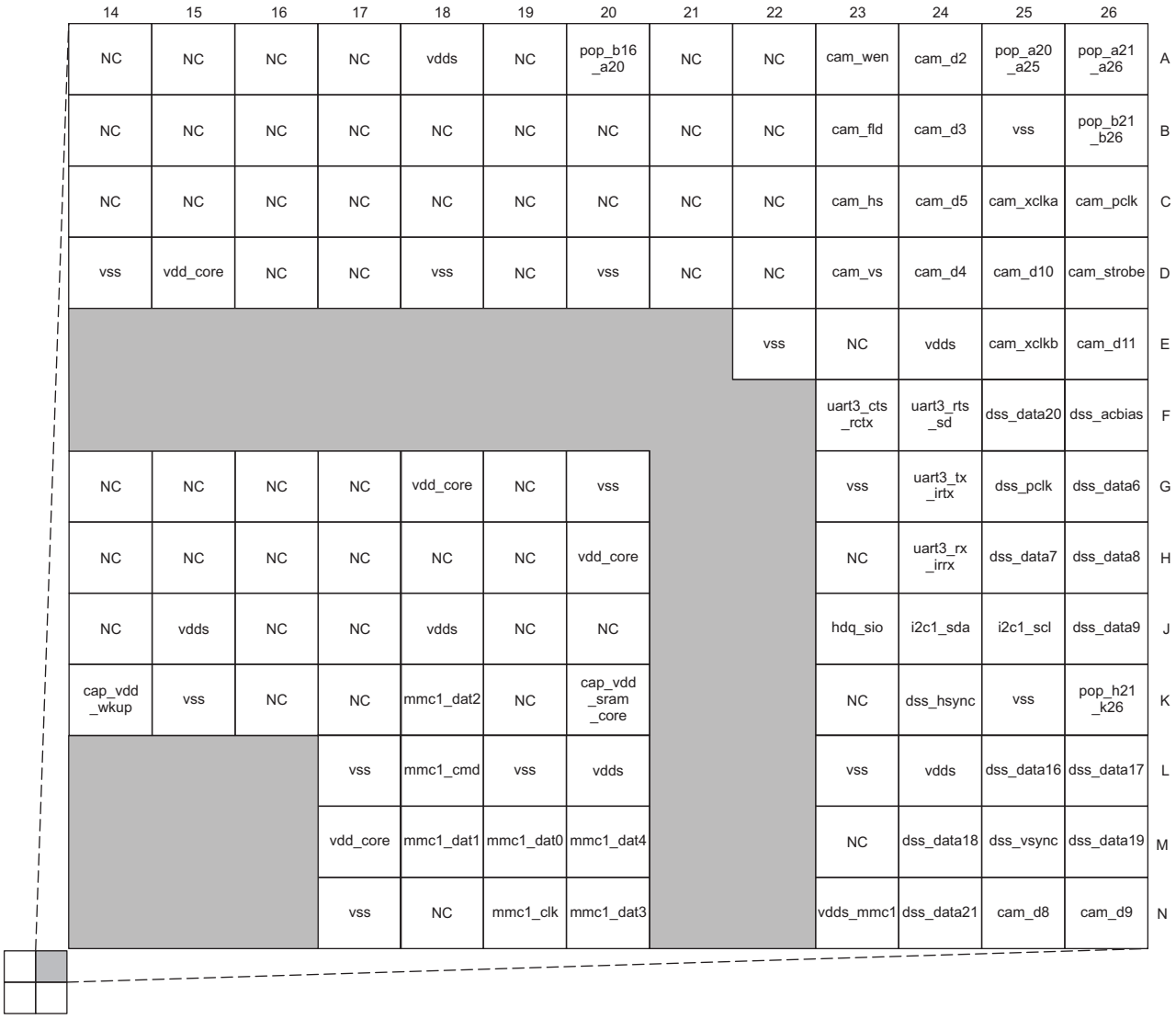


	1	2	3	4	5	6	7	8	9	10	11	12	13
A	pop_a1_a1	NC	gpmc_ncs2	NC	NC	vss	NC	vss	NC	NC	NC	NC	vss
B	NC	vss	gpmc_wait2	gpmc_ncs4	gpmc_ncs6	gpmc_ncs3	NC	NC	NC	NC	NC	NC	NC
C	i2c2_sda	i2c2_scl	sys_boot2	gpmc_ncs5	gpmc_ncs7	gpmc_wait3	NC	NC	NC	NC	vdds	vss	NC
D	gpmc_a9	gpmc_a10	sys_boot1	sys_boot6	NC	NC	vss	NC	vdds	vss	NC	vss	vdd_mpu_iva
E	gpmc_a7	gpmc_a8	sys_boot3	sys_boot4									
F	gpmc_a5	gpmc_a6	sys_boot0	NC									
G	vss	gpmc_a4	sys_boot5	vdds			NC	vss	vdd_mpu_iva	vss	vdd_core	vdd_mpu_iva	NC
H	gpmc_a2	gpmc_a3	uart1_rx	vss			vdd_mpu_iva	NC	NC	NC	NC	NC	NC
J	gpmc_nbe1	gpmc_a1	NC	NC			NC	NC	NC	NC	NC	NC	NC
K	vss	gpmc_nbe0_cle	mmc2_dat7	NC			NC	NC	NC	NC	vdd_mpu_iva	NC	vdds_dpll
L	pop_j1_l1	gpmc_d14	mmc2_dat6	uart1_tx			vdds	NC	vdd_mpu_iva	vss			
M	gpmc_nwe	gpmc_d15	mmc2_dat5	vdds			vdd_core	NC	vdd_mpu_iva	vdd_mpu_iva			
N	gpmc_clk	gpmc_noe	mcbsp3_dr	vss			vdd_mpu_iva	vdd_mpu_iva	cap_vdd_sram_mpu_iva	vss			

A. Top Views are provided to assist in hardware debugging efforts.

Figure 2-10. CBC Pin Map [Quadrant A - Top View]



14	15	16	17	18	19	20	21	22	23	24	25	26	
NC	NC	NC	NC	vdds	NC	pop_b16 _a20	NC	NC	cam_wen	cam_d2	pop_a20 _a25	pop_a21 _a26	A
NC	NC	NC	NC	NC	NC	NC	NC	NC	cam_fld	cam_d3	vss	pop_b21 _b26	B
NC	NC	NC	NC	NC	NC	NC	NC	NC	cam_hs	cam_d5	cam_xclka	cam_pclk	C
vss	vdd_core	NC	NC	vss	NC	vss	NC	NC	cam_vs	cam_d4	cam_d10	cam_strobe	D
								vss	NC	vdds	cam_xclkb	cam_d11	E
									uart3_cts _rctx	uart3_rts _sd	dss_data20	dss_acbias	F
NC	NC	NC	NC	vdd_core	NC	vss			vss	uart3_tx _irtx	dss_pclk	dss_data6	G
NC	NC	NC	NC	NC	NC	vdd_core			NC	uart3_rx _irrx	dss_data7	dss_data8	H
NC	vdds	NC	NC	vdds	NC	NC			hdq_sio	i2c1_sda	i2c1_scl	dss_data9	J
cap_vdd _wkup	vss	NC	NC	mmc1_dat2	NC	cap_vdd _sram _core			NC	dss_hsync	vss	pop_h21 _k26	K
			vss	mmc1_cmd	vss	vdds			vss	vdds	dss_data16	dss_data17	L
			vdd_core	mmc1_dat1	mmc1_dat0	mmc1_dat4			NC	dss_data18	dss_vsync	dss_data19	M
			vss	NC	mmc1_clk	mmc1_dat3			vdds_mmc1	dss_data21	cam_d8	cam_d9	N

Figure 2-11. CBC Pin Map [Quadrant B - Top View]

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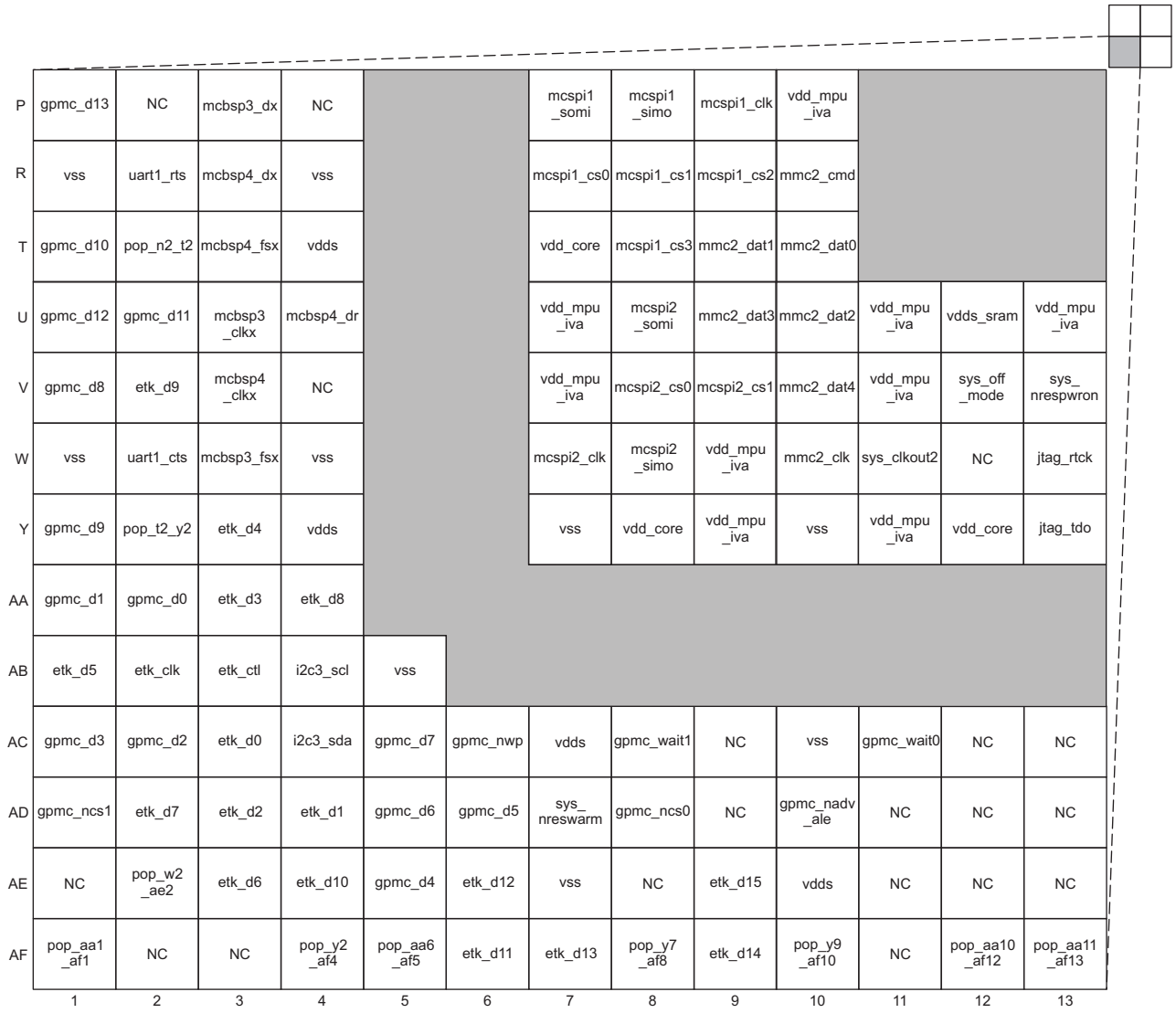
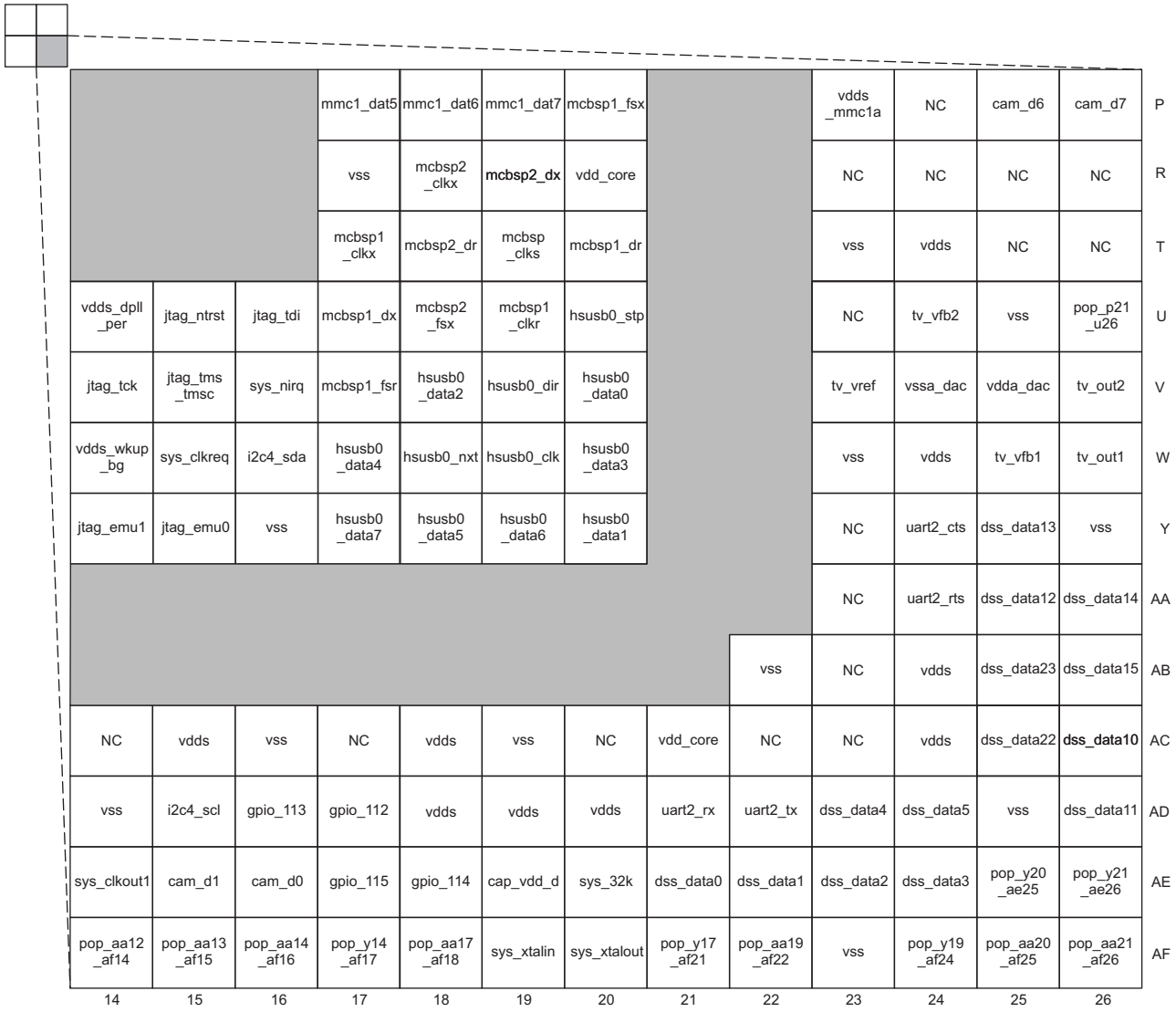


	1	2	3	4	5	6	7	8	9	10	11	12	13
P	gpmc_d13	NC	mcbsp3_dx	NC			mcspi1_somi	mcspi1_simo	mcspi1_clk	vdd_mpu_iva			
R	vss	uart1_rts	mcbsp4_dx	vss			mcspi1_cs0	mcspi1_cs1	mcspi1_cs2	mmc2_cmd			
T	gpmc_d10	pop_n2_t2	mcbsp4_fsx	vdds			vdd_core	mcspi1_cs3	mmc2_dat1	mmc2_dat0			
U	gpmc_d12	gpmc_d11	mcbsp3_clkx	mcbsp4_dr			vdd_mpu_iva	mcspi2_somi	mmc2_dat3	mmc2_dat2	vdd_mpu_iva	vdds_sram	vdd_mpu_iva
V	gpmc_d8	etk_d9	mcbsp4_clkx	NC			vdd_mpu_iva	mcspi2_cs0	mcspi2_cs1	mmc2_dat4	vdd_mpu_iva	sys_off_mode	sys_nrespwron
W	vss	uart1_cts	mcbsp3_fsx	vss			mcspi2_clk	mcspi2_simo	vdd_mpu_iva	mmc2_clk	sys_clkout2	NC	jtag_rtck
Y	gpmc_d9	pop_t2_y2	etk_d4	vdds			vss	vdd_core	vdd_mpu_iva	vss	vdd_mpu_iva	vdd_core	jtag_tdo
AA	gpmc_d1	gpmc_d0	etk_d3	etk_d8									
AB	etk_d5	etk_clk	etk_ctl	i2c3_scl	vss								
AC	gpmc_d3	gpmc_d2	etk_d0	i2c3_sda	gpmc_d7	gpmc_nwp	vdds	gpmc_wait1	NC	vss	gpmc_wait0	NC	NC
AD	gpmc_ncs1	etk_d7	etk_d2	etk_d1	gpmc_d6	gpmc_d5	sys_nreswarm	gpmc_ncs0	NC	gpmc_nadv_ale	NC	NC	NC
AE	NC	pop_w2_ae2	etk_d6	etk_d10	gpmc_d4	etk_d12	vss	NC	etk_d15	vdds	NC	NC	NC
AF	pop_aa1_af1	NC	NC	pop_y2_af4	pop_aa6_af5	etk_d11	etk_d13	pop_y7_af8	etk_d14	pop_y9_af10	NC	pop_aa10_af12	pop_aa11_af13

Figure 2-12. CBC Pin Map [Quadrant C - Top View]



			mmc1_dat5	mmc1_dat6	mmc1_dat7	mcbsp1_fsx		vdds _mmc1a	NC	cam_d6	cam_d7	P
			vss	mcbsp2 _clkx	mcbsp2_dx	vdd_core		NC	NC	NC	NC	R
			mcbsp1 _clkx	mcbsp2_dr	mcbsp _clks	mcbsp1_dr		vss	vdds	NC	NC	T
vdds_dpll _per	jtag_ntrst	jtag_tdi	mcbsp1_dx	mcbsp2 _fsx	mcbsp1 _clkr	hsusb0_stp		NC	tv_vfb2	vss	pop_p21 _u26	U
jtag_tck	jtag_tms _tmsc	sys_nirq	mcbsp1_fsr	hsusb0 _data2	hsusb0_dir	hsusb0 _data0		tv_vref	vssa_dac	vdda_dac	tv_out2	V
vdds_wkup _bg	sys_clkreq	i2c4_sda	hsusb0 _data4	hsusb0_nxt	hsusb0_clk	hsusb0 _data3		vss	vdds	tv_vfb1	tv_out1	W
jtag_emu1	jtag_emu0	vss	hsusb0 _data7	hsusb0 _data5	hsusb0 _data6	hsusb0 _data1		NC	uart2_cts	dss_data13	vss	Y
								NC	uart2_rts	dss_data12	dss_data14	AA
							vss	NC	vdds	dss_data23	dss_data15	AB
NC	vdds	vss	NC	vdds	vss	NC	vdd_core	NC	NC	vdds	dss_data22	dss_data10	AC
vss	i2c4_scl	gpio_113	gpio_112	vdds	vdds	vdds	uart2_rx	uart2_tx	dss_data4	dss_data5	vss	dss_data11	AD
sys_clkout1	cam_d1	cam_d0	gpio_115	gpio_114	cap_vdd_d	sys_32k	dss_data0	dss_data1	dss_data2	dss_data3	pop_y20 _ae25	pop_y21 _ae26	AE
pop_aa12 _af14	pop_aa13 _af15	pop_aa14 _af16	pop_y14 _af17	pop_aa17 _af18	sys_xtalin	sys_xtalout	pop_y17 _af21	pop_aa19 _af22	vss	pop_y19 _af24	pop_aa20 _af25	pop_aa21 _af26	AF
14	15	16	17	18	19	20	21	22	23	24	25	26	

Figure 2-13. CBC Pin Map [Quadrant D - Top View]

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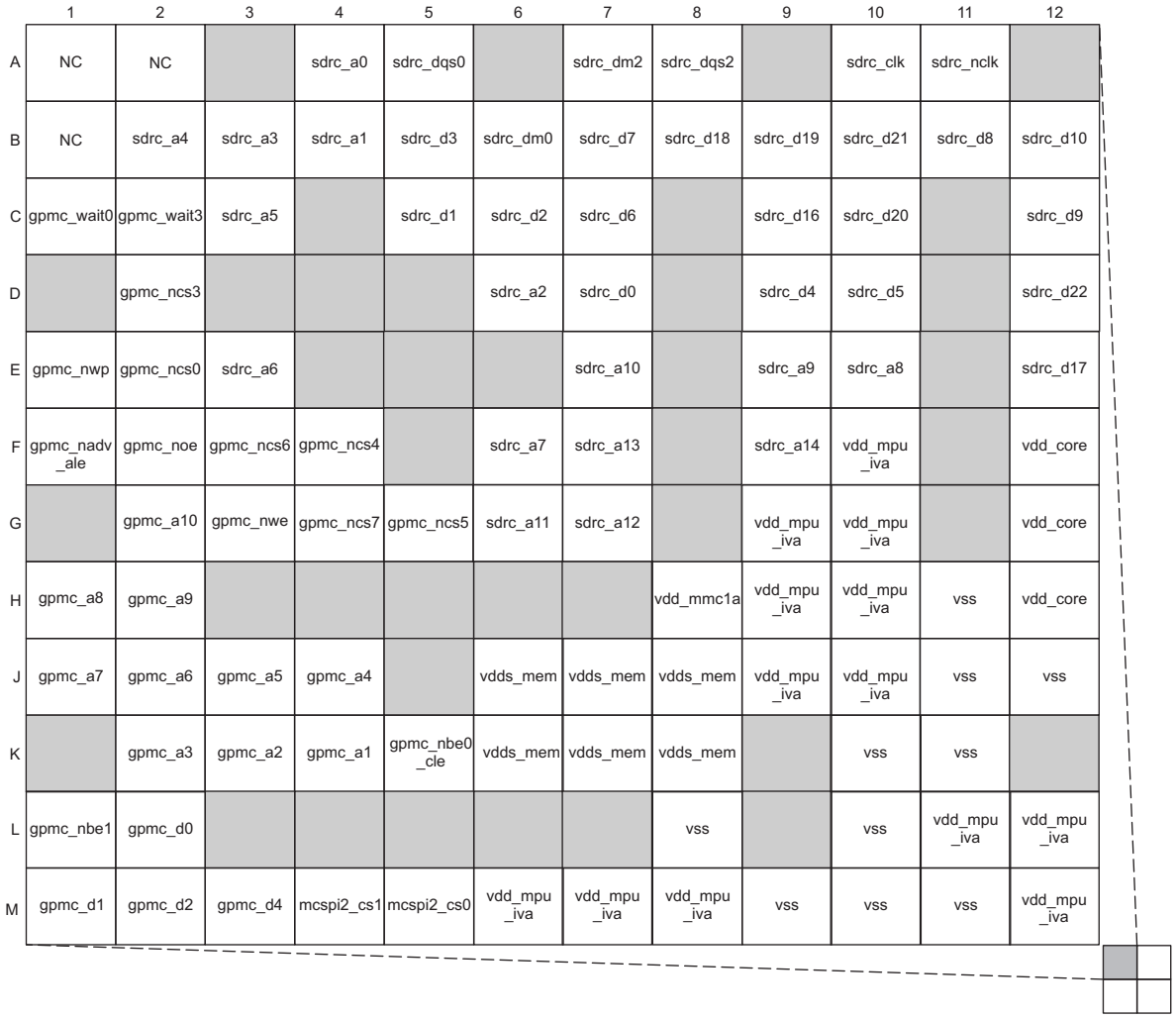
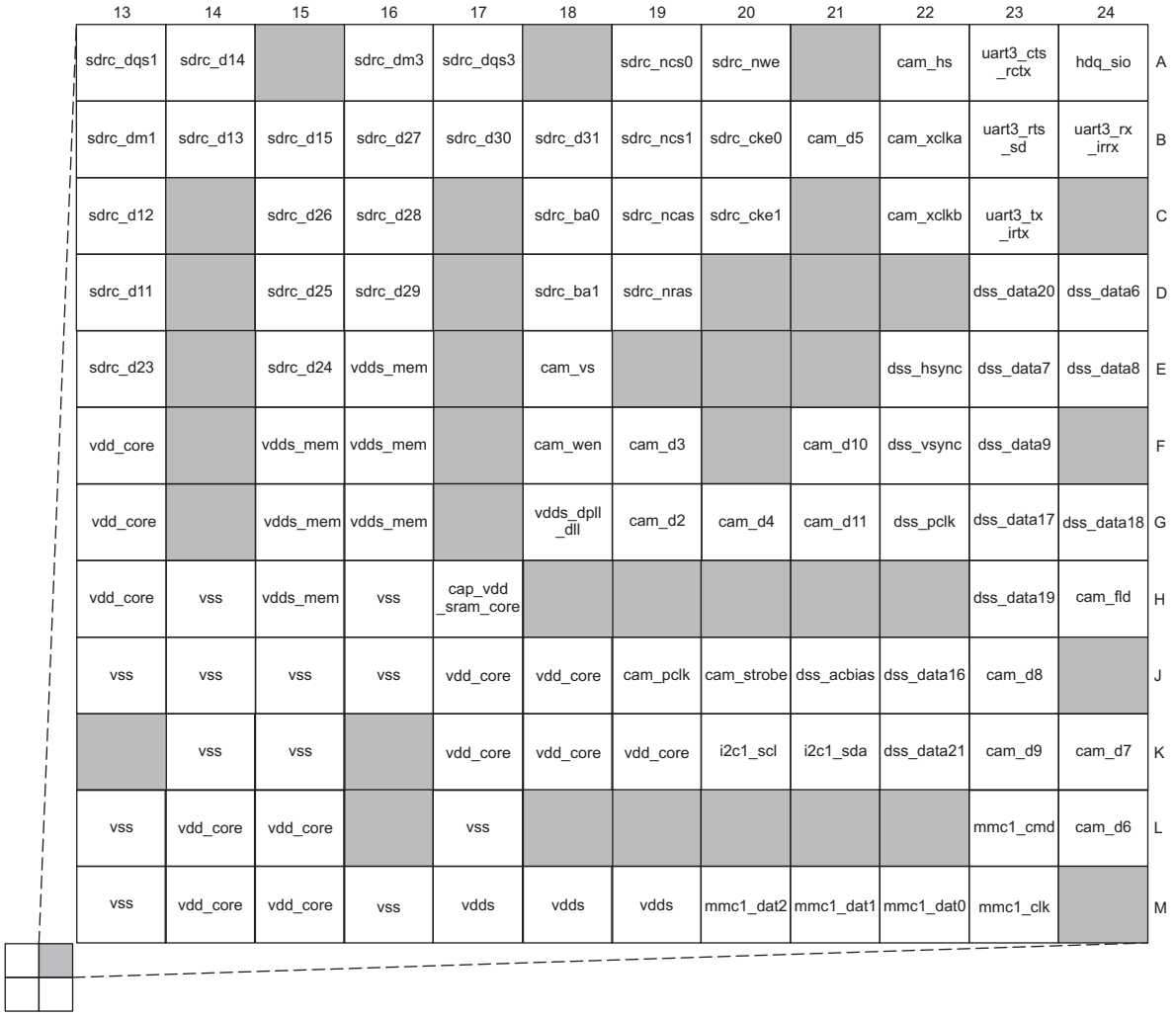


	1	2	3	4	5	6	7	8	9	10	11	12
A	NC	NC		sdrc_a0	sdrc_dqs0		sdrc_dm2	sdrc_dqs2		sdrc_clk	sdrc_nclk	
B	NC	sdrc_a4	sdrc_a3	sdrc_a1	sdrc_d3	sdrc_dm0	sdrc_d7	sdrc_d18	sdrc_d19	sdrc_d21	sdrc_d8	sdrc_d10
C	gpmc_wait0	gpmc_wait3	sdrc_a5		sdrc_d1	sdrc_d2	sdrc_d6		sdrc_d16	sdrc_d20		sdrc_d9
D		gpmc_ncs3				sdrc_a2	sdrc_d0		sdrc_d4	sdrc_d5		sdrc_d22
E	gpmc_nwp	gpmc_ncs0	sdrc_a6				sdrc_a10		sdrc_a9	sdrc_a8		sdrc_d17
F	gpmc_nadv_ale	gpmc_noe	gpmc_ncs6	gpmc_ncs4		sdrc_a7	sdrc_a13		sdrc_a14	vdd_mpu_iva		vdd_core
G		gpmc_a10	gpmc_nwe	gpmc_ncs7	gpmc_ncs5	sdrc_a11	sdrc_a12		vdd_mpu_iva	vdd_mpu_iva		vdd_core
H	gpmc_a8	gpmc_a9						vdd_mmc1a	vdd_mpu_iva	vdd_mpu_iva	vss	vdd_core
J	gpmc_a7	gpmc_a6	gpmc_a5	gpmc_a4		vdds_mem	vdds_mem	vdds_mem	vdd_mpu_iva	vdd_mpu_iva	vss	vss
K		gpmc_a3	gpmc_a2	gpmc_a1	gpmc_nbe0_cle	vdds_mem	vdds_mem	vdds_mem		vss	vss	
L	gpmc_nbe1	gpmc_d0						vss		vss	vdd_mpu_iva	vdd_mpu_iva
M	gpmc_d1	gpmc_d2	gpmc_d4	mcspi2_cs1	mcspi2_cs0	vdd_mpu_iva	vdd_mpu_iva	vdd_mpu_iva	vss	vss	vss	vdd_mpu_iva

A. Top Views are provided to assist in hardware debugging efforts.

Figure 2-14. CUS Pin Map [Quadrant A - Top View]



13	14	15	16	17	18	19	20	21	22	23	24	
sdrc_dqs1	sdrc_d14		sdrc_dm3	sdrc_dqs3		sdrc_ncs0	sdrc_nwe		cam_hs	uart3_cts_rctx	hdq_sio	A
sdrc_dm1	sdrc_d13	sdrc_d15	sdrc_d27	sdrc_d30	sdrc_d31	sdrc_ncs1	sdrc_cke0	cam_d5	cam_xclka	uart3_rts_sd	uart3_rx_irrx	B
sdrc_d12		sdrc_d26	sdrc_d28		sdrc_ba0	sdrc_ncas	sdrc_cke1		cam_xclkb	uart3_tx_irtx		C
sdrc_d11		sdrc_d25	sdrc_d29		sdrc_ba1	sdrc_nras				dss_data20	dss_data6	D
sdrc_d23		sdrc_d24	vdds_mem		cam_vs				dss_hsync	dss_data7	dss_data8	E
vdd_core		vdds_mem	vdds_mem		cam_wen	cam_d3		cam_d10	dss_vsync	dss_data9		F
vdd_core		vdds_mem	vdds_mem		vdds_dpll_dll	cam_d2	cam_d4	cam_d11	dss_pclk	dss_data17	dss_data18	G
vdd_core	vss	vdds_mem	vss	cap_vdd_sram_core						dss_data19	cam_fld	H
vss	vss	vss	vss	vdd_core	vdd_core	cam_pclk	cam_strobe	dss_acbias	dss_data16	cam_d8		J
	vss	vss		vdd_core	vdd_core	vdd_core	i2c1_scl	i2c1_sda	dss_data21	cam_d9	cam_d7	K
vss	vdd_core	vdd_core		vss						mmc1_cmd	cam_d6	L
vss	vdd_core	vdd_core	vss	vdds	vdds	vdds	mmc1_dat2	mmc1_dat1	mmc1_dat0	mmc1_clk		M

Figure 2-15. CUS Pin Map [Quadrant B - Top View]

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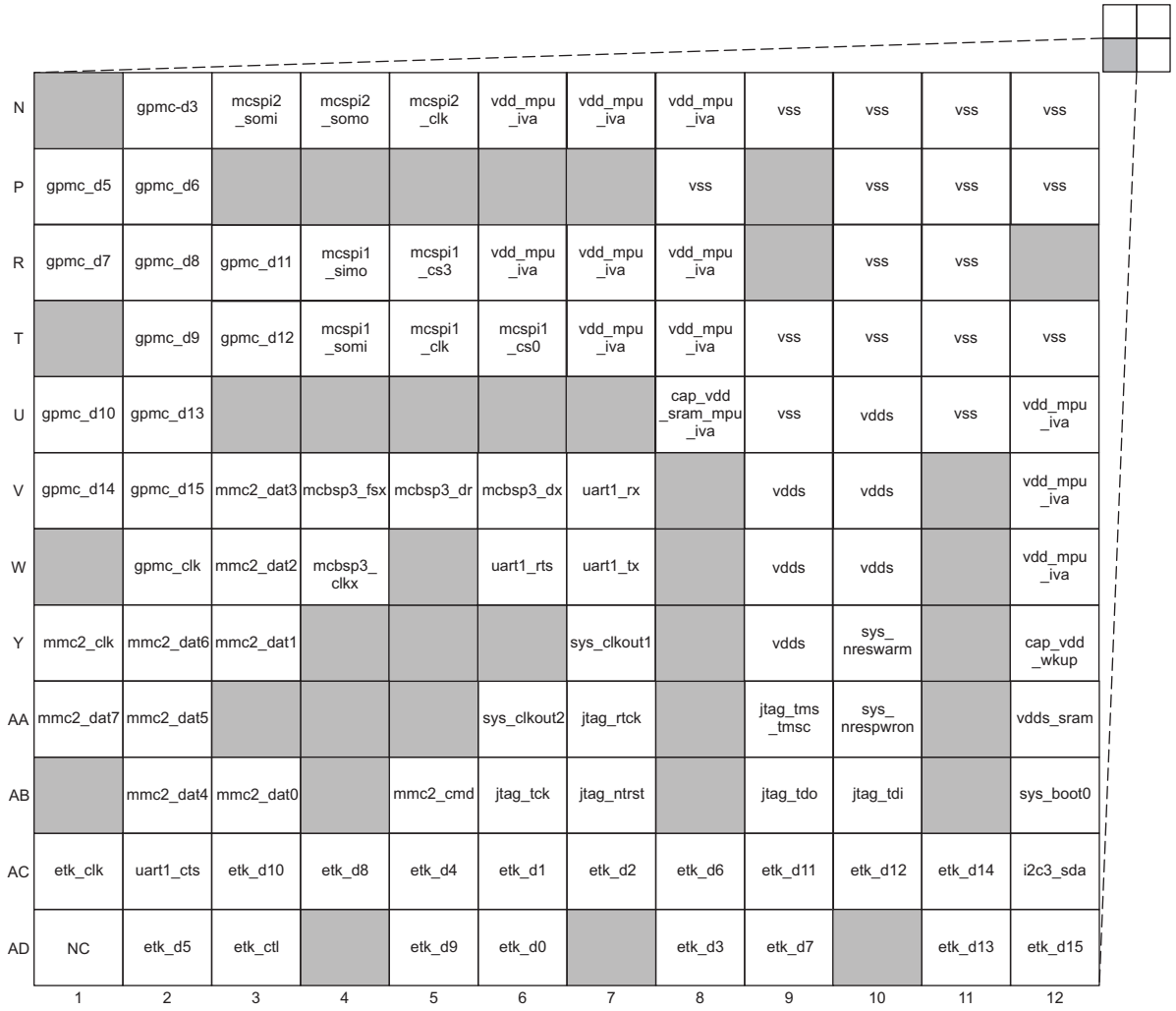
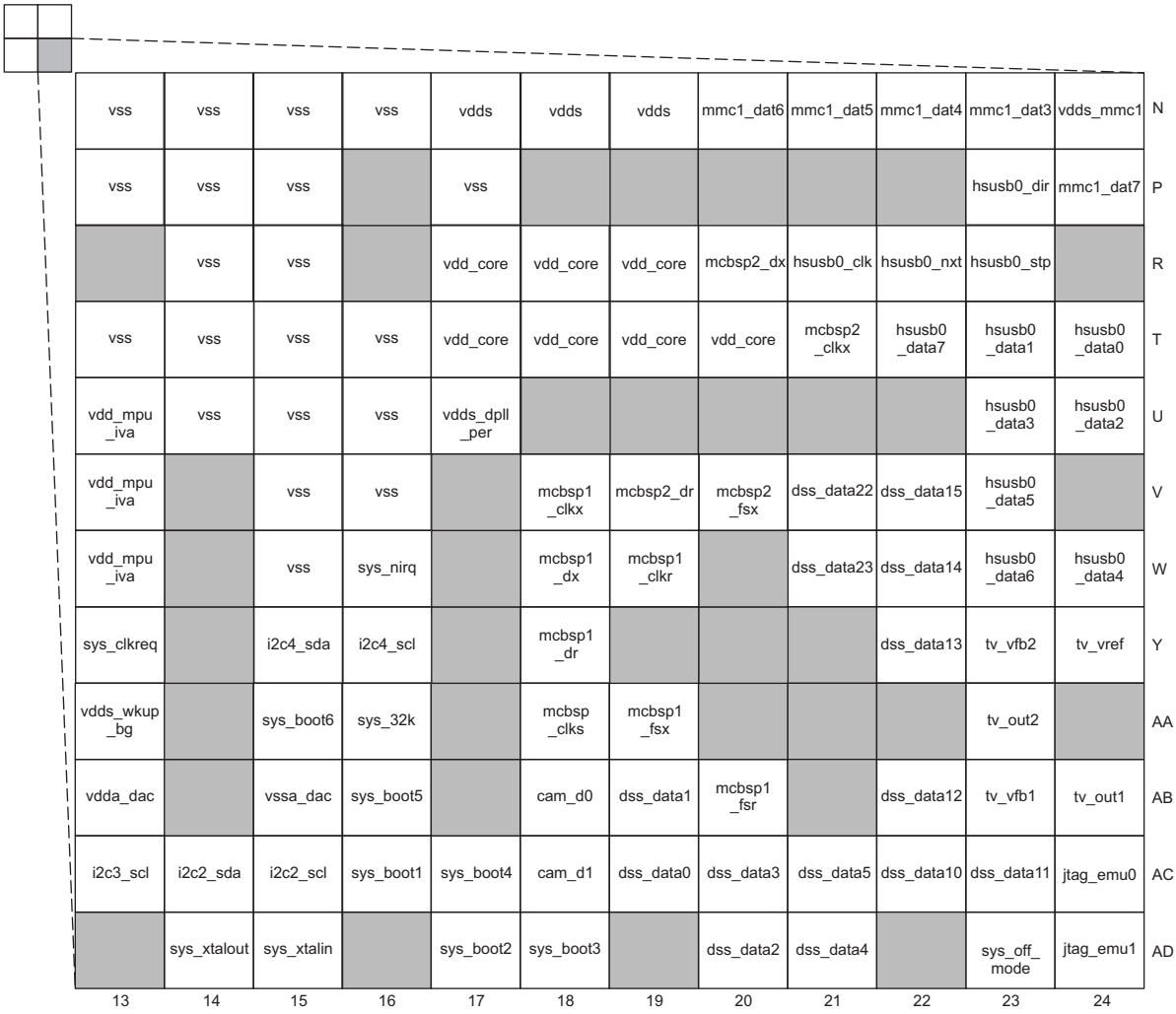


	1	2	3	4	5	6	7	8	9	10	11	12
N		gpmc-d3	mcspi2 _somi	mcspi2 _somo	mcspi2 _clk	vdd_mpu _iva	vdd_mpu _iva	vdd_mpu _iva	vss	vss	vss	vss
P	gpmc_d5	gpmc_d6						vss		vss	vss	vss
R	gpmc_d7	gpmc_d8	gpmc_d11	mcspi1 _simo	mcspi1 _cs3	vdd_mpu _iva	vdd_mpu _iva	vdd_mpu _iva		vss	vss	
T		gpmc_d9	gpmc_d12	mcspi1 _somi	mcspi1 _clk	mcspi1 _cs0	vdd_mpu _iva	vdd_mpu _iva	vss	vss	vss	vss
U	gpmc_d10	gpmc_d13						cap_vdd _sram_mpu _iva	vss	vdds	vss	vdd_mpu _iva
V	gpmc_d14	gpmc_d15	mmc2_dat3	mcbsp3_fsx	mcbsp3_dr	mcbsp3_dx	uart1_rx		vdds	vdds		vdd_mpu _iva
W		gpmc_clk	mmc2_dat2	mcbsp3_ clkx		uart1_rts	uart1_tx		vdds	vdds		vdd_mpu _iva
Y	mmc2_clk	mmc2_dat6	mmc2_dat1				sys_clkout1		vdds	sys_ nreswarm		cap_vdd _wkup
AA	mmc2_dat7	mmc2_dat5				sys_clkout2	jtag_rtck		jtag_tms _tmsc	sys_ nrespwron		vdds_sram
AB		mmc2_dat4	mmc2_dat0		mmc2_cmd	jtag_tck	jtag_ntrst		jtag_tdo	jtag_tdi		sys_boot0
AC	etk_clk	uart1_cts	etk_d10	etk_d8	etk_d4	etk_d1	etk_d2	etk_d6	etk_d11	etk_d12	etk_d14	i2c3_sda
AD	NC	etk_d5	etk_ctl		etk_d9	etk_d0		etk_d3	etk_d7		etk_d13	etk_d15

Figure 2-16. CUS Pin Map [Quadrant C - Top View]



	13	14	15	16	17	18	19	20	21	22	23	24	
N	vss	vss	vss	vss	vdds	vdds	vdds	mmc1_dat6	mmc1_dat5	mmc1_dat4	mmc1_dat3	vdds_mmc1	N
P	vss	vss	vss		vss						hsusb0_dir	mmc1_dat7	P
R		vss	vss		vdd_core	vdd_core	vdd_core	mcbsp2_dx	hsusb0_clk	hsusb0_nxt	hsusb0_stp		R
T	vss	vss	vss	vss	vdd_core	vdd_core	vdd_core	vdd_core	mcbsp2 _clkx	hsusb0 _data7	hsusb0 _data1	hsusb0 _data0	T
U	vdd_mpu _iva	vss	vss	vss	vdds_dpll _per						hsusb0 _data3	hsusb0 _data2	U
V	vdd_mpu _iva		vss	vss		mcbsp1 _clkx	mcbsp2_dr	mcbsp2 _fsx	dss_data22	dss_data15	hsusb0 _data5		V
W	vdd_mpu _iva		vss	sys_nirq		mcbsp1 _dx	mcbsp1 _clkr		dss_data23	dss_data14	hsusb0 _data6	hsusb0 _data4	W
Y	sys_clkreq		i2c4_sda	i2c4_scl		mcbsp1 _dr				dss_data13	tv_vfb2	tv_vref	Y
AA	vdds_wkup _bg		sys_boot6	sys_32k		mcbsp _clks	mcbsp1 _fsx				tv_out2		AA
AB	vdda_dac		vssa_dac	sys_boot5		cam_d0	dss_data1	mcbsp1 _fsr		dss_data12	tv_vfb1	tv_out1	AB
AC	i2c3_scl	i2c2_sda	i2c2_scl	sys_boot1	sys_boot4	cam_d1	dss_data0	dss_data3	dss_data5	dss_data10	dss_data11	jtag_emu0	AC
AD		sys_xtalout	sys_xtalin		sys_boot2	sys_boot3		dss_data2	dss_data4		sys_off_ mode	jtag_emu1	AD

Figure 2-17. CUS Pin Map [Quadrant D - Top View]

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2.3 Ball Characteristics

through describe the terminal characteristics and the signals multiplexed on each pin for the CBB, CBC, and CUS packages, respectively. The following list describes the table column headers.

1. **BALL BOTTOM:** Ball number(s) on the bottom side associated with each signal(s) on the bottom.
2. **BALL TOP:** Ball number(s) on the top side associated with each signal(s) on the top.
3. **PIN NAME:** Names of signals multiplexed on each ball (also notice that the name of the pin is the signal name in mode 0).
   Note: through do not take into account subsystem pin multiplexing options. Subsystem pin multiplexing options are described in Section 2.5, *Signal Descriptions.*
4. **MODE:** Multiplexing mode number.
   (a) Mode 0 is the primary mode; this means that when mode 0 is set, the function mapped on the pin corresponds to the name of the pin. There is always a function mapped on the primary mode. Notice that primary mode is not necessarily the default mode.

   Note: The default mode is the mode which is automatically configured on release of the internal GLOBAL_PWRON reset; also see the RESET REL. MODE column.
   (b) Modes 1 to 7 are possible modes for alternate functions. On each pin, some modes are effectively used for alternate functions, while some modes are not used and do not correspond to a functional configuration.
5. **TYPE:** Signal direction
   - I = Input
   - O = Output
   - I/O = Input/Output
   - D = Open drain
   - DS = Differential
   - A = Analog

   Note: In the safe_mode, the buffer is configured in high-impedance.
6. **BALL RESET STATE:** The state of the terminal at reset (power up).
   - 0: The buffer drives V_{OL} (pulldown/pullup resistor not activated)
     0(PD): The buffer drives V_{OL} with an active pulldown resistor.
   - 1: The buffer drives V_{OH} (pulldown/pullup resistor not activated)
     1(PU): The buffer drives V_{OH} with an active pullup resistor.
   - Z: High-impedance
   - L: High-impedance with an active pulldown resistor
   - H : High-impedance with an active pullup resistor
7. **BALL RESET REL. STATE:** The state of the terminal at reset release.
   - 0: The buffer drives V_{OL} (pulldown/pullup resistor not activated)
     0(PD): The buffer drives V_{OL} with an active pulldown resistor.
   - 1: The buffer drives V_{OH} (pulldown/pullup resistor not activated)
     1(PU): The buffer drives V_{OH} with an active pullup resistor.
   - Z: High-impedance
   - L: High-impedance with an active pulldown resistor
   - H : High-impedance with an active pullup resistor
8. **RESET REL. MODE:** This mode is automatically configured on release of the internal GLOBAL_PWRON reset.
9. **POWER:** The voltage supply that powers the terminal's I/O buffers.
10. **HYS:** Indicates if the input buffer is with hysteresis.
11. **BUFFER STRENGTH:** Drive strength of the associated output buffer.
12. **PULL U/D - TYPE:** Denotes the presence of an internal pullup or pulldown resistor. Pullup and pulldown resistors can be enabled or disabled via software.

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Note: The pullup/pulldown drive strength is equal to 100 µA except for CBB balls P27, P26, R27, and R25 and CUS balls N22, N21, N20, and P24, which the pulldown drive strength is equal to 1.8 kΩ.

13. **IO CELL:** IO cell information.

Note: Configuring two pins to the same input signal is not supported as it can yield unexpected results. This can be easily prevented with the proper software configuration.

Table 2-1. Ball Characteristics (CBB Pkg.)(1)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENG TH (mA) [11]	PULLUP /DOWN TYPE [12]	IO CELL [13]
D6	J2	sdrc_d0	0	IO	L	Z	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
C6	J1	sdrc_d1	0	IO	L	Z	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
B6	G2	sdrc_d2	0	IO	L	Z	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
C8	G1	sdrc_d3	0	IO	L	Z	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
C9	F2	sdrc_d4	0	IO	L	Z	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
A7	F1	sdrc_d5	0	IO	L	Z	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
B9	D2	sdrc_d6	0	IO	L	Z	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
A9	D1	sdrc_d7	0	IO	L	Z	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
C14	B13	sdrc_d8	0	IO	L	Z	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
B14	A13	sdrc_d9	0	IO	L	Z	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
C15	B14	sdrc_d10	0	IO	L	Z	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
B16	A14	sdrc_d11	0	IO	L	Z	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
D17	B16	sdrc_d12	0	IO	L	Z	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
C17	A16	sdrc_d13	0	IO	L	Z	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
B17	B19	sdrc_d14	0	IO	L	Z	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
D18	A19	sdrc_d15	0	IO	L	Z	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
D11	B3	sdrc_d16	0	IO	L	Z	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
B10	A3	sdrc_d17	0	IO	L	Z	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
C11	B5	sdrc_d18	0	IO	L	Z	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
D12	A5	sdrc_d19	0	IO	L	Z	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
C12	B8	sdrc_d20	0	IO	L	Z	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
A11	A8	sdrc_d21	0	IO	L	Z	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
B13	B9	sdrc_d22	0	IO	L	Z	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
D14	A9	sdrc_d23	0	IO	L	Z	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
C18	B21	sdrc_d24	0	IO	L	Z	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
A19	A21	sdrc_d25	0	IO	L	Z	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
B19	D22	sdrc_d26	0	IO	L	Z	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
B20	D23	sdrc_d27	0	IO	L	Z	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
D20	E22	sdrc_d28	0	IO	L	Z	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
A21	E23	sdrc_d29	0	IO	L	Z	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
B21	G22	sdrc_d30	0	IO	L	Z	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
C21	G23	sdrc_d31	0	IO	L	Z	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
H9	AB21	sdrc_ba0	0	O	0	0	0	vdds_ mem	No	4	NA	LVCMOS
H10	AC21	sdrc_ba1	0	O	0	0	0	vdds_ mem	No	4	NA	LVCMOS
A4	N22	sdrc_a0	0	O	0	0	0	vdds_ mem	No	4	NA	LVCMOS
B4	N23	sdrc_a1	0	O	0	0	0	vdds_ mem	No	4	NA	LVCMOS
B3	P22	sdrc_a2	0	O	0	0	0	vdds_ mem	No	4	NA	LVCMOS
C5	P23	sdrc_a3	0	O	0	0	0	vdds_ mem	No	4	NA	LVCMOS
C4	R22	sdrc_a4	0	O	0	0	0	vdds_ mem	No	4	NA	LVCMOS
D5	R23	sdrc_a5	0	O	0	0	0	vdds_ mem	No	4	NA	LVCMOS
C3	T22	sdrc_a6	0	O	0	0	0	vdds_ mem	No	4	NA	LVCMOS
C2	T23	sdrc_a7	0	O	0	0	0	vdds_ mem	No	4	NA	LVCMOS
C1	U22	sdrc_a8	0	O	0	0	0	vdds_ mem	No	4	NA	LVCMOS
D4	U23	sdrc_a9	0	O	0	0	0	vdds_ mem	No	4	NA	LVCMOS
D3	V22	sdrc_a10	0	O	0	0	0	vdds_ mem	No	4	NA	LVCMOS
D2	V23	sdrc_a11	0	O	0	0	0	vdds_ mem	No	4	NA	LVCMOS

(1) NA in this table stands for "Not Applicable".

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Table 2-1. Ball Characteristics (CBB Pkg.)[(1)] (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENG TH (mA) [11]	PULLUP /DOWN TYPE [12]	IO CELL [13]
D1	W22	sdrc_a12	0	O	0	0	0	vdds_ mem	No	4	NA	LVCMOS
E2	W23	sdrc_a13	0	O	0	0	0	vdds_ mem	No	4	NA	LVCMOS
E1	Y22	sdrc_a14	0	O	0	0	0	vdds_ mem	No	4	NA	LVCMOS
H11	M22	sdrc_ncs0	0	O	1	1	0	vdds_ mem	No	4	NA	LVCMOS
H12	M23	sdrc_ncs1	0	O	1	1	0	vdds_ mem	No	4	NA	LVCMOS
A13	A11	sdrc_clk	0	IO	L	0	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
A14	B11	sdrc_nclk	0	O	1	1	0	vdds_ mem	No	4	NA	LVCMOS
H16	J22	sdrc_cke0	0	O	H	1	7	vdds_ mem	Yes	4	PU/ PD	LVCMOS
		safe_mode	7									
H17	J23	sdrc_cke1	0	O	H	1	7	vdds_ mem	Yes	4	PU/ PD	LVCMOS
		safe_mode	7									
H14	L23	sdrc_nras	0	O	1	1	0	vdds_ mem	No	4	NA	LVCMOS
H13	L22	sdrc_ncas	0	O	1	1	0	vdds_ mem	No	4	NA	LVCMOS
H15	K23	sdrc_nwe	0	O	1	1	0	vdds_ mem	No	4	NA	LVCMOS
B7	C1	sdrc_dm0	0	O	0	0	0	vdds_ mem	No	4	NA	LVCMOS
A16	A17	sdrc_dm1	0	O	0	0	0	vdds_ mem	No	4	NA	LVCMOS
B11	A6	sdrc_dm2	0	O	0	0	0	vdds_ mem	No	4	NA	LVCMOS
C20	A20	sdrc_dm3	0	O	0	0	0	vdds_ mem	No	4	NA	LVCMOS
A6	C2	sdrc_dqs0	0	IO	L	Z	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
A17	B17	sdrc_dqs1	0	IO	L	Z	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
A10	B6	sdrc_dqs2	0	IO	L	Z	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
A20	B20	sdrc_dqs3	0	IO	L	Z	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
N4	AC15	gpmc_a1	0	O	L	L	7	vdds_ mem	Yes	4	PU/ PD	LVCMOS
		gpio_34	4	IO								
		safe_mode	7									
M4	AB15	gpmc_a2	0	O	L	L	7	vdds_ mem	Yes	4	PU/ PD	LVCMOS
		gpio_35	4	IO								
		safe_mode	7									
L4	AC16	gpmc_a3	0	O	L	L	7	vdds_ mem	Yes	4	PU/ PD	LVCMOS
		gpio_36	4	IO								
		safe_mode	7									
K4	AB16	gpmc_a4	0	O	L	L	7	vdds_ mem	Yes	4	PU/ PD	LVCMOS
		gpio_37	4	IO								
		safe_mode	7									
T3	AC17	gpmc_a5	0	O	L	L	7	vdds_ mem	Yes	4	PU/ PD	LVCMOS
		gpio_38	4	IO								
		safe_mode	7									
R3	AB17	gpmc_a6	0	O	H	H	7	vdds_ mem	Yes	4	PU/ PD	LVCMOS
		gpio_39	4	IO								
		safe_mode	7									
N3	AC18	gpmc_a7	0	O	H	H	7	vdds_ mem	Yes	4	PU/ PD	LVCMOS
		gpio_40	4	IO								
		safe_mode	7									
M3	AB18	gpmc_a8	0	O	H	H	7	vdds_ mem	Yes	4	PU/ PD	LVCMOS
		gpio_41	4	IO								
		safe_mode	7									
L3	AC19	gpmc_a9	0	O	H	H	7	vdds_ mem	Yes	4	PU/ PD	LVCMOS
		sys_ ndmareq2	1	I								
		gpio_42	4	IO								
		safe_mode	7									
K3	AB19	gpmc_a10	0	O	H	H	7	vdds_ mem	Yes	4	PU/ PD	LVCMOS
		sys_ ndmareq3	1	I								
		gpio_43	4	IO								

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Table 2-1. Ball Characteristics (CBB Pkg.)[(1)] (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENG TH (mA) [11]	PULLUP /DOWN TYPE [12]	IO CELL [13]
		safe_mode	7									
K1	M2	gpmc_d0	0	IO	H	H	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
L1	M1	gpmc_d1	0	IO	H	H	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
L2	N2	gpmc_d2	0	IO	H	H	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
P2	N1	gpmc_d3	0	IO	H	H	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
T1	R2	gpmc_d4	0	IO	H	H	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
V1	R1	gpmc_d5	0	IO	H	H	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
V2	T2	gpmc_d6	0	IO	H	H	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
W2	T1	gpmc_d7	0	IO	H	H	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
H2	AB3	gpmc_d8	0	IO	H	H	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
		gpio_44	4	IO								
		safe_mode	7									
K2	AC3	gpmc_d9	0	IO	H	H	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
		gpio_45	4	IO								
		safe_mode	7									
P1	AB4	gpmc_d10	0	IO	H	H	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
		gpio_46	4	IO								
		safe_mode	7									
R1	AC4	gpmc_d11	0	IO	H	H	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
		gpio_47	4	IO								
		safe_mode	7									
R2	AB6	gpmc_d12	0	IO	H	H	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
		gpio_48	4	IO								
		safe_mode	7									
T2	AC6	gpmc_d13	0	IO	H	H	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
		gpio_49	4	IO								
		safe_mode	7									
W1	AB7	gpmc_d14	0	IO	H	H	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
		gpio_50	4	IO								
		safe_mode	7									
Y1	AC7	gpmc_d15	0	IO	H	H	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
		gpio_51	4	IO								
		safe_mode	7									
G4	Y2	gpmc_ncs0	0	O	1	1	0	vdds_ mem	No	4	NA	LVCMOS
H3	Y1	gpmc_ncs1	0	O	H	1	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
		gpio_52	4	IO								
		safe_mode	7									
V8	NA	gpmc_ncs2	0	O	H	H	7	vdds_ mem	Yes	4	PU/ PD	LVCMOS
		gpio_53	4	IO								
		safe_mode	7									
U8	NA	gpmc_ncs3	0	O	H	H	7	vdds_ mem	Yes	4	PU/ PD	LVCMOS
		sys_ ndmareq0	1	I								
		gpio_54	4	IO								
		safe_mode	7									
T8	NA	gpmc_ncs4	0	O	H	H	7	vdds_ mem	Yes	4	PU/ PD	LVCMOS
		sys_ ndmareq1	1	I								
		mcbsp4_ clkx	2	IO								
		gpt9_pwm_e vt	3	IO								
		gpio_55	4	IO								
		safe_mode	7									
R8	NA	gpmc_ncs5	0	O	H	H	7	vdds_ mem	Yes	4	PU/ PD	LVCMOS
		sys_ ndmareq2	1	I								

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Table 2-1. Ball Characteristics (CBB Pkg.)[(1)] (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENG TH (mA) [11]	PULLUP /DOWN TYPE [12]	IO CELL [13]
		mcbsp4_dr	2	I								
		gpt10_pwm_evt	3	IO								
		gpio_56	4	IO								
		safe_mode	7									
P8	NA	gpmc_ncs6	0	O	H	H	7	vdds_ mem	Yes	4	PU/ PD	LVCMOS
		sys_ndmareq3	1	I								
		mcbsp4_dx	2	IO								
		gpt11_pwm_evt	3	IO								
		gpio_57	4	IO								
		safe_mode	7									
N8	NA	gpmc_ncs7	0	O	H	H	7	vdds_ mem	Yes	4	PU/ PD	LVCMOS
		gpmc_io_dir	1	O								
		mcbsp4_fsx	2	IO								
		gpt8_pwm_evt	3	IO								
		gpio_58	4	IO								
		safe_mode	7									
T4	W2	gpmc_clk	0	O	L	0	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
		gpio_59	4	IO								
		safe_mode	7									
F3	W1	gpmc_nadv_ale	0	O	0	0	0	vdds_ mem	No	4	NA	LVCMOS
G2	V2	gpmc_noe	0	O	1	1	0	vdds_ mem	No	4	NA	LVCMOS
F4	V1	gpmc_nwe	0	O	1	1	0	vdds_ mem	No	4	NA	LVCMOS
G3	AC12	gpmc_nbe0_cle	0	O	L	0	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
		gpio_60	4	IO								
		safe_mode	7									
U3	NA	gpmc_nbe1	0	O	L	L	7	vdds_ mem	Yes	4	PU/ PD	LVCMOS
		gpio_61	4	IO								
		safe_mode	7									
H1	AB10	gpmc_nwp	0	O	L	0	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
		gpio_62	4	IO								
		safe_mode	7									
M8	AB12	gpmc_wait0	0	I	H	H	0	vdds_ mem	Yes	NA	PU/ PD	LVCMOS
L8	AC10	gpmc_wait1	0	I	H	H	7	vdds_ mem	Yes	4	PU/ PD	LVCMOS
		gpio_63	4	IO								
		safe_mode	7									
K8	NA	gpmc_wait2	0	I	H	H	7	vdds_ mem	Yes	4	PU/ PD	LVCMOS
		gpio_64	4	IO								
		safe_mode	7									
J8	NA	gpmc_wait3	0	I	H	H	7	vdds_ mem	Yes	4	PU/ PD	LVCMOS
		sys_ndmareq1	1	I								
		gpio_65	4	IO								
		safe_mode	7									
D28	NA	dss_pclk	0	O	H	H	7	vdds	Yes	8	PU/ PD	LVCMOS
		gpio_66	4	IO								
		safe_mode	7									
D26	NA	dss_hsync	0	O	H	H	7	vdds	Yes	8	PU/ PD	LVCMOS
		gpio_67	4	IO								
		safe_mode	7									
D27	NA	dss_vsync	0	O	H	H	7	vdds	Yes	8	PU/ PD	LVCMOS
		gpio_68	4	IO								

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Table 2-1. Ball Characteristics (CBB Pkg.)[(1)] (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENG TH (mA) [11]	PULLUP /DOWN TYPE [12]	IO CELL [13]
		safe_mode	7									
E27	NA	dss_acbias	0	O	L	L	7	vdds	Yes	8	PU/ PD	LVCMOS
		gpio_69	4	IO								
		safe_mode	7									
AG22	NA	dss_data0	0	IO	L	L	7	vdds	Yes	8	PU/ PD	LVCMOS
		uart1_cts	2	I								
		gpio_70	4	IO								
		safe_mode	7									
AH22	NA	dss_data1	0	IO	L	L	7	vdds	Yes	8	PU/ PD	LVCMOS
		uart1_rts	2	O								
		gpio_71	4	IO								
		safe_mode	7									
AG23	NA	dss_data2	0	IO	L	L	7	vdds	Yes	8	PU/ PD	LVCMOS
		gpio_72	4	IO								
		safe_mode	7									
AH23	NA	dss_data3	0	IO	L	L	7	vdds	Yes	8	PU/ PD	LVCMOS
		gpio_73	4	IO								
		safe_mode	7									
AG24	NA	dss_data4	0	IO	L	L	7	vdds	Yes	8	PU/ PD	LVCMOS
		uart3_rx_ irrx	2	I								
		gpio_74	4	IO								
		safe_mode	7									
AH24	NA	dss_data5	0	IO	L	L	7	vdds	Yes	8	PU/ PD	LVCMOS
		uart3_tx_ irtx	2	O								
		gpio_75	4	IO								
		safe_mode	7									
E26	NA	dss_data6	0	IO	L	L	7	vdds	Yes	8	PU/ PD	LVCMOS
		uart1_tx	2	O								
		gpio_76	4	IO								
		safe_mode	7									
F28	NA	dss_data7	0	IO	L	L	7	vdds	Yes	8	PU/ PD	LVCMOS
		uart1_rx	2	I								
		gpio_77	4	IO								
		safe_mode	7									
F27	NA	dss_data8	0	IO	L	L	7	vdds	Yes	8	PU/ PD	LVCMOS
		gpio_78	4	IO								
		safe_mode	7									
G26	NA	dss_data9	0	IO	L	L	7	vdds	Yes	8	PU/ PD	LVCMOS
		gpio_79	4	IO								
		safe_mode	7									
AD28	NA	dss_data10	0	IO	L	L	7	vdds	Yes	8	PU/ PD	LVCMOS
		gpio_80	4	IO								
		safe_mode	7									
AD27	NA	dss_data11	0	IO	L	L	7	vdds	Yes	8	PU/ PD	LVCMOS
		gpio_81	4	IO								
		safe_mode	7									
AB28	NA	dss_data12	0	IO	L	L	7	vdds	Yes	8	PU/ PD	LVCMOS
		gpio_82	4	IO								
		safe_mode	7									
AB27	NA	dss_data13	0	IO	L	L	7	vdds	Yes	8	PU/ PD	LVCMOS
		gpio_83	4	IO								
		safe_mode	7									
AA28	NA	dss_data14	0	IO	L	L	7	vdds	Yes	8	PU/ PD	LVCMOS
		gpio_84	4	IO								
		safe_mode	7									

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Table 2-1. Ball Characteristics (CBB Pkg.)[(1)] (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENG TH (mA) [11]	PULLUP /DOWN TYPE [12]	IO CELL [13]
AA27	NA	dss_data15	0	IO	L	L	7	vdds	Yes	8	PU/ PD	LVCMOS
		gpio_85	4	IO								
		safe_mode	7									
G25	NA	dss_data16	0	IO	L	L	7	vdds	Yes	8	PU/ PD	LVCMOS
		gpio_86	4	IO								
		safe_mode	7									
H27	NA	dss_data17	0	IO	L	L	7	vdds	Yes	8	PU/ PD	LVCMOS
		gpio_87	4	IO								
		safe_mode	7									
H26	NA	dss_data18	0	IO	L	L	7	vdds	Yes	8	PU/ PD	LVCMOS
		mcspi3_clk	2	IO								
		dss_data0	3	IO								
		gpio_88	4	IO								
		safe_mode	7									
H25	NA	dss_data19	0	IO	L	L	7	vdds	Yes	8	PU/ PD	LVCMOS
		mcspi3_ simo	2	IO								
		dss_data1	3	IO								
		gpio_89	4	IO								
		safe_mode	7									
E28	NA	dss_data20	0	O	H	H	7	vdds	Yes	8	PU/ PD	LVCMOS
		mcspi3_ somi	2	IO								
		dss_data2	3	IO								
		gpio_90	4	IO								
		safe_mode	7									
J26	NA	dss_data21	0	O	L	L	7	vdds	Yes	8	PU/ PD	LVCMOS
		mcspi3_cs0	2	IO								
		dss_data3	3	IO								
		gpio_91	4	IO								
		safe_mode	7									
AC27	NA	dss_data22	0	O	L	L	7	vdds	Yes	8	PU/ PD	LVCMOS
		mcspi3_cs1	2	O								
		dss_data4	3	IO								
		gpio_92	4	IO								
		safe_mode	7									
AC28	NA	dss_data23	0	O	L	L	7	vdds	Yes	8	PU/ PD	LVCMOS
		dss_data5	3	IO								
		gpio_93	4	IO								
		safe_mode	7									
W28	NA	tv_out2	0	O	Z	0	0	vdda_dac		NA[(2)]	NA	10-bit DAC
Y28	NA	tv_out1	0	O	Z	0	0	vdda_dac		NA[(2)]	NA	10-bit DAC
Y27	NA	tv_vfb1	0	AO	Z	NA	0	vdda_dac		NA[(2)]	NA	10-bit DAC
W27	NA	tv_vfb2	0	AO	Z	NA	0	vdda_dac		NA[(2)]	NA	10-bit DAC
W26	NA	tv_vref	0	AO	Z	NA	0	vdda_dac		NA[(2)]	NA	10-bit DAC
A24	NA	cam_hs	0	IO	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
		gpio_94	4	IO								
		safe_mode	7									
A23	NA	cam_vs	0	IO	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
		gpio_95	4	IO								
		safe_mode	7									
C25	NA	cam_ xclka	0	O	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
		gpio_96	4	IO								
		safe_mode	7									

(2) The drive strength is fixed regardless of the load. The driver is designed to drive 75ohm for video applications.

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Table 2-1. Ball Characteristics (CBB Pkg.)[(1)] (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENG TH (mA) [11]	PULLUP /DOWN TYPE [12]	IO CELL [13]
C27	NA	cam_pclk	0	I	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
		gpio_97	4	IO								
		safe_mode	7									
C23	NA	cam_fld	0	IO	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
		cam_global_reset	2	IO								
		gpio_98	4	IO								
		safe_mode	7									
AG17	NA	cam_d0	0	I	L	L	7	vdds	Yes	NA	PU/PD	LVCMOS
		gpio_99	4	I								
		safe_mode	7									
AH17	NA	cam_d1	0	I	L	L	7	vdds	Yes	NA	PU/PD	LVCMOS
		gpio_100	4	I								
		safe_mode	7									
B24	NA	cam_d2	0	I	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
		gpio_101	4	IO								
		safe_mode	7									
C24	NA	cam_d3	0	I	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
		gpio_102	4	IO								
		safe_mode	7									
D24	NA	cam_d4	0	I	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
		gpio_103	4	IO								
		safe_mode	7									
A25	NA	cam_d5	0	I	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
		gpio_104	4	IO								
		safe_mode	7									
K28	NA	cam_d6	0	I	L	L	7	vdds	Yes	NA	PU/PD	LVCMOS
		gpio_105	4	IO						8		
		safe_mode	7							NA		
L28	NA	cam_d7	0	I	L	L	7	vdds	Yes	NA	PU/PD	LVCMOS
		gpio_106	4	IO						8		
		safe_mode	7							NA		
K27	NA	cam_d8	0	I	L	L	7	vdds	Yes	NA	PU/PD	LVCMOS
		gpio_107	4	IO						8		
		safe_mode	7							NA		
L27	NA	cam_d9	0	I	L	L	7	vdds	Yes	NA	PU/PD	LVCMOS
		gpio_108	4	IO						8		
		safe_mode	7							NA		
B25	NA	cam_d10	0	I	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
		gpio_109	4	IO								
		safe_mode	7									
C26	NA	cam_d11	0	I	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
		gpio_110	4	IO								
		safe_mode	7									
B26	NA	cam_ xclkb	0	O	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
		gpio_111	4	IO								
		safe_mode	7									
B23	NA	cam_wen	0	I	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
		cam_ shutter	2	O								
		gpio_167	4	IO								
		safe_mode	7									
D25	NA	cam_ strobe	0	O	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
		gpio_126	4	IO								
		safe_mode	7									
AG19	NA	gpio_112	4	I	L	L	7	vdds	Yes	NA	PU/PD	LVCMOS

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Table 2-1. Ball Characteristics (CBB Pkg.)[1] (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENG TH (mA) [11]	PULLUP /DOWN TYPE [12]	IO CELL [13]
		safe_mode	7									
AH19	NA	gpio_113	4	I	L	L	7	vdds	Yes	NA	PU/PD	LVCMOS
		safe_mode	7									
AG18	NA	gpio_114	4	I	L	L	7	vdds	Yes	NA	PU/PD	LVCMOS
		safe_mode	7									
AH18	NA	gpio_115	4	I	L	L	7	vdds	Yes	NA	PU/PD	LVCMOS
		safe_mode	7									
P21	NA	mcbsp2_fsx	0	IO	L	L	7	vdds	Yes	4[3]	PU/ PD	LVCMOS
		gpio_116	4	IO								
		safe_mode	7									
N21	NA	mcbsp2_ clkx	0	IO	L	L	7	vdds	Yes	4[3]	PU/ PD	LVCMOS
		gpio_117	4	IO								
		safe_mode	7									
R21	NA	mcbsp2_dr	0	I	L	L	7	vdds	Yes	4[3]	PU/ PD	LVCMOS
		gpio_118	4	IO								
		safe_mode	7									
M21	NA	mcbsp2_dx	0	IO	L	L	7	vdds	Yes	4[4]	PU/ PD	LVCMOS
		gpio_119	4	IO								
		safe_mode	7									
N28	NA	mmc1_clk	0	O	L	L	7	vdds_mmc1	Yes	8	PU/ PD[5]	LVCMOS
		gpio_120	4	IO								
		safe_mode	7									
M27	NA	mmc1_cmd	0	IO	L	L	7	vdds_mmc1	Yes	8	PU/ PD[5]	LVCMOS
		gpio_121	4	IO								
		safe_mode	7									
N27	NA	mmc1_dat0	0	IO	L	L	7	vdds_mmc1	Yes	8	PU/ PD[5]	LVCMOS
		gpio_122	4	IO								
		safe_mode	7									
N26	NA	mmc1_dat1	0	IO	L	L	7	vdds_mmc1	Yes	8	PU/ PD[5]	LVCMOS
		gpio_123	4	IO								
		safe_mode	7									
N25	NA	mmc1_dat2	0	IO	L	L	7	vdds_mmc1	Yes	8	PU/ PD [5]	LVCMOS
		gpio_124	4	IO								
		safe_mode	7									
P28	NA	mmc1_dat3	0	IO	L	L	7	vdds_mmc1	Yes	8	PU/ PD[5]	LVCMOS
		gpio_125	4	IO								
		safe_mode	7									
P27	NA	mmc1_dat4	0	IO	L	L	7	vdds_mmc1a	No	8	PD[5]	LVCMOS
		gpio_126	4	IO								
		safe_mode	7									
P26	NA	mmc1_dat5	0	IO	L	L	7	vdds_mmc1a	No	8	PD[5]	LVCMOS
		gpio_127	4	IO								
		safe_mode	7									
R27	NA	mmc1_dat6	0	IO	L	L	7	vdds_mmc1a	No	8	PD[5]	LVCMOS
		gpio_128	4	IO								
		safe_mode	7									
R25	NA	mmc1_dat7	0	IO	L	L	7	vdds_mmc1a	No	8	PD [5]	LVCMOS
		gpio_129	4	IO								
		safe_mode	7									

(3) The buffer strength of this IO cell is programmable (2, 4, 6, or 8 mA) according to the selected mode; the default value is described in the above table.
(4) The buffer strength of this IO cell is programmable (2, 4, 6, or 8 mA) according to the selected mode; the default value is described in the above table.
(5) The PU nominal drive strength of this IO cell is equal to 25 uA @ 1.8V and 41.6 uA @ 3.0V. The PD nominal drive strength of this IO cell is equal to 1 mA @ 1.8V and 1.66 mA @ 3.0V.

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Table 2-1. Ball Characteristics (CBB Pkg.)[(1)] (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENG TH (mA) [11]	PULLUP /DOWN TYPE [12]	IO CELL [13]
AE2	NA	mmc2_clk	0	O	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
		mcspi3_clk	1	IO								
		gpio_130	4	IO								
		safe_mode	7									
AG5	NA	mmc2_ cmd	0	IO	H	H	7	vdds	Yes	4	PU/ PD	LVCMOS
		mcspi3_ simo	1	IO								
		gpio_131	4	IO								
		safe_mode	7									
AH5	NA	mmc2_ dat0	0	IO	H	H	7	vdds	Yes	4	PU/ PD	LVCMOS
		mcspi3_ somi	1	IO								
		gpio_132	4	IO								
		safe_mode	7									
AH4	NA	mmc2_ dat1	0	IO	H	H	7	vdds	Yes	4	PU/ PD	LVCMOS
		gpio_133	4	IO								
		safe_mode	7									
AG4	NA	mmc2_ dat2	0	IO	H	H	7	vdds	Yes	4	PU/ PD	LVCMOS
		mcspi3_cs1	1	O								
		gpio_134	4	IO								
		safe_mode	7									
AF4	NA	mmc2_ dat3	0	IO	H	H	7	vdds	Yes	4	PU/ PD	LVCMOS
		mcspi3_cs0	1	IO								
		gpio_135	4	IO								
		safe_mode	7									
AE4	NA	mmc2_ dat4	0	IO	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
		mmc2_dir_da t0	1	O								
		mmc3_dat0	3	IO								
		gpio_136	4	IO								
		safe_mode	7									
AH3	NA	mmc2_ dat5	0	IO	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
		mmc2_dir_da t1	1	O								
		cam_global_r eset	2	IO								
		mmc3_dat1	3	IO								
		gpio_137	4	IO								
		hsusb3_tll_st p	5	IO								
		mm3_rxdp	6	IO								
		safe_mode	7									
AF3	NA	mmc2_ dat6	0	IO	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
		mmc2_dir_ cmd	1	O								
		cam_ shutter	2	O								
		mmc3_dat2	3	IO								
		gpio_138	4	IO								
		hsusb3_tll_di r	5	IO								
		safe_mode	7									
AE3	NA	mmc2_ dat7	0	IO	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
		mmc2_ clkin	1	I								
		mmc3_dat3	3	IO								
		gpio_139	4	IO								
		hsusb3_tll_n xt	5	IO								
		mm3_rxdm	6	IO								

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Table 2-1. Ball Characteristics (CBB Pkg.)[(1)] (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENG TH (mA) [11]	PULLUP /DOWN TYPE [12]	IO CELL [13]
		safe_mode	7									
AF6	NA	mcbsp3_dx	0	IO	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
		uart2_cts	1	I								
		gpio_140	4	IO								
		hsusb3_tll_ data4	5	IO								
		safe_mode	7									
AE6	NA	mcbsp3_dr	0	I	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
		uart2_rts	1	O								
		gpio_141	4	IO								
		hsusb3_tll_ data5	5	IO								
		safe_mode	7									
AF5	NA	mcbsp3_ clkx	0	IO	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
		uart2_tx	1	O								
		gpio_142	4	IO								
		hsusb3_tll_ data6	5	IO								
		safe_mode	7									
AE5	NA	mcbsp3_fsx	0	IO	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
		uart2_rx	1	I								
		gpio_143	4	IO								
		hsusb3_tll_ data7	5	IO								
		safe_mode	7									
AB26	NA	uart2_cts	0	I	H	H	7	vdds	Yes	4	PU/ PD	LVCMOS
		mcbsp3_dx	1	IO								
		gpt9_pwm_e vt	2	IO								
		gpio_144	4	IO								
		safe_mode	7									
AB25	NA	uart2_rts	0	O	H	H	7	vdds	Yes	4	PU/ PD	LVCMOS
		mcbsp3_dr	1	I								
		gpt10_pwm_ evt	2	IO								
		gpio_145	4	IO								
		safe_mode	7									
AA25	NA	uart2_tx	0	O	H	H	7	vdds	Yes	4	PU/ PD	LVCMOS
		mcbsp3_ clkx	1	IO								
		gpt11_pwm _evt	2	IO								
		gpio_146	4	IO								
		safe_mode	7									
AD25	NA	uart2_rx	0	I	H	H	7	vdds	Yes	4	PU/ PD	LVCMOS
		mcbsp3_fsx	1	IO								
		gpt8_pwm_e vt	2	IO								
		gpio_147	4	IO								
		safe_mode	7									
AA8	NA	uart1_tx	0	O	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
		gpio_148	4	IO								
		safe_mode	7									
AA9	NA	uart1_rts	0	O	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
		gpio_149	4	IO								
		safe_mode	7									
W8	NA	uart1_cts	0	I	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS

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Table 2-1. Ball Characteristics (CBB Pkg.)[(1)] (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENG TH (mA) [11]	PULLUP /DOWN TYPE [12]	IO CELL [13]
		gpio_150	4	IO								
		hsusb3_tll_clk	5	O								
		safe_mode	7									
Y8	NA	uart1_rx	0	I	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
		mcbsp1_ clkr	2	IO								
		mcspi4_clk	3	IO								
		gpio_151	4	IO								
		safe_mode	7									
AE1	NA	mcbsp4_ clkx	0	IO	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
		gpio_152	4	IO								
		hsusb3_tll_ data1	5	IO								
		mm3_txse0	6	IO								
		safe_mode	7									
AD1	NA	mcbsp4_dr	0	I	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
		gpio_153	4	IO								
		hsusb3_tll_ data0	5	IO								
		mm3_rxrcv	6	IO								
		safe_mode	7									
AD2	NA	mcbsp4_dx	0	IO	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
		gpio_154	4	IO								
		hsusb3_tll_ data2	5	IO								
		mm3_txdat	6	IO								
		safe_mode	7									
AC1	NA	mcbsp4_fsx	0	IO	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
		gpio_155	4	IO								
		hsusb3_tll_ data3	5	IO								
		mm3_txen_n	6	IO								
		safe_mode	7									
Y21	NA	mcbsp1_ clkr	0	IO	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
		mcspi4_clk	1	IO								
		gpio_156	4	IO								
		safe_mode	7									
AA21	NA	mcbsp1_fsr	0	IO	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
		cam_global_reset	2	IO								
		gpio_157	4	IO								
		safe_mode	7									
V21	NA	mcbsp1_dx	0	IO	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
		mcspi4_ simo	1	IO								
		mcbsp3_dx	2	IO								
		gpio_158	4	IO								
		safe_mode	7									
U21	NA	mcbsp1_dr	0	I	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
		mcspi4_ somi	1	IO								
		mcbsp3_dr	2	O								
		gpio_159	4	IO								
		safe_mode	7									
T21	NA	mcbsp_clks	0	I	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
		cam_ shutter	2	O								
		gpio_160	4	IO								

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Table 2-1. Ball Characteristics (CBB Pkg.)[(1)] (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENG TH (mA) [11]	PULLUP /DOWN TYPE [12]	IO CELL [13]
		uart1_cts	5	I								
		safe_mode	7									
K26	NA	mcbsp1_fsx	0	IO	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
		mcspi4_cs0	1	IO								
		mcbsp3_fsx	2	IO								
		gpio_161	4	IO								
		safe_mode	7									
W21	NA	mcbsp1_ clkx	0	IO	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
		mcbsp3_ clkx	2	IO								
		gpio_162	4	IO								
		safe_mode	7									
H18	NA	uart3_cts_ rctx	0	IO	H	H	7	vdds	Yes	4	PU/ PD	LVCMOS
		gpio_163	4	IO								
		safe_mode	7									
H19	NA	uart3_rts_ sd	0	O	H	H	7	vdds	Yes	4	PU/ PD	LVCMOS
		gpio_164	4	IO								
		safe_mode	7									
H20	NA	uart3_rx_ irrx	0	I	H	H	7	vdds	Yes	4	PU/ PD	LVCMOS
		gpio_165	4	IO								
		safe_mode	7									
H21	NA	uart3_tx_ irtx	0	O	H	H	7	vdds	Yes	4	PU/ PD	LVCMOS
		gpio_166	4	IO								
		safe_mode	7									
T28	NA	hsusb0_clk	0	I	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
		gpio_120	4	IO								
		safe_mode	7									
T25	NA	hsusb0_stp	0	O	H	H	7	vdds	Yes	4	PU/ PD	LVCMOS
		gpio_121	4	IO								
		safe_mode	7									
R28	NA	hsusb0_dir	0	I	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
		gpio_122	4	IO								
		safe_mode	7									
T26	NA	hsusb0_nxt	0	I	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
		gpio_124	4	IO								
		safe_mode	7									
T27	NA	hsusb0_ data0	0	IO	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
		uart3_tx_ irtx	2	O								
		gpio_125	4	IO								
		safe_mode	7									
U28	NA	hsusb0_ data1	0	IO	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
		uart3_rx_ irrx	2	I								
		gpio_130	4	IO								
		safe_mode	7									
U27	NA	hsusb0_ data2	0	IO	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
		uart3_rts_ sd	2	O								
		gpio_131	4	IO								
		safe_mode	7									
U26	NA	hsusb0_ data3	0	IO	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
		uart3_cts_ rctx	2	IO								
		gpio_169	4	IO								

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Table 2-1. Ball Characteristics (CBB Pkg.)[(1)] (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENG TH (mA) [11]	PULLUP /DOWN TYPE [12]	IO CELL [13]
		safe_mode	7									
U25	NA	hsusb0_ data4	0	IO	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
		gpio_188	4	IO								
		safe_mode	7									
V28	NA	hsusb0_ data5	0	IO	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
		gpio_189	4	IO								
		safe_mode	7									
V27	NA	hsusb0_ data6	0	IO	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
		gpio_190	4	IO								
		safe_mode	7									
V26	NA	hsusb0_ data7	0	IO	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
		gpio_191	4	IO								
		safe_mode	7									
K21	NA	i2c1_scl	0	IOD	H	H	0	vdds	Yes	4	PU/ PD	Open Drain
J21	NA	i2c1_sda	0	IOD	H	H	0	vdds	Yes	4	PU/ PD	Open Drain
AF15	NA	i2c2_scl	0	IOD	H	H	7	vdds	Yes	4	PU/ PD	Open Drain
		gpio_168	4	IO								
		safe_mode	7									
AE15	NA	i2c2_sda	0	IOD	H	H	7	vdds	Yes	4	PU/ PD	Open Drain
		gpio_183	4	IO								
		safe_mode	7									
AF14	NA	i2c3_scl	0	IOD	H	H	7	vdds	Yes	4	PU/ PD	Open Drain
		gpio_184	4	IO								
		safe_mode	7									
AG14	NA	i2c3_sda	0	IOD	H	H	7	vdds	Yes	4	PU/ PD	Open Drain
		gpio_185	4	IO								
		safe_mode	7									
AD26	NA	i2c4_scl	0	IOD	H	H	0	vdds	Yes	4	PU/ PD	Open Drain
		sys_ nvmode1	1	O								
		safe_mode	7									
AE26	NA	i2c4_sda	0	IOD	H	H	0	vdds	Yes	4	PU/ PD	Open Drain
		sys_ nvmode2	1	O								
		safe_mode	7									
J25	NA	hdq_sio	0	IOD	H	H	7	vdds	Yes	4	PU/ PD	LVCMOS
		sys_altclk	1	I								
		i2c2_sccbe	2	O								
		i2c3_sccbe	3	O								
		gpio_170	4	IO								
		safe_mode	7									
AB3	NA	mcspi1_clk	0	IO	L	L	7	vdds	Yes	4[(6)]	PU/ PD	LVCMOS
		mmc2_dat4	1	IO								
		gpio_171	4	IO								
		safe_mode	7									
AB4	NA	mcspi1_ simo	0	IO	L	L	7	vdds	Yes	4[(6)]	PU/ PD	LVCMOS
		mmc2_dat5	1	IO								
		gpio_172	4	IO								
		safe_mode	7									
AA4	NA	mcspi1_ somi	0	IO	L	L	7	vdds	Yes	4[(6)]	PU/ PD	LVCMOS

(6) The buffer strength of this IO cell is programmable (2, 4, 6, or 8 mA) according to the selected mode; the default value is described in the above table.

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Table 2-1. Ball Characteristics (CBB Pkg.)[(1)] (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENG TH (mA) [11]	PULLUP /DOWN TYPE [12]	IO CELL [13]
		mmc2_dat6	1	IO								
		gpio_173	4	IO								
		safe_mode	7									
AC2	NA	mcspi1_cs0	0	IO	H	H	7	vdds	Yes	4[(6)]	PU/ PD	LVCMOS
		mmc2_dat7	1	IO								
		gpio_174	4	IO								
		safe_mode	7									
AC3	NA	mcspi1_cs1	0	O	L	H	7	vdds	Yes	4 [(6)]	PU/ PD	LVCMOS
		mmc3_cmd	3	IO								
		gpio_175	4	IO								
		safe_mode	7									
AB1	NA	mcspi1_cs2	0	O	L	H	7	vdds	Yes	4[(6)]	PU/ PD	LVCMOS
		mmc3_clk	3	O								
		gpio_176	4	IO								
		safe_mode	7									
AB2	NA	mcspi1_cs3	0	O	H	H	7	vdds	Yes	4	PU/ PD	LVCMOS
		hsusb2_tll_ data2	2	IO								
		hsusb2_ data2	3	IO								
		gpio_177	4	IO								
		mm2_txdat	5	IO								
		safe_mode	7									
AA3	NA	mcspi2_clk	0	IO	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
		hsusb2_tll_ data7	2	IO								
		hsusb2_ data7	3	O								
		gpio_178	4	IO								
		safe_mode	7									
Y2	NA	mcspi2_ simo	0	IO	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
		gpt9_pwm_e vt	1	IO								
		hsusb2_tll_ data4	2	IO								
		hsusb2_ data4	3	I								
		gpio_179	4	IO								
		safe_mode	7									
Y3	NA	mcspi2_ somi	0	IO	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
		gpt10_pwm_ evt	1	IO								
		hsusb2_tll_ data5	2	IO								
		hsusb2_ data5	3	O								
		gpio_180	4	IO								
		safe_mode	7									
Y4	NA	mcspi2_cs0	0	IO	H	H	7	vdds	Yes	4	PU/ PD	LVCMOS
		gpt11_pwm_ evt	1	IO								
		hsusb2_tll_ data6	2	IO								
		hsusb2_ data6	3	O								
		gpio_181	4	IO								
		safe_mode	7									
V3	NA	mcspi2_cs1	0	O	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS

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Table 2-1. Ball Characteristics (CBB Pkg.)[(1)] (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENG TH (mA) [11]	PULLUP /DOWN TYPE [12]	IO CELL [13]
		gpt8_pwm_evt	1	IO								
		hsusb2_tll_data3	2	IO								
		hsusb2_data3	3	IO								
		gpio_182	4	IO								
		mm2_txen_n	5	IO								
		safe_mode	7									
AE25	NA	sys_32k	0	I	Z	I	NA	vdds	Yes	NA	NA	LVCMOS
AE17	NA	sys_xtalin	0	I	Z	I	NA	vdds	NA	NA	NA	LVCMOS
AF17	NA	sys_xtalout	0	O	Z	O	NA	vdds	NA	NA	NA	LVCMOS
AF25	NA	sys_clkreq	0	IO	0	1	0	vdds	Yes	8	PU/ PD	LVCMOS
		gpio_1	4	IO								
		safe_mode	7									
AF26	NA	sys_nirq	0	I	H	H	7	vdds	Yes	4	PU/ PD	LVCMOS
		gpio_0	4	IO								
		safe_mode	7									
AH25	NA	sys_nrespwron	0	I	Z	I	NA	vdds	Yes	NA	NA	LVCMOS
AF24	NA	sys_nreswarm	0	IOD	0	1 (PU)	0	vdds	Yes	8	PU/ PD	LVCMOS
		gpio_30	4	IO								Open Drain
		safe_mode	7									
AH26	NA	sys_boot0	0	I	Z	Z	0	vdds	Yes	4	PU/ PD	LVCMOS
		gpio_2	4	IO								
		safe_mode	7									
AG26	NA	sys_boot1	0	I	Z	Z	0	vdds	Yes	4	PU/ PD	LVCMOS
		gpio_3	4	IO								
		safe_mode	7									
AE14	NA	sys_boot2	0	I	Z	Z	0	vdds	Yes	4	PU/ PD	LVCMOS
		gpio_4	4	IO								
		safe_mode	7									
AF18	NA	sys_boot3	0	I	Z	Z	0	vdds	Yes	4	PU/ PD	LVCMOS
		gpio_5	4	IO								
		safe_mode	7									
AF19	NA	sys_boot4	0	I	Z	Z	0	vdds	Yes	4	PU/ PD	LVCMOS
		mmc2_dir_dat2	1	O								
		gpio_6	4	IO								
		safe_mode	7									
AE21	NA	sys_boot5	0	I	Z	Z	0	vdds	Yes	4	PU/ PD	LVCMOS
		mmc2_dir_dat3	1	O								
		gpio_7	4	IO								
		safe_mode	7									
AF21	NA	sys_boot6	0	I	Z	Z	0	vdds	Yes	4	PU/ PD	LVCMOS
		gpio_8	4	IO								
		safe_mode	7									
AF22	NA	sys_off_mode	0	O	0	L	7	vdds	Yes	8	PU/ PD	LVCMOS
		gpio_9	4	IO								
		safe_mode	7									
AG25	NA	sys_clkout1	0	O	L	L	7	vdds	Yes	8	PU/ PD	LVCMOS
		gpio_10	4	IO								
		safe_mode	7									
AE22	NA	sys_clkout2	0	O	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
		gpio_186	4	IO								

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Table 2-1. Ball Characteristics (CBB Pkg.)[(1)] (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENG TH (mA) [11]	PULLUP /DOWN TYPE [12]	IO CELL [13]
		safe_mode	7									
AA17	NA	jtag_ntrst	0	I	L	L	0	vdds	Yes	NA	PU/ PD	LVCMOS
AA13	NA	jtag_tck	0	I	L	L	0	vdds	Yes	NA	PU/ PD	LVCMOS
AA12	NA	jtag_rtck	0	O	L	0	0	vdds	Yes	8	PU/ PD	LVCMOS
AA18	NA	jtag_tms_tmsc	0	IO	H	H	0	vdds	Yes	8	PU/ PD	LVCMOS
AA20	NA	jtag_tdi	0	I	H	H	0	vdds	Yes	NA	PU/ PD	LVCMOS
AA19	NA	jtag_tdo	0	O	L	Z	0	vdds	Yes	8	PU/ PD	LVCMOS
AA11	NA	jtag_emu0	0	IO	H	H	0	vdds	Yes	8	PU/ PD	LVCMOS
		gpio_11	4	IO								
		safe_mode	7									
AA10	NA	jtag_emu1	0	IO	H	H	0	vdds	Yes	8	PU/ PD	LVCMOS
		gpio_31	4	IO								
		safe_mode	7									
AF10	NA	etk_clk	0	O	H	H	4	vdds	Yes	4	PU/ PD	LVCMOS
		mcbsp5_clkx	1	IO								
		mmc3_clk	2	O								
		hsusb1_stp	3	O								
		gpio_12	4	IO								
		mm1_rxdp	5	IO								
		hsusb1_tll_stp	6	I								
AE10	NA	etk_ctl	0	O	H	H	4	vdds	Yes	4	PU/ PD	LVCMOS
		mmc3_cmd	2	IO								
		hsusb1_clk	3	O								
		gpio_13	4	IO								
		hsusb1_tll_clk	6	O								
AF11	NA	etk_d0	0	O	H	H	4	vdds	Yes	4	PU/ PD	LVCMOS
		mcspi3_simo	1	IO								
		mmc3_dat4	2	IO								
		hsusb1_data0	3	IO								
		gpio_14	4	IO								
		mm1_rxrcv	5	IO								
		hsusb1_tll_data0	6	IO								
AG12	NA	etk_d1	0	O	H	H	4	vdds	Yes	4	PU/ PD	LVCMOS
		mcspi3_somi	1	IO								
		hsusb1_data1	3	IO								
		gpio_15	4	IO								
		mm1_txse0	5	IO								
		hsusb1_tll_data1	6	IO								
AH12	NA	etk_d2	0	O	H	H	4	vdds	Yes	4	PU/ PD	LVCMOS
		mcspi3_cs0	1	IO								
		hsusb1_data2	3	IO								
		gpio_16	4	IO								
		mm1_txdat	5	IO								
		hsusb1_tll_data2	6	IO								
AE13	NA	etk_d3	0	O	H	H	4	vdds	Yes	4	PU/ PD	LVCMOS
		mcspi3_clk	1	IO								
		mmc3_dat3	2	IO								

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Table 2-1. Ball Characteristics (CBB Pkg.)[(1)] (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENG TH (mA) [11]	PULLUP /DOWN TYPE [12]	IO CELL [13]
		hsusb1_ data7	3	IO								
		gpio_17	4	IO								
		hsusb1_tll_ data7	6	IO								
AE11	NA	etk_d4	0	O	L	L	4	vdds	Yes	4	PU/ PD	LVCMOS
		mcbsp5_dr	1	I								
		mmc3_dat0	2	IO								
		hsusb1_ data4	3	IO								
		gpio_18	4	IO								
		hsusb1_tll_ data4	6	IO								
AH9	NA	etk_d5	0	O	L	L	4	vdds	Yes	4	PU/ PD	LVCMOS
		mcbsp5_fsx	1	IO								
		mmc3_dat1	2	IO								
		hsusb1_ data5	3	IO								
		gpio_19	4	IO								
		hsusb1_tll_ data5	6	IO								
AF13	NA	etk_d6	0	O	L	L	4	vdds	Yes	4	PU/ PD	LVCMOS
		mcbsp5_dx	1	IO								
		mmc3_dat2	2	IO								
		hsusb1_ data6	3	IO								
		gpio_20	4	IO								
		hsusb1_tll_ data6	6	IO								
AH14	NA	etk_d7	0	O	L	L	4	vdds	Yes	4	PU/ PD	LVCMOS
		mcspi3_cs1	1	O								
		mmc3_dat7	2	IO								
		hsusb1_ data3	3	IO								
		gpio_21	4	IO								
		mm1_txen_n	5	IO								
		hsusb1_tll_ data3	6	IO								
AF9	NA	etk_d8	0	O	L	L	4	vdds	Yes	4	PU/ PD	LVCMOS
		sys_drm_ msecure	1	I								
		mmc3_dat6	2	IO								
		hsusb1_dir	3	I								
		gpio_22	4	IO								
		hsusb1_tll_di r	6	O								
AG9	NA	etk_d9	0	O	L	L	4	vdds	Yes	4	PU/ PD	LVCMOS
		sys_secure_i ndic ator	1	O								
		mmc3_dat5	2	IO								
		hsusb1_nxt	3	I								
		gpio_23	4	IO								
		mm1_rxdm	5	IO								
		hsusb1_tll_n xt	6	O								
AE7	NA	etk_d10	0	O	L	L	4	vdds	Yes	4	PU/ PD	LVCMOS
		uart1_rx	2	I								
		hsusb2_clk	3	O								
		gpio_24	4	IO								

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Table 2-1. Ball Characteristics (CBB Pkg.)[(1)] (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENG TH (mA) [11]	PULLUP /DOWN TYPE [12]	IO CELL [13]
		hsusb2_tll_clk	6	O								
AF7	NA	etk_d11	0	O	L	L	4	vdds	Yes	4	PU/ PD	LVCMOS
		hsusb2_stp	3	O								
		gpio_25	4	IO								
		mm2_rxdp	5	IO								
		hsusb2_tll_stp	6	I								
AG7	NA	etk_d12	0	O	L	L	4	vdds	Yes	4	PU/ PD	LVCMOS
		hsusb2_dir	3	I								
		gpio_26	4	IO								
		hsusb2_tll_dir	6	O								
AH7	NA	etk_d13	0	O	L	L	4	vdds	Yes	4	PU/ PD	LVCMOS
		hsusb2_nxt	3	I								
		gpio_27	4	IO								
		mm2_rxdm	5	IO								
		hsusb2_tll_nxt	6	O								
AG8	NA	etk_d14	0	O	L	L	4	vdds	Yes	4	PU/ PD	LVCMOS
		hsusb2_ data0	3	IO								
		gpio_28	4	IO								
		mm2_rxrcv	5	IO								
		hsusb2_tll_ data0	6	IO								
AH8	NA	etk_d15	0	O	L	L	4	vdds	Yes	4	PU/ PD	LVCMOS
		hsusb2_ data1	3	IO								
		gpio_29	4	IO								
		mm2_txse0	5	IO								
		hsusb2_tll_ data1	6	IO								
AE9, AE18, AE19, AE24, AC4, Y16, Y18, Y19, Y20, W18, W20, V20, U19, U20, T19, P20, N19, N20, M19, M25, L25, K18, K20, J4, J18, J19, J20, H4, E25, D8, D9, D15, D22, D23	NA	vdd_core	0	PWR	-	-	-	-	-	-	-	-
Y9, Y10, Y11, Y14, Y15, W9, W11, W12, W15, U10, T9, T10, R9, R10, N10, M9, M10, L9, L10, K11, K14, K13, J9, J10, J11, J14, J15	NA	vdd_mpu _iva	0	PWR	-	-	-	-	-	-	-	-
AH6, U1, R4, J1, J2, G28, F1, F2, D16, C16, C28, B5, B8, B12, B18, B22, A5, A8, A12, A18, A22	NA	vdds_mem	0	PWR	-	-	-	-	-	-	-	-

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Table 2-1. Ball Characteristics (CBB Pkg.)[(1)] (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENG TH (mA) [11]	PULLUP /DOWN TYPE [12]	IO CELL [13]
AG20, AG21, AG27, AF8, AF16, AF23, AE8, AE16, AE23, AE27, AD3, AD4, W4, H28, F25, F26	NA	vdds	0	PWR	-	-	-	-	-	-	-	-
W16	NA	vdds_sram	0									
K15	NA	vdds_dpll_dll	0	PWR	-	-	-	-	-	-	-	-
AA16	NA	vdds_dpll_per	0	PWR	-	-	-	-	-	-	-	-
AA14	NA	vdds_wkup_bg	0	PWR	-	-	-	-	-	-	-	-
K25, P25	NA	vdds_mmc1, vdds_mmc1a	0	PWR	-	-	-	-	-	-	-	-
V25	NA	vdda_dac	0	PWR	-	-	-	-	-	-	-	-
Y26	NA	vssa_dac	0	GND	-	-	-	-	-	-	-	-
AA26, AG2, AG3, AG6, AF12, AF20, AE12, AE20, AC25, AC26, AG16, AH21, Y12, Y13, Y17, Y25, W3, W10, W13, W14, W17, W19, W25, V9, V10, V19, U2, U9, T20, R19, R20, R26, P3, P4, P9, P10, P19, N9, M20, M28, L19, L20, L26, K9, K10, K12, K16, K17, K19, J3, J12, J13, J16, J17, G27, E3,E4, D7, D10, D13, D19, D21, C7, C10, C13, C19, C22, B2, B27, A3, A26	NA	vss	0	GND	-	-	-	-	-	-	-	-
AH20, AA15, V4, L21	NA	cap_vdd_d, cap_vdd_wkup, cap_vdd_sram_mpu _iva, cap_vdd_sram_core	0	PWR	-	-	-	-	-	-	-	-
AH1, AH2, AH10, AH11, AH13, AH15, AH16, AH27, AH28, AG1, AG10, AG11, AG13, AG15, AG28, AF1, AF2, AF27, AF28, AE28, AA1, AA2, N1, N2, M1, M2, M26, J27, J28, B15, B28, A2, A15, A27, A28	A2, A12, A22, A23, AA1, AA2, AA22, AA23, AB1, AB11, AB13, AB23, AB8, AB9, AC1, AC11, AC13, AC14, AC2, AC22, AC23, AC8, AC9, B12, B23, H22, H23, K1, K2, K22, L1, L2, U1, U2, Y23	FeedThrough Pins[(7)]	-	-	-	-	-	-	-	-	-	-
A1, B1, G1, U4	A1, AB2, AB22, B1, B2, B22	No Connect	-	-								

(7) These signals are feed-through balls. For more information, see Section 2.5.10.

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Table 2-2. Ball Characteristics (CBC Pkg.)(1)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENG TH (mA) [11]	PULLUP /DOWN TYPE [12]	IO CELL [13]
AE16	NA	cam_d0	0	I	L	L	7	vdds	Yes	4	PU100/ PD100	LVCMOS
		gpio_99	4	I								
		safe_mode	7	-								
AE15	NA	cam_d1	0	I	L	L	7	vdds	Yes	4	PU100/ PD100	LVCMOS
		gpio_100	4	I								
		safe_mode	7	-								
AD17	NA	gpio_112	4	I	L	L	7	vdds	Yes	4	PU100/ PD100	LVCMOS
		safe_mode	7	-								
AE18	NA	gpio_114	4	I	L	L	7	vdds	Yes	4	PU100/ PD100	LVCMOS
		safe_mode	7	-								
AD16	NA	gpio_113	4	I	L	L	7	vdds	Yes	4	PU100/ PD100	LVCMOS
		safe_mode	7	-								
AE17	NA	gpio_115	4	I	L	L	7	vdds	Yes	4	PU100/ PD100	LVCMOS
		safe_mode	7	-								
NA	G20	sdrc_a0	0	O	0	0	0	vdds	No	4(2)	NA	LVCMOS
NA	K20	sdrc_a1	0	O	0	0	0	vdds	No	4(2)	NA	LVCMOS
NA	J20	sdrc_a2	0	O	0	0	0	vdds	No	4(2)	NA	LVCMOS
NA	J21	sdrc_a3	0	O	0	0	0	vdds	No	4(2)	NA	LVCMOS
NA	U21	sdrc_a4	0	O	0	0	0	vdds	No	4(2)	NA	LVCMOS
NA	R20	sdrc_a5	0	O	0	0	0	vdds	No	4(2)	NA	LVCMOS
NA	M21	sdrc_a6	0	O	0	0	0	vdds	No	4(2)	NA	LVCMOS
NA	M20	sdrc_a7	0	O	0	0	0	vdds	No	4(2)	NA	LVCMOS
NA	N20	sdrc_a8	0	O	0	0	0	vdds	No	4 (2)	NA	LVCMOS
NA	K21	sdrc_a9	0	O	0	0	0	vdds	No	4(2)	NA	LVCMOS
NA	Y16	sdrc_a10	0	O	0	0	0	vdds	No	4(2)	NA	LVCMOS
NA	N21	sdrc_a11	0	O	0	0	0	vdds	No	4(2)	NA	LVCMOS
NA	R21	sdrc_a12	0	O	0	0	0	vdds	No	4(2)	NA	LVCMOS
NA	AA15	sdrc_a13	0	O	0	0	0	vdds	No	4(2)	NA	LVCMOS
NA	Y12	sdrc_a14	0	O	0	0	0	vdds	No	4(2)	NA	LVCMOS
NA	AA18	sdrc_ba0	0	O	0	0	0	vdds	No	4 (2)	NA	LVCMOS
NA	V20	sdrc_ba1	0	O	0	0	0	vdds	No	4 (2)	NA	LVCMOS
NA	Y15	sdrc_cke0	0	O	H	1	7	vdds	Yes	4 (2)	PU100/ PD100	LVCMOS
		safe_mode	7									
NA	Y13	sdrc_cke1	0	O	H	1	7	vdds	Yes	4 (2)	PU100/ PD100	LVCMOS
		safe_mode	7									
NA	A12	sdrc_clk	0	IO	L	0	0	vdds	Yes	4(2)	PU100/ PD100	LVCMOS
NA	D1	sdrc_d0	0	IO	L	Z	0	vdds	Yes	4(2)	PU100/ PD100	LVCMOS
NA	G1	sdrc_d1	0	IO	L	Z	0	vdds	Yes	4(2)	PU100/ PD100	LVCMOS
NA	G2	sdrc_d2	0	IO	L	Z	0	vdds	Yes	4(2)	PU100/ PD100	LVCMOS
NA	E1	sdrc_d3	0	IO	L	Z	0	vdds	Yes	4(2)	PU100/ PD100	LVCMOS
NA	D2	sdrc_d4	0	IO	L	Z	0	vdds	Yes	4(2)	PU100/ PD100	LVCMOS
NA	E2	sdrc_d5	0	IO	L	Z	0	vdds	Yes	4(2)	PU100/ PD100	LVCMOS

(1) NA in this table stands for Not Applicable.
(2) The drive strength is programmable vs the capacity load: load range = [2 pF to 6 pF] per default or [6 pF to 12 pF] according to the selected mode.

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Table 2-2. Ball Characteristics (CBC Pkg.)[(1)] (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENG TH (mA) [11]	PULLUP /DOWN TYPE [12]	IO CELL [13]
NA	B3	sdrc_d6	0	IO	L	Z	0	vdds	Yes	4[(2)]	PU100/ PD100	LVCMOS
NA	B4	sdrc_d7	0	IO	L	Z	0	vdds	Yes	4[(2)]	PU100/ PD100	LVCMOS
NA	A10	sdrc_d8	0	IO	L	Z	0	vdds	Yes	4[(2)]	PU100/ PD100	LVCMOS
NA	B11	sdrc_d9	0	IO	L	Z	0	vdds	Yes	4[(2)]	PU100/ PD100	LVCMOS
NA	A11	sdrc_d10	0	IO	L	Z	0	vdds	Yes	4[(2)]	PU100/ PD100	LVCMOS
NA	B12	sdrc_d11	0	IO	L	Z	0	vdds	Yes	4 [(2)]	PU100/ PD100	LVCMOS
NA	A16	sdrc_d12	0	IO	L	Z	0	vdds	Yes	4[(2)]	PU100/ PD100	LVCMOS
NA	A17	sdrc_d13	0	IO	L	Z	0	vdds	Yes	4[(2)]	PU100/ PD100	LVCMOS
NA	B17	sdrc_d14	0	IO	L	Z	0	vdds	Yes	4[(2)]	PU100/ PD100	LVCMOS
NA	B18	sdrc_d15	0	IO	L	Z	0	vdds	Yes	4[(2)]	PU100/ PD100	LVCMOS
NA	B7	sdrc_d16	0	IO	L	Z	0	vdds	Yes	4 [(3)]	PU100/ PD100	LVCMOS
NA	A5	sdrc_d17	0	IO	L	Z	0	vdds	Yes	4[(3)]	PU100/ PD100	LVCMOS
NA	B6	sdrc_d18	0	IO	L	Z	0	vdds	Yes	4[(3)]	PU100/ PD100	LVCMOS
NA	A6	sdrc_d19	0	IO	L	Z	0	vdds	Yes	4[(3)]	PU100/ PD100	LVCMOS
NA	A8	sdrc_d20	0	IO	L	Z	0	vdds	Yes	4[(3)]	PU100/ PD100	LVCMOS
NA	B9	sdrc_d21	0	IO	L	Z	0	vdds	Yes	4[(3)]	PU100/ PD100	LVCMOS
NA	A9	sdrc_d22	0	IO	L	Z	0	vdds	Yes	4[(3)]	PU100/ PD100	LVCMOS
NA	B10	sdrc_d23	0	IO	L	Z	0	vdds	Yes	4[(3)]	PU100/ PD100	LVCMOS
NA	C21	sdrc_d24	0	IO	L	Z	0	vdds	Yes	4[(3)]	PU100/ PD100	LVCMOS
NA	D20	sdrc_d25	0	IO	L	Z	0	vdds	Yes	4 [(3)]	PU100/ PD100	LVCMOS
NA	B19	sdrc_d26	0	IO	L	Z	0	vdds	Yes	4[(3)]	PU100/ PD100	LVCMOS
NA	C20	sdrc_d27	0	IO	L	Z	0	vdds	Yes	4[(3)]	PU100/ PD100	LVCMOS
NA	D21	sdrc_d28	0	IO	L	Z	0	vdds	Yes	4 [(3)]	PU100/ PD100	LVCMOS
NA	E20	sdrc_d29	0	IO	L	Z	0	vdds	Yes	4[(3)]	PU100/ PD100	LVCMOS
NA	E21	sdrc_d30	0	IO	L	Z	0	vdds	Yes	4[(3)]	PU100/ PD100	LVCMOS
NA	G21	sdrc_d31	0	IO	L	Z	0	vdds	Yes	4[(3)]	PU100/ PD100	LVCMOS
NA	H1	sdrc_dm0	0	O	0	0	0	vdds	No	4[(3)]	NA	LVCMOS
NA	A14	sdrc_dm1	0	O	0	0	0	vdds	No	4[(3)]	NA	LVCMOS
NA	A4	sdrc_dm2	0	O	0	0	0	vdds	No	4 [(3)]	NA	LVCMOS
NA	A18	sdrc_dm3	0	O	0	0	0	vdds	No	4[(3)]	NA	LVCMOS
NA	C2	sdrc_dqs0	0	IO	L	Z	0	vdds	Yes	4[(3)]	PU100/ PD100	LVCMOS
NA	B15	sdrc_dqs1	0	IO	L	Z	0	vdds	Yes	4[(3)]	PU100/ PD100	LVCMOS
NA	B8	sdrc_dqs2	0	IO	L	Z	0	vdds	Yes	4 [(3)]	PU100/ PD100	LVCMOS
NA	A19	sdrc_dqs3	0	IO	L	Z	0	vdds	Yes	4[(3)]	PU100/ PD100	LVCMOS

(3) The drive strength is programmable vs the capacity load: load range = [2 pF to 6 pF] per default or [6 pF to 12 pF] according to the selected mode.

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Table 2-2. Ball Characteristics (CBC Pkg.)[1] (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENG TH (mA) [11]	PULLUP /DOWN TYPE [12]	IO CELL [13]
NA	U20	sdrc_ncas	0	O	1	1	0	vdds	No	4[3]	NA	LVCMOS
NA	B13	sdrc_nclk	0	O	1	1	0	vdds	No	4[3]	NA	LVCMOS
NA	T21	sdrc_ncs0	0	O	1	1	0	vdds	No	4[3]	NA	LVCMOS
NA	T20	sdrc_ncs1	0	O	1	1	0	vdds	No	4[3]	NA	LVCMOS
NA	V21	sdrc_nras	0	O	1	1	0	vdds	No	4 [3]	NA	LVCMOS
NA	Y18	sdrc_nwe	0	O	1	1	0	vdds	No	4[3]	NA	LVCMOS
AE21	NA	dss_data0	0	IO	L	L	7	vdds	No	4	PU100/ PD100	LVCMOS
		uart1_cts	2	I								
		gpio_70	4	IO								
		safe_mode	7	-								
AE22	NA	dss_data1	0	IO	L	L	7	vdds	No	4	PU100/ PD100	LVCMOS
		uart1_rts	2	O								
		gpio_71	4	IO								
		safe_mode	7	-								
AE23	NA	dss_data2	0	IO	L	L	7	vdds	No	4	PU100/ PD100	LVCMOS
		gpio_72	4	IO								
		safe_mode	7	-								
AE24	NA	dss_data3	0	IO	L	L	7	vdds	No	4	PU100/ PD100	LVCMOS
		gpio_73	4	IO								
		safe_mode	7	-								
AD23	NA	dss_data4	0	IO	L	L	7	vdds	No	4	PU100/ PD100	LVCMOS
		uart3_rx_irrx	2	I								
		gpio_74	4	IO								
		safe_mode	7	-								
AD24	NA	dss_data5	0	IO	L	L	7	vdds	No	4	PU100/ PD100	LVCMOS
		uart3_tx_irtx	2	O								
		gpio_75	4	IO								
		safe_mode	7	-								
AC26	NA	dss_data10	0	IO	L	L	7	vdds	NA	4	PU100/ PD100	LVCMOS
		gpio_80	4	IO								
		safe_mode	7	-								
AD26	NA	dss_data11	0	IO	L	L	7	vdds	NA	4	PU100/ PD100	LVCMOS
		gpio_81	4	IO								
		safe_mode	7	-								
AA25	NA	dss_data12	0	IO	L	L	7	vdds	NA	4	PU100/ PD100	LVCMOS
		gpio_82	4	IO								
		safe_mode	7	-								
Y25	NA	dss_data13	0	IO	L	L	7	vdds	NA	4	PU100/ PD100	LVCMOS
		gpio_83	4	IO								
		safe_mode	7	-								
AA26	NA	dss_data14	0	IO	L	L	7	vdds	NA	4	PU100/ PD100	LVCMOS
		gpio_84	4	IO								
		safe_mode	7	-								
AB26	NA	dss_data15	0	IO	L	L	7	vdds	NA	4	PU100/ PD100	LVCMOS
		gpio_85	4	IO								
		safe_mode	7	-								
F25	NA	dss_data20	0	O	H	H	7	vdds	Yes	4	PU100/ PD100	LVCMOS

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Table 2-2. Ball Characteristics (CBC Pkg.)[(1)] (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENG TH (mA) [11]	PULLUP /DOWN TYPE [12]	IO CELL [13]
		mcspi3_somi	2	IO								
		dss_data2	3	IO								
		gpio_90	4	IO								
		safe_mode	7	-								
AC25	NA	dss_data22	0	O	L	L	7	vdds	NA	4	PU100/ PD100	LVCMOS
		mcspi3_cs1	2	O								
		dss_data4	3	IO								
		gpio_92	4	IO								
		safe_mode	7	-								
AB25	NA	dss_data23	0	O	L	L	7	vdds	NA	4	PU100/ PD100	LVCMOS
		dss_data5	3	IO								
		gpio_93	4	IO								
		safe_mode	7	-								
G25	NA	dss_pclk	0	O	H	H	7	vdds	Yes	4	PU100/ PD100	LVCMOS
		gpio_66	4	IO								
		hw_dbg12	5	O								
		safe_mode	7	-								
J2	NA	gpmc_a1	0	O	L	L	7	vdds	Yes	4 [(4)]	PU100/ PD100	LVCMOS
		gpio_34	4	IO								
		safe_mode	7	-								
H1	NA	gpmc_a2	0	O	L	L	7	vdds	Yes	4[(4)]	PU100/ PD100	LVCMOS
		gpio_35	4	IO								
		safe_mode	7	-								
H2	NA	gpmc_a3	0	O	L	L	7	vdds	Yes	4[(4)]	PU100/ PD100	LVCMOS
		gpio_36	4	IO								
		safe_mode	7	-								
G2	NA	gpmc_a4	0	O	L	L	7	vdds	Yes	4 [(4)]	PU100/ PD100	LVCMOS
		gpio_37	4	IO								
		safe_mode	7	-								
F1	NA	gpmc_a5	0	O	L	L	7	vdds	Yes	4[(4)]	PU100/ PD100	LVCMOS
		gpio_38	4	IO								
		safe_mode	7	-								
F2	NA	gpmc_a6	0	O	H	H	7	vdds	Yes	4 [(4)]	PU100/ PD100	LVCMOS
		gpio_39	4	IO								
		safe_mode	7	-								
E1	NA	gpmc_a7	0	O	H	H	7	vdds	Yes	4[(4)]	PU100/ PD100	LVCMOS
		gpio_40	4	IO								
		safe_mode	7	-								
E2	NA	gpmc_a8	0	O	H	H	7	vdds	Yes	4[(4)]	PU100/ PD100	LVCMOS
		gpio_41	4	IO								
		safe_mode	7	-								
D1	NA	gpmc_a9	0	O	H	H	7	vdds	Yes	4[(4)]	PU100/ PD100	LVCMOS
		sys_ndmareq 2	1	I								
		gpio_42	4	IO								
		safe_mode	7	-								

(4) The drive strength is programmable vs the capacity load: load range = [2 pF to 6 pF] per default or [6 pF to 12 pF] according to the selected mode.

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Table 2-2. Ball Characteristics (CBC Pkg.)[(1)] (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENG TH (mA) [11]	PULLUP /DOWN TYPE [12]	IO CELL [13]
D2	NA	gpmc_a10	0	O	H	H	7	vdds	Yes	4[(4)]	PU100/ PD100	LVCMOS
		sys_ndmareq 3	1	I								
		gpio_43	4	IO								
		safe_mode	7	-								
N1	L1	gpmc_clk	0	O	L	0	0	vdds	Yes	4[(4)]	PU100/ PD100	LVCMOS
		gpio_59	4	IO								
		safe_mode	7	-								
AA2	U2	gpmc_d0	0	IO	H	H	0	vdds	Yes	4[(4)]	PU100/ PD100	LVCMOS
AA1	U1	gpmc_d1	0	IO	H	H	0	vdds	Yes	4[(4)]	PU100/ PD100	LVCMOS
AC2	V2	gpmc_d2	0	IO	H	H	0	vdds	Yes	4[(4)]	PU100/ PD100	LVCMOS
AC1	V1	gpmc_d3	0	IO	H	H	0	vdds	Yes	4[(4)]	PU100/ PD100	LVCMOS
AE5	AA3	gpmc_d4	0	IO	H	H	0	vdds	Yes	4[(4)]	PU100/ PD100	LVCMOS
AD6	AA4	gpmc_d5	0	IO	H	H	0	vdds	Yes	4[(5)]	PU100/ PD100	LVCMOS
AD5	Y3	gpmc_d6	0	IO	H	H	0	vdds	Yes	4[(5)]	PU100/ PD100	LVCMOS
AC5	Y4	gpmc_d7	0	IO	H	H	0	vdds	Yes	4[(5)]	PU100/ PD100	LVCMOS
V1	R1	gpmc_d8	0	IO	H	H	0	vdds	Yes	4 [(5)]	PU100/ PD100	LVCMOS
		gpio_44	4	IO								
		safe_mode	7	-								
Y1	T1	gpmc_d9	0	IO	H	H	0	vdds	Yes	4[(5)]	PU100/ PD100	LVCMOS
		gpio_45	4	IO								
		safe_mode	7	-								
T1	N1	gpmc_d10	0	IO	H	H	0	vdds	Yes	4[(5)]	PU100/ PD100	LVCMOS
		gpio_46	4	IO								
		safe_mode	7	-								
U2	P2	gpmc_d11	0	IO	H	H	0	vdds	Yes	4[(5)]	PU100/ PD100	LVCMOS
		gpio_47	4	IO								
		safe_mode	7	-								
U1	P1	gpmc_d12	0	IO	H	H	0	vdds	Yes	4[(5)]	PU100/ PD100	LVCMOS
		gpio_48	4	IO								
		safe_mode	7	-								
P1	M1	gpmc_d13	0	IO	H	H	0	vdds	Yes	4[(5)]	PU100/ PD100	LVCMOS
		gpio_49	4	IO								
		safe_mode	7	-								
L2	J2	gpmc_d14	0	IO	H	H	0	vdds	Yes	4 [(5)]	PU100/ PD100	LVCMOS
		gpio_50	4	IO								
		safe_mode	7	-								
M2	K2	gpmc_d15	0	IO	H	H	0	vdds	Yes	4[(5)]	PU100/ PD100	LVCMOS
		gpio_51	4	IO								
		safe_mode	7	-								
AD10	AA9	gpmc_nadv_ ale	0	O	0	0	0	vdds	No	4 [(5)]	NA	LVCMOS

(5) The drive strength is programmable vs the capacity load: load range = [2 pF to 6 pF] per default or [6 pF to 12 pF] according to the selected mode.

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Table 2-2. Ball Characteristics (CBC Pkg.)[1] (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENG TH (mA) [11]	PULLUP /DOWN TYPE [12]	IO CELL [13]
K2	NA	gpmc_nbe0_cle	0	O	L	0	0	vdds	Yes	4[5]	PU100/ PD100	LVCMOS
		gpio_60	4	IO								
		safe_mode	7	-								
J1	NA	gpmc_nbe1	0	O	L	L	7	vdds	Yes	4 [5]	PU100/ PD100	LVCMOS
		gpio_61	4	IO								
		safe_mode	7	-								
AD8	AA8	gpmc_ncs0	0	O	1	1	0	vdds	No	4[5]	NA	LVCMOS
AD1	W1	gpmc_ncs1	0	O	H	1	0	vdds	Yes	4 [5]	PU100/ PD100	LVCMOS
		gpio_52	4	IO								
		safe_mode	7	-								
A3	NA	gpmc_ncs2	0	O	H	H	7	vdds	Yes	4 [5]	PU100/ PD100	LVCMOS
		gpio_53	4	IO								
		safe_mode	7	-								
B6	NA	gpmc_ncs3	0	O	H	H	7	vdds	Yes	4[5]	PU100/ PD100	LVCMOS
		sys_ndmareq0	1	I								
		gpio_54	4	IO								
		safe_mode	7	-								
B4	NA	gpmc_ncs4	0	O	H	H	7	vdds	Yes	4 [6]	PU100/ PD100	LVCMOS
		sys_ndmareq1	1	I								
		mcbsp4_clkx	2	IO								
		gpt9_pwm_evt	3	IO								
		gpio_55	4	IO								
		safe_mode	7	-								
C4	NA	gpmc_ncs5	0	O	H	H	7	vdds	Yes	4[6]	PU100/ PD100	LVCMOS
		sys_ndmareq2	1	I								
		mcbsp4_dr	2	I								
		gpt10_pwm_evt	3	IO								
		gpio_56	4	IO								
		safe_mode	7	-								
B5	NA	gpmc_ncs6	0	O	H	H	7	vdds	Yes	4[6]	PU100/ PD100	LVCMOS
		sys_ndmareq3	1	I								
		mcbsp4_dx	2	IO								
		gpt11_pwm_evt	3	IO								
		gpio_57	4	IO								
		safe_mode	7	-								
C5	NA	gpmc_ncs7	0	O	H	H	7	vdds	Yes	4[6]	PU100/ PD100	LVCMOS
		gpmc_io_dir	1	O								
		mcbsp4_fsx	2	IO								
		gpt8_pwm_evt	3	IO								
		gpio_58	4	IO								
		safe_mode	7	-								
N2	L2	gpmc_noe	0	O	1	1	0	vdds	No	4[6]	NA	LVCMOS

(6) The drive strength is programmable vs the capacity load: load range = [2 pF to 6 pF] per default or [6 pF to 12 pF] according to the selected mode.

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Table 2-2. Ball Characteristics (CBC Pkg.)[(1)] (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENG TH (mA) [11]	PULLUP /DOWN TYPE [12]	IO CELL [13]
M1	K1	gpmc_nwe	0	O	1	1	0	vdds	No	4[(6)]	NA	LVCMOS
AC6	Y5	gpmc_nwp	0	O	L	0	0	vdds	Yes	4 [(6)]	PU100/ PD100	LVCMOS
		gpio_62	4	IO								
		safe_mode	7	-								
AC11	Y10	gpmc_wait0	0	I	H	H	0	vdds	Yes	4[(6)]	PU100/ PD100	LVCMOS
AC8	Y8	gpmc_wait1	0	I	H	H	7	vdds	Yes	4[(6)]	PU100/ PD100	LVCMOS
		gpio_63	4	IO								
		safe_mode	7	-								
B3	NA	gpmc_wait2	0	I	H	H	7	vdds	Yes	4[(6)]	PU100/ PD100	LVCMOS
		gpio_64	4	IO								
		safe_mode	7	-								
C6	NA	gpmc_wait3	0	I	H	H	7	vdds	Yes	4[(6)]	PU100/ PD100	LVCMOS
		sys_ndmareq 1	1	I								
		gpio_65	4	IO								
		safe_mode	7	-								
W19	NA	hsusb0_clk	0	I	L	L	7	vdds	Yes	4[(7)]	PU100/ PD100	LVCMOS
		gpio_120	4	IO								
		safe_mode	7	-								
V20	NA	hsusb0_data 0	0	IO	L	L	7	vdds	Yes	4 [(7)]	PU100/ PD100	LVCMOS
		uart3_tx_irtx	2	O								
		gpio_125	4	IO								
		safe_mode	7	-								
Y20	NA	hsusb0_data 1	0	IO	L	L	7	vdds	Yes	4 [(7)]	PU100/ PD100	LVCMOS
		uart3_rx_irrx	2	I								
		gpio_130	4	IO								
		safe_mode	7	-								
V18	NA	hsusb0_data 2	0	IO	L	L	7	vdds	Yes	4[(7)]	PU100/ PD100	LVCMOS
		uart3_rts_sd	2	O								
		gpio_131	4	IO								
		safe_mode	7	-								
W20	NA	hsusb0_data 3	0	IO	L	L	7	vdds	Yes	4[(7)]	PU100/ PD100	LVCMOS
		uart3_cts_rct x	2	IO								
		gpio_169	4	IO								
		safe_mode	7	-								
W17	NA	hsusb0_data 4	0	IO	L	L	7	vdds	Yes	4[(7)]	PU100/ PD100	LVCMOS
		gpio_188	4	IO								
		safe_mode	7	-								
Y18	NA	hsusb0_data 5	0	IO	L	L	7	vdds	Yes	4 [(7)]	PU100/ PD100	LVCMOS
		gpio_189	4	IO								
		safe_mode	7	-								
Y19	NA	hsusb0_data 6	0	IO	L	L	7	vdds	Yes	4[(7)]	PU100/ PD100	LVCMOS
		gpio_190	4	IO								
		safe_mode	7	-								
Y17	NA	hsusb0_data 7	0	IO	L	L	7	vdds	Yes	4[(7)]	PU100/ PD100	LVCMOS

(7) The capacity load range is [2 pf to 6 pF].

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Table 2-2. Ball Characteristics (CBC Pkg.)[1] (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENG TH (mA) [11]	PULLUP /DOWN TYPE [12]	IO CELL [13]
		gpio_191	4	IO								
		safe_mode	7	-								
V19	NA	hsusb0_dir	0	I	L	L	7	vdds	Yes	4 [7]	PU100/ PD100	LVCMOS
		gpio_122	4	IO								
		safe_mode	7	-								
W18	NA	hsusb0_nxt	0	I	L	L	7	vdds	Yes	4[7]	PU100/ PD100	LVCMOS
		gpio_124	4	IO								
		safe_mode	7	-								
U20	NA	hsusb0_stp	0	O	H	H	7	vdds	Yes	4[7]	PU100/ PD100	LVCMOS
		gpio_121	4	IO								
		safe_mode	7	-								
U15	NA	jtag_ntrst	0	I	L	L	0	vdds	Yes	NA	PU100/ PD100	LVCMOS
W13	NA	jtag_rtck	0	O	L	0	0	vdds	Yes	4	PU100/ PD100	LVCMOS
V14	NA	jtag_tck	0	I	L	L	0	vdds	Yes	NA	PU100/ PD100	LVCMOS
U16	NA	jtag_tdi	0	I	H	H	0	vdds	Yes	NA	PU100/ PD100	LVCMOS
Y13	NA	jtag_tdo	0	O	L	Z	0	vdds	Yes	4	PU100/ PD100	LVCMOS
V15	NA	jtag_tms_tmsc	0	IO	H	H	0	vdds	Yes	4	PU100/ PD100	LVCMOS
N19	NA	mmc1_clk	0	O	L	L	7	vdds_mmc1	Yes	8	PU100/ PD100	LVCMOS
		gpio_120	4	IO								
		safe_mode	7	-								
L18	NA	mmc1_cmd	0	IO	L	L	7	vdds_mmc1	Yes	8	PU100/ PD100	LVCMOS
		gpio_121	4	IO								
		safe_mode	7	-								
M19	NA	mmc1_dat0	0	IO	L	L	7	vdds_mmc1	Yes	8	PU100/ PD100	LVCMOS
		gpio_122	4	IO								
		safe_mode	7	-								
M18	NA	mmc1_dat1	0	IO	L	L	7	vdds_mmc1	Yes	8	PU100/ PD100	LVCMOS
		gpio_123	4	IO								
		safe_mode	7	-								
K18	NA	mmc1_dat2	0	IO	L	L	7	vdds_mmc1	Yes	8	PU100/ PD100	LVCMOS
		gpio_124	4	IO								
		safe_mode	7	-								
N20	NA	mmc1_dat3	0	IO	L	L	7	vdds_mmc1	Yes	8	PU100/ PD100	LVCMOS
		gpio_125	4	IO								
		safe_mode	7	-								
M20	NA	mmc1_dat4	0	IO	L	L	7	vdds_mmc1a	No	8	PU/PD[8]	LVCMOS
		gpio_126	4	IO								
		safe_mode	7	-								
P17	NA	mmc1_dat5	0	IO	L	L	7	vdds_mmc1a	No	8	PU/PD[8]	LVCMOS
		gpio_127	4	IO								
		safe_mode	7	-								
P18	NA	mmc1_dat6	0	IO	L	L	7	vdds_mmc1a	No	8	PU/PD[8]	LVCMOS
		gpio_128	4	IO								
		safe_mode	7	-								

(8) The PU nominal drive strength of this IO cell is equal to 25 mA @ 1.8 V and 41.6 mA @ 3.0 V. The PD nominal drive strength of this IO cell is equal to 1 mA @ 1.8 V and 1.66 mA @ 3.0 V.

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Table 2-2. Ball Characteristics (CBC Pkg.)[1] (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENG TH (mA) [11]	PULLUP /DOWN TYPE [12]	IO CELL [13]
P19	NA	mmc1_dat7	0	IO	L	L	7	vdds_mmc1a	No	8	PU/PD[8]	LVCMOS
		gpio_129	4	IO								
		safe_mode	7	-								
J25	NA	i2c1_scl	0	IOD	H	H	0	vdds	Yes	3	PU100/ PD100	Open Drain
J24	NA	i2c1_sda	0	IOD	H	H	0	vdds	Yes	3	PU100/ PD100	Open Drain
C2	NA	i2c2_scl	0	IOD	H	H	7	vdds	Yes	3	PU100/ PD100	Open Drain
		gpio_168	4	IO						4		
		safe_mode	7	-						4		
C1	NA	i2c2_sda	0	IOD	H	H	7	vdds	Yes	3	PU100/ PD100	Open Drain
		gpio_183	4	IO						4		
		safe_mode	7	-						4		
AB4	NA	i2c3_scl	0	IOD	H	H	7	vdds	Yes	3	PU100/ PD100	Open Drain
		gpio_184	4	IO						4		
		safe_mode	7	-						4		
AC4	NA	i2c3_sda	0	IOD	H	H	7	vdds	Yes	3	PU100/ PD100	Open Drain
		gpio_185	4	IO						4		
		safe_mode	7	-						4		
U19	NA	mcbsp1_clkr	0	IO	L	L	7	vdds	Yes	4 [9]	PU100/ PD100	LVCMOS
		mcspi4_clk	1	IO								
		gpio_156	4	IO								
		safe_mode	7	-								
T17	NA	mcbsp1_clkx	0	IO	L	L	7	vdds	Yes	4 [9]	PU100/ PD100	LVCMOS
		mcbsp3_clkx	2	IO								
		gpio_162	4	IO								
		safe_mode	7	-								
T20	NA	mcbsp1_dr	0	I	L	L	7	vdds	Yes	4[9]	PU100/ PD100	LVCMOS
		mcspi4_somi	1	IO								
		mcbsp3_dr	2	I								
		gpio_159	4	IO								
		safe_mode	7	-								
U17	NA	mcbsp1_dx	0	IO	L	L	7	vdds	Yes	4[9]	PU100/ PD100	LVCMOS
		mcspi4_simo	1	IO								
		mcbsp3_dx	2	IO								
		gpio_158	4	IO								
		safe_mode	7	-								
V17	NA	mcbsp1_fsr	0	IO	L	L	7	vdds	Yes	4 [9]	PU100/ PD100	LVCMOS
		cam_global_reset	2	IO								
		gpio_157	4	IO								
		safe_mode	7	-								
P20	NA	mcbsp1_fsx	0	IO	L	L	7	vdds	Yes	4[9]	PU100/ PD100	LVCMOS
		mcspi4_cs0	1	IO								
		mcbsp3_fsx	2	IO								
		gpio_161	4	IO								
		safe_mode	7	-								

(9) The capacity load range is [2 pf to 6 pF].

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Table 2-2. Ball Characteristics (CBC Pkg.)[(1)] (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENG TH (mA) [11]	PULLUP /DOWN TYPE [12]	IO CELL [13]
R18	NA	mcbsp2_clkx	0	IO	L	L	7	vdds	Yes	4[(10)]	PU100/ PD100	LVCMOS
		gpio_117	4	IO								
		safe_mode	7	-								
T18	NA	mcbsp2_dr	0	I	L	L	7	vdds	Yes	4[(10)]	PU100/ PD100	LVCMOS
		gpio_118	4	IO								
		safe_mode	7	-								
R19	NA	mcbsp2_dx	0	IO	L	L	7	vdds	Yes	4[(10)]	PU100/ PD100	LVCMOS
		gpio_119	4	IO								
		safe_mode	7	-								
U18	NA	mcbsp2_fsx	0	IO	L	L	7	vdds	Yes	4[(10)]	PU100/ PD100	LVCMOS
		gpio_116	4	IO								
		safe_mode	7	-								
P9	NA	mcspi1_clk	0	IO	L	L	7	vdds	Yes	4[(10)]	PU100/ PD100	LVCMOS
		mmc2_dat4	1	IO								
		gpio_171	4	IO								
		safe_mode	7	-								
R7	NA	mcspi1_cs0	0	IO	H	H	7	vdds	Yes	4[(11)]	PU100/ PD100	LVCMOS
		mmc2_dat7	1	IO								
		gpio_174	4	IO								
		safe_mode	7	-								
R9	NA	mcspi1_cs2	0	O	H	H	7	vdds	Yes	4[(11)]	PU100/ PD100	LVCMOS
		mmc3_clk	3	O								
		gpio_176	4	IO								
		safe_mode	7	-								
P8	NA	mcspi1_simo	0	IO	L	L	7	vdds	Yes	4 [(11)]	PU100/ PD100	LVCMOS
		mmc2_dat5	1	IO								
		gpio_172	4	IO								
		safe_mode	7	-								
P7	NA	mcspi1_somi	0	IO	L	L	7	vdds	Yes	4[(11)]	PU100/ PD100	LVCMOS
		mmc2_dat6	1	IO								
		gpio_173	4	IO								
		safe_mode	7	-								
W7	NA	mcspi2_clk	0	IO	L	L	7	vdds	Yes	4[(12)]	PU100/ PD100	LVCMOS
		hsusb2_tll_data7	2	IO								
		hsusb2_data7	3	O								
		gpio_178	4	IO								
		safe_mode	7	-								
V8	NA	mcspi2_cs0	0	IO	H	H	7	vdds	Yes	4[(12)]	PU100/ PD100	LVCMOS
		gpt11_pwm_evt	1	IO								
		hsusb2_tll_data6	2	IO								

(10) The buffer strength of this IO cell is programmable (2, 4, 6, or 8 mA) according to the selected mode; the default value is described in the above table.
(11) The buffer strength of this IO cell is programmable (2, 4, 6, or 8 mA) according to the selected mode; the default value is described in the above table.
(12) The capacity load range is [2 pf to 6 pF].

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Table 2-2. Ball Characteristics (CBC Pkg.)[1] (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENG TH (mA) [11]	PULLUP /DOWN TYPE [12]	IO CELL [13]
		hsusb2_data6	3	O								
		gpio_181	4	IO								
		safe_mode	7	-								
W8	NA	mcspi2_simo	0	IO	L	L	7	vdds	Yes	4[12]	PU100/ PD100	LVCMOS
		gpt9_pwm_evt	1	IO								
		hsusb2_tll_data4	2	IO								
		hsusb2_data4	3	I								
		gpio_179	4	IO								
		safe_mode	7	-								
U8	NA	mcspi2_somi	0	IO	L	L	7	vdds	Yes	4[12]	PU100/ PD100	LVCMOS
		gpt10_pwm_evt	1	IO								
		hsusb2_tll_data5	2	IO								
		hsusb2_data5	3	O								
		gpio_180	4	IO								
		safe_mode	7	-								
W10	NA	mmc2_clk	0	O	L	L	7	vdds	Yes	4[13]	PU100/ PD100	LVCMOS
		mcspi3_clk	1	IO								
		gpio_130	4	IO								
		safe_mode	7	-								
R10	NA	mmc2_cmd	0	IO	H	H	7	vdds	Yes	4[13]	PU100/ PD100	LVCMOS
		mcspi3_simo	1	IO								
		gpio_131	4	IO								
		safe_mode	7	-								
T10	NA	mmc2_dat0	0	IO	H	H	7	vdds	Yes	4[13]	PU100/ PD100	LVCMOS
		mcspi3_somi	1	IO								
		gpio_132	4	IO								
		safe_mode	7	-								
T9	NA	mmc2_dat1	0	IO	H	H	7	vdds	Yes	4[13]	PU100/ PD100	LVCMOS
		gpio_133	4	IO								
		safe_mode	7	-								
U10	NA	mmc2_dat2	0	IO	H	H	7	vdds	Yes	4[13]	PU100/ PD100	LVCMOS
		mcspi3_cs1	1	O								
		gpio_134	4	IO								
		safe_mode	7	-								
U9	NA	mmc2_dat3	0	IO	H	H	7	vdds	Yes	4[13]	PU100/ PD100	LVCMOS
		mcspi3_cs0	1	IO								
		gpio_135	4	IO								
		safe_mode	7	-								
V10	NA	mmc2_dat4	0	IO	L	L	7	vdds	Yes	4[13]	PU100/ PD100	LVCMOS
		mmc2_dir_dat0	1	O								
		mmc3_dat0	3	IO								
		gpio_136	4	IO								
		safe_mode	7	-								

(13) The capacity load range is [2 pf to 6 pF].

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Table 2-2. Ball Characteristics (CBC Pkg.)[1] (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENG TH (mA) [11]	PULLUP /DOWN TYPE [12]	IO CELL [13]
R2	NA	uart1_rts	0	O	L	L	7	vdds	Yes	4[13]	PU100/ PD100	LVCMOS
		gpio_149	4	IO								
		safe_mode	7	-								
H3	NA	uart1_rx	0	I	L	L	7	vdds	Yes	4 [13]	PU100/ PD100	LVCMOS
		mcbsp1_clkr	2	IO								
		mcspi4_clk	3	IO								
		gpio_151	4	IO								
		safe_mode	7	-								
L4	NA	uart1_tx	0	O	L	L	7	vdds	Yes	4[13]	PU100/ PD100	LVCMOS
		gpio_148	4	IO								
		safe_mode	7	-								
Y24	NA	uart2_cts	0	I	H	H	7	vdds	Yes	4	PU100/ PD100	LVCMOS
		mcbsp3_dx	1	IO								
		gpt9_pwm_evt	2	IO								
		gpio_144	4	IO								
		safe_mode	7	-								
AA24	NA	uart2_rts	0	O	H	H	7	vdds	Yes	4	PU100/ PD100	LVCMOS
		mcbsp3_dr	1	I								
		gpt10_pwm_evt	2	IO								
		gpio_145	4	IO								
		safe_mode	7	-								
AD21	NA	uart2_rx	0	I	H	H	7	vdds	Yes	4	PU100/ PD100	LVCMOS
		mcbsp3_fsx	1	IO								
		gpt8_pwm_evt	2	IO								
		gpio_147	4	IO								
		safe_mode	7	-								
AD22	NA	uart2_tx	0	O	H	H	7	vdds	Yes	4	PU100/ PD100	LVCMOS
		mcbsp3_clkx	1	IO								
		gpt11_pwm_evt	2	IO								
		gpio_146	4	IO								
		safe_mode	7	-								
F23	NA	uart3_cts_rctx	0	IO	H	H	7	vdds	Yes	4	PU100/ PD100	LVCMOS
		gpio_163	4	IO								
		safe_mode	7	-								
F24	NA	uart3_rts_sd	0	O	H	H	7	vdds	Yes	4	PU100/ PD100	LVCMOS
		gpio_164	4	IO								
		safe_mode	7	-								
H24	NA	uart3_rx_irrx	0	I	H	H	7	vdds	Yes	4	PU100/ PD100	LVCMOS
		gpio_165	4	IO								
		safe_mode	7	-								
G24	NA	uart3_tx_irtx	0	O	H	H	7	vdds	Yes	4	PU100/ PD100	LVCMOS
		gpio_166	4	IO								
		safe_mode	7	-								
J23	NA	hdq_sio	0	IOD	H	H	7	vdds	Yes	4	PU100/ PD100	LVCMOS
		sys_altclk	1	I								

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Table 2-2. Ball Characteristics (CBC Pkg.)[(1)] (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENG TH (mA) [11]	PULLUP /DOWN TYPE [12]	IO CELL [13]
		i2c2_sccbe	2	O								
		i2c3_sccbe	3	O								
		gpio_170	4	IO								
		safe_mode	7	-								
AD15	NA	i2c4_scl	0	IOD	H	H	0	vdds	Yes	3	PU100/ PD100	Open Drain
		sys_nvmode1	1	O						4		
		safe_mode	7	-						4		
W16	NA	i2c4_sda	0	IOD	H	H	0	vdds	Yes	3	PU100/ PD100	Open Drain
		sys_nvmode2	1	O						4		
		safe_mode	7	-						4		
F3	NA	sys_boot0	0	I	Z	Z	0	vdds	Yes	4	PU100/ PD100	LVCMOS
		gpio_2	4	IO								
		safe_mode	7	-								
D3	NA	sys_boot1	0	I	Z	Z	0	vdds	Yes	4	PU100/ PD100	LVCMOS
		gpio_3	4	IO								
		safe_mode	7	-								
C3	NA	sys_boot2	0	I	Z	Z	0	vdds	Yes	4	PU100/ PD100	LVCMOS
		gpio_4	4	IO								
		safe_mode	7	-								
E3	NA	sys_boot3	0	I	Z	Z	0	vdds	Yes	4	PU100/ PD100	LVCMOS
		gpio_5	4	IO								
		safe_mode	7	-								
E4	NA	sys_boot4	0	I	Z	Z	0	vdds	Yes	4	PU100/ PD100	LVCMOS
		mmc2_dir_dat2	1	O								
		gpio_6	4	IO								
		safe_mode	7	-								
G3	NA	sys_boot5	0	I	Z	Z	0	vdds	Yes	4	PU100/ PD100	LVCMOS
		mmc2_dir_dat3	1	O								
		gpio_7	4	IO								
		safe_mode	7	-								
D4	NA	sys_boot6	0	I	Z	Z	0	vdds	Yes	4	PU100/ PD100	LVCMOS
		gpio_8	4	IO								
		safe_mode	7	-								
AE14	NA	sys_clkout1	0	O	L	L	7	vdds	Yes	4	PU100/ PD100	LVCMOS
		gpio_10	4	IO								
		safe_mode	7	-								
W11	NA	sys_clkout2	0	O	L	L	7	vdds	Yes	4[(14)]	PU100/ PD100	LVCMOS
		gpio_186	4	IO								
		safe_mode	7	-								
W15	NA	sys_clkreq	0	IO	0	1	0	vdds	Yes	4	PU100/ PD100	LVCMOS
		gpio_1	4	IO								
		safe_mode	7	-								
V16	NA	sys_nirq	0	I	H	H	7	vdds	Yes	4	PU100/ PD100	LVCMOS

(14) The capacity load range is [2 pf to 6 pF].

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Table 2-2. Ball Characteristics (CBC Pkg.)[(1)] (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENG TH (mA) [11]	PULLUP /DOWN TYPE [12]	IO CELL [13]
		gpio_0	4	IO								
		safe_mode	7	-								
V13	NA	sys_nrespwron	0	I	Z	I	NA	vdds	Yes	NA	NA	LVCMOS
AD7	AA5	sys_nreswarm	0	IOD	0	1 (PU)	0	vdds	Yes	4	PU100/ PD100	LVCMOS
		gpio_30	4	IO								Open Drain
		safe_mode	7	-								
V12	NA	sys_off_mode	0	O	0	L	7	vdds	Yes	4	PU100/ PD100	LVCMOS
		gpio_9	4	IO								
		safe_mode	7	-								
AF19	NA	sys_xtalin	0	I	Z	I	NA	vdds	Yes	NA	NA	LVCMOS
AF20	NA	sys_xtalout	0	O	Z	O	NA	vdds	Yes	NA	NA	LVCMOS
W26	NA	tv_out1	0	AO	Z	0	0	vdda_dac	No	8	NA	10-bit DAC
V26	NA	tv_out2	0	AO	Z	0	0	vdda_dac	No	8	NA	10-bit DAC
W25	NA	tv_vfb1	0	O	Z	NA	0	vdda_dac	No	2	NA	10-bit DAC
U24	NA	tv_vfb2	0	O	Z	NA	0	vdda_dac	No	2	NA	10-bit DAC
V23	NA	tv_vref	0	I	Z	NA	0	vdda_dac	No	NA	NA	10-bit DAC
AE20	NA	sys_32k	0	I	Z	I	NA	vdds	Yes	NA	NA	LVCMOS
A24	NA	cam_d2	0	I	L	L	7	vdds	Yes	4(15)	PU100/ PD100	LVCMOS
		gpio_101	4	IO								
		hw_dbg4	5	O								
		safe_mode	7	-								
B24	NA	cam_d3	0	I	L	L	7	vdds	Yes	4(15)	PU100/ PD100	LVCMOS
		gpio_102	4	IO								
		hw_dbg5	5	O								
		safe_mode	7	-								
D24	NA	cam_d4	0	I	L	L	7	vdds	Yes	4(15)	PU100/ PD100	LVCMOS
		gpio_103	4	IO								
		hw_dbg6	5	O								
		safe_mode	7	-								
C24	NA	cam_d5	0	I	L	L	7	vdds	Yes	4 (15)	PU100/ PD100	LVCMOS
		gpio_104	4	IO								
		hw_dbg7	5	O								
		safe_mode	7	-								
D25	NA	cam_d10	0	I	L	L	7	vdds	Yes	4(15)	PU100/ PD100	LVCMOS
		gpio_109	4	IO								
		hw_dbg8	5	O								
		safe_mode	7	-								
E26	NA	cam_d11	0	I	L	L	7	vdds	Yes	4(15)	PU100/ PD100	LVCMOS
		gpio_110	4	IO								
		hw_dbg9	5	O								
		safe_mode	7	-								
B23	NA	cam_fld	0	IO	L	L	7	vdds	Yes	4(15)	PU100/ PD100	LVCMOS
		cam_global_reset	2	IO								
		gpio_98	4	IO								
		hw_dbg3	5	O								
		safe_mode	7	-								

(15) The capacity load range is [2 pf to 6 pF].

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Table 2-2. Ball Characteristics (CBC Pkg.)[1] (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENG TH (mA) [11]	PULLUP /DOWN TYPE [12]	IO CELL [13]
C23	NA	cam_hs	0	IO	L	L	7	vdds	Yes	4[15]	PU100/ PD100	LVCMOS
		gpio_94	4	IO								
		hw_dbg0	5	O								
		safe_mode	7	-								
C26	NA	cam_pclk	0	I	L	L	7	vdds	Yes	4[15]	PU100/ PD100	LVCMOS
		gpio_97	4	IO								
		hw_dbg2	5	O								
		safe_mode	7	-								
D26	NA	cam_strobe	0	O	L	L	7	vdds	Yes	4[15]	PU100/ PD100	LVCMOS
		gpio_126	4	IO								
		hw_dbg11	5	O								
		safe_mode	7	-								
C25	NA	cam_xclka	0	O	L	L	7	vdds	Yes	4[15]	PU100/ PD100	LVCMOS
		gpio_96	4	IO								
		safe_mode	7	-								
E25	NA	cam_xclkb	0	O	L	L	7	vdds	Yes	4[16]	PU100/ PD100	LVCMOS
		gpio_111	4	IO								
		safe_mode	7	-								
P25	NA	cam_d6	0	I	L	L	7	vdds	NA	4	PU100/ PD100	SubLVDS
		gpio_105	4	IO								
		safe_mode	7	-								
P26	NA	cam_d7	0	I	L	L	7	vdds	NA	4	PU100/ PD100	SubLVDS
		gpio_106	4	IO								
		safe_mode	7	-								
N25	NA	cam_d8	0	I	L	L	7	vdds	NA	4	PU100/ PD100	SubLVDS
		gpio_107	4	IO								
		safe_mode	7	-								
N26	NA	cam_d9	0	I	L	L	7	vdds	NA	4	PU100/ PD100	SubLVDS
		gpio_108	4	IO								
		safe_mode	7	-								
D23	NA	cam_vs	0	IO	L	L	7	vdds	Yes	4[16]	PU100/ PD100	LVCMOS
		gpio_95	4	IO								
		hw_dbg1	5	O								
		safe_mode	7	-								
A23	NA	cam_wen	0	I	L	L	7	vdds	Yes	4 [16]	PU100/ PD100	LVCMOS
		cam_shutter	2	O								
		gpio_167	4	IO								
		hw_dbg10	5	O								
		safe_mode	7	-								
F26	NA	dss_acbias	0	O	L	L	7	vdds	Yes	8	PU100/ PD100	LVCMOS
		gpio_69	4	IO								
		safe_mode	7	-								
G26	NA	dss_data6	0	IO	L	L	7	vdds	Yes	8	PU100/ PD100	LVCMOS
		uart1_tx	2	O								
		gpio_76	4	IO								
		hw_dbg14	5	O								

(16) The capacity load range is [2 pf to 6 pF].

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Table 2-2. Ball Characteristics (CBC Pkg.)[1] (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENG TH (mA) [11]	PULLUP /DOWN TYPE [12]	IO CELL [13]
		safe_mode	7	-								
H25	NA	dss_data7	0	IO	L	L	7	vdds	Yes	8	PU100/ PD100	LVCMOS
		uart1_rx	2	I								
		gpio_77	4	IO								
		hw_dbg15	5	O								
		safe_mode	7	-								
H26	NA	dss_data8	0	IO	L	L	7	vdds	Yes	8	PU100/ PD100	LVCMOS
		gpio_78	4	IO								
		hw_dbg16	5	O								
		safe_mode	7	-								
J26	NA	dss_data9	0	IO	L	L	7	vdds	Yes	8	PU100/ PD100	LVCMOS
		gpio_79	4	IO								
		hw_dbg17	5	O								
		safe_mode	7	-								
L25	NA	dss_data16	0	IO	L	L	7	vdds	Yes	8	PU100/ PD100	LVCMOS
		gpio_86	4	IO								
		safe_mode	7	-								
L26	NA	dss_data17	0	IO	L	L	7	vdds	Yes	8	PU100/ PD100	LVCMOS
		gpio_87	4	IO								
		safe_mode	7	-								
M24	NA	dss_data18	0	IO	L	L	7	vdds	Yes	8	PU100/ PD100	LVCMOS
		mcspi3_clk	2	IO								
		dss_data0	3	IO								
		gpio_88	4	IO								
		safe_mode	7	-								
M26	NA	dss_data19	0	IO	L	L	7	vdds	Yes	8	PU100/ PD100	LVCMOS
		mcspi3_simo	2	IO								
		dss_data1	3	IO								
		gpio_89	4	IO								
		safe_mode	7	-								
N24	NA	dss_data21	0	O	L	L	7	vdds	Yes	8	PU100/ PD100	LVCMOS
		mcspi3_cs0	2	IO								
		dss_data3	3	IO								
		gpio_91	4	IO								
		safe_mode	7	-								
K24	NA	dss_hsync	0	O	H	H	7	vdds	Yes	4	PU100/ PD100	LVCMOS
		gpio_67	4	IO								
		hw_dbg13	5	O								
		safe_mode	7	-								
M25	NA	dss_vsync	0	O	H	H	7	vdds	Yes	4	PU100/ PD100	LVCMOS
		gpio_68	4	IO								
		safe_mode	7	-								
R8	NA	mcspi1_cs1	0	O	H	H	7	vdds	Yes	4(17)	PU100/ PD100	LVCMOS
		mmc3_cmd	3	IO								
		gpio_175	4	IO								
		safe_mode	7	-								

(17) The buffer strength of this IO cell is programmable (2, 4, 6, or 8 mA) according to the selected mode; the default value is described in the above table.

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Table 2-2. Ball Characteristics (CBC Pkg.)[1] (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENG TH (mA) [11]	PULLUP /DOWN TYPE [12]	IO CELL [13]
T8	NA	mcspi1_cs3	0	O	H	H	7	vdds	Yes	4[18]	PU100/ PD100	LVCMOS
		hsusb2_tll_data2	2	IO								
		hsusb2_data2	3	IO								
		gpio_177	4	IO								
		mm2_txdat	5	IO								
		safe_mode	7	-								
V9	NA	mcspi2_cs1	0	O	L	L	7	vdds	Yes	4[18]	PU100/ PD100	LVCMOS
		gpt8_pwm_evt	1	IO								
		hsusb2_tll_data3	2	IO								
		hsusb2_data3	3	IO								
		gpio_182	4	IO								
		mm2_txen_n	5	IO								
		safe_mode	7	-								
T19	NA	mcbsp_clks	0	I	L	L	7	vdds	Yes	4 [19]	PU100/ PD100	LVCMOS
		cam_shutter	2	O								
		gpio_160	4	IO								
		uart1_cts	5	I								
		safe_mode	7	-								
AB2	NA	etk_clk	0	O	H	H	4	vdds	Yes	4[19]	PU100/ PD100	LVCMOS
		mcbsp5_clkx	1	IO								
		mmc3_clk	2	O								
		hsusb1_stp	3	O								
		gpio_12	4	IO								
		mm1_rxdp	5	IO								
		hsusb1_tll_stp	6	I								
		hw_dbg0	7	O								
AB3	NA	etk_ctl	0	O	H	H	4	vdds	Yes	4[19]	PU100/ PD100	LVCMOS
		mmc3_cmd	2	IO								
		hsusb1_clk	3	O								
		gpio_13	4	IO								
		hsusb1_tll_clk	6	O								
		hw_dbg1	7	O								
AC3	NA	etk_d0	0	O	H	H	4	vdds	Yes	4 [19]	PU100/ PD100	LVCMOS
		mcspi3_simo	1	IO								
		mmc3_dat4	2	IO								
		hsusb1_data0	3	IO								
		gpio_14	4	IO								
		mm1_rxrcv	5	IO								
		hsusb1_tll_data0	6	IO								
		hw_dbg2	7	O								
AD4	NA	etk_d1	0	O	H	H	4	vdds	Yes	4[19]	PU100/ PD100	LVCMOS
		mcspi3_somi	1	IO								

(18) The capacity load range is [2 pf to 6 pF].
(19) The capacity load range is [2 pf to 6 pF].

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Table 2-2. Ball Characteristics (CBC Pkg.)[1] (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENG TH (mA) [11]	PULLUP /DOWN TYPE [12]	IO CELL [13]
		hsusb1_data 1	3	IO								
		gpio_15	4	IO								
		mm1_txse0	5	IO								
		hsusb1_tll_d ata1	6	IO								
		hw_dbg3	7	O								
AD3	NA	etk_d2	0	O	H	H	4	vdds	Yes	4[19]	PU100/ PD100	LVCMOS
		mcspi3_cs0	1	IO								
		hsusb1_data 2	3	IO								
		gpio_16	4	IO								
		mm1_txdat	5	IO								
		hsusb1_tll_d ata2	6	IO								
		hw_dbg4	7	O								
AA3	NA	etk_d3	0	O	H	H	4	vdds	Yes	4[19]	PU100/ PD100	LVCMOS
		mcspi3_clk	1	IO								
		mmc3_dat3	2	IO								
		hsusb1_data 7	3	IO								
		gpio_17	4	IO								
		hsusb1_tll_d ata7	6	IO								
		hw_dbg5	7	O								
Y3	NA	etk_d4	0	O	L	L	4	vdds	Yes	4[20]	PU100/ PD100	LVCMOS
		mcbsp5_dr	1	I								
		mmc3_dat0	2	IO								
		hsusb1_data 4	3	IO								
		gpio_18	4	IO								
		hsusb1_tll_d ata4	6	IO								
		hw_dbg6	7	O								
AB1	NA	etk_d5	0	O	L	L	4	vdds	Yes	4[20]	PU100/ PD100	LVCMOS
		mcbsp5_fsx	1	IO								
		mmc3_dat1	2	IO								
		hsusb1_data 5	3	IO								
		gpio_19	4	IO								
		hsusb1_tll_d ata5	6	IO								
		hw_dbg7	7	O								
AE3	NA	etk_d6	0	O	L	L	4	vdds	Yes	4 [20]	PU100/ PD100	LVCMOS
		mcbsp5_dx	1	IO								
		mmc3_dat2	2	IO								
		hsusb1_data 6	3	IO								
		gpio_20	4	IO								
		hsusb1_tll_d ata6	6	IO								
		hw_dbg8	7	O								
AD2	NA	etk_d7	0	O	L	L	4	vdds	Yes	4[20]	PU100/ PD100	LVCMOS
		mcspi3_cs1	1	O								

(20) The capacity load range is [2 pf to 6 pF].

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Table 2-2. Ball Characteristics (CBC Pkg.)[1] (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENG TH (mA) [11]	PULLUP /DOWN TYPE [12]	IO CELL [13]
		mmc3_dat7	2	IO								
		hsusb1_data3	3	IO								
		gpio_21	4	IO								
		mm1_txen_n	5	IO								
		hsusb1_tll_data3	6	IO								
		hw_dbg9	7	O								
AA4	NA	etk_d8	0	O	L	L	4	vdds	Yes	4[20]	PU100/ PD100	LVCMOS
		sys_drm_msecure	1	O								
		mmc3_dat6	2	IO								
		hsusb1_dir	3	I								
		gpio_22	4	IO								
		hsusb1_tll_dir	6	O								
		hw_dbg10	7	O								
V2	NA	etk_d9	0	O	L	L	4	vdds	Yes	4 [21]	PU100/ PD100	LVCMOS
		sys_secure_indicator	1	O								
		mmc3_dat5	2	IO								
		hsusb1_nxt	3	I								
		gpio_23	4	IO								
		mm1_rxdm	5	IO								
		hsusb1_tll_nxt	6	O								
		hw_dbg11	7	O								
AE4	NA	etk_d10	0	O	L	L	4	vdds	Yes	4[21]	PU100/ PD100	LVCMOS
		uart1_rx	2	I								
		hsusb2_clk	3	O								
		gpio_24	4	IO								
		hsusb2_tll_clk	6	O								
		hw_dbg12	7	O								
AF6	NA	etk_d11	0	O	L	L	4	vdds	Yes	4[21]	PU100/ PD100	LVCMOS
		hsusb2_stp	3	O								
		gpio_25	4	IO								
		mm2_rxdp	5	IO								
		hsusb2_tll_stp	6	I								
		hw_dbg13	7	O								
AE6	NA	etk_d12	0	O	L	L	4	vdds	Yes	4[21]	PU100/ PD100	LVCMOS
		hsusb2_dir	3	I								
		gpio_26	4	IO								
		hsusb2_tll_dir	6	O								
		hw_dbg14	7	O								
AF7	NA	etk_d13	0	O	L	L	4	vdds	Yes	4[21]	PU100/ PD100	LVCMOS
		hsusb2_nxt	3	I								
		gpio_27	4	IO								
		mm2_rxdm	5	IO								
		hsusb2_tll_nxt	6	O								
		hw_dbg15	7	O								

(21) The capacity load range is [2 pf to 6 pF].

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Table 2-2. Ball Characteristics (CBC Pkg.)[1] (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENG TH (mA) [11]	PULLUP /DOWN TYPE [12]	IO CELL [13]
AF9	NA	etk_d14	0	O	L	L	4	vdds	Yes	4[21]	PU100/ PD100	LVCMOS
		hsusb2_data 0	3	IO								
		gpio_28	4	IO								
		mm2_rxrcv	5	IO								
		hsusb2_tll_d ata0	6	IO								
		hw_dbg16	7	O								
AE9	NA	etk_d15	0	O	L	L	4	vdds	Yes	4[21]	PU100/ PD100	LVCMOS
		hsusb2_data 1	3	IO								
		gpio_29	4	IO								
		mm2_txse0	5	IO								
		hsusb2_tll_d ata1	6	IO								
		hw_dbg17	7	O								
Y15	NA	jtag_emu0	0	IO	H	H	0	vdds	Yes	4	PU100/ PD100	LVCMOS
		gpio_11	4	IO								
		safe_mode	7	-								
Y14	NA	jtag_emu1	0	IO	H	H	0	vdds	Yes	4	PU100/ PD100	LVCMOS
		gpio_31	4	IO								
		safe_mode	7	-								
U3	NA	mcbsp3_clkx	0	IO	L	L	7	vdds	Yes	4[22]	PU100/ PD100	LVCMOS
		uart2_tx	1	O								
		gpio_142	4	IO								
		hsusb3_tll_d ata6	5	IO								
		safe_mode	7	-								
N3	NA	mcbsp3_dr	0	I	L	L	7	vdds	Yes	4[22]	PU100/ PD100	LVCMOS
		uart2_rts	1	O								
		gpio_141	4	IO								
		hsusb3_tll_d ata5	5	IO								
		safe_mode	7	-								
P3	NA	mcbsp3_dx	0	IO	L	L	7	vdds	Yes	4[22]	PU100/ PD100	LVCMOS
		uart2_cts	1	I								
		gpio_140	4	IO								
		hsusb3_tll_d ata4	5	IO								
		safe_mode	7	-								
W3	NA	mcbsp3_fsx	0	IO	L	L	7	vdds	Yes	4[22]	PU100/ PD100	LVCMOS
		uart2_rx	1	I								
		gpio_143	4	IO								
		hsusb3_tll_d ata7	5	IO								
		safe_mode	7	-								
V3	NA	mcbsp4_clkx	0	IO	L	L	7	vdds	Yes	4 [22]	PU100/ PD100	LVCMOS
		gpio_152	4	IO								
		hsusb3_tll_d ata1	5	IO								
		mm3_txse0	6	IO								

(22) The capacity load range is [2 pf to 6 pF].

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Table 2-2. Ball Characteristics (CBC Pkg.)(1) (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENG TH (mA) [11]	PULLUP /DOWN TYPE [12]	IO CELL [13]
		safe_mode	7	-								
U4	NA	mcbsp4_dr	0	I	L	L	7	vdds	Yes	4 (22)	PU100/ PD100	LVCMOS
		gpio_153	4	IO								
		hsusb3_tll_data0	5	IO								
		mm3_rxrcv	6	IO								
		safe_mode	7	-								
R3	NA	mcbsp4_dx	0	IO	L	L	7	vdds	Yes	4(22)	PU100/ PD100	LVCMOS
		gpio_154	4	IO								
		hsusb3_tll_data2	5	IO								
		mm3_txdat	6	IO								
		safe_mode	7	-								
T3	NA	mcbsp4_fsx	0	IO	L	L	7	vdds	Yes	4 (22)	PU100/ PD100	LVCMOS
		gpio_155	4	IO								
		hsusb3_tll_data3	5	IO								
		mm3_txen_n	6	IO								
		safe_mode	7	-								
M3	NA	mmc2_dat5	0	IO	L	L	7	vdds	Yes	4(23)	PU100/ PD100	LVCMOS
		mmc2_dir_dat1	1	O								
		cam_global_reset	2	IO								
		mmc3_dat1	3	IO								
		gpio_137	4	IO								
		hsusb3_tll_stp	5	I								
		mm3_rxdp	6	IO								
		safe_mode	7	-								
L3	NA	mmc2_dat6	0	IO	L	L	7	vdds	Yes	4 (23)	PU100/ PD100	LVCMOS
		mmc2_dir_cmd	1	O								
		cam_shutter	2	O								
		mmc3_dat2	3	IO								
		gpio_138	4	IO								
		hsusb3_tll_dir	5	O								
		safe_mode	7	-								
K3	NA	mmc2_dat7	0	IO	L	L	7	vdds	Yes	4 (23)	PU100/ PD100	LVCMOS
		mmc2_clkin	1	I								
		mmc3_dat3	3	IO								
		gpio_139	4	IO								
		hsusb3_tll_nxt	5	IO								
		mm3_rxdm	6	IO								
		safe_mode	7	-								
W2	NA	uart1_cts	0	I	L	L	7	vdds	Yes	4(23)	PU100/ PD100	LVCMOS
		gpio_150	4	IO								
		hsusb3_tll_clk	5	O								
		safe_mode	7	-								

(23) The capacity load range is [2 pf to 6 pF].

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Table 2-2. Ball Characteristics (CBC Pkg.)[(1)] (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENG TH (mA) [11]	PULLUP /DOWN TYPE [12]	IO CELL [13]
AC21, D15, G11, G18, H20, M7, M17, R20, T7, Y8, Y12	NA	vdd_core	0	PWR	-	-	-	-	-	-	-	-
D13, G9, G12, H7, K11, L9, M9, M10, N7, N8, P10, U7, U11, U13, V7, V11, W9, Y9, Y11	NA	vdd_mpu _iva	0	PWR	-	-	-	-	-	-	-	-
A18, AC7, AC15, AC18, AC24, AD20, AE10, C11, D9, E24, G4, J15, J18, L7, L24, M4, T4, T24, W24, Y4, L20, AB24, AD18, AD19	NA	vdds	0	PWR	-	-	-	-	-	-	-	-
U12	NA	vdds_sram	0	PWR	-	-	-	-	-	-	-	-
K13	NA	vdds_dpll_dll	0	PWR	-	-	-	-	-	-	-	-
U14	NA	vdds_dpll_per	0	PWR	-	-	-	-	-	-	-	-
W14	NA	vdds_wkup_bg	0	PWR	-	-	-	-	-	-	-	-
N23, P23	NA	vdds_mmc1, vdds_mmc1a	0	PWR	-	-	-	-	-	-	-	-
V25	NA	vdda_dac	0	PWR	-	-	-	-	-	-	-	-
V24	NA	vssa_dac	0	PWR	-	-	-	-	-	-	-	-
A6, A8, A13, AB5, AB22, AC10, AC16, AC19, AD14, AD25,AE7, AF23, B2, B25, C12, D7, D10, D12, D14, D18, D20, E22, G1, G8, G10, G20, G23, H4, K1, K15, K25, L10, L17, L19, L23, N4, N10, N17, R1, R4, R17, T23, U25, W1, W4, W23, Y7, Y10, Y16, Y26	NA	vss	0	GND	-	-	-	-	-	-	-	-
K14, K20, N9, AE19	NA	cap_vdd_wkup, cap_vdd_sram_core, cap_vdd_sram_mpu _iva, cap_vdd_d	0	PWR	-	-	-	-	-	-	-	-
A1, L1, AF1, T2, Y2, AE2, AF4, AF5, AF8, AF10, AF12, AF13, AF14, AF15, AF17, AF16, A20, AF21, AF18, AF24, AF22, A25, AE25, AF25, A26, B26, K26, U26, AE26, AF26	A1, J1, AA1, N2, T2, W2, Y2, AA6, Y7, Y9, AA10, AA11, AA12, AA13, Y14, AA14, B16, Y17, AA17, Y19, AA19, A20, Y20, AA20, A21, B21, H21, P21, Y21, AA21	FeedThrough Pins[(24)]	-	-	-	-	-	-	-	-	-	-

(24) These signals are feed-through balls. For more information, refer to Section 2.5.10.

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Table 2-2. Ball Characteristics (CBC Pkg.)[(1)] (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENG TH (mA) [11]	PULLUP /DOWN TYPE [12]	IO CELL [13]
A2, A4, A5, A7, A9, A10, A11, A12, A14, A15, A16, A17, A19, A21, A22, AA23, AB23, AC9, AC12, AC13, AC14, AC17, AC20, AC22, AC23, AD9, AD11, AD12, AD13, AE1, AE8, AE11, AE12, AE13, AF2, AF3, AF11, B1, B7, B8, B9, B10, B11, B12, B13, B14, B15, B16, B17, B18, B19, B20, B21, B22, C7, C8, C9, C10, C13, C14, C15, C16, C17 C18, C19, C20, C21, C22, D5, D6, D8, D11, D16, D17, D19, D21, D22, E23, F4, G7, G13, G14, G15, G16, G17, G19, H8, H9, H10, H11, H12, H13, H14, H15, H16, H17, H18, H19, H23, J3, J4, J7, J8, J9, J10, J11, J12, J13, J14, J16, J17, J19, J20, K4, K7, K8, K9, K10, K12, K16, K17, K19, K23, L8, M8, M23, N18, P2, P4, P24, R23, R24, R25, R26, T25, T26, U23, V4, W12, Y23	-	No Connect	-	-	-	-	-	-	-	-	-	-

Table 2-3. Ball Characteristics (CUS Pkg.)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENG TH (mA) [11]	PULLUP /DOWN TYPE [12]
D7	sdrc_d0	0	IO	L	Z	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
C5	sdrc_d1	0	IO	L	Z	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
C6	sdrc_d2	0	IO	L	Z	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
B5	sdrc_d3	0	IO	L	Z	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
D9	sdrc_d4	0	IO	L	Z	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
D10	sdrc_d5	0	IO	L	Z	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
C7	sdrc_d6	0	IO	L	Z	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
B7	sdrc_d7	0	IO	L	Z	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
B11	sdrc_d8	0	IO	L	Z	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS

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Table 2-3. Ball Characteristics (CUS Pkg.) (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENG TH (mA) [11]	PULLUP /DOWN TYPE [12]
C12	sdrc_d9	0	IO	L	Z	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
B12	sdrc_d10	0	IO	L	Z	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
D13	sdrc_d11	0	IO	L	Z	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
C13	sdrc_d12	0	IO	L	Z	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
B14	sdrc_d13	0	IO	L	Z	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
A14	sdrc_d14	0	IO	L	Z	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
B15	sdrc_d15	0	IO	L	Z	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
C9	sdrc_d16	0	IO	L	Z	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
E12	sdrc_d17	0	IO	L	Z	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
B8	sdrc_d18	0	IO	L	Z	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
B9	sdrc_d19	0	IO	L	Z	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
C10	sdrc_d20	0	IO	L	Z	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
B10	sdrc_d21	0	IO	L	Z	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
D12	sdrc_d22	0	IO	L	Z	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
E13	sdrc_d23	0	IO	L	Z	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
E15	sdrc_d24	0	IO	L	Z	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
D15	sdrc_d25	0	IO	L	Z	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
C15	sdrc_d26	0	IO	L	Z	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
B16	sdrc_d27	0	IO	L	Z	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
C16	sdrc_d28	0	IO	L	Z	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
D16	sdrc_d29	0	IO	L	Z	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
B17	sdrc_d30	0	IO	L	Z	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
B18	sdrc_d31	0	IO	L	Z	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
C18	sdrc_ba0	0	O	0	0	0	vdds_ mem	No	4	NA	LVCMOS
D18	sdrc_ba1	0	O	0	0	0	vdds_ mem	No	4	NA	LVCMOS
A4	sdrc_a0	0	O	0	0	0	vdds_ mem	No	4	NA	LVCMOS
B4	sdrc_a1	0	O	0	0	0	vdds_ mem	No	4	NA	LVCMOS
D6	sdrc_a2	0	O	0	0	0	vdds_ mem	No	4	NA	LVCMOS
B3	sdrc_a3	0	O	0	0	0	vdds_ mem	No	4	NA	LVCMOS
B2	sdrc_a4	0	O	0	0	0	vdds_ mem	No	4	NA	LVCMOS
C3	sdrc_a5	0	O	0	0	0	vdds_ mem	No	4	NA	LVCMOS
E3	sdrc_a6	0	O	0	0	0	vdds_ mem	No	4	NA	LVCMOS
F6	sdrc_a7	0	O	0	0	0	vdds_ mem	No	4	NA	LVCMOS
E10	sdrc_a8	0	O	0	0	0	vdds_ mem	No	4	NA	LVCMOS
E9	sdrc_a9	0	O	0	0	0	vdds_ mem	No	4	NA	LVCMOS
E7	sdrc_a10	0	O	0	0	0	vdds_ mem	No	4	NA	LVCMOS
G6	sdrc_a11	0	O	0	0	0	vdds_ mem	No	4	NA	LVCMOS
G7	sdrc_a12	0	O	0	0	0	vdds_ mem	No	4	NA	LVCMOS
F7	sdrc_a13	0	O	0	0	0	vdds_ mem	No	4	NA	LVCMOS
F9	sdrc_a14	0	O	0	0	0	vdds_ mem	No	4	NA	LVCMOS
A19	sdrc_ncs0	0	O	1	1	0	vdds_ mem	No	4	NA	LVCMOS
B19	sdrc_ncs1	0	O	1	1	0	vdds_ mem	No	4	NA	LVCMOS
A10	sdrc_clk	0	IO	L	0	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
A11	sdrc_nclk	0	O	1	1	0	vdds_ mem	No	4	NA	LVCMOS
B20	sdrc_cke0	0	O	H	1	7	vdds_ mem	Yes	4	PU/ PD	LVCMOS
	safe_mode	7									
C20	sdrc_cke1	0	O	H	1	7	vdds_ mem	Yes	4	PU/ PD	LVCMOS
	safe_mode	7									
D19	sdrc_nras	0	O	1	1	0	vdds_ mem	No	4	NA	LVCMOS
C19	sdrc_ncas	0	O	1	1	0	vdds_ mem	No	4	NA	LVCMOS
A20	sdrc_nwe	0	O	1	1	0	vdds_ mem	No	4	NA	LVCMOS
B6	sdrc_dm0	0	O	0	0	0	vdds_ mem	No	4	NA	LVCMOS
B13	sdrc_dm1	0	O	0	0	0	vdds_ mem	No	4	NA	LVCMOS
A7	sdrc_dm2	0	O	0	0	0	vdds_ mem	No	4	NA	LVCMOS
A16	sdrc_dm3	0	O	0	0	0	vdds_ mem	No	4	NA	LVCMOS

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Table 2-3. Ball Characteristics (CUS Pkg.) (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENG TH (mA) [11]	PULLUP /DOWN TYPE [12]
A5	sdrc_dqs0	0	IO	L	Z	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
A13	sdrc_dqs1	0	IO	L	Z	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
A8	sdrc_dqs2	0	IO	L	Z	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
A17	sdrc_dqs3	0	IO	L	Z	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
K4	gpmc_a1	0	O	L	L	7	vdds_ mem	Yes	4	PU/ PD	LVCMOS
	gpio_34	4	IO								
	safe_mode	7									
K3	gpmc_a2	0	O	L	L	7	vdds_ mem	Yes	4	PU/ PD	LVCMOS
	gpio_35	4	IO								
	safe_mode	7									
K2	gpmc_a3	0	O	L	L	7	vdds_ mem	Yes	4	PU/ PD	LVCMOS
	gpio_36	4	IO								
	safe_mode	7									
J4	gpmc_a4	0	O	L	L	7	vdds_ mem	Yes	4	PU/ PD	LVCMOS
	gpio_37	4	IO								
	safe_mode	7									
J3	gpmc_a5	0	O	L	L	7	vdds_ mem	Yes	4	PU/ PD	LVCMOS
	gpio_38	4	IO								
	safe_mode	7									
J2	gpmc_a6	0	O	H	H	7	vdds_ mem	Yes	4	PU/ PD	LVCMOS
	gpio_39	4	IO								
	safe_mode	7									
J1	gpmc_a7	0	O	H	H	7	vdds_ mem	Yes	4	PU/ PD	LVCMOS
	gpio_40	4	IO								
	safe_mode	7									
H1	gpmc_a8	0	O	H	H	7	vdds_ mem	Yes	4	PU/ PD	LVCMOS
	gpio_41	4	IO								
	safe_mode	7									
H2	gpmc_a9	0	O	H	H	7	vdds_ mem	Yes	4	PU/ PD	LVCMOS
	sys_ ndmareq2	1	I								
	gpio_42	4	IO								
	safe_mode	7									
G2	gpmc_a10	0	O	H	H	7	vdds_ mem	Yes	4	PU/ PD	LVCMOS
	sys_ ndmareq3	1	I								
	gpio_43	4	IO								
	safe_mode	7									
L2	gpmc_d0	0	IO	H	H	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
M1	gpmc_d1	0	IO	H	H	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
M2	gpmc_d2	0	IO	H	H	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
N2	gpmc_d3	0	IO	H	H	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
M3	gpmc_d4	0	IO	H	H	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
P1	gpmc_d5	0	IO	H	H	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
P2	gpmc_d6	0	IO	H	H	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
R1	gpmc_d7	0	IO	H	H	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
R2	gpmc_d8	0	IO	H	H	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
	gpio_44	4	IO								
	safe_mode	7									
T2	gpmc_d9	0	IO	H	H	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
	gpio_45	4	IO								
	safe_mode	7									
U1	gpmc_d10	0	IO	H	H	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
	gpio_46	4	IO								
	safe_mode	7									

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Table 2-3. Ball Characteristics (CUS Pkg.) (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENG TH (mA) [11]	PULLUP /DOWN TYPE [12]
R3	gpmc_d11	0	IO	H	H	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
	gpio_47	4	IO								
	safe_mode	7									
T3	gpmc_d12	0	IO	H	H	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
	gpio_48	4	IO								
	safe_mode	7									
U2	gpmc_d13	0	IO	H	H	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
	gpio_49	4	IO								
	safe_mode	7									
V1	gpmc_d14	0	IO	H	H	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
	gpio_50	4	IO								
	safe_mode	7									
V2	gpmc_d15	0	IO	H	H	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
	gpio_51	4	IO								
	safe_mode	7									
E2	gpmc_ncs0	0	O	1	1	0	vdds_ mem	No	4	NA	LVCMOS
D2	gpmc_ncs3	0	O	H	H	7	vdds_ mem	Yes	4	PU/ PD	LVCMOS
	sys_ ndmareq0	1	I								
	gpio_54	4	IO								
	safe_mode	7									
F4	gpmc_ncs4	0	O	H	H	7	vdds_ mem	Yes	4	PU/ PD	LVCMOS
	sys_ ndmareq1	1	I								
	mcbsp4_ clkx	2	IO								
	gpt9_pwm_evt	3	IO								
	gpio_55	4	IO								
	safe_mode	7									
G5	gpmc_ncs5	0	O	H	H	7	vdds_ mem	Yes	4	PU/ PD	LVCMOS
	sys_ ndmareq2	1	I								
	mcbsp4_dr	2	I								
	gpt10_pwm_evt	3	IO								
	gpio_56	4	IO								
	safe_mode	7									
F3	gpmc_ncs6	0	O	H	H	7	vdds_ mem	Yes	4	PU/ PD	LVCMOS
	sys_ ndmareq3	1	I								
	mcbsp4_dx	2	IO								
	gpt11_pwm_evt	3	IO								
	gpio_57	4	IO								
	safe_mode	7									
G4	gpmc_ncs7	0	O	H	H	7	vdds_ mem	Yes	4	PU/ PD	LVCMOS
	gpmc_io_dir	1	O								
	mcbsp4_fsx	2	IO								
	gpt8_pwm_evt	3	IO								
	gpio_58	4	IO								
	safe_mode	7									
W2	gpmc_clk	0	O	L	0	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
	gpio_59	4	IO								
	safe_mode	7									
F1	gpmc_nadv_ale	0	O	0	0	0	vdds_ mem	No	4	NA	LVCMOS
F2	gpmc_noe	0	O	1	1	0	vdds_ mem	No	4	NA	LVCMOS
G3	gpmc_nwe	0	O	1	1	0	vdds_ mem	No	4	NA	LVCMOS

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Table 2-3. Ball Characteristics (CUS Pkg.) (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENG TH (mA) [11]	PULLUP /DOWN TYPE [12]
K5	gpmc_nbe0_cle	0	O	L	0	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
	gpio_60	4	IO								
	safe_mode	7									
L1	gpmc_nbe1	0	O	L	L	7	vdds_ mem	Yes	4	PU/ PD	LVCMOS
	gpio_61	4	IO								
	safe_mode	7									
E1	gpmc_nwp	0	O	L	0	0	vdds_ mem	Yes	4	PU/ PD	LVCMOS
	gpio_62	4	IO								
	safe_mode	7									
C1	gpmc_wait0	0	I	H	H	0	vdds_ mem	Yes	NA	PU/ PD	LVCMOS
C2	gpmc_wait3	0	I	H	H	7	vdds_ mem	Yes	4	PU/ PD	LVCMOS
	sys_ ndmareq1	1	I								
	gpio_65	4	IO								
	safe_mode	7									
G22	dss_pclk	0	O	H	H	7	vdds	Yes	4	PU/ PD	LVCMOS
	gpio_66	4	IO								
	safe_mode	7									
E22	dss_hsync	0	O	H	H	7	vdds	Yes	4	PU/ PD	LVCMOS
	gpio_67	4	IO								
	safe_mode	7									
F22	dss_vsync	0	O	H	H	7	vdds	Yes	4	PU/ PD	LVCMOS
	gpio_68	4	IO								
	safe_mode	7									
J21	dss_acbias	0	O	L	L	7	vdds	Yes	8	PU/ PD	LVCMOS
	gpio_69	4	IO								
	safe_mode	7									
AC19	dss_data0	0	IO	L	L	7	vdds	No	4	PU/ PD	LVCMOS
	uart1_cts	2	I								
	gpio_70	4	IO								
	safe_mode	7									
AB19	dss_data1	0	IO	L	L	7	vdds	No	4	PU/ PD	LVCMOS
	uart1_rts	2	O								
	gpio_71	4	IO								
	safe_mode	7									
AD20	dss_data2	0	IO	L	L	7	vdds	No	4	PU/ PD	LVCMOS
	gpio_72	4	IO								
	safe_mode	7									
AC20	dss_data3	0	IO	L	L	7	vdds	No	4	PU/ PD	LVCMOS
	gpio_73	4	IO								
	safe_mode	7									
AD21	dss_data4	0	IO	L	L	7	vdds	No	4	PU/ PD	LVCMOS
	uart3_rx_ irrx	2	I								
	gpio_74	4	IO								
	safe_mode	7									
AC21	dss_data5	0	IO	L	L	7	vdds	No	4	PU/ PD	LVCMOS
	uart3_tx_ irtx	2	O								
	gpio_75	4	IO								
	safe_mode	7									
D24	dss_data6	0	IO	L	L	7	vdds	Yes	8	PU/ PD	LVCMOS
	uart1_tx	2	O								
	gpio_76	4	IO								
	safe_mode	7									
E23	dss_data7	0	IO	L	L	7	vdds	Yes	8	PU/ PD	LVCMOS

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Table 2-3. Ball Characteristics (CUS Pkg.) (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENG TH (mA) [11]	PULLUP /DOWN TYPE [12]
	uart1_rx	2	I								
	gpio_77	4	IO								
	safe_mode	7									
E24	dss_data8	0	IO	L	L	7	vdds	Yes	8	PU/ PD	LVCMOS
	gpio_78	4	IO								
	safe_mode	7									
F23	dss_data9	0	IO	L	L	7	vdds	Yes	8	PU/ PD	LVCMOS
	gpio_79	4	IO								
	safe_mode	7									
AC22	dss_data10	0	IO	L	L	7	vdds	NA	4	PU/ PD	LVCMOS
	gpio_80	4	IO								
	safe_mode	7									
AC23	dss_data11	0	IO	L	L	7	vdds	NA	4	PU/ PD	LVCMOS
	gpio_81	4	IO								
	safe_mode	7									
AB22	dss_data12	0	IO	L	L	7	vdds	NA	4	PU/ PD	LVCMOS
	gpio_82	4	IO								
	safe_mode	7									
Y22	dss_data13	0	IO	L	L	7	vdds	NA	4	PU/ PD	LVCMOS
	gpio_83	4	IO								
	safe_mode	7									
W22	dss_data14	0	IO	L	L	7	vdds	NA	4	PU/ PD	LVCMOS
	gpio_84	4	IO								
	safe_mode	7									
V22	dss_data15	0	IO	L	L	7	vdds	NA	4	PU/ PD	LVCMOS
	gpio_85	4	IO								
	safe_mode	7									
J22	dss_data16	0	IO	L	L	7	vdds	Yes	8	PU/ PD	LVCMOS
	gpio_86	4	IO								
	safe_mode	7									
G23	dss_data17	0	IO	L	L	7	vdds	Yes	8	PU/ PD	LVCMOS
	gpio_87	4	IO								
	safe_mode	7									
G24	dss_data18	0	IO	L	L	7	vdds	Yes	8	PU/ PD	LVCMOS
	mcspi3_clk	2	IO								
	dss_data0	3	IO								
	gpio_88	4	IO								
	safe_mode	7									
H23	dss_data19	0	IO	L	L	7	vdds	Yes	8	PU/ PD	LVCMOS
	mcspi3_ simo	2	IO								
	dss_data1	3	IO								
	gpio_89	4	IO								
	safe_mode	7									
D23	dss_data20	0	O	H	H	7	vdds	Yes	4	PU/ PD	LVCMOS
	mcspi3_ somi	2	IO								
	dss_data2	3	IO								
	gpio_90	4	IO								
	safe_mode	7									
K22	dss_data21	0	O	L	L	7	vdds	Yes	8	PU/ PD	LVCMOS
	mcspi3_cs0	2	IO								
	dss_data3	3	IO								
	gpio_91	4	IO								
	safe_mode	7									
V21	dss_data22	0	O	L	L	7	vdds	NA	4	PU/ PD	LVCMOS
	mcspi3_cs1	2	O								

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Table 2-3. Ball Characteristics (CUS Pkg.) (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENG TH (mA) [11]	PULLUP /DOWN TYPE [12]
	dss_data4	3	IO								
	gpio_92	4	IO								
	safe_mode	7									
W21	dss_data23	0	O	L	L	7	vdds	NA	4	PU/ PD	LVCMOS
	dss_data5	3	IO								
	gpio_93	4	IO								
	safe_mode	7									
AA23	tv_out2	0	O	Z	0	0	vdda_dac		8	NA	10-bit DAC
AB24	tv_out1	0	O	Z	0	0	vdda_dac		8	NA	10-bit DAC
AB23	tv_vfb1	0	O	Z	NA	0	vdda_dac			NA	10-bit DAC
Y23	tv_vfb2	0	O	Z	NA	0	vdda_dac			NA	10-bit DAC
Y24	tv_vref	0	I	Z	NA	0	vdda_dac			NA	10-bit DAC
A22	cam_hs	0	IO	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
	gpio_94	4	IO								
	safe_mode	7									
E18	cam_vs	0	IO	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
	gpio_95	4	IO								
	safe_mode	7									
B22	cam_ xclka	0	O	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
	gpio_96	4	IO								
	safe_mode	7									
J19	cam_pclk	0	I	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
	gpio_97	4	IO								
	safe_mode	7									
H24	cam_fld	0	IO	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
	cam_global_reset	2	IO								
	gpio_98	4	IO								
	safe_mode	7									
AB18	cam_d0	0	I	L	L	7	vdds	Yes	4	PD	LVCMOS
	gpio_99	4	I								
	safe_mode	7									
AC18	cam_d1	0	I	L	L	7	vdds	Yes	4	PD	LVCMOS
	gpio_100	4	I								
	safe_mode	7									
G19	cam_d2	0	I	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
	gpio_101	4	IO								
	safe_mode	7									
F19	cam_d3	0	I	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
	gpio_102	4	IO								
	safe_mode	7									
G20	cam_d4	0	I	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
	gpio_103	4	IO								
	safe_mode	7									
B21	cam_d5	0	I	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
	gpio_104	4	IO								
	safe_mode	7									
L24	cam_d6	0	I	L	L	7	vdds	NA	4	PD	LVCMOS
	gpio_105	4	IO								
	safe_mode	7									
K24	cam_d7	0	I	L	L	7	vdds	NA	4	PD	LVCMOS
	gpio_106	4	IO								
	safe_mode	7									
J23	cam_d8	0	I	L	L	7	vdds	NA	4	PD	LVCMOS
	gpio_107	4	IO								

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Table 2-3. Ball Characteristics (CUS Pkg.) (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENG TH (mA) [11]	PULLUP /DOWN TYPE [12]
	safe_mode	7									
K23	cam_d9	0	I	L	L	7	vdds	NA	4	PD	LVCMOS
	gpio_108	4	IO								
	safe_mode	7									
F21	cam_d10	0	I	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
	gpio_109	4	IO								
	safe_mode	7									
G21	cam_d11	0	I	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
	gpio_110	4	IO								
	safe_mode	7									
C22	cam_ xclkb	0	O	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
	gpio_111	4	IO								
	safe_mode	7									
F18	cam_wen	0	I	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
	cam_ shutter	2	O								
	gpio_167	4	IO								
	safe_mode	7									
J20	cam_ strobe	0	O	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
	gpio_126	4	IO								
	safe_mode	7									
V20	mcbsp2_fsx	0	IO	L	L	7	vdds	Yes	4(1)	PU/ PD	LVCMOS
	gpio_116	4	IO								
	safe_mode	7									
T21	mcbsp2_ clkx	0	IO	L	L	7	vdds	Yes	4(1)	PU/ PD	LVCMOS
	gpio_117	4	IO								
	safe_mode	7									
V19	mcbsp2_dr	0	I	L	L	7	vdds	Yes	4 (1)	PU/ PD	LVCMOS
	gpio_118	4	IO								
	safe_mode	7									
R20	mcbsp2_dx	0	IO	L	L	7	vdds	Yes	4(1)	PU/ PD	LVCMOS
	gpio_119	4	IO								
	safe_mode	7									
M23	mmc1_clk	0	O	L	L	7	vdds_mmc1	Yes	8	PU/ PD	LVCMOS
	gpio_120	4	IO								
	safe_mode	7									
L23	mmc1_cmd	0	IO	L	L	7	vdds_mmc1	Yes	8	PU/ PD	LVCMOS
	gpio_121	4	IO								
	safe_mode	7									
M22	mmc1_dat0	0	IO	L	L	7	vdds_mmc1	Yes	8	PU/ PD	LVCMOS
	gpio_122	4	IO								
	safe_mode	7									
M21	mmc1_dat1	0	IO	L	L	7	vdds_mmc1	Yes	8	PU/ PD	LVCMOS
	gpio_123	4	IO								
	safe_mode	7									
M20	mmc1_dat2	0	IO	L	L	7	vdds_mmc1	Yes	8	PU/ PD	LVCMOS
	gpio_124	4	IO								
	safe_mode	7									
N23	mmc1_dat3	0	IO	L	L	7	vdds_mmc1	Yes	8	PU/ PD	LVCMOS
	gpio_125	4	IO								
	safe_mode	7									
N22	mmc1_dat4	0	IO	L	L	7	vdds_mmc1a	No	8	PD	LVCMOS
	gpio_126	4	IO								
	safe_mode	7									
N21	mmc1_dat5	0	IO	L	L	7	vdds_mmc1a	No	8	PD	LVCMOS

(1) The buffer strength of this IO cell is programmable (2, 4, 6, or 8 mA) according to the selected mode; the default value is described in

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Table 2-3. Ball Characteristics (CUS Pkg.) (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENG TH (mA) [11]	PULLUP /DOWN TYPE [12]
	gpio_127	4	IO								
	safe_mode	7									
N20	mmc1_dat6	0	IO	L	L	7	vdds_mmc1a	No	8	PD	LVCMOS
	gpio_128	4	IO								
	safe_mode	7									
P24	mmc1_dat7	0	IO	L	L	7	vdds_mmc1a	No	8	PD	LVCMOS
	gpio_129	4	IO								
	safe_mode	7									
Y1	mmc2_clk	0	O	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
	mcspi3_clk	1	IO								
	gpio_130	4	IO								
	safe_mode	7									
AB5	mmc2_ cmd	0	IO	H	H	7	vdds	Yes	4	PU/ PD	LVCMOS
	mcspi3_ simo	1	IO								
	gpio_131	4	IO								
	safe_mode	7									
AB3	mmc2_ dat0	0	IO	H	H	7	vdds	Yes	4	PU/ PD	LVCMOS
	mcspi3_ somi	1	IO								
	gpio_132	4	IO								
	safe_mode	7									
Y3	mmc2_ dat1	0	IO	H	H	7	vdds	Yes	4	PU/ PD	LVCMOS
	gpio_133	4	IO								
	safe_mode	7									
W3	mmc2_ dat2	0	IO	H	H	7	vdds	Yes	4	PU/ PD	LVCMOS
	mcspi3_cs1	1	O								
	gpio_134	4	IO								
	safe_mode	7									
V3	mmc2_ dat3	0	IO	H	H	7	vdds	Yes	4	PU/ PD	LVCMOS
	mcspi3_cs0	1	IO								
	gpio_135	4	IO								
	safe_mode	7									
AB2	mmc2_ dat4	0	IO	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
	mmc2_dir_dat 0	1	O								
	mmc3_dat0	3	IO								
	gpio_136	4	IO								
	safe_mode	7									
AA2	mmc2_ dat5	0	IO	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
	mmc2_dir_dat 1	1	O								
	cam_global_re set	2	IO								
	mmc3_dat1	3	IO								
	gpio_137	4	IO								
	safe_mode	7									
Y2	mmc2_ dat6	0	IO	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
	mmc2_dir_ cmd	1	O								
	cam_ shutter	2	O								
	mmc3_dat2	3	IO								
	gpio_138	4	IO								
	safe_mode	7									
AA1	mmc2_ dat7	0	IO	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
	mmc2_ clkin	1	I								
	mmc3_dat3	3	IO								
	gpio_139	4	IO								

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Table 2-3. Ball Characteristics (CUS Pkg.) (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENG TH (mA) [11]	PULLUP /DOWN TYPE [12]
	safe_mode	7									
V6	mcbsp3_dx	0	IO	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
	uart2_cts	1	I								
	gpio_140	4	IO								
	safe_mode	7									
V5	mcbsp3_dr	0	I	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
	uart2_rts	1	O								
	gpio_141	4	IO								
	safe_mode	7									
W4	mcbsp3_ clkx	0	IO	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
	uart2_tx	1	O								
	gpio_142	4	IO								
	safe_mode	7									
V4	mcbsp3_fsx	0	IO	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
	uart2_rx	1	I								
	gpio_143	4	IO								
	safe_mode	7									
W7	uart1_tx	0	O	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
	gpio_148	4	IO								
	safe_mode	7									
W6	uart1_rts	0	O	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
	gpio_149	4	IO								
	safe_mode	7									
AC2	uart1_cts	0	I	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
	gpio_150	4	IO								
	safe_mode	7									
V7	uart1_rx	0	I	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
	mcbsp1_ clkr	2	IO								
	mcspi4_clk	3	IO								
	gpio_151	4	IO								
	safe_mode	7									
W19	mcbsp1_ clkr	0	IO	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
	mcspi4_clk	1	IO								
	gpio_156	4	IO								
	safe_mode	7									
AB20	mcbsp1_fsr	0	IO	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
	cam_global_reset	2	IO								
	gpio_157	4	IO								
	safe_mode	7									
W18	mcbsp1_dx	0	IO	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
	mcspi4_ simo	1	IO								
	mcbsp3_dx	2	IO								
	gpio_158	4	IO								
	safe_mode	7									
Y18	mcbsp1_dr	0	I	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
	mcspi4_ somi	1	IO								
	mcbsp3_dr	2	O								
	gpio_159	4	IO								
	safe_mode	7									
AA18	mcbsp_clks	0	I	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
	cam_ shutter	2	O								
	gpio_160	4	IO								
	uart1_cts	5	I								
	safe_mode	7									

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Table 2-3. Ball Characteristics (CUS Pkg.) (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENG TH (mA) [11]	PULLUP /DOWN TYPE [12]
AA19	mcbsp1_fsx	0	IO	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
	mcspi4_cs0	1	IO								
	mcbsp3_fsx	2	IO								
	gpio_161	4	IO								
	safe_mode	7									
V18	mcbsp1_ clkx	0	IO	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
	mcbsp3_ clkx	2	IO								
	gpio_162	4	IO								
	safe_mode	7									
A23	uart3_cts_ rctx	0	IO	H	H	7	vdds	Yes	4	PU/ PD	LVCMOS
	gpio_163	4	IO								
	safe_mode	7									
B23	uart3_rts_ sd	0	O	H	H	7	vdds	Yes	4	PU/ PD	LVCMOS
	gpio_164	4	IO								
	safe_mode	7									
B24	uart3_rx_ irrx	0	I	H	H	7	vdds	Yes	4	PU/ PD	LVCMOS
	gpio_165	4	IO								
	safe_mode	7									
C23	uart3_tx_ irtx	0	O	H	H	7	vdds	Yes	4	PU/ PD	LVCMOS
	gpio_166	4	IO								
	safe_mode	7									
R21	hsusb0_clk	0	I	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
	gpio_120	4	IO								
	safe_mode	7									
R23	hsusb0_stp	0	O	H	H	7	vdds	Yes	4	PU/ PD	LVCMOS
	gpio_121	4	IO								
	safe_mode	7									
P23	hsusb0_dir	0	I	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
	gpio_122	4	IO								
	safe_mode	7									
R22	hsusb0_nxt	0	I	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
	gpio_124	4	IO								
	safe_mode	7									
T24	hsusb0_ data0	0	IO	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
	uart3_tx_ irtx	2	O								
	gpio_125	4	IO								
	safe_mode	7									
T23	hsusb0_ data1	0	IO	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
	uart3_rx_ irrx	2	I								
	gpio_130	4	IO								
	safe_mode	7									
U24	hsusb0_ data2	0	IO	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
	uart3_rts_ sd	2	O								
	gpio_131	4	IO								
	safe_mode	7									
U23	hsusb0_ data3	0	IO	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
	uart3_cts_ rctx	2	IO								
	gpio_169	4	IO								
	safe_mode	7									
W24	hsusb0_ data4	0	IO	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
	gpio_188	4	IO								
	safe_mode	7									
V23	hsusb0_ data5	0	IO	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
	gpio_189	4	IO								
	safe_mode	7									

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Table 2-3. Ball Characteristics (CUS Pkg.) (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENG TH (mA) [11]	PULLUP /DOWN TYPE [12]
W23	hsusb0_ data6	0	IO	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
	gpio_190	4	IO								
	safe_mode	7									
T22	hsusb0_ data7	0	IO	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
	gpio_191	4	IO								
	safe_mode	7									
K20	i2c1_scl	0	IOD	H	H	0	vdds	Yes	4	PU/ PD	Open Drain
K21	i2c1_sda	0	IOD	H	H	0	vdds	Yes	4	PU/ PD	Open Drain
AC15	i2c2_scl	0	IOD	H	H	7	vdds	Yes	4	PU/ PD	Open Drain
	gpio_168	4	IO								
	safe_mode	7									
AC14	i2c2_sda	0	IOD	H	H	7	vdds	Yes	4	PU/ PD	Open Drain
	gpio_183	4	IO								
	safe_mode	7									
AC13	i2c3_scl	0	IOD	H	H	7	vdds	Yes	4	PU/ PD	Open Drain
	gpio_184	4	IO								
	safe_mode	7									
AC12	i2c3_sda	0	IOD	H	H	7	vdds	Yes	4	PU/ PD	Open Drain
	gpio_185	4	IO								
	safe_mode	7									
Y16	i2c4_scl	0	IOD	H	H	0	vdds	Yes	4	PU/ PD	Open Drain
	sys_ nvmode1	1	O								
	safe_mode	7									
Y15	i2c4_sda	0	IOD	H	H	0	vdds	Yes	4	PU/ PD	Open Drain
	sys_ nvmode2	1	O								
	safe_mode	7									
A24	hdq_sio	0	IOD	H	H	7	vdds	Yes	4	PU/ PD	LVCMOS
	sys_altclk	1	I								
	i2c2_sccbe	2	O								
	i2c3_sccbe	3	O								
	gpio_170	4	IO								
	safe_mode	7									
T5	mcspi1_clk	0	IO	L	L	7	vdds	Yes	4(2)	PU/ PD	LVCMOS
	mmc2_dat4	1	IO								
	gpio_171	4	IO								
	safe_mode	7									
R4	mcspi1_ simo	0	IO	L	L	7	vdds	Yes	4(2)	PU/ PD	LVCMOS
	mmc2_dat5	1	IO								
	gpio_172	4	IO								
	safe_mode	7									
T4	mcspi1_ somi	0	IO	L	L	7	vdds	Yes	4 (2)	PU/ PD	LVCMOS
	mmc2_dat6	1	IO								
	gpio_173	4	IO								
	safe_mode	7									
T6	mcspi1_cs0	0	IO	H	H	7	vdds	Yes	4(2)	PU/ PD	LVCMOS
	mmc2_dat7	1	IO								
	gpio_174	4	IO								
	safe_mode	7									
R5	mcspi1_cs3	0	O	H	H	7	vdds	Yes	4	PU/ PD	LVCMOS
	hsusb2_tll_ data2	2	IO								
	hsusb2_ data2	3	IO								
	gpio_177	4	IO								
	mm2_txdat	5	IO								

(2) The buffer strength of this IO cell is programmable (2, 4, 6, or 8 mA) according to the selected mode; the default value is described in

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Table 2-3. Ball Characteristics (CUS Pkg.) (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENG TH (mA) [11]	PULLUP /DOWN TYPE [12]
	safe_mode	7									
N5	mcspi2_clk	0	IO	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
	hsusb2_tll_ data7	2	IO								
	hsusb2_ data7	3	O								
	gpio_178	4	IO								
	safe_mode	7									
N4	mcspi2_ simo	0	IO	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
	gpt9_pwm_evt	1	IO								
	hsusb2_tll_ data4	2	IO								
	hsusb2_ data4	3	I								
	gpio_179	4	IO								
	safe_mode	7									
N3	mcspi2_ somi	0	IO	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
	gpt10_pwm_evt	1	IO								
	hsusb2_tll_ data5	2	IO								
	hsusb2_ data5	3	O								
	gpio_180	4	IO								
	safe_mode	7									
M5	mcspi2_cs0	0	IO	H	H	7	vdds	Yes	4	PU/ PD	LVCMOS
	gpt11_pwm_evt	1	IO								
	hsusb2_tll_ data6	2	IO								
	hsusb2_ data6	3	O								
	gpio_181	4	IO								
	safe_mode	7									
M4	mcspi2_cs1	0	O	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
	gpt8_pwm_evt	1	IO								
	hsusb2_tll_ data3	2	IO								
	hsusb2_ data3	3	IO								
	gpio_182	4	IO								
	mm2_txen_n	5	IO								
	safe_mode	7									
AA16	sys_32k	0	I	Z	I	NA	vdds	Yes	NA	NA	LVCMOS
AD15	sys_xtalin	0	I	Z	I	NA	vdds	Yes		NA	LVCMOS
AD14	sys_xtalout	0	O	Z	O	NA	vdds	Yes		NA	LVCMOS
Y13	sys_clkreq	0	IO	0	1	0	vdds	Yes	4	PU/ PD	LVCMOS
	gpio_1	4	IO								
	safe_mode	7									
W16	sys_nirq	0	I	H	H	7	vdds	Yes	4	PU/ PD	LVCMOS
	gpio_0	4	IO								
	safe_mode	7									
AA10	sys_ nrespwron	0	I	Z	I	NA	vdds	Yes	NA	NA	LVCMOS
Y10	sys_ nreswarm	0	IOD	0	1 (PU)	0	vdds	Yes	4	PU/ PD	LVCMOS
	gpio_30	4	IO								
	safe_mode	7									
AB12	sys_boot0	0	I	Z	Z	0	vdds	Yes	4	PU/ PD	LVCMOS
	gpio_2	4	IO								
	safe_mode	7									
AC16	sys_boot1	0	I	Z	Z	0	vdds	Yes	4	PU/ PD	LVCMOS
	gpio_3	4	IO								

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Table 2-3. Ball Characteristics (CUS Pkg.) (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENG TH (mA) [11]	PULLUP /DOWN TYPE [12]
	safe_mode	7									
AD17	sys_boot2	0	I	Z	Z	0	vdds	Yes	4	PU/ PD	LVCMOS
	gpio_4	4	IO								
	safe_mode	7									
AD18	sys_boot3	0	I	Z	Z	0	vdds	Yes	4	PU/ PD	LVCMOS
	gpio_5	4	IO								
	safe_mode	7									
AC17	sys_boot4	0	I	Z	Z	0	vdds	Yes	4	PU/ PD	LVCMOS
	mmc2_dir_dat 2	1	O								
	gpio_6	4	IO								
	safe_mode	7									
AB16	sys_boot5	0	I	Z	Z	0	vdds	Yes	4	PU/ PD	LVCMOS
	mmc2_dir_dat 3	1	O								
	gpio_7	4	IO								
	safe_mode	7									
AA15	sys_boot6	0	I	Z	Z	0	vdds	Yes	4	PU/ PD	LVCMOS
	gpio_8	4	IO								
	safe_mode	7									
AD23	sys_off_ mode	0	O	0	L	7	vdds	Yes	4	PU/ PD	LVCMOS
	gpio_9	4	IO								
	safe_mode	7									
Y7	sys_clkout1	0	O	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
	gpio_10	4	IO								
	safe_mode	7									
AA6	sys_clkout2	0	O	L	L	7	vdds	Yes	4	PU/ PD	LVCMOS
	gpio_186	4	IO								
	safe_mode	7									
AB7	jtag_ntrst	0	I	L	L	0	vdds	Yes	NA	PU/ PD	LVCMOS
AB6	jtag_tck	0	I	L	L	0	vdds	Yes	NA	PU/ PD	LVCMOS
AA7	jtag_rtck	0	O	L	0	0	vdds	Yes	4	PU/ PD	LVCMOS
AA9	jtag_tms_tmsc	0	IO	H	H	0	vdds	Yes	4	PU/ PD	LVCMOS
AB10	jtag_tdi	0	I	H	H	0	vdds	Yes	NA	PU/ PD	LVCMOS
AB9	jtag_tdo	0	O	L	Z	0	vdds	Yes	4	PU/ PD	LVCMOS
AC24	jtag_emu0	0	IO	H	H	0	vdds	Yes	4	PU/ PD	LVCMOS
	gpio_11	4	IO								
	safe_mode	7									
AD24	jtag_emu1	0	IO	H	H	0	vdds	Yes	4	PU/ PD	LVCMOS
	gpio_31	4	IO								
	safe_mode	7									
AC1	etk_clk	0	O	H	H	4	vdds	Yes	4	PU/ PD	LVCMOS
	mcbsp5_ clkx	1	IO								
	mmc3_clk	2	O								
	hsusb1_stp	3	O								
	gpio_12	4	IO								
	mm1_rxdp	5	IO								
	hsusb1_tll_stp	6	I								
AD3	etk_ctl	0	O	H	H	4	vdds	Yes	4	PU/ PD	LVCMOS
	mmc3_cmd	2	IO								
	hsusb1_clk	3	O								
	gpio_13	4	IO								
	hsusb1_tll_clk	6	O								
AD6	etk_d0	0	O	H	H	4	vdds	Yes	4	PU/ PD	LVCMOS
	mcspi3_ simo	1	IO								

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Table 2-3. Ball Characteristics (CUS Pkg.) (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENG TH (mA) [11]	PULLUP /DOWN TYPE [12]
	mmc3_dat4	2	IO								
	hsusb1_ data0	3	IO								
	gpio_14	4	IO								
	mm1_rxrcv	5	IO								
	hsusb1_tll_ data0	6	IO								
AC6	etk_d1	0	O	H	H	4	vdds	Yes	4	PU/ PD	LVCMOS
	mcspi3_ somi	1	IO								
	hsusb1_ data1	3	IO								
	gpio_15	4	IO								
	mm1_txse0	5	IO								
	hsusb1_tll_ data1	6	IO								
AC7	etk_d2	0	O	H	H	4	vdds	Yes	4	PU/ PD	LVCMOS
	mcspi3_cs0	1	IO								
	hsusb1_ data2	3	IO								
	gpio_16	4	IO								
	mm1_txdat	5	IO								
	hsusb1_tll_dat a2	6	IO								
AD8	etk_d3	0	O	H	H	4	vdds	Yes	4	PU/ PD	LVCMOS
	mcspi3_clk	1	IO								
	mmc3_dat3	2	IO								
	hsusb1_ data7	3	IO								
	gpio_17	4	IO								
	hsusb1_tll_ data7	6	IO								
AC5	etk_d4	0	O	L	L	4	vdds	Yes	4	PU/ PD	LVCMOS
	mcbsp5_dr	1	I								
	mmc3_dat0	2	IO								
	hsusb1_ data4	3	IO								
	gpio_18	4	IO								
	hsusb1_tll_ data4	6	IO								
AD2	etk_d5	0	O	L	L	4	vdds	Yes	4	PU/ PD	LVCMOS
	mcbsp5_fsx	1	IO								
	mmc3_dat1	2	IO								
	hsusb1_ data5	3	IO								
	gpio_19	4	IO								
	hsusb1_tll_ data5	6	IO								
AC8	etk_d6	0	O	L	L	4	vdds	Yes	4	PU/ PD	LVCMOS
	mcbsp5_dx	1	IO								
	mmc3_dat2	2	IO								
	hsusb1_ data6	3	IO								
	gpio_20	4	IO								
	hsusb1_tll_ data6	6	IO								
AD9	etk_d7	0	O	L	L	4	vdds	Yes	4	PU/ PD	LVCMOS
	mcspi3_cs1	1	O								
	mmc3_dat7	2	IO								
	hsusb1_ data3	3	IO								
	gpio_21	4	IO								
	mm1_txen_n	5	IO								
	hsusb1_tll_ data3	6	IO								
AC4	etk_d8	0	O	L	L	4	vdds	Yes	4	PU/ PD	LVCMOS

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Table 2-3. Ball Characteristics (CUS Pkg.) (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENG TH (mA) [11]	PULLUP /DOWN TYPE [12]
	sys_drm_ msecure	1	O								
	mmc3_dat6	2	IO								
	hsusb1_dir	3	I								
	gpio_22	4	IO								
	hsusb1_tll_dir	6	O								
AD5	etk_d9	0	O	L	L	4	vdds	Yes	4	PU/ PD	LVCMOS
	sys_secure_in dic ator	1	O								
	mmc3_dat5	2	IO								
	hsusb1_nxt	3	I								
	gpio_23	4	IO								
	mm1_rxdm	5	IO								
	hsusb1_tll_nxt	6	O								
AC3	etk_d10	0	O	L	L	4	vdds	Yes	4	PU/ PD	LVCMOS
	uart1_rx	2	I								
	hsusb2_clk	3	O								
	gpio_24	4	IO								
	hsusb2_tll_clk	6	O								
AC9	etk_d11	0	O	L	L	4	vdds	Yes	4	PU/ PD	LVCMOS
	hsusb2_stp	3	O								
	gpio_25	4	IO								
	mm2_rxdp	5	IO								
	hsusb2_tll_stp	6	I								
AC10	etk_d12	0	O	L	L	4	vdds	Yes	4	PU/ PD	LVCMOS
	hsusb2_dir	3	I								
	gpio_26	4	IO								
	hsusb2_tll_dir	6	O								
AD11	etk_d13	0	O	L	L	4	vdds	Yes	4	PU/ PD	LVCMOS
	hsusb2_nxt	3	I								
	gpio_27	4	IO								
	mm2_rxdm	5	IO								
	hsusb2_tll_nxt	6	O								
AC11	etk_d14	0	O	L	L	4	vdds	Yes	4	PU/ PD	LVCMOS
	hsusb2_ data0	3	IO								
	gpio_28	4	IO								
	mm2_rxrcv	5	IO								
	hsusb2_tll_ data0	6	IO								
AD12	etk_d15	0	O	L	L	4	vdds	Yes	4	PU/ PD	LVCMOS
	hsusb2_ data1	3	IO								
	gpio_29	4	IO								
	mm2_txse0	5	IO								
	hsusb2_tll_ data1	6	IO								
E16, F15, F16, G15, G16, H15, J6, J7, J8, K6, K7, K8	vdds_mem	0	PWR	-	-	-	-	-	-	-	-
F12, F13, G12, G13, H12, H13, J17, J18, K17, K18, K19, L14, L15, M14, M15, R17, R18, R19, T17, T18, T19, T20	vdd_core	0	PWR	-	-	-	-	-	-	-	-

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Table 2-3. Ball Characteristics (CUS Pkg.) (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENG TH (mA) [11]	PULLUP /DOWN TYPE [12]
F10, G9, G10, H9, H10, J9, J10, L11, L12, M6, M7, M8, M12, N6, N7, N8, R6, R7, R8, T7, T8, U12, U13, V12, V13, W12, W13	vdd_mpu _iva	0	PWR	-	-	-	-	-	-	-	-
H8	vdds_mmc1a	0	PWR	-	-	-	-	-	-	-	-
M17, M18, M19, N17, N18, N19, U10, V9, V10, W9, W10, Y9	vdds	0	PWR	-	-	-	-	-	-	-	-
N24	vdds_mmc1	0	PWR	-	-	-	-	-	-	-	-
Y12, U8, H17	cap_vdd_wkup, cap_vdd_sram_mpu _iva, cap_vdd_sram_core	0	PWR	-	-	-	-	-	-	-	-
G18	vdds_dpll_dll	0	PWR	-	-	-	-	-	-	-	-
U17	vdds_dpll_per	0	PWR	-	-	-	-	-	-	-	-
AA12	vdds_sram	0	PWR	-	-	-	-	-	-	-	-
AA13	vdds_wkup_bg	0	PWR	-	-	-	-	-	-	-	-
AB15	vssa_dac	0	GND	-	-	-	-	-	-	-	-
AB13	vdda_dac	0	PWR	-	-	-	-	-	-	-	-
H11, H14, H16, J11, J12, J13, J14, J15, J16, K10, K11, K14, K15, L8, L10, L13, L17, M9, M10, M11, M13, M16, N9, N10, N11, N12, N13, N14, N15, N16, P8, P10, P11, P12, P13, P14, P15, P17, R10, R11, R14, R15, T9, T10, T11, T12, T13, T14, T15, T16, U9, U11, U14, U15, U16, V15, V16, W15	vss	0	GND	-	-	-	-	-	-	-	-
AD1, A1, A2, B1	No Connect	-	-	-	-	-	-	-	-	-	-

2.4 Multiplexing Characteristics

Table 2-4 provides a description of the OMAP3530/25 multiplexing on the CBB, CBC, and CUS packages, respectively.

Note: The following does not take into account subsystem pin multiplexing options. Subsystem pin multiplexing options are described in Section 2.5, *Signal Description.*

Table 2-4. Multiplexing Characteristics

CBB		CBC		CUS	MODE 0	MODE 1	MODE 2	MODE 3	MODE 4	MODE 5	MODE 6	MODE 7
Bottom	Top	Bottom	Top									
D6	J2	NA	D1	D7	sdrc_d0							
C6	J1	NA	G1	C5	sdrc_d1							
B6	G2	NA	G2	C6	sdrc_d2							
C8	G1	NA	E1	B5	sdrc_d3							
C9	F2	NA	D2	D9	sdrc_d4							
A7	F1	NA	E2	D10	sdrc_d5							
B9	D2	NA	B3	C7	sdrc_d6							
A9	D1	NA	B4	B7	sdrc_d7							
C14	B13	NA	A10	B11	sdrc_d8							
B14	A13	NA	B11	C12	sdrc_d9							
C15	B14	NA	A11	B12	sdrc_d10							
B16	A14	NA	B12	D13	sdrc_d11							
D17	B16	NA	A16	C13	sdrc_d12							
C17	A16	NA	A17	B14	sdrc_d13							
B17	B19	NA	B17	A14	sdrc_d14							
D18	A19	NA	B18	B15	sdrc_d15							
D11	B3	NA	B7	C9	sdrc_d16							
B10	A3	NA	A5	E12	sdrc_d17							
C11	B5	NA	B6	B8	sdrc_d18							
D12	A5	NA	A6	B9	sdrc_d19							
C12	B8	NA	A8	C10	sdrc_d20							
A11	A8	NA	B9	B10	sdrc_d21							
B13	B9	NA	A9	D12	sdrc_d22							
D14	A9	NA	B10	E13	sdrc_d23							
C18	B21	NA	C21	E15	sdrc_d24							
A19	A21	NA	D20	D15	sdrc_d25							
B19	D22	NA	B19	C15	sdrc_d26							
B20	D23	NA	C20	B16	sdrc_d27							
D20	E22	NA	D21	C16	sdrc_d28							
A21	E23	NA	E20	D16	sdrc_d29							
B21	G22	NA	E21	B17	sdrc_d30							
C21	G23	NA	G21	B18	sdrc_d31							
H9	AB21	NA	AA18	C18	sdrc_ba0							
H10	AC21	NA	V20	D18	sdrc_ba1							
A4	N22	NA	G20	A4	sdrc_a0							
B4	N23	NA	K20	B4	sdrc_a1							
B3	P22	NA	J20	D6	sdrc_a2							
C5	P23	NA	J21	B3	sdrc_a3							
C4	R22	NA	U21	B2	sdrc_a4							
D5	R23	NA	R20	C3	sdrc_a5							
C3	T22	NA	M21	E3	sdrc_a6							
C2	T23	NA	M20	F6	sdrc_a7							
C1	U22	NA	N20	E10	sdrc_a8							
D4	U23	NA	K21	E9	sdrc_a9							
D3	V22	NA	Y16	E7	sdrc_a10							
D2	V23	NA	N21	G6	sdrc_a11							
D1	W22	NA	R21	G7	sdrc_a12							

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Table 2-4. Multiplexing Characteristics (continued)

CBB		CBC		CUS	MODE 0	MODE 1	MODE 2	MODE 3	MODE 4	MODE 5	MODE 6	MODE 7
Bottom	Top	Bottom	Top									
E2	W23	NA	AA15	F7	sdrc_a13							
E1	Y22	NA	Y12	F9	sdrc_a14							
H11	M22	NA	T21	A19	sdrc_ncs0							
H12	M23	NA	T20	B19	sdrc_ncs1							
A13	A11	NA	A12	A10	sdrc_clk							
A14	B11	NA	B13	A11	sdrc_nclk							
H16	J22	NA	Y15	B20	sdrc_cke0							safe_mode
H17	J23	NA	Y13	C20	sdrc_cke1							safe_mode
H14	L23	NA	V21	D19	sdrc_nras							
H13	L22	NA	U20	C19	sdrc_ncas							
H15	K23	NA	Y18	A20	sdrc_nwe							
B7	C1	NA	H1	B6	sdrc_dm0							
A16	A17	NA	A14	B13	sdrc_dm1							
B11	A6	NA	A4	A7	sdrc_dm2							
C20	A20	NA	A18	A16	sdrc_dm3							
A6	C2	NA	C2	A5	sdrc_dqs0							
A17	B17	NA	B15	A13	sdrc_dqs1							
A10	B6	NA	B8	A8	sdrc_dqs2							
A20	B20	NA	A19	A17	sdrc_dqs3							
N4	AC15	J2	NA	K4	gpmc_a1				gpio_34			safe_mode
M4	AB15	H1	NA	K3	gpmc_a2				gpio_35			safe_mode
L4	AC16	H2	NA	K2	gpmc_a3				gpio_36			safe_mode
K4	AB16	G2	NA	J4	gpmc_a4				gpio_37			safe_mode
T3	AC17	F1	NA	J3	gpmc_a5				gpio_38			safe_mode
R3	AB17	F2	NA	J2	gpmc_a6				gpio_39			safe_mode
N3	AC18	E1	NA	J1	gpmc_a7				gpio_40			safe_mode
M3	AB18	E2	NA	H1	gpmc_a8				gpio_41			safe_mode
L3	AC19	D1	NA	H2	gpmc_a9	sys_ndmareq 2			gpio_42			safe_mode
K3	AB19	D2	NA	G2	gpmc_a10	sys_ndmareq 3			gpio_43			safe_mode
K1	M2	AA2	U2	L2	gpmc_d0							
L1	M1	AA1	U1	M1	gpmc_d1							
L2	N2	AC2	V2	M2	gpmc_d2							
P2	N1	AC1	V1	N2	gpmc_d3							
T1	R2	AE5	AA3	M3	gpmc_d4							
V1	R1	AD6	AA4	P1	gpmc_d5							
V2	T2	AD5	Y3	P2	gpmc_d6							
W2	T1	AC5	Y4	R1	gpmc_d7							
H2	AB3	V1	R1	R2	gpmc_d8				gpio_44			safe_mode
K2	AC3	Y1	T1	T2	gpmc_d9				gpio_45			safe_mode
P1	AB4	T1	N1	U1	gpmc_d10				gpio_46			safe_mode
R1	AC4	U2	P2	R3	gpmc_d11				gpio_47			safe_mode
R2	AB6	U1	P1	T3	gpmc_d12				gpio_48			safe_mode
T2	AC6	P1	M1	U2	gpmc_d13				gpio_49			safe_mode
W1	AB7	L2	J2	V1	gpmc_d14				gpio_50			safe_mode
Y1	AC7	M2	K2	V2	gpmc_d15				gpio_51			safe_mode
G4	Y2	AD8	AA8	E2	gpmc_ncs0							
H3	Y1	AD1	W1	NA	gpmc_ncs1				gpio_52			safe_mode
V8	NA	A3	NA	NA	gpmc_ncs2				gpio_53			safe_mode
U8	NA	B6	NA	D2	gpmc_ncs3	sys_ndmareq 0			gpio_54			safe_mode
T8	NA	B4	NA	F4	gpmc_ncs4	sys_ndmareq 1	mcbsp4_clkx	gpt9_pwm_evt	gpio_55			safe_mode
R8	NA	C4	NA	G5	gpmc_ncs5	sys_ndmareq 2	mcbsp4_dr	gpt10_pwm_evt	gpio_56			safe_mode

Table 2-4. Multiplexing Characteristics (continued)

CBB		CBC		CUS	MODE 0	MODE 1	MODE 2	MODE 3	MODE 4	MODE 5	MODE 6	MODE 7
Bottom	Top	Bottom	Top									
P8	NA	B5	NA	F3	gpmc_ncs6	sys_ndmareq 3	mcbsp4_dx	gpt11_pwm_ evt	gpio_57			safe_mode
N8	NA	C5	NA	G4	gpmc_ncs7	gpmc_io_dir	mcbsp4_fsx	gpt8_pwm_e vt	gpio_58			safe_mode
T4	W2	N1	L1	W2	gpmc_clk				gpio_59			safe_mode
F3	W1	AD10	AA9	F1	gpmc_nadv_ ale							
G2	V2	N2	L2	F2	gpmc_noe							
F4	V1	M1	K1	G3	gpmc_nwe							
G3	AC12	K2	FT(1)	K5	gpmc_nbe0_ cle				gpio_60			safe_mode
U3	NA	J1	NA	L1	gpmc_nbe1				gpio_61			safe_mode
H1	AB10	AC6	Y5	E1	gpmc_nwp				gpio_62			safe_mode
M8	AB12	AC11	Y10	C1	gpmc_wait0							
L8	AC10	AC8	Y8	NA	gpmc_wait1				gpio_63			safe_mode
K8	NA	B3	NA	NA	gpmc_wait2				gpio_64			safe_mode
J8	NA	C6	NA	C2	gpmc_wait3	sys_ndmareq 1			gpio_65			safe_mode
D28	NA	G25	NA	G22	dss_pclk				gpio_66	hw_dbg12		safe_mode
D26	NA	K24	NA	E22	dss_hsync				gpio_67	hw_dbg13		safe_mode
D27	NA	M25	NA	F22	dss_vsync				gpio_68			safe_mode
E27	NA	F26	NA	J21	dss_acbias				gpio_69			safe_mode
AG22	NA	AE21	NA	AC19	dss_data0		uart1_cts	dssvenc656_ data0	gpio_70			safe_mode
AH22	NA	AE22	NA	AB19	dss_data1		uart1_rts	dssvenc656_ data1	gpio_71			safe_mode
AG23	NA	AE23	NA	AD20	dss_data2			dssvenc656_ data2	gpio_72			safe_mode
AH23	NA	AE24	NA	AC20	dss_data3			dssvenc656_ data3	gpio_73			safe_mode
AG24	NA	AD23	NA	AD21	dss_data4		uart3_rx_irrx	dssvenc656_ data4	gpio_74			safe_mode
AH24	NA	AD24	NA	AC21	dss_data5		uart3_tx_irtx	dssvenc656_ data5	gpio_75			safe_mode
E26	NA	G26	NA	D24	dss_data6		uart1_tx	dssvenc656_ data6	gpio_76	hw_dbg14		safe_mode
F28	NA	H25	NA	E23	dss_data7		uart1_rx	dssvenc656_ data7	gpio_77	hw_dbg15		safe_mode
F27	NA	H26	NA	E24	dss_data8				gpio_78	hw_dbg16		safe_mode
G26	NA	J26	NA	F23	dss_data9				gpio_79	hw_dbg17		safe_mode
AD28	NA	AC26	NA	AC22	dss_data10				gpio_80			safe_mode
AD27	NA	AD26	NA	AC23	dss_data11				gpio_81			safe_mode
AB28	NA	AA25	NA	AB22	dss_data12				gpio_82			safe_mode
AB27	NA	Y25	NA	Y22	dss_data13				gpio_83			safe_mode
AA28	NA	AA26	NA	W22	dss_data14				gpio_84			safe_mode
AA27	NA	AB26	NA	V22	dss_data15				gpio_85			safe_mode
G25	NA	L25	NA	J22	dss_data16				gpio_86			safe_mode
H27	NA	L26	NA	G23	dss_data17				gpio_87			safe_mode
H26	NA	M24	NA	G24	dss_data18		mcspi3_clk	dss_data0	gpio_88			safe_mode
H25	NA	M26	NA	H23	dss_data19		mcspi3_simo	dss_data1	gpio_89			safe_mode
E28	NA	F25	NA	D23	dss_data20		mcspi3_somi	dss_data2	gpio_90			safe_mode
J26	NA	N24	NA	K22	dss_data21		mcspi3_cs0	dss_data3	gpio_91			safe_mode
AC27	NA	AC25	NA	V21	dss_data22		mcspi3_cs1	dss_data4	gpio_92			safe_mode
AC28	NA	AB25	NA	W21	dss_data23			dss_data5	gpio_93			safe_mode
W28	NA	V26	NA	AA23	tv_out2							
Y28	NA	W26	NA	AB24	tv_out1							
Y27	NA	W25	NA	AB23	tv_vfb1							
W27	NA	U24	NA	Y23	tv_vfb2							
W26	NA	V23	NA	Y24	tv_vref							

(1) "FT" indicates Feed-Through. For more information, refer to Section 2.5.10.

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Table 2-4. Multiplexing Characteristics (continued)

CBB		CBC		CUS	MODE 0	MODE 1	MODE 2	MODE 3	MODE 4	MODE 5	MODE 6	MODE 7
Bottom	Top	Bottom	Top									
A24	NA	C23	NA	A22	cam_hs				gpio_94	hw_dbg0		safe_mode
A23	NA	D23	NA	E18	cam_vs				gpio_95	hw_dbg1		safe_mode
C25	NA	C25	NA	B22	cam_xclka				gpio_96			safe_mode
C27	NA	C26	NA	J19	cam_pclk				gpio_97	hw_dbg2		safe_mode
C23	NA	B23	NA	H24	cam_fld		cam_global_reset		gpio_98	hw_dbg3		safe_mode
AG17	NA	AE16	NA	AB18	cam_d0				gpio_99			safe_mode
AH17	NA	AE15	NA	AC18	cam_d1				gpio_100			safe_mode
B24	NA	A24	NA	G19	cam_d2				gpio_101	hw_dbg4		safe_mode
C24	NA	B24	NA	F19	cam_d3				gpio_102	hw_dbg5		safe_mode
D24	NA	D24	NA	G20	cam_d4				gpio_103	hw_dbg6		safe_mode
A25	NA	C24	NA	B21	cam_d5				gpio_104	hw_dbg7		safe_mode
K28	NA	P25	NA	L24	cam_d6				gpio_105			safe_mode
L28	NA	P26	NA	K24	cam_d7				gpio_106			safe_mode
K27	NA	N25	NA	J23	cam_d8				gpio_107			safe_mode
L27	NA	N26	NA	K23	cam_d9				gpio_108			safe_mode
B25	NA	D25	NA	F21	cam_d10				gpio_109	hw_dbg8		safe_mode
C26	NA	E26	NA	G21	cam_d11				gpio_110	hw_dbg9		safe_mode
B26	NA	E25	NA	C22	cam_xclkb				gpio_111			safe_mode
B23	NA	A23	NA	F18	cam_wen		cam_shutter		gpio_167	hw_dbg10		safe_mode
D25	NA	D26	NA	J20	cam_strobe				gpio_126	hw_dbg11		safe_mode
AG19	NA	AD17	NA	NA					gpio_112			safe_mode
AH19	NA	AD16	NA	NA					gpio_113			safe_mode
AG18	NA	AE18	NA	NA					gpio_114			safe_mode
AH18	NA	AE17	NA	NA					gpio_115			safe_mode
P21	NA	U18	NA	V20	mcbsp2_fsx				gpio_116			safe_mode
N21	NA	R18	NA	T21	mcbsp2_clkx				gpio_117			safe_mode
R21	NA	T18	NA	V19	mcbsp2_dr				gpio_118			safe_mode
M21	NA	R19	NA	R20	mcbsp2_dx				gpio_119			safe_mode
N28	NA	N19	NA	M23	mmc1_clk				gpio_120			safe_mode
M27	NA	L18	NA	L23	mmc1_cmd				gpio_121			safe_mode
N27	NA	M19	NA	M22	mmc1_dat0				gpio_122			safe_mode
N26	NA	M18	NA	M21	mmc1_dat1				gpio_123			safe_mode
N25	NA	K18	NA	M20	mmc1_dat2				gpio_124			safe_mode
P28	NA	N20	NA	N23	mmc1_dat3				gpio_125			safe_mode
P27	NA	M20	NA	N22	mmc1_dat4				gpio_126			safe_mode
P26	NA	P17	NA	N21	mmc1_dat5				gpio_127			safe_mode
R27	NA	P18	NA	N20	mmc1_dat6				gpio_128			safe_mode
R25	NA	P19	NA	P24	mmc1_dat7				gpio_129			safe_mode
AE2	NA	W10	NA	Y1	mmc2_clk	mcspi3_clk			gpio_130			safe_mode
AG5	NA	R10	NA	AB5	mmc2_cmd	mcspi3_simo			gpio_131			safe_mode
AH5	NA	T10	NA	AB3	mmc2_dat0	mcspi3_somi			gpio_132			safe_mode
AH4	NA	T9	NA	Y3	mmc2_dat1				gpio_133			safe_mode
AG4	NA	U10	NA	W3	mmc2_dat2	mcspi3_cs1			gpio_134			safe_mode
AF4	NA	U9	NA	V3	mmc2_dat3	mcspi3_cs0			gpio_135			safe_mode
AE4	NA	V10	NA	AB2	mmc2_dat4	mmc2_dir_dat0		mmc3_dat0	gpio_136			safe_mode
AH3	NA	M3	NA	AA2	mmc2_dat5	mmc2_dir_dat1	cam_global_reset	mmc3_dat1	gpio_137	hsusb3_tll_stp	mm3_rxdp	safe_mode
AF3	NA	L3	NA	Y2	mmc2_dat6	mmc2_dir_cmd	cam_shutter	mmc3_dat2	gpio_138	hsusb3_tll_dir		safe_mode
AE3	NA	K3	NA	AA1	mmc2_dat7	mmc2_clkin		mmc3_dat3	gpio_139	hsusb3_tll_nxt	mm3_rxdm	safe_mode
AF6	NA	P3	NA	V6	mcbsp3_dx	uart2_cts			gpio_140	hsusb3_tll_data4		safe_mode
AE6	NA	N3	NA	V5	mcbsp3_dr	uart2_rts			gpio_141	hsusb3_tll_data5		safe_mode

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Table 2-4. Multiplexing Characteristics (continued)

CBB		CBC		CUS	MODE 0	MODE 1	MODE 2	MODE 3	MODE 4	MODE 5	MODE 6	MODE 7
Bottom	Top	Bottom	Top									
AF5	NA	U3	NA	W4	mcbsp3_clkx	uart2_tx			gpio_142	hsusb3_tll_data6		safe_mode
AE5	NA	W3	NA	V4	mcbsp3_fsx	uart2_rx			gpio_143	hsusb3_tll_data7		safe_mode
AB26	NA	Y24	NA	NA	uart2_cts	mcbsp3_dx	gpt9_pwm_evt		gpio_144			safe_mode
AB25	NA	AA24	NA	NA	uart2_rts	mcbsp3_dr	gpt10_pwm_evt		gpio_145			safe_mode
AA25	NA	AD22	NA	NA	uart2_tx	mcbsp3_clkx	gpt11_pwm_evt		gpio_146			safe_mode
AD25	NA	AD21	NA	NA	uart2_rx	mcbsp3_fsx	gpt8_pwm_evt		gpio_147			safe_mode
AA8	NA	L4	NA	W7	uart1_tx				gpio_148			safe_mode
AA9	NA	R2	NA	W6	uart1_rts				gpio_149			safe_mode
W8	NA	W2	NA	AC2	uart1_cts				gpio_150	hsusb3_tll_clk		safe_mode
Y8	NA	H3	NA	V7	uart1_rx		mcbsp1_clkr	mcspi4_clk	gpio_151			safe_mode
AE1	NA	V3	NA	NA	mcbsp4_clkx				gpio_152	hsusb3_tll_data1	mm3_txse0	safe_mode
AD1	NA	U4	NA	NA	mcbsp4_dr				gpio_153	hsusb3_tll_data0	mm3_rxrcv	safe_mode
AD2	NA	R3	NA	NA	mcbsp4_dx				gpio_154	hsusb3_tll_data2	mm3_txdat	safe_mode
AC1	NA	T3	NA	NA	mcbsp4_fsx				gpio_155	hsusb3_tll_data3	mm3_txen_n	safe_mode
Y21	NA	U19	NA	W19	mcbsp1_clkr	mcspi4_clk			gpio_156			safe_mode
AA21	NA	V17	NA	AB20	mcbsp1_fsr		cam_global_reset		gpio_157			safe_mode
V21	NA	U17	NA	W18	mcbsp1_dx	mcspi4_simo	mcbsp3_dx		gpio_158			safe_mode
U21	NA	T20	NA	Y18	mcbsp1_dr	mcspi4_somi	mcbsp3_dr		gpio_159			safe_mode
T21	NA	T19	NA	AA18	mcbsp_clks		cam_shutter		gpio_160	uart1_cts		safe_mode
K26	NA	P20	NA	AA19	mcbsp1_fsx	mcspi4_cs0	mcbsp3_fsx		gpio_161			safe_mode
W21	NA	T17	NA	V18	mcbsp1_clkx		mcbsp3_clkx		gpio_162			safe_mode
H18	NA	F23	NA	A23	uart3_cts_rctx				gpio_163			safe_mode
H19	NA	F24	NA	B23	uart3_rts_sd				gpio_164			safe_mode
H20	NA	H24	NA	B24	uart3_rx_irrx				gpio_165			safe_mode
H21	NA	G24	NA	C23	uart3_tx_irtx				gpio_166			safe_mode
T28	NA	W19	NA	R21	hsusb0_clk				gpio_120			safe_mode
T25	NA	U20	NA	R23	hsusb0_stp				gpio_121			safe_mode
R28	NA	V19	NA	P23	hsusb0_dir				gpio_122			safe_mode
T26	NA	W18	NA	R22	hsusb0_nxt				gpio_124			safe_mode
T27	NA	V20	NA	T24	hsusb0_data0		uart3_tx_irtx		gpio_125			safe_mode
U28	NA	Y20	NA	T23	hsusb0_data1		uart3_rx_irrx		gpio_130			safe_mode
U27	NA	V18	NA	U24	hsusb0_data2		uart3_rts_sd		gpio_131			safe_mode
U26	NA	W20	NA	U23	hsusb0_data3		uart3_cts_rctx		gpio_169			safe_mode
U25	NA	W17	NA	W24	hsusb0_data4				gpio_188			safe_mode
V28	NA	Y18	NA	V23	hsusb0_data5				gpio_189			safe_mode
V27	NA	Y19	NA	W23	hsusb0_data6				gpio_190			safe_mode
V26	NA	Y17	NA	T22	hsusb0_data7				gpio_191			safe_mode
K21	NA	J25	NA	K20	i2c1_scl							
J21	NA	J24	NA	K21	i2c1_sda							
AF15	NA	C2	NA	AC15	i2c2_scl				gpio_168			safe_mode
AE15	NA	C1	NA	AC14	i2c2_sda				gpio_183			safe_mode
AF14	NA	AB4	NA	AC13	i2c3_scl				gpio_184			safe_mode

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Table 2-4. Multiplexing Characteristics (continued)

CBB		CBC		CUS	MODE 0	MODE 1	MODE 2	MODE 3	MODE 4	MODE 5	MODE 6	MODE 7
Bottom	Top	Bottom	Top									
AG14	NA	AC4	NA	AC12	i2c3_sda				gpio_185			safe_mode
AD26	NA	AD15	NA	Y16	i2c4_scl	sys_nvmode1						safe_mode
AE26	NA	W16	NA	Y15	i2c4_sda	sys_nvmode2						safe_mode
J25	NA	J23	NA	A24	hdq_sio	sys_altclk	i2c2_sccbe	i2c3_sccbe	gpio_170			safe_mode
AB3	NA	P9	NA	T5	mcspi1_clk	mmc2_dat4			gpio_171			safe_mode
AB4	NA	P8	NA	R4	mcspi1_simo	mmc2_dat5			gpio_172			safe_mode
AA4	NA	P7	NA	T4	mcspi1_somi	mmc2_dat6			gpio_173			safe_mode
AC2	NA	R7	NA	T6	mcspi1_cs0	mmc2_dat7			gpio_174			safe_mode
AC3	NA	R8	NA	NA	mcspi1_cs1			mmc3_cmd	gpio_175			safe_mode
AB1	NA	R9	NA	NA	mcspi1_cs2			mmc3_clk	gpio_176			safe_mode
AB2	NA	T8	NA	R5	mcspi1_cs3		hsusb2_tll_data2	hsusb2_data2	gpio_177	mm2_txdat		safe_mode
AA3	NA	W7	NA	N5	mcspi2_clk		hsusb2_tll_data7	hsusb2_data7	gpio_178			safe_mode
Y2	NA	W8	NA	N4	mcspi2_simo	gpt9_pwm_evt	hsusb2_tll_data4	hsusb2_data4	gpio_179			safe_mode
Y3	NA	U8	NA	N3	mcspi2_somi	gpt10_pwm_evt	hsusb2_tll_data5	hsusb2_data5	gpio_180			safe_mode
Y4	NA	V8	NA	M5	mcspi2_cs0	gpt11_pwm_evt	hsusb2_tll_data6	hsusb2_data6	gpio_181			safe_mode
V3	NA	V9	NA	M4	mcspi2_cs1	gpt8_pwm_evt	hsusb2_tll_data3	hsusb2_data3	gpio_182	mm2_txen_n		safe_mode
AE25	NA	AE20	NA	AA16	sys_32k							
AE17	NA	AF19	NA	AD15	sys_xtalin							
AF17	NA	AF20	NA	AD14	sys_xtalout							
AF25	NA	W15	NA	Y13	sys_clkreq				gpio_1			safe_mode
AF26	NA	V16	NA	W16	sys_nirq				gpio_0			safe_mode
AH25	NA	V13	NA	AA10	sys_nrespwron							
AF24	NA	AD7	NA	Y10	sys_nreswarm				gpio_30			safe_mode
AH26	NA	F3	NA	AB12	sys_boot0				gpio_2			safe_mode
AG26	NA	D3	NA	AC16	sys_boot1				gpio_3			safe_mode
AE14	NA	C3	NA	AD17	sys_boot2				gpio_4			safe_mode
AF18	NA	E3	NA	AD18	sys_boot3				gpio_5			safe_mode
AF19	NA	E4	NA	AC17	sys_boot4	mmc2_dir_dat2			gpio_6			safe_mode
AE21	NA	G3	NA	AB16	sys_boot5	mmc2_dir_dat3			gpio_7			safe_mode
AF21	NA	D4	NA	AA15	sys_boot6				gpio_8			safe_mode
AF22	NA	V12	NA	AD23	sys_off_mode				gpio_9			safe_mode
AG25	NA	AE14	NA	Y7	sys_clkout1				gpio_10			safe_mode
AE22	NA	W11	NA	AA6	sys_clkout2				gpio_186			safe_mode
AA17	NA	U15	NA	AB7	jtag_ntrst							
AA13	NA	V14	NA	AB6	jtag_tck							
AA12	NA	W13	NA	AA7	jtag_rtck							
AA18	NA	V15	NA	AA9	jtag_tms_tmsc							
AA20	NA	U16	NA	AB10	jtag_tdi							
AA19	NA	Y13	NA	AB9	jtag_tdo							
AA11	NA	Y15	NA	AC24	jtag_emu0				gpio_11			safe_mode
AA10	NA	Y14	NA	AD24	jtag_emu1				gpio_31			safe_mode
AF10	NA	AB2	NA	AC1	etk_clk	mcbsp5_clkx	mmc3_clk	hsusb1_stp	gpio_12	mm1_rxdp	hsusb1_tll_stp	hw_dbg0
AE10	NA	AB3	NA	AD3	etk_ctl		mmc3_cmd	hsusb1_clk	gpio_13		hsusb1_tll_clk	hw_dbg1
AF11	NA	AC3	NA	AD6	etk_d0	mcspi3_simo	mmc3_dat4	hsusb1_data0	gpio_14	mm1_rxrcv	hsusb1_tll_data0	hw_dbg2

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Table 2-4. Multiplexing Characteristics (continued)

CBB		CBC		CUS	MODE 0	MODE 1	MODE 2	MODE 3	MODE 4	MODE 5	MODE 6	MODE 7
Bottom	Top	Bottom	Top									
AG12	NA	AD4	NA	AC6	etk_d1	mcspi3_somi		hsusb1_data1	gpio_15	mm1_txse0	hsusb1_tll_data1	hw_dbg3
AH12	NA	AD3	NA	AC7	etk_d2	mcspi3_cs0		hsusb1_data2	gpio_16	mm1_txdat	hsusb1_tll_data2	hw_dbg4
AE13	NA	AA3	NA	AD8	etk_d3	mcspi3_clk	mmc3_dat3	hsusb1_data7	gpio_17		hsusb1_tll_data7	hw_dbg5
AE11	NA	Y3	NA	AC5	etk_d4	mcbsp5_dr	mmc3_dat0	hsusb1_data4	gpio_18		hsusb1_tll_data4	hw_dbg6
AH9	NA	AB1	NA	AD2	etk_d5	mcbsp5_fsx	mmc3_dat1	hsusb1_data5	gpio_19		hsusb1_tll_data5	hw_dbg7
AF13	NA	AE3	NA	AC8	etk_d6	mcbsp5_dx	mmc3_dat2	hsusb1_data6	gpio_20		hsusb1_tll_data6	hw_dbg8
AH14	NA	AD2	NA	AD9	etk_d7	mcspi3_cs1	mmc3_dat7	hsusb1_data3	gpio_21	mm1_txen_n	hsusb1_tll_data3	hw_dbg9
AF9	NA	AA4	NA	AC4	etk_d8	sys_drm_msecure	mmc3_dat6	hsusb1_dir	gpio_22		hsusb1_tll_dir	hw_dbg10
AG9	NA	V2	NA	AD5	etk_d9	sys_secure_indicator	mmc3_dat5	hsusb1_nxt	gpio_23	mm1_rxdm	hsusb1_tll_nxt	hw_dbg11
AE7	NA	AE4	NA	AC3	etk_d10		uart1_rx	hsusb2_clk	gpio_24		hsusb2_tll_clk	hw_dbg12
AF7	NA	AF6	NA	AC9	etk_d11			hsusb2_stp	gpio_25	mm2_rxdp	hsusb2_tll_stp	hw_dbg13
AG7	NA	AE6	NA	AC10	etk_d12			hsusb2_dir	gpio_26		hsusb2_tll_dir	hw_dbg14
AH7	NA	AF7	NA	AD11	etk_d13			hsusb2_nxt	gpio_27	mm2_rxdm	hsusb2_tll_nxt	hw_dbg15
AG8	NA	AF9	NA	AC11	etk_d14			hsusb2_data0	gpio_28	mm2_rxrcv	hsusb2_tll_data0	hw_dbg16
AH8	NA	AE9	NA	AD12	etk_d15			hsusb2_data1	gpio_29	mm2_txse0	hsusb2_tll_data1	hw_dbg17
AC4, J4, H4, D8, AE9, D9, D15, Y16, AE18, Y18, W18, K18, J18, AE19, Y19, U19, T19, N19, M19, J19, Y20, W20, V20, U20, P20, N20, K20, J20, D22, D23, AE24, M25, L25, E25	NA	AC21, D15, G11, G18, H20, M7, M17, R20, T7, Y8, Y12	NA	F12, F13, G12, G13, H12, H13, J17, J18, K17, K18, K19, L14, L15, M14, M15, R17, R18, R19, T17, T18, T19, T20	vdd_core							
Y9, W9, T9, R9, M9, L9, J9, Y10, U10, T10, R10, N10, M10, L10, J10, Y11, W11, K11, J11, W12, K13, Y14, K14, J14, Y15, W15, J15	NA	D13, G9, G12, H7, K11, L9, M9, M10, N7, N8, P10, U7, U11, U13, V7, V11, W9, Y9, Y11	NA	F10, G9, G10, H9, H10, J9, J10, L11, L12, M6, M7, M8, M12, N6, N7, N8, R6, R7, R8, T7, T8, U12, U13, V12, V13, W12, W13	vdd_mpu_iva							
AA15	NA	K14	NA	Y12	cap_vdd_wkup							
K15	NA	K13	NA	G18	vdds_dpll_dll							
W16	NA	U12	NA	AA12	vdds_sram							
AD3, AD4, W4, AF8, AE8, AF16, AE16, AF23, AE23, F25, F26, AG27	NA	A18, AC7, AC15, AC18, AC24, AD20, AE10, C11, D9, E24, G4, J15, J18, L7, L24, M4, T4, T24, W24, Y4, L20, AB24, AD18, AD19	NA	M17, M18, M19, N17, N18, N19, U10, V9, V10, W9, W10, Y9	vdds							

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Table 2-4. Multiplexing Characteristics (continued)

CBB		CBC		CUS	MODE 0	MODE 1	MODE 2	MODE 3	MODE 4	MODE 5	MODE 6	MODE 7
Bottom	Top	Bottom	Top									
U1, J1, F1, J2, F2, R4, B5, A5, AH6, B8, A8, B12, A12, D16, C16, B18, A18, B22, A22, G28, C28	NA		NA	E16, F15, F16, G15, G16, H15, J6, J7, J8, K6, K7, K8	vdds_mem							
AA16	NA	U14	NA	U17	vdds_dpll_per							
AA14	NA	W14	NA	AA13	vdds_wkup_bg							
AG2, U2, B2, AG3, W3, P3, J3, E3, A3, P4, E4, AG6, D7, C7, V9, U9, P9, N9, K9, W10, V10, P10, K10, D10, C10, AF12, AE12, Y12, K12, J12, Y13, W13, J13, D13, C13, W14, K16, J16, Y17, W17, K17, J17, W19, V19, R19, P19, L19, K19, D19, C19, AF20, AE20, T20, R2	NA	A6, A8, A13, AB5, AB22, AC10, AC16, AC19, AD14, AD25,AE7, AF23, B2, B25, C12, D7, D10, D12, D14, D18, D20, E22, G1, G8, G10, G20, G23, H4, K1, K15, K25, L10, L17, L19, L23, N4, N10, N17, R1, R4, R17, T23, U25, W1, W4, W23, Y7, Y10, Y16, Y26	NA	H11, H14, H16, J11, J12, J13, J14, J15, J16, K10, K11, K14, K15, L8, L10, L13, L17, M9, M10, M11, M13, M16, N9, N10, N11, N12, N13, N14, N15, N16, P8, P10, P11, P12, P13, P14, P15, P17, R10, R11, R14, R15, T9, T10, T11, T12, T13, T14, T15, T16, U9, U11, U14, U15, U16, V15, V16, W15	vss							
V25	NA	V25	NA	AB13	vdda_dac							
Y26	NA	V24	NA	AB15	vssa_dac							
K25	NA	N23	NA	N24	vdds_mmc1							
P25	NA	P23	NA	H8	vdds_mmc1a							
AA26	NA	Y26	NA	NA	vss							
AE27	NA	AB24	NA	NA	vdds							
AG21	NA	AD19	NA	NA	vdds							
AH20	NA	AE19	NA	NA	cap_vdd_d							
AH21	NA	AC19	NA	NA	vss							
AG16	NA	NA	NA	NA	vss							
AG20	NA	NA	NA	NA	vdds							
M28	NA	L19	NA	NA	vss							
H28	NA	L20	NA	NA	vdds							
V4	NA	N9	NA	U8	cap_vdd_sram_mpu _iva							
L21	NA	K20	NA	H17	cap_vdd_sram_core							

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2.5 Signal Description

Many signals are available on multiple pins according to the software configuration of the pin multiplexing options.

1. **SIGNAL NAME:** The signal name
2. **DESCRIPTION:** Description of the signal
3. **TYPE:** Type = Ball type for this specific function:
   - I = Input
   - O = Output
   - Z = High-impedance
   - D = Open Drain
   - DS = Differential
   - A = Analog
4. **BALL BOTTOM:** Associated ball(s) bottom
5. **BALL TOP:** Associated ball(s) top
6. **SUBSYSTEM PIN MULTIPLEXING:** Contains a list of the pin multiplexing options at the module/subsystem level. The pin function is selected at the module/system level.

   Note: The Subsystem Multiplexing Signals are not described in the following tables.

2.5.1 External Memory Interfaces

Table 2-5. External Memory Interfaces – GPMC Signals Description

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM (CBB Pkg.) [4]	BALL TOP (CBB Pkg.) [5]	BALL BOTTOM (CBC Pkg.) [4]	BALL TOP (CBC Pkg.) [5]	BALL BOTTOM (CUS Pkg.) [4]	SUBSYSTEM PIN MULTIPLEXING [6]
gpmc_a1	General-purpose memory address bit 1	O	N4 / K1	AC15 / M2	J2 / AA2	NA / U2	K4/ L2	/ gpmc_d0
gpmc_a2	General-purpose memory address bit 2	O	M4 / L1	AB15 / M1	H1 / AA1	NA / U1	K3/ M1	gpmc_a18/ gpmc_d1
gpmc_a3	General-purpose memory address bit 3	O	L4 / L2	AC16 / N2	H2 / AC2	NA / V2	K2/ M2	gpmc_a19/ gpmc_d2
gpmc_a4	General-purpose memory address bit 4	O	K4 / P2	AB16 / N1	G2 / AC1	NA / V1	J4/ N2	gpmc_a20/ gpmc_d3
gpmc_a5	General-purpose memory address bit 5	O	T3 / T1	AC17 / R2	F1 / AE5	NA / AA3	J3/ M3	gpmc_a21/ gpmc_d4
gpmc_a6	General-purpose memory address bit 6	O	R3 / V1	AB17 / R1	F2 / AD6	NA / AA4	J2/ P1	gpmc_a22/ gpmc_d5
gpmc_a7	General-purpose memory address bit 7	O	N3 / V2	AC18 / T2	E1 / AD5	NA / Y3	J1/ P2	gpmc_a23/ gpmc_d6
gpmc_a8	General-purpose memory address bit 8	O	M3 / W2	AB18 / T1	E2 / AC5	NA / Y4	H1/ R1	gpmc_a24/ gpmc_d7
gpmc_a9	General-purpose memory address bit 9	O	L3 / H2	AC19 / AB3	D1 / V1	NA / R1	H2/ R2	gpmc_a25/ gpmc_d8
gpmc_a10	General-purpose memory address bit 10	O	K3 / K2	AB19 / AC3	D2 / Y1	T1	G2/ T2	gpmc_a26/ gpmc_d9
gpmc_a11	General-purpose memory address bit 11	O	P1	AB4	T1	N1	U1	gpmc_d10
gpmc_a12	General-purpose memory address bit 12	O	R1	AC4	U2	P2	R3	gpmc_d11
gpmc_a13	General-purpose memory address bit 13	O	R2	AB6	U1	P1	T3	gpmc_d12
gpmc_a14	General-purpose memory address bit 14	O	T2	AC6	P1	M1	U2	gpmc_d13
gpmc_a15	General-purpose memory address bit 15	O	W1	AB7	L2	J2	V1	gpmc_d14
gpmc_a16	General-purpose memory address bit 16	O	Y1	AC7	M2	K2	V2	gpmc_d15

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Table 2-5. External Memory Interfaces – GPMC Signals Description (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM (CBB Pkg.) [4]	BALL TOP (CBB Pkg.) [5]	BALL BOTTOM (CBC Pkg.) [4]	BALL TOP (CBC Pkg.) [5]	BALL BOTTOM (CUS Pkg.) [4]	SUBSYSTEM PIN MULTIPLEXING [6]
gpmc_a17	General-purpose memory address bit 17	O	N4	AC15	J2	NA	K4	gpmc_a1
gpmc_a18	General-purpose memory address bit 18	O	M4	AB15	H1	NA	K3	gpmc_a2
gpmc_a19	General-purpose memory address bit 19	O	L4	AC16	H2	NA	K2	gpmc_a3
gpmc_a20	General-purpose memory address bit 20	O	K4	AB16	G2	NA	J4	gpmc_a4
gpmc_a21	General-purpose memory address bit 21	O	T3	AC17	F1	NA	J3	gpmc_a5
gpmc_a22	General-purpose memory address bit 22	O	R3	AB17	F2	NA	J2	gpmc_a6
gpmc_a23	General-purpose memory address bit 23	O	N3	AC18	E1	NA	J1	gpmc_a7
gpmc_a24	General-purpose memory address bit 24	O	M3	AB18	E2	NA	H1	gpmc_a8
gpmc_a25	General-purpose memory address bit 25	O	L3	AC19	D1	NA	H2	gpmc_a9
gpmc_a26	General-purpose memory address bit 26	O	K3	AB19	D2	NA	G2	gpmc_a10
gpmc_d0	GPMC Data bit 0	IO	K1	M2	AA2	U2	L2	gpmc_a1/ gpmc_d0
gpmc_d1	GPMC Data bit 1	IO	L1	M1	AA1	U1	M1	gpmc_a2/ gpmc_d1
gpmc_d2	GPMC Data bit 2	IO	L2	N2	AC2	V2	M2	gpmc_a3/ gpmc_d2
gpmc_d3	GPMC Data bit 3	IO	P2	N1	AC1	V1	N2	gpmc_a4/ gpmc_d3
gpmc_d4	GPMC Data bit 4	IO	T1	R2	AE5	AA3	M3	gpmc_a5/ gpmc_d4
gpmc_d5	GPMC Data bit 5	IO	V1	R1	AD6	AA4	P1	gpmc_a6/ gpmc_d5
gpmc_d6	GPMC Data bit 6	IO	V2	T2	AD5	Y3	P2	gpmc_a7 /gpmc_d6
gpmc_d7	GPMC Data bit 7	IO	W2	T1	AC5	Y4	R1	gpmc_a8/ gpmc_d7
gpmc_d8	GPMC Data bit 8	IO	H2	AB3	V1	R1	R2	gpmc_a9/ gpmc_d8
gpmc_d9	GPMC Data bit 9	IO	K2	AC3	Y1	T1	T2	gpmc_a10/ gpmc_d9
gpmc_d10	GPMC Data bit 10	IO	P1	AB4	T1	N1	U1	gpmc_a11/ gpmc_d10
gpmc_d11	GPMC Data bit 11	IO	R1	AC4	U2	P2	R3	gpmc_a12/ gpmc_d11
gpmc_d12	GPMC Data bit 12	IO	R2	AB6	U1	P1	T3	gpmc_a13/ gpmc_d12
gpmc_d13	GPMC Data bit 13	IO	T2	AC6	P1	M1	U2	gpmc_a14/ gpmc_d13
gpmc_d14	GPMC Data bit 14	IO	W1	AB7	L2	J2	V1	gpmc_a15/ gpmc_d14
gpmc_d15	GPMC Data bit 15	IO	Y1	AC7	M2	K2	V2	gpmc_a16/ gpmc_d15
gpmc_ncs0	GPMC Chip Select bit 0	O	G4	Y2	AD8	AA8	E2	NA
gpmc_ncs1	GPMC Chip Select bit 1	O	H3	Y1	AD1	W1	NA	NA
gpmc_ncs2	GPMC Chip Select bit 2	O	V8	NA	A3	NA	NA	NA
gpmc_ncs3	GPMC Chip Select bit 3	O	U8	NA	B6	NA	D2	NA
gpmc_ncs4	GPMC Chip Select bit 4	O	T8	NA	B4	NA	F4	NA
gpmc_ncs5	GPMC Chip Select bit 5	O	R8	NA	C4	NA	G5	NA

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Table 2-5. External Memory Interfaces – GPMC Signals Description (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM (CBB Pkg.) [4]	BALL TOP (CBB Pkg.) [5]	BALL BOTTOM (CBC Pkg.) [4]	BALL TOP (CBC Pkg.) [5]	BALL BOTTOM (CUS Pkg.) [4]	SUBSYSTEM PIN MULTIPLEXING [6]
gpmc_ncs6	GPMC Chip Select bit 6	O	P8	NA	B5	NA	F3	NA
gpmc_ncs7	GPMC Chip Select bit 7	O	N8	NA	C5	NA	G4	NA
gpmc_io_dir	GPMC IO direction control for use with external transceivers	O	N8	NA	C5	NA	G4	NA
gpmc_clk	GPMC clock	O	T4	W2	N1	L1	W2	NA
gpmc_nadv_ale	Address Valid or Address Latch Enable	O	F3	W1	AD10	AA9	F1	NA
gpmc_noe	Output Enable	O	G2	V2	N2	L2	F2	NA
gpmc_nwe	Write Enable	O	F4	V1	M1	K1	G3	NA
gpmc_nbe0_cle	Lower Byte Enable. Also used for Command Latch Enable	O	G3	AC12	K2	FT(1)	K5	NA
gpmc_nbe1	Upper Byte Enable	O	U3	NA	J1	NA	L1	NA
gpmc_nwp	Flash Write Protect	O	H1	AB10	AC6	Y5	E1	NA
gpmc_wait0	External indication of wait	I	M8	AB12	AC11	Y10	C1	NA
gpmc_wait1	External indication of wait	I	L8	AC10	AC8	Y8	NA	NA
gpmc_wait2	External indication of wait	I	K8	NA	B3	NA	NA	NA
gpmc_wait3	External indication of wait	I	J8	NA	C6	NA	C2	NA

(1) FT indicates "Feed-Through. For more information, refer to Section 2.5.10.

Table 2-6. External Memory Interfaces – SDRC Signals Description

SIGNAL NAME	DESCRIPTION	TYPE(1)	BALL BOTTOM (CBB Pkg.)	BALL TOP (CBB Pkg.)	BALL BOTTOM (CBC Pkg.)	BALL TOP (CBC Pkg.)	BALL BOTTOM (CUS Pkg.)
sdrc_d0	SDRAM data bit 0	IO	D6	J2	NA	D1	D7
sdrc_d1	SDRAM data bit 1	IO	C6	J1	NA	G1	C5
sdrc_d2	SDRAM data bit 2	IO	B6	G2	NA	G2	C6
sdrc_d3	SDRAM data bit 3	IO	C8	G1	NA	E1	B5
sdrc_d4	SDRAM data bit 4	IO	C9	F2	NA	D2	D9
sdrc_d5	SDRAM data bit 5	IO	A7	F1	NA	E2	D10
sdrc_d6	SDRAM data bit 6	IO	B9	D2	NA	B3	C7
sdrc_d7	SDRAM data bit 7	IO	A9	D1	NA	B4	B7
sdrc_d8	SDRAM data bit 8	IO	C14	B13	NA	A10	B11
sdrc_d9	SDRAM data bit 9	IO	B14	A13	NA	B11	C12
sdrc_d10	SDRAM data bit 10	IO	C15	B14	NA	A11	B12
sdrc_d11	SDRAM data bit 11	IO	B16	A14	NA	B12	D13
sdrc_d12	SDRAM data bit 12	IO	D17	B16	NA	A16	C13
sdrc_d13	SDRAM data bit 13	IO	C17	A16	NA	A17	B14
sdrc_d14	SDRAM data bit 14	IO	B17	B19	NA	B17	A14
sdrc_d15	SDRAM data bit 15	IO	D18	A19	NA	B18	B15
sdrc_d16	SDRAM data bit 16	IO	D11	B3	NA	B7	C9
sdrc_d17	SDRAM data bit 17	IO	B10	A3	NA	A5	E12
sdrc_d18	SDRAM data bit 18	IO	C11	B5	NA	B6	B8
sdrc_d19	SDRAM data bit 19	IO	D12	A5	NA	A6	B9
sdrc_d20	SDRAM data bit 20	IO	C12	B8	NA	A8	C10
sdrc_d21	SDRAM data bit 21	IO	A11	A8	NA	B9	B10
sdrc_d22	SDRAM data bit 22	IO	B13	B9	NA	A9	D12
sdrc_d23	SDRAM data bit 23	IO	D14	A9	NA	B10	E13
sdrc_d24	SDRAM data bit 24	IO	C18	B21	NA	C21	E15
sdrc_d25	SDRAM data bit 25	IO	A19	A21	NA	D20	D15
sdrc_d26	SDRAM data bit 26	IO	B19	D22	NA	B19	C15

(1) Type = Ball type for this specific function (I = Input, O = Output, Z = high-impedance, D = Open Drain, DS = Differential, A = Analog).

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Table 2-6. External Memory Interfaces – SDRC Signals Description (continued)

SIGNAL NAME	DESCRIPTION	TYPE[1]	BALL BOTTOM (CBB Pkg.)	BALL TOP (CBB Pkg.)	BALL BOTTOM (CBC Pkg.)	BALL TOP (CBC Pkg.)	BALL BOTTOM (CUS Pkg.)
sdrc_d27	SDRAM data bit 27	IO	B20	D23	NA	C20	B16
sdrc_d28	SDRAM data bit 28	IO	D20	E22	NA	D21	C16
sdrc_d29	SDRAM data bit 29	IO	A21	E23	NA	E20	D16
sdrc_d30	SDRAM data bit 30	IO	B21	G22	NA	E21	B17
sdrc_d31	SDRAM data bit 31	IO	C21	G23	NA	G21	B18
sdrc_ba0	SDRAM bank select 0	O	H9	AB21	NA	AA18	C18
sdrc_ba1	SDRAM bank select 1	O	H10	AC21	NA	V20	D18
sdrc_a0	SDRAM address bit 0	O	A4	N22	NA	G20	A4
sdrc_a1	SDRAM address bit 1	O	B4	N23	NA	K20	B4
sdrc_a2	SDRAM address bit 2	O	B3	P22	NA	J20	D6
sdrc_a3	SDRAM address bit 3	O	C5	P23	NA	J21	B3
sdrc_a4	SDRAM address bit 4	O	C4	R22	NA	U21	B2
sdrc_a5	SDRAM address bit 5	O	D5	R23	NA	R20	C3
sdrc_a6	SDRAM address bit 6	O	C3	T22	NA	M21	E3
sdrc_a7	SDRAM address bit 7	O	C2	T23	NA	M20	F6
sdrc_a8	SDRAM address bit 8	O	C1	U22	NA	N20	E10
sdrc_a9	SDRAM address bit 9	O	D4	U23	NA	K21	E9
sdrc_a10	SDRAM address bit 10	O	D3	V22	NA	Y16	E7
sdrc_a11	SDRAM address bit 11	O	D2	V23	NA	N21	G6
sdrc_a12	SDRAM address bit 12	O	D1	W22	NA	R21	G7
sdrc_a13	SDRAM address bit 13	O	E2	W23	NA	AA15	F7
sdrc_a14	SDRAM address bit 14	O	E1	Y22	NA	Y12	F9
sdrc_ncs0	Chip select 0	O	H11	M22	NA	T21	A19
sdrc_ncs1	Chip select 1	O	H12	M23	NA	T20	B19
sdrc_clk	Clock	IO	A13	A11	NA	A12	A10
sdrc_nclk	Clock Invert	O	A14	B11	NA	B13	A11
sdrc_cke0	Clock Enable 0	O	H16	J22	NA	Y15	B20
sdrc_cke1	Clock Enable 1	O	H17	J23	NA	Y13	C20
sdrc_nras	SDRAM Row Access	O	H14	L23	NA	V21	D19
sdrc_ncas	SDRAM column address strobe	O	H13	L22	NA	U20	C19
sdrc_nwe	SDRAM write enable	O	H15	K23	NA	Y18	A20
sdrc_dm0	Data Mask 0	O	B7	C1	NA	H1	B6
sdrc_dm1	Data Mask 1	O	A16	A17	NA	A14	B13
sdrc_dm2	Data Mask 2	O	B11	A6	NA	A4	A7
sdrc_dm3	Data Mask 3	O	C20	A20	NA	A18	A16
sdrc_dqs0	Data Strobe 0	IO	A6	C2	NA	C2	A5
sdrc_dqs1	Data Strobe 1	IO	A17	B17	NA	B15	A13
sdrc_dqs2	Data Strobe 2	IO	A10	B6	NA	B8	A8
sdrc_dqs3	Data Strobe 3	IO	A20	B20	NA	A19	A17

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2.5.2 Video Interfaces

Table 2-7. Video Interfaces – CAM Signals Description

SIGNAL NAME	DESCRIPTION	TYPE(1)	BALL BOTTOM (CBB Pkg.)	BALL BOTTOM (CBC Pkg.)	BALL BOTTOM (CUS Pkg.)
cam_hs	Camera Horizontal Synchronization	IO	A24	C23	A22
cam_vs	Camera Vertical Synchronization	IO	A23	D23	E18
cam_xclka	Camera Clock Output a	O	C25	C25	B22
cam_xclkb	Camera Clock Output b	O	B26	E25	C22
cam_d0	Camera digital image data bit 0	I	AG17	AE16	AB18
cam_d1	Camera digital image data bit 1	I	AH17	AE15	AC18
cam_d2	Camera digital image data bit 2	I	B24	A24	G19
cam_d3	Camera digital image data bit 3	I	C24	B24	F19
cam_d4	Camera digital image data bit 4	I	D24	D24	G20
cam_d5	Camera digital image data bit 5	I	A25	C24	B21
cam_d6	Camera digital image data bit 6	I	K28	P25	L24
cam_d7	Camera digital image data bit 7	I	L28	P26	K24
cam_d8	Camera digital image data bit 8	I	K27	N25	J23
cam_d9	Camera digital image data bit 9	I	L27	N26	K23
cam_d10	Camera digital image data bit 10	I	B25	D25	F21
cam_d11	Camera digital image data bit 11	I	C26	E26	G21
cam_fld	Camera field identification	IO	C23	B23	H24
cam_pclk	Camera pixel clock	I	C27	C26	J19
cam_wen	Camera Write Enable	I	B23	A23	F18
cam_strobe	Flash strobe control signal	O	D25	D26	J20
cam_global_reset	Global reset is used strobe synchronization	IO	C23 / AH3 / AA21	B23/M3/V17	H24/ AA2/ AB20
cam_shutter	Mechanical shutter control signal	O	B23 / AF3 / T21	A23 / T19	F18/ Y2/ AA18

(1) Type = Ball type for this specific function (I = Input, O = Output, Z = high-impedance, D = Open Drain, DS = Differential, A = Analog).

Table 2-8. Video Interfaces – DSS Signals Description

SIGNAL NAME	DESCRIPTION	TYPE(1)	BALL BOTTOM (CBB Pkg.)	BALL BOTTOM (CBC Pkg.)	BALL BOTTOM (CUS Pkg.)
dss_pclk	LCD Pixel Clock	O	D28	G25	G22
dss_hsync	LCD Horizontal Synchronization	O	D26	K24	E22
dss_vsync	LCD Vertical Synchronization	O	D27	M25	F22
dss_acbias	AC bias control (STN) or pixel data enable (TFT) output	O	E27	F26	J21
dss_data0	LCD Pixel Data bit 0	IO	AG22 / H26	AE21 / M24	AC19/G24
dss_data1	LCD Pixel Data bit 1	IO	AH22 / H25	AE22 / M26	AB19/H23
dss_data2	LCD Pixel Data bit 2	IO	AG23 / E28	AE23 / F25	AD20/D23
dss_data3	LCD Pixel Data bit 3	IO	AH23 / J26	AE24 / N24	AC20/K22
dss_data4	LCD Pixel Data bit 4	IO	AG24 / AC27	AD23 / AC25	AD21/V21
dss_data5	LCD Pixel Data bit 5	IO	AH24 / AC28	AD24/ AB25	AC21/W21
dss_data6	LCD Pixel Data bit 6	IO	E26	G26	D24
dss_data7	LCD Pixel Data bit 7	IO	F28	H25	E23
dss_data8	LCD Pixel Data bit 8	IO	F27	H26	E24
dss_data9	LCD Pixel Data bit 9	IO	G26	J26	F23
dss_data10	LCD Pixel Data bit 10	IO	AD28	AC26	AC22
dss_data11	LCD Pixel Data bit 11	IO	AD27	AD26	AC23
dss_data12	LCD Pixel Data bit 12	IO	AB28	AA25	AB22
dss_data13	LCD Pixel Data bit 13	IO	AB27	Y25	Y22
dss_data14	LCD Pixel Data bit 14	IO	AA28	AA26	W22

(1) Type = Ball type for this specific function (I = Input, O = Output, Z = high-impedance, D = Open Drain, DS = Differential, A = Analog).

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Table 2-8. Video Interfaces – DSS Signals Description (continued)

SIGNAL NAME	DESCRIPTION	TYPE(1)	BALL BOTTOM (CBB Pkg.)	BALL BOTTOM (CBC Pkg.)	BALL BOTTOM (CUS Pkg.)
dss_data15	LCD Pixel Data bit 15	IO	AA27	AB26	V22
dss_data16	LCD Pixel Data bit 16	IO	G25	L25	J22
dss_data17	LCD Pixel Data bit 17	IO	H27	L26	G23
dss_data18	LCD Pixel Data bit 18	IO	H26	M24	G24
dss_data19	LCD Pixel Data bit 19	IO	H25	M26	H23
dss_data20	LCD Pixel Data bit 20	O	E28	F25	D23
dss_data21	LCD Pixel Data bit 21	O	J26	N24	K22
dss_data22	LCD Pixel Data bit 22	O	AC27	AC25	V21
dss_data23	LCD Pixel Data bit 23	O	AC28	AB25	W21

Table 2-9. Video Interfaces – RFBI Signals Description

SIGNAL NAME	DESCRIPTION	TYPE(1)	BALL BOTTOM (CBB Pkg.)	BALL BOTTOM (CBC Pkg.)	BALL BOTTOM (CUS Pkg.)	SUBSYSTEM PIN MULTIPLEXING(2)
rfbi_a0	RFBI command/data control	O	E27	F26	J21	dss_acbias
rfbi_cs0	1st LCD chip select	O	D26	K24	E22	dss_hsync
rfbi_da0	RFBI data bus 0	IO	AG22	AE21	AC19	dss_data0
rfbi_da1	RFBI data bus 1	IO	AH22	AE22	AB19	dss_data1
rfbi_da2	RFBI data bus 2	IO	AG23	AE23	AD20	dss_data2
rfbi_da3	RFBI data bus 3	IO	AH23	AE24	AC20	dss_data3
rfbi_da4	RFBI data bus 4	IO	AG24	AD23	AD21	dss_data4
rfbi_da5	RFBI data bus 5	IO	AH24	AD24	AC21	dss_data5
rfbi_da6	RFBI data bus 6	IO	E26	G26	D24	dss_data6
rfbi_da7	RFBI data bus 7	IO	F28	H25	E23	dss_data7
rfbi_da8	RFBI data bus 8	IO	F27	H26	E24	dss_data8
rfbi_da9	RFBI data bus 9	IO	G26	J26	F23	dss_data9
rfbi_da10	RFBI data bus 10	IO	AD28	AC26	AC22	dss_data10
rfbi_da11	RFBI data bus 11	IO	AD27	AD26	AC23	dss_data11
rfbi_da12	RFBI data bus 12	IO	AB28	AA25	AB22	dss_data12
rfbi_da13	RFBI data bus 13	IO	AB27	Y25	Y22	dss_data13
rfbi_da14	RFBI data bus 14	IO	AA28	AA26	W22	dss_data14
rfbi_da15	RFBI data bus 15	IO	AA27	AB26	V22	dss_data15
rfbi_rd	Read enable for RFBI	O	D28	G25	G22	dss_pclk
rfbi_wr	Write Enable for RFBI	O	D27	M25	F22	dss_vsync
rfbi_te_vsync 0	tearing effect removal and Vsync input from 1st LCD	I	G25	L25	J22	dss_data16
rfbi_hsync0	Hsync for 1st LCD	I	H27	L26	G23	dss_data17
rfbi_te_vsync 1	tearing effect removal and Vsync input from 2nd LCD	I	H26	M24	G24	dss_data18
rfbi_hsync1	Hsync for 2nd LCD	I	H25	M26	H23	dss_data19
rfbi_cs1	2nd LCD chip select	O	E28	F25	D23	dss_data20

(1) Type = Ball type for this specific function (I = Input, O = Output, Z = high-impedance, D = Open Drain, DS = Differential, A = Analog).
(2) The subsystem pin multiplexing options are not described in and

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Table 2-10. Video Interfaces – TV Signals Description

SIGNAL NAME	DESCRIPTION	TYPE(1)	BALL BOTTOM (CBB Pkg.)	BALL BOTTOM (CBC Pkg.)	BALL BOTTOM (CUS Pkg.)
tv_out1	TV analog output Composite: tv_out1	O	Y28	W26	AB24
tv_out2	TV analog output S-VIDEO: tv_out2	O	W28	V26	AA23
tv_vfb1	tv_vfb1: Feedback through external resistor to composite	AO	Y27	W25	AB23
tv_vfb2	tv_vfb2: Feedback through external resistor to S-VIDEO	AO	W27	U24	Y23
tv_vref	External capacitor	AO	W26	V23	Y24

(1) Type = Ball type for this specific function (I = Input, O = Output, Z = high-impedance, D = Open Drain, DS = Differential, A = Analog).

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2.5.3 Serial Communication Interfaces

Table 2-11. Serial Communication Interfaces – HDQ/1-Wire Signals Description

SIGNAL NAME	DESCRIPTION	TYPE(1)	BALL BOTTOM (CBB Pkg.)	BALL BOTTOM (CBC Pkg.)	BALL BOTTOM (CUS Pkg.)
hdq_sio	Bidirectional HDQ 1-Wire control and data Interface. Output is open drain.	IOD	J25	J23	A24

(1) Type = Ball type for this specific function (I = Input, O = Output, Z = high-impedance, D = Open Drain, DS = Differential, A = Analog).

Table 2-12. Serial Communication Interfaces – I^2C Signals Description

SIGNAL NAME	DESCRIPTION	TYPE(1)	BALL BOTTOM (CBB Pkg.)	BALL BOTTOM (CBC Pkg.)	BALL BOTTOM (CUS Pkg.)
INTER-INTEGRATED CIRCUIT INTERFACE (I2C1)					
i2c1_scl	I^2C Master Serial clock. Output is open drain.	IOD	K21	J25	K20
i2c1_sda	I^2C Serial Bidirectional Data. Output is open drain.	IOD	J21	J24	K21
INTER-INTEGRATED CIRCUIT INTERFACE (I2C3)					
i2c3_scl	I^2C Master Serial clock. Output is open drain.	IOD	AF14	AB4	AC13
i2c3_sda	I^2C Serial Bidirectional Data. Output is open drain.	IOD	AG14	AC4	AC12
i2c3_sccbe	Serial Camera Control Bus Enable	O	J25	J23	A24
INTER-INTEGRATED CIRCUIT INTERFACE (I2C2)					
i2c2_scl	I^2C Master Serial clock. Output is open drain.	IOD	AF15	C2	AC15
i2c2_sda	I^2C Serial Bidirectional Data. Output is open drain.	IOD	AE15	C1	AC14
i2c2_sccbe	Serial Camera Control Bus Enable	O	J25	J23	A24

(1) Type = Ball type for this specific function (I = Input, O = Output, Z = high-impedance, D = Open Drain, DS = Differential, A = Analog).

Table 2-13. Serial Communication Interfaces – SmartReflex Signals Description(1)

SIGNAL NAME	DESCRIPTION	TYPE(2)	BALL BOTTOM (CBB Pkg.)	BALL BOTTOM (CBC Pkg.)	BALL BOTTOM (CUS Pkg.)
INTER-INTEGRATED CIRCUIT INTERFACE (I2C4)					
i2c4_scl	I^2C Master Serial clock. Output is open drain.	IOD	AD26	AD15	Y16
i2c4_sda	I^2C Serial Bidirectional Data. Output is open drain.	IOD	AE26	W16	Y15

(1) For more information on SmartReflex voltage control, see the PRCM chapter of the *OMAP35x Technical Reference Manual (TRM)* [literature number SPRUFA5].
(2) Type = Ball type for this specific function (I = Input, O = Output, Z = high-impedance, D = Open Drain, DS = Differential, A = Analog).

Table 2-14. Serial Communication Interfaces – McBSP LP Signals Description

SIGNAL NAME	DESCRIPTION	TYPE(1)	BALL BOTTOM (CBB Pkg.)	BALL BOTTOM (CBC Pkg.)	BALL BOTTOM (CUS Pkg.)
MULTICHANNEL SERIAL (McBSP LP 1)					
mcbsp1_dr	Received serial data	I	U21	T20	Y18
mcbsp1_clkr	Receive Clock	IO	Y8 / Y21	U19 / H3	V7 / W19
mcbsp1_fsr	Receive frame synchronization	IO	AA21	V17	AB20
mcbsp1_dx	Transmitted serial data	IO	V21	U17	W18
mcbsp1_clkx	Transmit clock	IO	W21	T17	V18
mcbsp1_fsx	Transmit frame synchronization	IO	K26	P20	AA19
mcbsp_clks	External clock input (shared by McBSP1, 2, 3, 4, and 5)	I	T21	T19	AA18
MULTICHANNEL SERIAL (McBSP LP 2)					

(1) Type = Ball type for this specific function (I = Input, O = Output, Z = high-impedance, D = Open Drain, DS = Differential, A = Analog)

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Table 2-14. Serial Communication Interfaces – McBSP LP Signals Description (continued)

SIGNAL NAME	DESCRIPTION	TYPE(1)	BALL BOTTOM (CBB Pkg.)	BALL BOTTOM (CBC Pkg.)	BALL BOTTOM (CUS Pkg.)
mcbsp2_dr	Received serial data	I	R21	T18	V19
mcbsp2_dx	Transmitted serial data	IO	M21	R19	R20
mcbsp2_clkx	Combined serial clock	IO	N21	R18	T21
mcbsp2_fsx	Combined frame synchronization	IO	P21	U18	V20
MULTICHANNEL SERIAL (McBSP LP 3)					
mcbsp3_dr	Received serial data	I	AE6 / AB25 / U21	T20 / AA24 / N3	V5 / Y18
mcbsp3_dx	Transmitted serial data	IO	AF6 / AB26 / V21	U17 / Y24 / P3	V6 / W18
mcbsp3_clkx	Combined serial clock	IO	AF5 / AA25 / W21	T17 / AD22 / U3	W4 / V18
mcbsp3_fsx	Combined frame synchronization	IO	AE5 / AD25 / K26	P20 / AD21 / W3	V4 / AA19
MULTICHANNEL SERIAL (McBSP LP 4)					
mcbsp4_dr	Received serial data	I	R8 / AD1	C4 / U4	G5
mcbsp4_dx	Transmitted serial data	IO	P8 / AD2	B5 / R3	F3
mcbsp4_clkx	Combined serial clock	IO	T8 / AE1	B4 / V3	F4
mcbsp4_fsx	Combined frame synchronization	IO	N8 / AC1	C5 / T3	G4
MULTICHANNEL SERIAL (McBSP LP 5)					
mcbsp5_dr	Received serial data	I	AE11	Y3	AC5
mcbsp5_dx	Transmitted serial data	IO	AF13	AE3	AC8
mcbsp5_clkx	Combined serial clock	IO	AF10	AB2	AC1
mcbsp5_fsx	Combined frame synchronization	IO	AH9	AB1	AD2

Table 2-15. Serial Communication Interfaces – McSPI Signals Description

SIGNAL NAME	DESCRIPTION	TYPE(1)	BALL BOTTOM (CBB Pkg.)	BALL BOTTOM (CBC Pkg.)	BALL BOTTOM (CUS Pkg.)
MULTICHANNEL SERIAL PORT INTERFACE (McSPI1)					
mcspi1_clk	SPI Clock	IO	AB3	P9	T5
mcspi1_simo	Slave data in, master data out	IO	AB4	P8	R4
mcspi1_somi	Slave data out, master data in	IO	AA4	P7	T4
mcspi1_cs0	SPI Enable 0, polarity configured by software	IO	AC2	R7	T6
mcspi1_cs1	SPI Enable 1, polarity configured by software	O	AC3	R8	NA
mcspi1_cs2	SPI Enable 2, polarity configured by software	O	AB1	R9	NA
mcspi1_cs3	SPI Enable 3, polarity configured by software	O	AB2	T8	R5
MULTICHANNEL SERIAL PORT INTERFACE (McSPI2)					
mcspi2_clk	SPI Clock	IO	AA3	W7	N5
mcspi2_simo	Slave data in, master data out	IO	Y2	W8	N4
mcspi2_somi	Slave data out, master data in	IO	Y3	U8	N3
mcspi2_cs0	SPI Enable 0, polarity configured by software	IO	Y4	V8	M5
mcspi2_cs1	SPI Enable 1, polarity configured by software	O	V3	V9	M4
MULTICHANNEL SERIAL PORT INTERFACE (McSPI3)					
mcspi3_clk	SPI Clock	IO	H26 / AE2 / AE13	W10 / M24 / AA3	G24 / Y1 / AD8
mcspi3_simo	Slave data in, master data out	IO	H25 / AG5 / AF11	R10 / M26 / AC3	H23 / AB5 / AD6
mcspi3_somi	Slave data out, master data in	IO	E28 / AH5 / AG12	F25 / T10 / AD4	D23 / AB3 / AC6
mcspi3_cs0	SPI Enable 0, polarity configured by software	IO	J26 / AF4 / AH12	U9 / N24 / AD3	K22 / V3 / AC7
mcspi3_cs1	SPI Enable 1, polarity configured by software	O	AC27 / AG4 / AH14	AC25 / U10 / AD2	V21 / W3 / AD9
MULTICHANNEL SERIAL PORT INTERFACE (McSPI4)					

(1) Type = Ball type for this specific function (I = Input, O = Output, Z = high-impedance, D = Open Drain, DS = Differential, A = Analog)

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Table 2-15. Serial Communication Interfaces – McSPI Signals Description (continued)

SIGNAL NAME	DESCRIPTION	TYPE(1)	BALL BOTTOM (CBB Pkg.)	BALL BOTTOM (CBC Pkg.)	BALL BOTTOM (CUS Pkg.)
mcspi4_clk	SPI Clock	IO	Y8 / Y21	U19 / H3	V7 / W19
mcspi4_simo	Slave data in, master data out	IO	V21	U17	W18
mcspi4_somi	Slave data out, master data in	IO	U21	T20	Y18
mcspi4_cs0	SPI Enable 0, polarity configured by software	IO	K26	P20	AA19

Table 2-16. Serial Communication Interfaces – UARTs Signals Description

SIGNAL NAME	DESCRIPTION	TYPE(1)	BALL BOTTOM (CBB Pkg.)	BALL BOTTOM (CBC Pkg.)	BALL BOTTOM (CUS Pkg.)
UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER (UART1)					
uart1_cts	UART1 Clear To Send	I	AG22 / W8 / T21	AE21 / T19 / W2	AC19 / AC2 / AA18
uart1_rts	UART1 Request To Send	O	AH22 / AA9	AE22 / R2	W6 / AB19
uart1_rx	UART1 Receive data	I	F28 / Y8 / AE7	H3 / H25 / AE4	E23 / V7 / AC3
uart1_tx	UART1 Transmit data	O	E26 / AA8	L4 / G26	D24 / W7
UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER (UART2)					
uart2_cts	UART2 Clear To Send	I	AF6 / AB26	N23/Y24	V6
uart2_rts	UART2 Request To Send	O	AE6 / AB25	P3/AA24	V5
uart2_rx	UART2 Receive data	I	AE5 / AD25	W3/AD21	V4
uart2_tx	UART2 Transmit data	O	AF5 / AA25	V3/AD22	W4
UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER (UART3) / IrDA					
uart3_cts_rctx	UART3 Clear To Send (input), Remote TX (output)	IO	H18 / U26	W20 / F23	A23 / U23
uart3_rts_sd	UART3 Request To Send, IR enable	O	H19 / U27	V18 / F24	B23 / U24
uart3_rx_irrx	UART3 Receive data, IR and Remote RX	I	AG24 / H20 / U28	AD23 / Y20 / H24	AD21 / B24 / T23
uart3_tx_irtx	UART3 Transmit data, IR TX	O	AH24 / H21 / T27	AD24 / V20 / G24	AC21 / C23 / T24

(1) Type = Ball type for this specific function (I = Input, O = Output, Z = high-impedance, D = Open Drain, DS = Differential, A = Analog)

Table 2-17. Serial Communication Interfaces – USB Signals Description

SIGNAL NAME	DESCRIPTION	TYPE(1)	BALL BOTTOM (CBB Pkg.)	BALL BOTTOM (CBC Pkg.)	BALL BOTTOM (CUS Pkg.)
HIGH-SPEED UNIVERSAL SERIAL BUS INTERFACE (HSUSB0)					
hsusb0_clk	Dedicated for external transceiver 60-MHz clock input to PHY	O	T28	W19	R21
hsusb0_stp	Dedicated for external transceiver Stop signal	O	T25	U20	R23
hsusb0_dir	Dedicated for external transceiver Data direction control from PHY	I	R28	V19	P23
hsusb0_nxt	Dedicated for external transceiver Next signal from PHY	I	T26	W18	R22
hsusb0_data0	Dedicated for external transceiver Bidirectional data bus	IO	T27	V20	T24
hsusb0_data1	Dedicated for external transceiver Bidirectional data bus	IO	U28	Y20	T23
hsusb0_data2	Dedicated for external transceiver Bidirectional data bus	IO	U27	V18	U24
hsusb0_data3	Dedicated for external transceiver Bidirectional data bus	IO	U26	W20	U23
hsusb0_data4	Dedicated for external transceiver Bidirectional data bus additional signals for 12-pin ULPI operation	IO	U25	W17	W24
hsusb0_data5	Dedicated for external transceiver Bidirectional data bus additional signals for 12-pin ULPI operation	IO	V28	Y18	V23
hsusb0_data6	Dedicated for external transceiver Bidirectional data bus additional signals for 12-pin ULPI operation	IO	V27	Y19	W23
hsusb0_data7	Dedicated for external transceiver Bidirectional data bus additional signals for 12-pin ULPI operation	IO	V26	Y17	T22
MM_FSUSB3					
mm3_rxdm	Vminus receive data (not used in 3- or 4-pin configurations)	IO	AE3	K3	NA(2)

(1) Type = Ball type for this specific function (I = Input, O = Output, Z = high-impedance, D = Open Drain, DS = Differential, A = Analog)
(2) This pin is not available on the CUS package. For a list of pins not supported on a particular package, see Table 1-1.

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Table 2-17. Serial Communication Interfaces – USB Signals Description (continued)

SIGNAL NAME	DESCRIPTION	TYPE[1]	BALL BOTTOM (CBB Pkg.)	BALL BOTTOM (CBC Pkg.)	BALL BOTTOM (CUS Pkg.)
mm3_rxdp	Vplus receive data (not used in 3- or 4-pin configurations)	IO	AH3	M3	NA[2]
mm3_rxrcv	Differential receiver signal input (not used in 3-pin mode)	IO	AD1	U4	NA
mm3_txse0	Single-ended zero. Used as VM in 4-pin VP_VM mode.	IO	AE1	V3	NA
mm3_txdat	USB data. Used as VP in 4-pin VP_VM mode.	IO	AD2	R3	NA
mm3_txen_n	Transmit enable	IO	AC1	T3	NA
MM_FSUSB2					
mm2_rxdm	Vminus receive data (not used in 3- or 4-pin configurations)	IO	AH7	AF7	AD11
mm2_rxdp	Vplus receive data (not used in 3- or 4-pin configurations)	IO	AF7	AF6	AC9
mm2_rxrcv	Differential receiver signal input (not used in 3-pin mode)	IO	AG8	AF9	AC11
mm2_txse0	Single-ended zero. Used as VM in 4-pin VP_VM mode.	IO	AH8	AE9	AD12
mm2_txdat	USB data. Used as VP in 4-pin VP_VM mode.	IO	AB2	T8	R5
mm2_txen_n	Transmit enable	IO	V3	V9	M4
MM_FSUSB1					
mm1_rxdm	Vminus receive data (not used in 3- or 4-pin configurations)	IO	AG9	V2	AD5
mm1_rxdp	Vplus receive data (not used in 3- or 4-pin configurations)	IO	AF10	AB2	AC1
mm1_rxrcv	Differential receiver signal input (not used in 3-pin mode)	IO	AF11	AC3	AD6
mm1_txse0	Single-ended zero. Used as VM in 4-pin VP_VM mode.	IO	AG12	AD4	AC6
mm1_txdat	USB data. Used as VP in 4-pin VP_VM mode.	IO	AH12	AD3	AC7
mm1_txen_n	Transmit enable	IO	AH14	AD2	AD9
HSUSB3_TLL					
hsusb3_tll_clk	Dedicated for external transceiver 60-MHz clock input to PHY	O	W8	W2	NA
hsusb3_tll_stp	Dedicated for external transceiver Stop signal	I	AH3	M3	NA
hsusb3_tll_dir	dedicated for external transceiver Data direction control from PHY	O	AF3	L3	NA
hsusb3_tll_nxt	Dedicated for external transceiver Next signal from PHY	O	AE3	K3	NA
hsusb3_tll_data0	Dedicated for external transceiver Bidirectional data bus	IO	AD1	U4	NA
hsusb3_tll_data1	Dedicated for external transceiver Bidirectional data bus	IO	AE1	V3	NA
hsusb3_tll_data2	Dedicated for external transceiver Bidirectional data bus	IO	AD2	R3	NA
hsusb3_tll_data3	Dedicated for external transceiver Bidirectional data bus	IO	AC1	T3	NA
hsusb3_tll_data4	Dedicated for external transceiver Bidirectional data bus	IO	AF6	P3	NA
hsusb3_tll_data5	Dedicated for external transceiver Bidirectional data bus	IO	AE6	N3	NA
hsusb3_tll_data6	Dedicated for external transceiver Bidirectional data bus	IO	AF5	V3	NA
hsusb3_tll_data7	Dedicated for external transceiver Bidirectional data bus	IO	AE5	W3	NA
HSUSB2					
hsusb2_clk	Dedicated for external transceiver 60-MHz clock input to PHY	O	AE7	AE4	AC3
hsusb2_stp	Dedicated for external transceiver Stop signal	O	AF7	AF6	AC9
hsusb2_dir	Dedicated for external transceiver Data direction control from PHY	I	AG7	AE6	AC10
hsusb2_nxt	Dedicated for external transceiver Next signal from PHY	I	AH7	AF7	AD11
hsusb2_data0	Dedicated for external transceiver Bidirectional data bus	IO	AG8	AF9	AC11
hsusb2_data1	Dedicated for external transceiver Bidirectional data bus	IO	AH8	AE9	AD12
hsusb2_data2	Dedicated for external transceiver Bidirectional data bus	IO	AB2	T8	R5
hsusb2_data3	Dedicated for external transceiver Bidirectional data bus	IO	V3	V9	M4
hsusb2_data4	Dedicated for external transceiver Bidirectional data bus additional signals for 12-pin ULPI operation	IO	Y2	W8	N4
hsusb2_data5	Dedicated for external transceiver Bidirectional data bus additional signals for 12-pin ULPI operation	IO	Y3	U8	N3
hsusb2_data6	Dedicated for external transceiver Bidirectional data bus additional signals for 12-pin ULPI operation	IO	Y4	V8	M5
hsusb2_data7	Dedicated for external transceiver Bidirectional data bus additional signals for 12-pin ULPI operation	IO	AA3	W7	N5
HSUSB2_TLL					
hsusb2_tll_clk	Dedicated for external transceiver 60-MHz clock input to PHY	O	AE7	AE4	AC3

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Table 2-17. Serial Communication Interfaces – USB Signals Description (continued)

SIGNAL NAME	DESCRIPTION	TYPE(1)	BALL BOTTOM (CBB Pkg.)	BALL BOTTOM (CBC Pkg.)	BALL BOTTOM (CUS Pkg.)
hsusb2_tll_stp	Dedicated for external transceiver Stop signal	I	AF7	AF6	AC9
hsusb2_tll_dir	Dedicated for external transceiver data direction control from PHY	O	AG7	AE6	AC10
hsusb2_tll_nxt	Dedicated for external transceiver Next signal from PHY	O	AH7	AF7	AD11
hsusb2_tll_data0	Dedicated for external transceiver Bidirectional data bus	IO	AG8	AF9	AC11
hsusb2_tll_data1	Dedicated for external transceiver Bidirectional data bus	IO	AH8	AE9	AD12
hsusb2_tll_data2	Dedicated for external transceiver Bidirectional data bus	IO	AB2	T8	R5
hsusb2_tll_data3	Dedicated for external transceiver Bidirectional data bus	IO	V3	V9	M4
hsusb2_tll_data4	Dedicated for external transceiver Bidirectional data bus additional signals for 12-pin ULPI operation	IO	Y2	W8	N4
hsusb2_tll_data5	Dedicated for external transceiver Bidirectional data bus additional signals for 12-pin ULPI operation	IO	Y3	U8	N3
hsusb2_tll_data6	Dedicated for external transceiver Bidirectional data bus additional signals for 12-pin ULPI operation	IO	Y4	V8	M5
hsusb2_tll_data7	Dedicated for external transceiver Bidirectional data bus additional signals for 12-pin ULPI operation	IO	AA3	W7	N5
HSUSB1					
hsusb1_clk	Dedicated for external transceiver 60-MHz clock input to PHY	O	AE10	AB3	AD3
hsusb1_stp	Dedicated for external transceiver Stop signal	O	AF10	AB2	AC1
hsusb1_dir	Dedicated for external transceiver data direction control from PHY	I	AF9	AA4	AC4
hsusb1_nxt	Dedicated for external transceiver Next signal from PHY	I	AG9	V2	AD5
hsusb1_data0	Dedicated for external transceiver Bidirectional data bus	IO	AF11	AC3	AD6
hsusb1_data1	Dedicated for external transceiver Bidirectional data bus	IO	AG12	AD4	AC6
hsusb1_data2	Dedicated for external transceiver Bidirectional data bus	IO	AH12	AD3	AC7
hsusb1_data3	Dedicated for external transceiver Bidirectional data bus	IO	AH14	AD2	AD9
hsusb1_data4	Dedicated for external transceiver Bidirectional data bus additional signals for 12-pin ULPI operation	IO	AE11	Y3	AC5
hsusb1_data5	Dedicated for external transceiver Bidirectional data bus additional signals for 12-pin ULPI operation	IO	AH9	AB1	AD2
hsusb1_data6	Dedicated for external transceiver Bidirectional data bus additional signals for 12-pin ULPI operation	IO	AF13	AE3	AC8
hsusb1_data7	Dedicated for external transceiver Bidirectional data bus additional signals for 12-pin ULPI operation	IO	AE13	AA3	AD8
HSUSB1_TLL					
hsusb1_tll_clk	Dedicated for external transceiver 60-MHz clock input to PHY	O	AE10	AB3	AD3
hsusb1_tll_stp	Dedicated for external transceiver Stop signal	I	AF10	AB2	AC1
hsusb1_tll_dir	Dedicated for external transceiver data direction control from PHY	O	AF9	AA4	AC4
hsusb1_tll_nxt	Dedicated for external transceiver Next signal from PHY	O	AG9	V2	AD5
hsusb1_tll_data0	Dedicated for external transceiver Bidirectional data bus	IO	AF11	AC3	AD6
hsusb1_tll_data1	Dedicated for external transceiver Bidirectional data bus	IO	AG12	AD4	AC6
hsusb1_tll_data2	Dedicated for external transceiver Bidirectional data bus	IO	AH12	AD3	AC7
hsusb1_tll_data3	Dedicated for external transceiver Bidirectional data bus	IO	AH14	AD2	AD9
hsusb1_tll_data4	Dedicated for external transceiver Bidirectional data bus additional signals for 12-pin ULPI operation	IO	AE11	Y3	AC5
hsusb1_tll_data5	Dedicated for external transceiver Bidirectional data bus additional signals for 12-pin ULPI operation	IO	AH9	AB1	AD2
hsusb1_tll_data6	Dedicated for external transceiver Bidirectional data bus additional signals for 12-pin ULPI operation	IO	AF13	AE3	AC8
hsusb1_tll_data7	Dedicated for external transceiver Bidirectional data bus additional signals for 12-pin ULPI operation	IO	AE13	AA3	AD8

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2.5.4 Removable Media Interfaces

Table 2-18. Removable Media Interfaces – MMC/SDIO Signals Description

SIGNAL NAME	DESCRIPTION	TYPE(1)	BALL BOTTOM (CBB Pkg.)	BALL BOTTOM (CBC Pkg.)	BALL BOTTOM (CUS Pkg.)
MULTIMEDIA MEMORY CARD (MMC1) / SECURE DIGITAL IO (SDIO1)					
mmc1_clk	MMC/SD Output Clock	O	N28	N19	M23
mmc1_cmd	MMC/SD command signal	IO	M27	L18	L23
mmc1_dat0	MMC/SD Card Data bit 0 / SPI Serial Input	IO	N27	M19	M22
mmc1_dat1	MMC/SD Card Data bit 1	IO	N26	M18	M21
mmc1_dat2	MMC/SD Card Data bit 2	IO	N25	K18	M20
mmc1_dat3	MMC/SD Card Data bit 3	IO	P28	N20	N23
mmc1_dat4	MMC/SD Card Data bit 4	IO	P27	M20	N22
mmc1_dat5	MMC/SD Card Data bit 5	IO	P26	P17	N21
mmc1_dat6	MMC/SD Card Data bit 6	IO	R27	P18	N20
mmc1_dat7	MMC/SD Card Data bit 7	IO	R25	P19	P24
MULTIMEDIA MEMORY CARD (MMC2) / SECURE DIGITAL IO (SDIO2)					
mmc2_clk	MMC/SD Output Clock	O	AE2	W10	Y1
mmc2_dir_dat0	Direction control for DAT0 signal case an external transceiver used	O	AE4	V10	AB2
mmc2_dir_dat1	Direction control for DAT1 and DAT3 signals case an external transceiver used	O	AH3	M3	AA2
mmc2_dir_dat2	Direction control for DAT2 signal case an external transceiver used	O	AF19	E4	AC17
mmc2_dir_dat3	Direction control for DAT4, DAT5, DAT6, and DAT7 signals case an external transceiver used	O	AE21	G3	AB16
mmc2_clkin	MMC/SD input Clock	I	AE3	K3	AA1
mmc2_dat0	MMC/SD Card Data bit 0	IO	AH5	T10	AB3
mmc2_dat1	MMC/SD Card Data bit 1	IO	AH4	T9	Y3
mmc2_dat2	MMC/SD Card Data bit 2	IO	AG4	U10	W3
mmc2_dat3	MMC/SD Card Data bit 3	IO	AF4	U9	V3
mmc2_dat4	MMC/SD Card Data bit 4	IO	AE4 / AB3	P9 / V10	AB2 / T5
mmc2_dat5	MMC/SD Card Data bit 5	IO	AH3 / AB4	M3/P8	AA2 / R4
mmc2_dat6	MMC/SD Card Data bit 6	IO	AF3 / AA4	L3/P7	Y2 / T4
mmc2_dat7	MMC/SD Card Data bit 7	IO	AE3 / AC2	K3/R7	AA1 / T6
mmc2_dir_cmd	Direction control for CMD signal case an external transceiver is used	O	AF3	L3	Y2
mmc2_cmd	MMC/SD command signal	IO	AG5	R10	AB5
MULTIMEDIA MEMORY CARD (MMC3) / SECURE DIGITAL IO (SDIO3)					
mmc3_clk	MMC/SD Output Clock	O	AB1 / AF10	R9 / AB2	AC1
mmc3_cmd	MMC/SD command signal	IO	AC3 / AE10	R8 / AB3	AD3
mmc3_dat0	MMC/SD Card Data bit 0 / SPI Serial Input	IO	AE4 / AE11	V10 / Y3	AB2 / AC5
mmc3_dat1	MMC/SD Card Data bit 1	IO	AH3 / AH9	M3/AB1	AA2 / AD2
mmc3_dat2	MMC/SD Card Data bit 2	IO	AF3 / AF13	L3/AE3	Y2 / AC8
mmc3_dat3	MMC/SD Card Data bit 3	IO	AE3 / AE13	K3/AA3	AA1 / AD8
mmc3_dat4	MMC/SD Card Data bit 4	IO	AF11	AC3	AD6
mmc3_dat5	MMC/SD Card Data bit 5	IO	AG9	V2	AD5
mmc3_dat6	MMC/SD Card Data bit 6	IO	AF9	AA4	AC4
mmc3_dat7	MMC/SD Card Data bit 7	IO	AH14	AD2	AD9

(1) Type = Ball type for this specific function (I = Input, O = Output, Z = high-impedance, D = Open Drain, DS = Differential, A = Analog)

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2.5.5 Test Interfaces

Table 2-19. Test Interfaces – ETK Signals Description

SIGNAL NAME	DESCRIPTION	TYPE(1)	BALL BOTTOM (CBB Pkg.)	BALL BOTTOM (CBC Pkg.)	BALL BOTTOM (CUS Pkg.)
etk_ctl	ETK trace ctl	O	AE10	AB2	AD3
etk_clk	ETK trace clock	O	AF10	AB3	AC1
etk_d0	ETK data 0	O	AF11	AC3	AD6
etk_d1	ETK data 1	O	AG12	AD4	AC6
etk_d2	ETK data 2	O	AH12	AD3	AC7
etk_d3	ETK data 3	O	AE13	AA3	AD8
etk_d4	ETK data 4	O	AE11	Y3	AC5
etk_d5	ETK data 5	O	AH9	AB1	AD2
etk_d6	ETK data 6	O	AF13	AE3	AC8
etk_d7	ETK data 7	O	AH14	AD2	AD9
etk_d8	ETK data 8	O	AF9	AA4	AC4
etk_d9	ETK data 9	O	AG9	V2	AD5
etk_d10	ETK data 10	O	AE7	AE4	AC3
etk_d11	ETK data 11	O	AF7	AF6	AC9
etk_d12	ETK data 12	O	AG7	AE6	AC10
etk_d13	ETK data 13	O	AH7	AF7	AD11
etk_d14	ETK data 14	O	AG8	AF9	AC11
etk_d15	ETK data 15	O	AH8	AE9	AD12

(1) Type = Ball type for this specific function (I = Input, O = Output, Z = high-impedance, D = Open Drain, DS = Differential, A = Analog)

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Table 2-20. Test Interfaces – JTAG Signals Description

SIGNAL NAME	DESCRIPTION	TYPE(1)	BALL BOTTOM (CBB Pkg.)	BALL BOTTOM (CBC Pkg.)	BALL BOTTOM (CUS Pkg.)
jtag_ntrst	Test Reset	I	AA17	U15	AB7
jtag_tck	Test Clock	I	AA13	V14	AB6
jtag_rtck	ARM Clock Emulation	O	AA12	W13	AA7
jtag_tms_tmsc	Test Mode Select	IO	AA18	V15	AA9
jtag_tdi	Test Data Input	I	AA20	U16	AB10
jtag_tdo	Test Data Output	O	AA19	Y13	AB9
jtag_emu0	Test emulation 0	IO	AA11	Y15	AC24
jtag_emu1	Test emulation 1	IO	AA10	Y14	AD24

(1) Type = Ball type for this specific function (I = Input, O = Output, Z = high-impedance, D = Open Drain, DS = Differential, A = Analog)

Table 2-21. Test Interfaces – SDTI Signals Description

SIGNAL NAME	DESCRIPTION	TYPE(1)	BALL BOTTOM (CBB Pkg.)	BALL BOTTOM (CBC Pkg.)	BALL BOTTOM (CUS Pkg.)	SUBSYSTEM SIGNAL MULTIPLEXING(2)
sdti_clk	Serial clock dual edge	O	AF7 / AA11 / AG8	AF6 / Y15 / AF9	AC9 / AC24 / AC11	etk_d11 / jtag_emu0 / etk_d14
sdti_txd0	Serial data out (System Trace messages)	O	AG7 / AA10 / AA11	AE6 / Y14 / Y15	AC10 / AD24 / AC24	etk_d12 / jtag_emu1 / jtag_emu0
sdti_txd1	Serial data out (System Trace messages)	O	AH7 / AA10	AF7 / Y14	AD11 / AD24	etk_d13 / jtag_emu1
sdti_txd2	Serial data out (System Trace messages)	O	AG8	AF9	AC11	etk_d14
sdti_txd3	Serial data out (System Trace messages)	O	AH8	AE9	AD12	etk_d15

(1) Type = Ball type for this specific function (I = Input, O = Output, Z = high-impedance, D = Open Drain, DS = Differential, A = Analog)
(2) The subsystem pin multiplexing options are not described in and

Table 2-22. Test Interfaces – HWDBG Signals Description

SIGNAL NAME	DESCRIPTION	TYPE(1)	BALL BOTTOM (CBB Pkg.)	BALL BOTTOM (CBC Pkg.)	BALL BOTTOM (CUS Pkg.)
hw_dbg0	Debug signal 0	O	A24 / AF10	C23/AB2	AC1/A22
hw_dbg1	Debug signal 1	O	A23 / AE10	D23/AB3	AD3/E18
hw_dbg2	Debug signal 2	O	C27/ AF11	C26/AC3	AD6/J19
hw_dbg3	Debug signal 3	O	C23 / AG12	B23/AD4	AC6/H24
hw_dbg4	Debug signal 4	O	B24 / AH12	A24/AD3	AC7/G19
hw_dbg5	Debug signal 5	O	C24 / AE13	B24/AA3	AD8/F19
hw_dbg6	Debug signal 6	O	D24 / AE11	D24/Y3	AC5/G20
hw_dbg7	Debug signal 7	O	A25 / AH9	C24/AB1	AD2/B21
hw_dbg8	Debug signal 8	O	B25 / AF13	D25/AE3	AC8/F21
hw_dbg9	Debug signal 9	O	C26 / AH14	E26/AD2	AD9/G21
hw_dbg10	Debug signal 10	O	B23 / AF9	A23/AA4	AC4/F18
hw_dbg11	Debug signal 11	O	D25 / AG9	D26/V2	AD5/J20
hw_dbg12	Debug signal 12	O	D28 / AE7	G25/AE4	AC3/G22
hw_dbg13	Debug signal 13	O	D26 / AF7	K24/AF6	AC9/E22
hw_dbg14	Debug signal 14	O	E26 / AG7	G26/AE6	AC10/D24
hw_dbg15	Debug signal 15	O	F28 / AH7	H25/AF7	AD11/E23
hw_dbg16	Debug signal 16	O	F27 / AG8	H26/AF9	AC11/E24
hw_dbg17	Debug signal 17	O	G26 / AH8	J26/AE9	AD12/F23

(1) Type = Ball type for this specific function (I = Input, O = Output, Z = high-impedance, D = Open Drain, DS = Differential, A = Analog)

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2.5.6 Miscellaneous

Table 2-23. Miscellaneous – GP Timer Signals Description

SIGNAL NAME	DESCRIPTION	TYPE(1)	BALL BOTTOM (CBB Pkg.)	BALL BOTTOM (CBC Pkg.)	BALL BOTTOM (CUS Pkg.)
gpt8_pwm_evt	PWM or event for GP timer 8	IO	N8 / AD25 / V3	C5 / AD21/ V9	G4/ M4
gpt9_pwm_evt	PWM or event for GP timer 9	IO	T8 / AB26 / Y2	B4 / W8 / Y24	F4 / N4
gpt10_pwm_evt	PWM or event for GP timer 10	IO	R8 / AB25 / Y3	C4 / U8 / AA24	G5 / N3
gpt11_pwm_evt	PWM or event for GP timer 11	IO	P8 / AA25 / Y4	B5 / V8 / AD22	F3 / M5

(1) Type = Ball type for this specific function (I = Input, O = Output, Z = high-impedance, D = Open Drain, DS = Differential, A = Analog)

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2.5.7 General-Purpose IOs

Table 2-24. General-Purpose IOs Signals Description(1)

SIGNAL NAME	DESCRIPTION	TYPE(2)	BALL BOTTOM (CBB Pkg.)	BALL BOTTOM (CBC Pkg.)	BALL BOTTOM (CUS Pkg.)
gpio_0	General-purpose IO 0	IO	AF26	V16	W16
gpio_1	General-purpose IO 1	IO	AF25	W15	Y13
gpio_2	General-purpose IO 2	IO	AH26	F3	AB12
gpio_3	General-purpose IO 3	IO	AG26	D3	AC16
gpio_4	General-purpose IO 4	IO	AE14	C3	AD17
gpio_5	General-purpose IO 5	IO	AF18	E3	AD18
gpio_6	General-purpose IO 6	IO	AF19	E4	AC17
gpio_7	General-purpose IO 7	IO	AE21	G3	AB16
gpio_8	General-purpose IO 8	IO	AF21	D4	AA15
gpio_9	General-purpose IO 9	IO	AF22	V12	AD23
gpio_10	General-purpose IO 10	IO	AG25	AE14	Y7
gpio_11	General-purpose IO 11	IO	AA11	Y15	AC24
gpio_12	General-purpose IO 12	IO	AF10	AB2	AC1
gpio_13	General-purpose IO 13	IO	AE10	AB3	AD3
gpio_14	General-purpose IO 14	IO	AF11	AC3	AD6
gpio_15	General-purpose IO 15	IO	AG12	AD4	AC6
gpio_16	General-purpose IO 16	IO	AH12	AD3	AC7
gpio_17	General-purpose IO 17	IO	AE13	AA3	AD8
gpio_18	General-purpose IO 18	IO	AE11	Y3	AC5
gpio_19	General-purpose IO 19	IO	AH9	AB1	AD2
gpio_20	General-purpose IO 20	IO	AF13	AE3	AC8
gpio_21	General-purpose IO 21	IO	AH14	AD2	AD9
gpio_22	General-purpose IO 22	IO	AF9	AA4	AC4
gpio_23	General-purpose IO 23	IO	AG9	V2	AD5
gpio_24	General-purpose IO 24	IO	AE7	AE4	AC3
gpio_25	General-purpose IO 25	IO	AF7	AF6	AC9
gpio_26	General-purpose IO 26	IO	AG7	AE6	AC10
gpio_27	General-purpose IO 27	IO	AH7	AF7	AD11
gpio_28	General-purpose IO 28	IO	AG8	AF9	AC11
gpio_29	General-purpose IO 29	IO	AH8	AE9	AD12
gpio_30	General-purpose IO 30	IO	AF24	AD7	Y10
gpio_31	General-purpose IO 31	IO	AA10	Y14	AD24
gpio_34	General-purpose IO 34	IO	N4	J2	K4
gpio_35	General-purpose IO 35	IO	M4	H1	K3
gpio_36	General-purpose IO 36	IO	L4	H2	K2
gpio_37	General-purpose IO 37	IO	K4	G2	J4
gpio_38	General-purpose IO 38	IO	T3	F1	J3
gpio_39	General-purpose IO 39	IO	R3	F2	J2
gpio_40	General-purpose IO 40	IO	N3	E1	J1
gpio_41	General-purpose IO 41	IO	M3	E2	H1
gpio_42	General-purpose IO 42	IO	L3	D1	H2
gpio_43	General-purpose IO 43	IO	K3	D2	G2
gpio_44	General-purpose IO 44	IO	H2	V1	R2
gpio_45	General-purpose IO 45	IO	K2	Y1	T2
gpio_46	General-purpose IO 46	IO	P1	T1	U1
gpio_47	General-purpose IO 47	IO	R1	U2	R3
gpio_48	General-purpose IO 48	IO	R2	U1	T3

(1) NA in table stands for "Not Applicable".
(2) Type = Ball type for this specific function (I = Input, O = Output, Z = high-impedance, D = Open Drain, DS = Differential, A = Analog)

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Table 2-24. General-Purpose IOs Signals Description[1] (continued)

SIGNAL NAME	DESCRIPTION	TYPE[2]	BALL BOTTOM (CBB Pkg.)	BALL BOTTOM (CBC Pkg.)	BALL BOTTOM (CUS Pkg.)
gpio_49	General-purpose IO 49	IO	T2	P1	U2
gpio_50	General-purpose IO 50	IO	W1	L2	V1
gpio_51	General-purpose IO 51	IO	Y1	M2	V2
gpio_52	General-purpose IO 52	IO	H3	AD1	NA
gpio_53	General-purpose IO 53	IO	V8	A3	NA
gpio_54	General-purpose IO 54	IO	U8	B6	D2
gpio_55	General-purpose IO 55	IO	T8	B4	F4
gpio_56	General-purpose IO 56	IO	R8	C4	G5
gpio_57	General-purpose IO 57	IO	P8	B5	F3
gpio_58	General-purpose IO 58	IO	N8	C5	G4
gpio_59	General-purpose IO 59	IO	T4	N1	W2
gpio_60	General-purpose IO 60	IO	G3	K2	K5
gpio_61	General-purpose IO 61	IO	U3	J1	L1
gpio_62	General-purpose IO 62	IO	H1	AC6	E1
gpio_63	General-purpose IO 63	IO	L8	AC8	NA
gpio_64	General-purpose IO 64	IO	K8	B3	NA
gpio_65	General-purpose IO 65	IO	J8	C6	C2
gpio_66	General-purpose IO 66	IO	D28	G25	G22
gpio_67	General-purpose IO 67	IO	D26	K24	E22
gpio_68	General-purpose IO 68	IO	D27	M25	F22
gpio_69	General-purpose IO 69	IO	E27	F26	J21
gpio_70	General-purpose IO 70	IO	AG22	AE21	AC19
gpio_71	General-purpose IO 71	IO	AH22	AE22	AB19
gpio_72	General-purpose IO 72	IO	AG23	AE23	AD20
gpio_73	General-purpose IO 73	IO	AH23	AE24	AC20
gpio_74	General-purpose IO 74	IO	AG24	AD23	AD21
gpio_75	General-purpose IO 75	IO	AH24	AD24	AC21
gpio_76	General-purpose IO 76	IO	E26	G26	D24
gpio_77	General-purpose IO 77	IO	F28	H25	E23
gpio_78	General-purpose IO 78	IO	F27	H26	E24
gpio_79	General-purpose IO 79	IO	G26	J26	F23
gpio_80	General-purpose IO 80	IO	AD28	AC26	AC22
gpio_81	General-purpose IO 81	IO	AD27	AD26	AC23
gpio_82	General-purpose IO 82	IO	AB28	AA25	AB22
gpio_83	General-purpose IO 83	IO	AB27	Y25	Y22
gpio_84	General-purpose IO 84	IO	AA28	AA26	W22
gpio_85	General-purpose IO 85	IO	AA27	AB26	V22
gpio_86	General-purpose IO 86	IO	G25	L25	J22
gpio_87	General-purpose IO 87	IO	H27	L26	G23
gpio_88	General-purpose IO 88	IO	H26	M24	G24
gpio_89	General-purpose IO 89	IO	H25	M26	H23
gpio_90	General-purpose IO 90	IO	E28	F25	D23
gpio_91	General-purpose IO 91	IO	J26	N24	K22
gpio_92	General-purpose IO 92	IO	AC27	AC25	V21
gpio_93	General-purpose IO 93	IO	AC28	AB25	W21
gpio_94	General-purpose IO 94	IO	A24	C23	A22
gpio_95	General-purpose IO 95	IO	A23	D23	E18
gpio_96	General-purpose IO 96	IO	C25	C25	B22
gpio_97	General-purpose IO 97	IO	C27	C26	J19
gpio_98	General-purpose IO 98	IO	C23	B23	H24
gpio_99	General-purpose IO 99	I	AG17	AE16	AB18

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Table 2-24. General-Purpose IOs Signals Description[1] (continued)

SIGNAL NAME	DESCRIPTION	TYPE[2]	BALL BOTTOM (CBB Pkg.)	BALL BOTTOM (CBC Pkg.)	BALL BOTTOM (CUS Pkg.)
gpio_100	General-purpose IO 100	I	AH17	AE15	AC18
gpio_101	General-purpose IO 101	IO	B24	A24	G19
gpio_102	General-purpose IO 102	IO	C24	B24	F19
gpio_103	General-purpose IO 103	IO	D24	D24	G20
gpio_104	General-purpose IO 104	IO	A25	C24	B21
gpio_105	General-purpose IO 105	IO	K28	P25	L24
gpio_106	General-purpose IO 106	IO	L28	P26	K24
gpio_107	General-purpose IO 107	IO	K27	N25	J23
gpio_108	General-purpose IO 108	IO	L27	N26	K23
gpio_109	General-purpose IO 109	IO	B25	D25	F21
gpio_110	General-purpose IO 110	IO	C26	E26	G21
gpio_111	General-purpose IO 111	IO	B26	E25	C22
gpio_112	General-purpose IO 112	I	AG19	AD17	NA
gpio_113	General-purpose IO 113	I	AH19	AD16	NA
gpio_114	General-purpose IO 114	I	AG18	AE18	NA
gpio_115	General-purpose IO 115	I	AH18	AE17	NA
gpio_116	General-purpose IO 116	IO	P21	U18	V20
gpio_117	General-purpose IO 117	IO	N21	R18	T21
gpio_118	General-purpose IO 118	IO	R21	T18	V19
gpio_119	General-purpose IO 119	IO	M21	R19	R20
gpio_120	General-purpose IO 120	IO	N28 / T28	W19 / N19	M23 / R21
gpio_121	General-purpose IO 121	IO	M27 / T25	U20 / L18	L23 / R23
gpio_122	General-purpose IO 122	IO	N27 / R28	V19 / M19	M22 / P23
gpio_123	General-purpose IO 123	IO	N26	M18	M21
gpio_124	General-purpose IO 124	IO	N25 / T26	W18 / K18	M20/R22
gpio_125	General-purpose IO 125	IO	P28 / T27	V20 / N20	N23/T24
gpio_126	General-purpose IO 126	IO	D25 / P27	M20 / D26	J20 / N22
gpio_127	General-purpose IO 127	IO	P26	P17	N21
gpio_128	General-purpose IO 128	IO	R27	P18	N20
gpio_129	General-purpose IO 129	IO	R25	P19	P24
gpio_130	General-purpose IO 130	IO	AE2 / U28	Y20 / W10	Y1 / T23
gpio_131	General-purpose IO 131	IO	AG5 / U27	V18 / R10	AB5 / U24
gpio_132	General-purpose IO 132	IO	AH5	T10	AB3
gpio_133	General-purpose IO 133	IO	AH4	T9	Y3
gpio_134	General-purpose IO 134	IO	AG4	U10	W3
gpio_135	General-purpose IO 135	IO	AF4	U9	V3
gpio_136	General-purpose IO 136	IO	AE4	V10	AB2
gpio_137	General-purpose IO 137	IO	AH3	M3	AA2
gpio_138	General-purpose IO 138	IO	AF3	L3	Y2
gpio_139	General-purpose IO 139	IO	AE3	K3	AA1
gpio_140	General-purpose IO 140	IO	AF6	N3	V6
gpio_141	General-purpose IO 141	IO	AE6	P3	V5
gpio_142	General-purpose IO 142	IO	AF5	V3	W4
gpio_143	General-purpose IO 143	IO	AE5	W3	V4
gpio_144	General-purpose IO 144	IO	AB26	Y24	NA
gpio_145	General-purpose IO 145	IO	AB25	AA24	NA
gpio_146	General-purpose IO 146	IO	AA25	AD22	NA
gpio_147	General-purpose IO 147	IO	AD25	AD21	NA
gpio_148	General-purpose IO 148	IO	AA8	L4	W7
gpio_149	General-purpose IO 149	IO	AA9	R2	W6
gpio_150	General-purpose IO 150	IO	W8	W2	AC2

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Table 2-24. General-Purpose IOs Signals Description[1] (continued)

SIGNAL NAME	DESCRIPTION	TYPE[2]	BALL BOTTOM (CBB Pkg.)	BALL BOTTOM (CBC Pkg.)	BALL BOTTOM (CUS Pkg.)
gpio_151	General-purpose IO 151	IO	Y8	H3	V7
gpio_152	General-purpose IO 152	IO	AE1	V3	NA
gpio_153	General-purpose IO 153	IO	AD1	U4	NA
gpio_154	General-purpose IO 154	IO	AD2	R3	NA
gpio_155	General-purpose IO 155	IO	AC1	T3	NA
gpio_156	General-purpose IO 156	IO	Y21	U19	W19
gpio_157	General-purpose IO 157	IO	AA21	V17	AB20
gpio_158	General-purpose IO 158	IO	V21	U17	W18
gpio_159	General-purpose IO 159	IO	U21	T20	Y18
gpio_160	General-purpose IO 160	IO	T21	T19	AA18
gpio_161	General-purpose IO 161	IO	K26	P20	AA19
gpio_162	General-purpose IO 162	IO	W21	T17	V18
gpio_163	General-purpose IO 163	IO	H18	F23	A23
gpio_164	General-purpose IO 164	IO	H19	F24	B23
gpio_165	General-purpose IO 165	IO	H20	H24	B24
gpio_166	General-purpose IO 166	IO	H21	G24	C23
gpio_167	General-purpose IO 167	IO	B23	A23	F18
gpio_168	General-purpose IO 168	IO	AF15	C2	AC15
gpio_169	General-purpose IO 169	IO	U26	W20	U23
gpio_170	General-purpose IO 170	IO	J25	J23	A24
gpio_171	General-purpose IO 171	IO	AB3	P9	T5
gpio_172	General-purpose IO 172	IO	AB4	P8	R4
gpio_173	General-purpose IO 173	IO	AA4	P7	T4
gpio_174	General-purpose IO 174	IO	AC2	R7	T6
gpio_175	General-purpose IO 175	IO	AC3	R8	NA
gpio_176	General-purpose IO 176	IO	AB1	R9	NA
gpio_177	General-purpose IO 177	IO	AB2	T8	R5
gpio_178	General-purpose IO 178	IO	AA3	W7	N5
gpio_179	General-purpose IO 179	IO	Y2	W8	N4
gpio_180	General-purpose IO 180	IO	Y3	U8	N3
gpio_181	General-purpose IO 181	IO	Y4	V8	M5
gpio_182	General-purpose IO 182	IO	V3	V9	M4
gpio_183	General-purpose IO 183	IO	AE15	C1	AC14
gpio_184	General-purpose IO 184	IO	AF14	AB4	AC13
gpio_185	General-purpose IO 185	IO	AG14	AC4	AC12
gpio_186	General-purpose IO 186	IO	AE22	W11	AA6
gpio_188	General-purpose IO 188	IO	U25	W17	W24
gpio_189	General-purpose IO 189	IO	V28	Y18	V23
gpio_190	General-purpose IO 190	IO	V27	Y19	W23
gpio_191	General-purpose IO 191	IO	V26	Y17	T22

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2.5.8 Power Supplies

Table 2-25. Power Supplies Signals Description(1)

SIGNAL NAME	DESCRIPTION	BALL BOTTOM (CBB Pkg.)	BALL TOP (CBB Pkg.)	BALL BOTTOM (CBC Pkg.)	BALL TOP (CBC Pkg.)	BALL BOTTOM (CUS Pkg.)
vdd_mpu _iva	ARM /IVA power domain	Y9 / W9 / T9 / R9 / M9 / L9 / J9 / Y10 / U10 / T10 / R10 / N10 / M10 / L10 / J10 / Y11 / W11 / K11 / J11 / W12 / K13 / Y14 / K14 / J14 / Y15 / W15 / J15	NA	H7/ N7/ U7/ V7/ N8/ G9/ L9/ M9/ W9/ Y9/ M10/ P10/ K11/ U11/ V11/ Y11/ G12/ D13/ U13	NA	W13/ W12/ V13/ V12/ U13/ U12/ T8/ T7/ R8/ R7/ R6/ N8/ N7/ N6/ M12/ M8/ M7/ M6/ L12/ L11/ J10/ J9/ H10/ H9/ G10/ G9/F10
vdd_core	Core power domain	AC4 / J4 / H4 / D8 / AE9 / D9 / D15 / Y16 / AE18 / Y18 / W18 / K18 / J18 / AE19 / Y19 / U19 / T19 / N19 / M19 / J19 / Y20 / W20 / V20 / U20 / P20 / N20 / K20 / J20 / D22 / D23 / AE24 / M25 / L25 / E25	NA	M7/ T7/ Y8/ G11/ Y12/ D15/ M17/ G18/ H20/ R20/ AC21	NA	T20/ T19/ T18/ T17/ R19/ R18/ R17/ M15/ M14/ L15/ L14/ K19/ K18/ K17/ J18/ J17/ H13/ H12/ G13/ G12/ F13/ F12
cap_vdd_wkup	Wakeup/EMU/memory domains, connect capacitor	AA15	NA	K14	NA	Y12
cap_vdd_d	Decoupling capacitor	AH20	NA	AE19	NA	NA
vdds_dpll_dll	DLL IO power domain (1.8 V): internal connection to PLL_VDDS, power supply for 3PLL (1.8 V)	K15	NA	K13	NA	G18
vdda_dac	Video DAC power plane	V25	NA	V25	NA	AB13
vssa_dac	Video DAC ground plane	Y26	NA	V24	NA	AB15
vdds	IO power plane	AD3 / AD4 / W4 / AF8 / AE8 / AF16 / AE16 / AF23 / AE23 / F25 / F26 / AG27/ AE27/ AG20/ H28/ AG21	NA	G4/ M4/ T4/ Y4/ L7/ AC7/ D9/ AE10/ C11/ J15/ AC15/ A18/ J18/ AC18/ AD20/ E24/ L24/ T24/ W24/ AC24	NA	Y9 / W10 / W9 / V10 / V9 / U10 / N19 / N18 / N17 / M19 / M18 / M17
vdds_mem	Memory IO power plane	U1 / J1 / F1 / J2 / F2 / R4 / B5 / A5 / AH6 / B8 / A8 / B12 / A12 / D16 / C16 / B18 / A18 / B22 / A22 / G28 / C28	AC5 / P1 / H1 / F23 / E1 / C23 / A4 / A7 / A10 / A15 / A18			K8 / K7 / K6 / J8 / J7 / J6 / H15 / G16 / G15 / F16 / F15 / E16
vdds_dpll_per	Peripheral DPLLs power rail	AA16	NA	U14	NA	U17
vdds_wkup_bg	For wakeup LDO and VDDA (2 LDOs SRAM and BG)	AA14	NA	W14	NA	AA13

(1) NA in this table stands for "Not applicable".

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Table 2-25. Power Supplies Signals Description[(1)] (continued)

SIGNAL NAME	DESCRIPTION	BALL BOTTOM (CBB Pkg.)	BALL TOP (CBB Pkg.)	BALL BOTTOM (CBC Pkg.)	BALL TOP (CBC Pkg.)	BALL BOTTOM (CUS Pkg.)
vss	Ground	AG2 / U2 / B2 / AG3 / W3 / P3 / J3 / E3 / A3 / P4 / E4 / AG6 / D7 / C7 / V9 / U9 / P9 / N9 / K9 / W10 / V10 / P10 / K10 / D10 / C10 / AF12 / AE12 / Y12 / K12 / J12 / Y13 / W13 / J13 / D13 / C13 / W14 / K16 / J16 / Y17 / W17 / K17 / J17 / W19 / V19 / R19 / P19 / L19 / K19 / D19 / C19 / AF20 / AE20 / T20 / R20 / M20 / L20 / D21 / C22 / AC25 / Y25 / W25 / AC26 / R26 / L26 / A26 / G27 / B27/ AA26/ M28/ AG16/ AH21	H2 / B18 / AC20 / AB5 / AB14 / AB20 / P2 / F22 / E2 / C22 / B4 / B7 / B10 / B15	G1/ K1/ R1/ W1/ B2/ H4/ N4/ R4/ W4/ AB5/ A6/ D7/ Y7/AE7/ A8/ G8/ D10/ G10/ L10/ N10/ Y10/ AC10/ C12/ D12/A13/ D14/ AD14/ K15/ Y16/ L17/ N17/ R17/ D18/ D20/G20/ E22/ AB22/ G23/ L23/ T23/ W23/ AF23/ B25/ K25/U25/ AD25	C1/ F1/ H2/ M2/ R2/ Y6/AA7/ Y11/ AA16/ W20/P20/ L21/ H20/ F20/ B14/A13/ A7	W15/ V16/ V15/ U16/ U15/ U14/ U11/ U9/T16/ T15/ T14/ T13/ T12/ T11/ T10/ T9/ R15/ R14/ R11/ R10/ P17/ P15/ P14/ P13/P12/ P11/ P10/ P8/ N16/ N15/ N14/ N13/ N12/ N11/ N10/ N9/ M16/ M13/ M11/ M10/ M9/ L17/ L13/ L10/ L8/ K15/ K14/ K11/ K10/ J16/ J15/ J14/ J13/ J12/ J11/H16/ H14/ H11
vdds_sram	SRAM LDOs	W16	NA	U12	NA	AA12
vdds_mmc1	MMC IO power domain for CMD, CLK, and DAT(0..3)	K25	NA	N23	NA	N24
vdds_mmc1a	Power supply for MMC DAT [4..7]	P25	NA	P23	NA	H8
cap_vdd_sram_mpu _iva	SRAM LDO capacitance for VDDRAM1	V4	NA	N9	NA	U8
cap_vdd_sram_core	SRAM LDO capacitance for VDDRAM2	L21	NA	K20	NA	H17

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2.5.9 System and Miscellaneous Terminals

Table 2-26. System and Miscellaneous Signals Description

SIGNAL NAME	DESCRIPTION	TYPE(1)	BALL BOTTOM (CBB Pkg.)	BALL TOP (CBB Pkg.)	BALL BOTTOM (CBC Pkg.)	BALL TOP (CBC Pkg.)	BALL BOTTOM (CUS Pkg.)
sys_32k	32-kHz clock input	I	AE25	NA	AE20	NA	AA16
sys_xtalin	Main input clock. Oscillator input or LVCMOS at 19.2, 13, or 12 MHz.	I	AE17	NA	AF19	NA	AD15
sys_xtalout	Output of oscillator	O	AF17	NA	AF20	NA	AD14
sys_altclk	Alternate clock source selectable for GPTIMERs (maximum 54 MHz), USB (48 MHz), or NTSC/PAL (54 MHz)	I	J25	NA	J23	NA	A24
sys_clkreq	Request from OMAP3530/25 device for system clock (open source type)	IO	AF25	NA	W15	NA	Y13
sys_clkout1	Configurable output clock1	O	AG25	NA	AE14	NA	Y7
sys_clkout2	Configurable output clock2	O	AE22	NA	W11	NA	AA6
sys_boot0	Boot configuration mode bit 0	I	AH26	NA	F3	NA	AB12
sys_boot1	Boot configuration mode bit 1	I	AG26	NA	D3	NA	AC16
sys_boot2	Boot configuration mode bit 2	I	AE14	NA	C3	NA	AD17
sys_boot3	Boot configuration mode bit 3	I	AF18	NA	E3	NA	AD18
sys_boot4	Boot configuration mode bit 4	I	AF19	NA	E4	NA	AC17
sys_boot5	Boot configuration mode bit 5	I	AE21	NA	G3	NA	AB16
sys_boot6	Boot configuration mode bit 6	I	AF21	NA	D4	NA	AA15
sys_nrespwron	Power On Reset	I	AH25	NA	V13	NA	AA10
sys_nreswarm	Warm Boot Reset (open drain output)	IOD	AF24	NA	AD7	NA	Y10
sys_nirq	External FIQ input	I	AF26	NA	V16	NA	W16
sys_nvmode1	Indicates the voltage mode	O	AD26	NA	AD15	NA	Y16
sys_nvmode2	Indicates the voltage mode	O	AE26	NA	W16	NA	Y15
sys_off_mode	Indicates the voltage mode	O	AF22	NA	V12	NA	AD23
sys_ndmareq0	External DMA request 0 (system expansion). Level (active low) or edge (falling) selectable.	I	U8	NA	B6	NA	D2
sys_ndmareq1	External DMA request 1 (system expansion). Level (active low) or edge (falling) selectable.	I	T8 / J8	NA	B4 / C6	NA	F4 / C2
sys_ndmareq2	External DMA request 2 (system expansion). Level (active low) or edge (falling) selectable.	I	L3 / R8	NA	D1 / C4	NA	H2 / G5
sys_ndmareq3	External DMA request 3 (system expansion). Level (active low) or edge (falling) selectable.	I	K3 / P8	NA	D2 / B5	NA	G2 / F3
sys_secure_ indicator	MSECURE transactions indicator	O	AG9	NA	V2	NA	AD5
sys_drm_ msecure	MSECURE output	O	AF9	NA	AA4	NA	AC4

(1) Type = Ball type for this specific function (I = Input, O = Output, Z = high-impedance, D = Open Drain, DS = Differential, A = Analog)

2.5.10 Feed-Through Balls (CBC and CBB Packages)

Feed-through pins represent a wire. That is, they do not connect to the silicon die, but rather just connect from the bottom ball to the top ball. The purpose of these balls is to allow for different PoP packages. Table 2-27 and Table 2-28 list the feed-through balls on the OMAP35x CBC and CBB packages, respectively.

Table 2-27. CBC Package Feed-Through Balls

JEDEC 14x14mm, 0.65mm, 152ball	JEDEC DESCRIPTION (1)	BALL TOP	BALL BOTTOM	FEED-THROUGH BALL NAME
NC	No Connect	A1	A1	pop_a1_a1
d-vdd	DDR Supply	J1	L1	pop_j1_l1
NC	No Connect	AA1	AF1	pop_aa1_af1

(1) For more details on the feedthrough pin connections, please refer to the PoP memory datasheet.

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Table 2-27. CBC Package Feed-Through Balls (continued)

f-vdd	Flash Supply	N2	T2	pop_n2_t2
f-vdd	Flash Supply	T2	Y2	pop_t2_y2
NC	No Connect	W2	AE2	pop_w2_ae2
NC	No Connect	Y2	AF4	pop_y2_af4
f-vdd	Flash Supply	AA6	AF5	pop_aa6_af5
f-vdd	Flash Supply	Y7	AF8	pop_y7_af8
NC, Int	No Connect; Interrupt when using OneNAND POP	Y9	AF10	pop_y9_af10
f-nbe0, cle0	No Connect/CLE	AA10	AF12	pop_aa10_af12
d-vdd	DDR Supply/ POP FLASH vpp supply	AA11	AF13	pop_aa11_af13
d-tq	No Connect/ DDR die temperature sensor	AA12	AF14	pop_aa12_af14
vss	Shared Ground	AA13	AF15	pop_aa13_af15
d-vdd	DDR Supply	Y14	AF17	pop_y14_af17
d-vddq	DDR Supply	AA14	AF16	pop_aa14_af16
d-vdd	DDR Supply	B16	A20	pop_b16_a20
vss	Shared Ground	Y17	AF21	pop_y17_af21
d-vdd	DDR Supply	AA17	AF18	pop_aa17_af18
vss	Shared Ground	Y19	AF24	pop_y19_af24
d-vddq	DDR Supply	AA19	AF22	pop_aa19_af22
NC	No Connect	A20	A25	pop_a20_a25
NC	No Connect	Y20	AE25	pop_y20_ae25
NC	No Connect	AA20	AF25	pop_aa20_af25
NC	No Connect	A21	A26	pop_a21_a26
NC	No Connect	B21	B26	pop_b21_b26
d-vdd	DDR Supply	H21	K26	pop_h21_k26
d-vdd	DDR Supply	P21	U26	pop_p21_u26
NC	No Connect	Y21	AE26	pop_y21_ae26
NC	No Connect	AA21	AF26	pop_aa21_af26

Table 2-28. CBB Package Feed-Through Balls

JEDEC 12x12, 0.5mm, 168ball	JEDEC DESCRIPTION (1)	BALL TOP	BALL BOTTOM	FEED-THROUGH BALL NAME
d-vdd	DDR Supply	A12	A15	pop_a12_a15
d-vdd	DDR Supply	AA23	AE28	pop_aa23_ae28
d-vdd	DDR Supply	H23	AF28	pop_h23_af28
d-vdd	DDR Supply	K1	J28	pop_k1_j28
d-vdd	DDR Supply	Y23	M1	pop_y23_m1
f-vdd	Flash Supply	AA1	AA1	pop_aa1_aa1
f-vdd	Flash Supply	AC8	AF1	pop_ac8_af1
f-vdd	Flash Supply	AC13	AH10	pop_ac13_ah10
f-vdd	Flash Supply	L1	AH15	pop_l1_ah15
f-vdd	Flash Supply	U1	N1	pop_u1_n1
f-vpp	Flash vpp supply	AC11	AH13	pop_ac11_ah13
NC, int0	No Connect/PoP OneNAND interrupt	AB9	AG11	pop_ab9_ag11
NC, int1	No Connect/PoP OneNAND interrupt	AC9	AH11	pop_ac9_ah11
NC	No Connect	A1	A1	pop_a1_a1
NC	No Connect	A2	A2	pop_a2_a2
NC	No Connect	A22	A27	pop_a22_a27
NC	No Connect	A23	A28	pop_a23_a28

(1) For more details on the feedthrough pin connections, please refer to the PoP memory datasheet.

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Table 2-28. CBB Package Feed-Through Balls (continued)

NC	No Connect	AB1	AG1	pop_ab1_ag1
NC	No Connect	AB2	NA	NA
NC	No Connect	AB22	NA	NA
NC	No Connect	AB23	AG28	pop_ab23_ag28
NC	No Connect	AC1	AH1	pop_ac1_ah1
NC	No Connect	AC2	AH2	pop_ac2_ah2
NC	No Connect	AC22	AH27	pop_ac22_ah27
NC	No Connect	AC23	AH28	pop_ac23_ah28
NC	No Connect	B1	B1	pop_b1_b1
NC	No Connect	B2	NA	NA
NC	No Connect	B22	NA	NA
NC	No Connect	B23	B28	pop_b23_b28
f-rst#, rp#	Flash reset	AB11	AG13	pop_ab11_ag13
d-tq	DDR temperature alert	AC14	AH16	pop_ac14_ah16
vss	Shared Ground	AA2	AA2	pop_aa2_aa2
vss	Shared Ground	U2	AF2	pop_u2_af2
vss	Shared Ground	AA22	AF27	pop_aa22_af27
vss	Shared Ground	AB8	AG10	pop_ab8_ag10
vss	Shared Ground	AB13	AG15	pop_ab13_ag15
vss	Shared Ground	B12	B15	pop_b12_b15
vss	Shared Ground	H22	J27	pop_h22_j27
vss	Shared Ground	K2	M2	pop_k2_m2
vss	Shared Ground	K22	M26	pop_k22_m26
vss	Shared Ground	L2	N2	pop_l2_n2

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3 ELECTRICAL CHARACTERISTICS

3.1 Power Domains

The OMAP3530/25 device integrates enhanced features that dynamically adapt energy consumption according to application needs and performance requirements.

The OMAP3530/25 device includes an enhanced power-management scheme based on:

- Nine independent functional voltage domains on chip partitioning
- Multiple voltage domains
- Voltage scaling support
- Enhanced memory retention support
- Optimized device off mode
- Centralized management of power, reset, and clock

The external power supplies of OMAP3530/25 are:

- vdd_mpu _iva for the ARM and IVA2.2 processors
- vdd_core for macros
- vdds for IO macros
- vdds_mem for memory macros
- vdds_sram for SRAM LDOs
- vdds_dpll_dll for DLL IO
- vdds_dpll_per for peripheral DPLLs
- vdds_wkup_bg for wakeup LDO and VDDA (2 LDOs: SRAM and BandGap)
- vdda_dac for video DAC
- vdds_mmc1 and vdds_mmc1a for MMC IO
- The supply voltages are detailed in Table 3-3.

Figure 3-1 illustrates the power domains:

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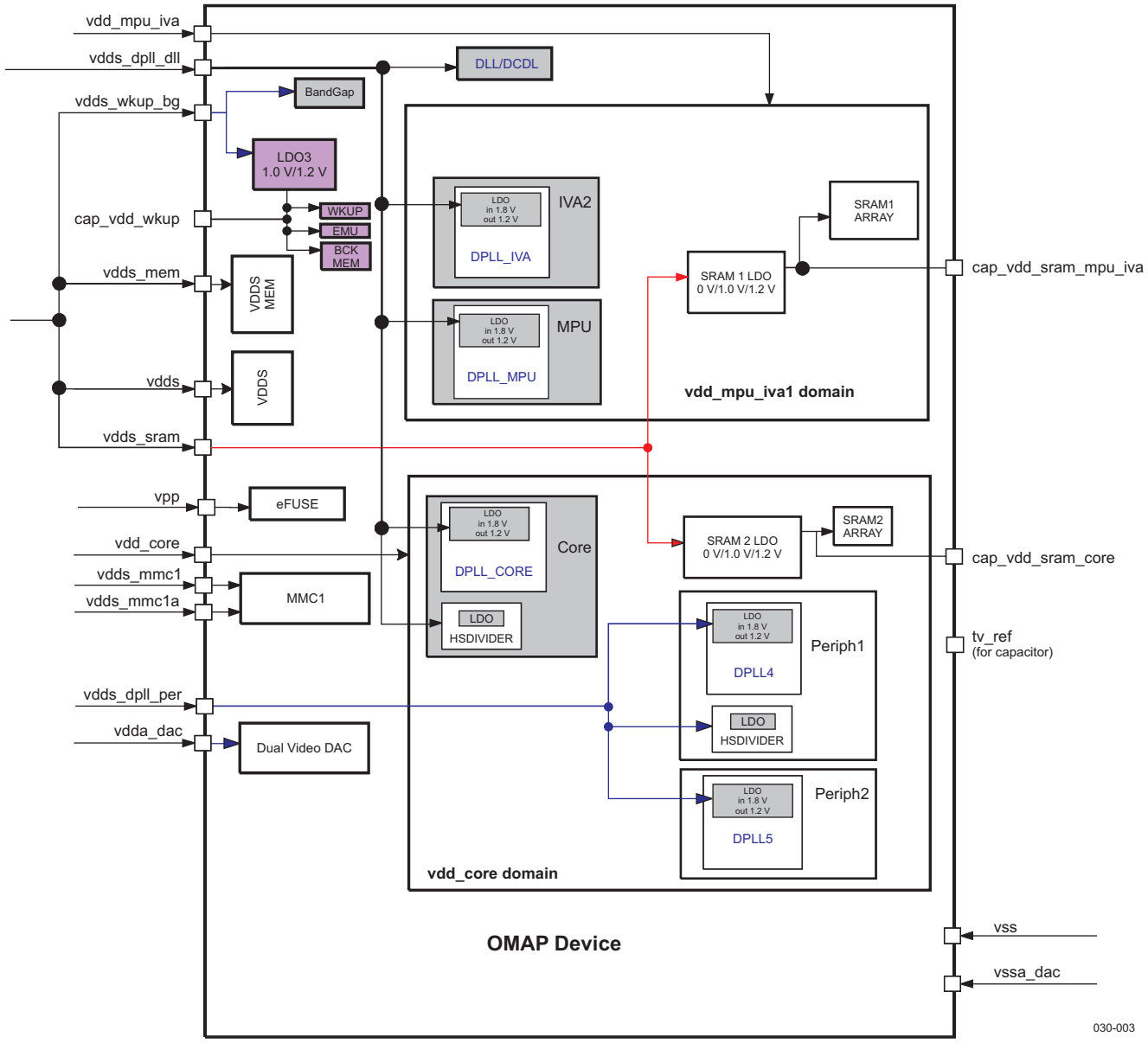

Figure 3-1. OMAP3530/25 Power Domains

This power domain segmentation switches off (or places in retention state) domains that are unused while keeping others active. This implementation is based on internal switches that independently control each power domain.

A power domain regular logic is attached to one of the device V_{DD} supplies through a primary domain switch. When the primary switch is open, most of the logic supply is off, resulting in a low-leakage state of the domain. Embedded switches are implemented for all power domains except the wake-up domain. This allows the domain to be powered off, if not being used, to give maximum power savings. For more information, see the PRCM chapter of the *OMAP35x Technical Reference Manual (TRM)* [literature number SPRUFA5].

All domain output signals at the interface between power domains are connected through isolation latch cells. These cells ensure a proper electrical isolation between the domains and an appropriate interface state at the domain boundaries.

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3.2 Absolute Maximum Ratings

The following table specifies the absolute maximum ratings over the operating junction temperature range of OMAP commercial and extended temperature devices. Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Notes:

- Logic functions and parameter values are not assured out of the range specified in the recommended operating conditions.
- The OMAP3530/25 device adheres to EIA/JESD22−A114, Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM). Minimum pass level for HBM is ±1 kV.

Table 3-1. Absolute Maximum Ratings Over Operating Junction Temperature Range

PARAMETER				MIN	MAX	UNIT
vdd_mpu _iva vdd_core	Supply voltage range for core macros			–0.5	1.6	V
vdds vdds_mem	Second supply voltage range for 1.8-V I/O macros			–0.5	2.25	V
vdds_mmc1	Supply voltage range for MMC1 CMD, CLK and DAT[3:0] and for memory stick I/Os		1.8-V mode	–0.5	2.45	V
			3.0-V mode	-0.5	3.50	
vdds_ vdds_mmc1a	Second supply voltage range for MMC1 DAT[7:4]		1.8-V mode	–0.5	2.45	V
			3.0-V mode	-0.5	3.50	
vdds_dpll_dll vdds_dpll_per	Supply voltage for DLL DPLL Supply voltage for Per DPLL			–0.5	2.10	V
vdds_sram vdds_wkup_bg	Supply voltage for SRAM LDOs Supply voltage for wakeup LDO and VDDA (2 LDOs SRAM and BG)			–0.5	2.25	V
V_{PAD}	Voltage range at PAD	MMC1, MS (Balls N28, M27, N27, N26, N25, P28) MMC1 (Balls P27, P26, R27, R25)	Supply voltage range for 1.8-V IOs	–0.54(1)	2.34(1)	
			Supply voltage range for 3.0-V IOs	–0.45(2)	3.45(2)	
		I2C1, I2C2, I2C3, I2C4 (Balls K21, J21, AF15, AE15, AF14, AG14, AD26, AE26)		–0.63(1)	2.73(1)	
		Crystal (xtalin/xtalout) (Balls AE17, AF17)		–0.5	2.71	
		Other balls		–0.5	vddsx(3) + 0.5	
vdda_dac	Supply voltage range for analog macros			–0.5	2.43	V
V_{ESD}	ESD stress voltage(4)	HBM (human body model)(5)	vdds_ MMC1a , mmc1_dat[7-4] (CBB pkg only)(6)		500	V
			Other pins		1000	
		CDM (charged device model)(7)	MMC1 signals (CBB pkg only) (6)		300	
			Other pins		500	
I_{IOI}	Current-pulse injection on each I/O pin(8)				200	mA
I_{clamp}	Clamp current for an input or output			–20	20	mA
T_{stg}	Storage temperature range(9)			–65	150	°C

(1) For a maximum time of 30% time period.
(2) For a maximum time of 15% time period.
(3) Depending on ball, vddsx can be vdds_mem or vdds.
(4) Electrostatic discharge (ESD) to measure device sensitivity/immunity to damage caused by electrostatic discharges into the device.
(5) JEDEC JESD22–A114F
(6) Corresponding signals: mmc1_dat0, mmc1_dat1, mmc1_dat2, mmc1_dat3, mmc1_dat4, mmc1_dat5, mmc1_dat6, mmc1_dat7, mmc1_clk, mmc1_cmd and vdds_mmc1 (CBB pkg only).
(7) JEDEC JESD22−C101D
(8) Each device is tested with I/O pin injection of 200 mA with a stress voltage of 1.5 times maximum vdd at room temperature.
(9) These temperatures extreme do not simulate actual operating conditions but exaggerate any faults that might exist.

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This section includes the maximum power consumption for each power domain (core, IVA2, etc.). Table 3-2 summarizes the power consumption at the ball level.

Table 3-2. Estimated Maximum Power Consumption At Ball Level

PARAMETER			MAX (T = 90°C)	MAX (T = 105°C)	UNIT
Signal	**Description**				
vdd_mpu_iva	Processors(1)	OMAP3530/25 (SmartReflex™ Enabled - OPP5)	994	1051	mA
		OMAP3530/25 (SmartReflex™ Disabled - OPP5)	1236	1317	mA
		OMAP3530 (SmartReflex™ Enabled - OPP6)	1177	1233	mA
		OMAP3530 (SmartReflex™ Disabled - OPP6)	1457	1538	mA
vdd_core	Core(1)	OMAP3530 (SmartReflex™ Enabled - OPP5/6)	439	489	mA
		OMAP3530 (SmartReflex™ Disabled - OPP5/6)	539	609	mA
		OMAP3525 (SmartReflex™ Enabled - OPP5)	353	403	mA
		OMAP3525 (SmartReflex™ Disabled - OPP5)	438	507	mA
vdda_dac	Video DAC		65	65	mA
vdss_dpll_dll	DLL + DPLL MPU, DSP, and core		25	25	mA
vdds_dpll_per	DPLL peripheral 1 and peripheral 2		15	15	mA
vdds_sram	Processors and core LDO (LDO1 and LDO2)		41	41	mA
vdds_wkup_bg	Bandgap, wakeup + LDO, EMU off		6	6	mA
vdds_mem	Standard I/Os (SDRC+GPMC)		37	37	mA
vdds	Standard I/Os (all excluding SDRC and GPMC)		63	63	mA
vdds_mmc1	MMC I/O(2)		20	20	mA
vdds_mmc1a	Power supply for MMC IO [DAT4 – DAT7]		2	2	mA
vpp	eFuse		50	50	mA

(1) OPP6 is only supported on high-speed grade OMAP3530 devices.
(2) MMC card and I/O card are not included.

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3.3 Recommended Operating Conditions

All OMAP3530/25 modules are used under the operating conditions contained in Table 3-3. The information in the notes below is provided solely for convenience and does not extend or modify the warranty provided under TI's standard terms and conditions for TI semiconductor products.

Note (POH Limitations):

To avoid significant device degradation for commercial temperature OMAP3530/OMAP3525 devices (0°C ≤ T_j ≤ 90°C), the device power-on hours (POH) must be limited to one of the following:

- 100K total POH when operating across all OPPs and keeping the time spent *at* OPP5-OPP6 to less than 23K POH.
- 50K total POH when operating at OPP5 - OPP6.
- 44K total POH with *no restrictions* to the proportion of these POH at operating points OPP1 - OPP6.

To avoid significant device degradation for extended temperature OMAP3530A/OMAP3525A devices (-40°C ≤ T_j ≤ 105°C), the following restrictions apply:

- OPP5 and OPP6 are not supported.*
- The total device POH must be limited to less than 50K.*

*If an extended temperature device is operated such that T_j never exceeds 90C (-40°C ≤T_j ≤ 90°C) then the OPP POH limits for commercial devices indicated above apply.

Note: Logic functions and parameter values are not guaranteed out of the range specified in the recommended operating conditions. The above notations cannot be deemed a warranty or deemed to extend or modify the warranty under TI's standard terms and conditions for TI semiconductor products.

Table 3-3. Recommended Operating Conditions

PARAMETER	DESCRIPTION		MIN	NOM	MAX	UNIT
V_{DD1} (vdd_mpu_iva), SmartReflex Disabled	OMAP processor logic supply	OPP6: Overdrive (1)	V_{DD1NOM} - (0.05*V_{DD1NOM})	1.35	V_{DD1NOM} + (0.05*V_{DD1NOM})	V
		OPP5: Overdrive	V_{DD1NOM} - (0.05*V_{DD1NOM})	1.35	V_{DD1NOM} + (0.05*V_{DD1NOM})	V
		OPP4: Mid-Overdrive	V_{DD1NOM} - (0.05*V_{DD1NOM})	1.27	V_{DD1NOM} + (0.05*V_{DD1NOM})	V
		OPP3: Nominal	V_{DD1NOM} - (0.05*V_{DD1NOM})	1.20	V_{DD1NOM} + (0.05*V_{DD1NOM})	V
		OPP2: Low-Power	V_{DD1NOM} - (0.05*V_{DD1NOM})	1.06	V_{DD1NOM} + (0.05*V_{DD1NOM})	V
		OPP1: Ultra Low-Power (2)	V_{DD1NOM} - (0.05*V_{DD1NOM})	0.985	V_{DD1NOM} + (0.05*V_{DD1NOM})	V
V_{DD2} (vdd_core) SmartReflex Disabled	OMAP core logic supply (3)	OPP3: Nominal	V_{DD2NOM} - (0.05*V_{DD2NOM})	1.15	V_{DD2NOM} + (0.05*V_{DD2NOM})	V
		OPP2: Low-Power	V_{DD2NOM} - (0.05*V_{DD2NOM})	1.06	V_{DD2NOM} + (0.05*V_{DD2NOM})	V
		OPP1: Ultra Low-Power (2)	V_{DD2NOM} - (0.05*V_{DD2NOM})	0.985	V_{DD2NOM} + (0.05*V_{DD2NOM})	V
vdds	Supply voltage for I/O macros		1.71	1.8	1.91	V
	Noise (peak-peak)				90	mVpp
vdds_mem	Supply voltage for memory I/O macros		1.71	1.8	1.89	V
	Noise (peak-peak)				90	mVpp
vdds_mmc1	Supply voltage range for MMC1 CMD, CLK and DAT[3:0] and for memory stick I/Os	1.8-V mode	1.71	1.8	1.89	V
		3.0-V mode	2.7	3.0	3.3	V

(1) OPP6 is only supported on high-speed grade OMAP3530/25 devices.
(2) Cannot boot in OPP1. If OPP1 is desired, boot in higher OPP then switch to OPP1.
(3) Core logic includes interconnect, graphics processor, and peripherals.

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Table 3-3. Recommended Operating Conditions (continued)

PARAMETER	DESCRIPTION		MIN	NOM	MAX	UNIT
vdds_mmc1a	Second supply voltage range for MMC1 DAT[7:4]	1.8-V mode	1.71	1.8	1.89	V
		3.0-V mode	2.7	3.0	3.3	
vdds_wkup_bg	Wakeup LDO		1.71	1.8	1.89	V
	Noise (peak-peak)				50	mVpp
vdda_dac	Analog supply voltage for video DAC		1.71	1.8	1.89	V
	Noise (peak-peak)	For a frequency of 0 to 100 kHz (For a frequency < 100 kHz, decreases 20dB / sec)			30	mVpp
vdds_sram	SRAM LDOs		1.71	1.8	1.89	V
	Noise (peak-peak)				50	mVpp
vdds_dpll_per	Peripherals DPLLs power supply		1.71	1.8	1.89	V
	Noise (peak-peak)				36	mVpp
vdds_dpll_dll	Supply voltage for DPLLs I/Os		1.71	1.8	1.89	V
	Noise (peak-peak)				30	mVpp
vpp(4)	eFuse programming					V
vss	Ground		0	0	0	V
vssa_dac	Dedicated ground for DAC		0	0	0	V
T_a	Operating free air temperature range	Commercial Temperature	0	–	70	°C
		Extended Temperature	-40	-	85	
T_j	Operating junction temperature(5)	Commercial Temperature	0	–	90	°C
		Extended Temperature	-40	-	105	

(4) It is recommended not to connect this pin. It is just used for eFuse programming on package unit.
(5) For proper device operation, Tj must be within the specified range.

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3.4 DC Electrical Characteristics

Table 3-4 summarizes the dc electrical characteristics.

Table 3-4. DC Electrical Characteristics

PARAMETER			MIN	NOM	MAX	UNIT
LVCMOS Pin Buffers - CBB: N28, M27, N27, N26, N25, P28,P27, P26, R27, R25/ CBC: N19, L18, M19, M18, K18, N20, M20, P17, P18, P19/ CUS: M23, L23, M22, M21, M20, N23						
V_{IH}	High-level input voltage	vdds(1) = 1.8 V	0.65 × vdds(1)		vdds + 0.3	V
		vdds(1) = 3.0 V	0.625 × vdds(1)		vdds + 0.3	
V_{IL}	Low-level input voltage	vdds(1) = 1.8 V	–0.3		0.35 × vdds	V
		vdds(1) = 3.0 V	–0.3		0.25 × vdds	
V_{OH}	High-level output voltage(2)	vdds(1) = 1.8 V	vdds(1) – 0.2			V
		vdds(1) = 3.0 V	0.75 × vdds(1)			
V_{OL}	Low-level output voltage(2)	vdds(1) = 1.8 V			0.2	V
		vdds(1) = 3.0 V			0.125 × vdds(1)	
t_T	Input transition time (rise time, t_R or fall time, t_F evaluated between 10% and 90% at PAD)	Normal Mode			10	ns
		High-Speed Mode			3	
LVDS/CMOS Pin Buffers - CBB: AG19, AH19, AG18, AH18, AG17, AH17/ CBC: AE16, AE15, AD17, AE18, AD16, AE17/ CUS: AB18, AC18						
Low-Power Receiver (LP-RX)						
V_{IL}	Low-level input threshold				500	mV
V_{IH}	High-level input threshold		800			mV
V_{HYS}	Input hysteresis		25			mV
Ultralow-Power Receiver (ULP-RX)						
$V_{IL-ULPM}$	Low-level input threshold, ULPM				300	mV
V_{IH}	High-level input threshold		880			mV
High-Speed Receiver (HS-RX)						
V_{IDTH}	Differential input high threshold		70			mV
V_{IDTL}	Differential input low threshold				–70	mV
V_{IDMAX}	Maximum differential input voltage				270	mV
V_{ILHS}	Single-ended input low voltage		–40			mV
V_{IHHS}	Single-ended input high voltage				460	mV
V_{CMRXDC}	Common-mode voltage		70		330	mV
LVDS/CMOS Pin Buffers - CBB: K28, L28, K27, L27/ CBC: P25, P26, N25, N26 / CUS: L24, K24, J23, K23						
V_{CM}	Input common mode voltage range		600	900	1200	mV
Vos	Receiver Input dc offset		–20		20	mV
Vid	Receiver input differential amplitude		70	100	200	mV(3)
t_T	Input transition time (rise time, t_R or fall time, t_F evaluated between 10% and 90% at PAD)		267		533	ps
LVDS/CMOS Pin Buffers - CBB: AG22, AH22, AG23, AH23, AG24, AH24/ CBC: AE21, AE22, AE23, AE24, AD23, AD24 / CUS: AC19, AB19, AD20, AC20, AD21, AC21						
High-Speed Transceiver (HS-TX)						
V_{OHHS}	HS output high voltage				360	mV
$\|V_{OD}\|$	HS transmit differential voltage		140	200	270	mV
V_{CMTX}	HS transmit static common mode voltage		150	200	250	mV
Low-Power Transceiver (LP-TX)						

(1) This global value may be overridden on a per interface basis if another value is explicitly defined for that interface (for example, I^2C).
(2) With 100 µA sink / source current at vddsxmin.
(3) Corresponds to peak-to-peak values: minimum = 140 mV_{pp}; nominal = 200 mV_{pp}; maximum = 400 mV_{pp}.

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Table 3-4. DC Electrical Characteristics (continued)

PARAMETER			MIN	NOM	MAX	UNIT
V_{OL}	Thevenin output low level		–50		50	mV
V_{OH}	Thevenin output high level		1.1	1.2	1.3	V
Low-Power Receiver (LP-RX)						
V_{IL}	Low-level input threshold				550	mV
V_{IH}	High-level input threshold		880			mV
V_{HYST}	Input hysteresis		25			mV
Ultralow-Power Receiver (ULP-RX)						
$V_{IL-ULPS}$	Low-level input threshold, ULPM				300	mV
V_{IH}	High-level input threshold		880			mV
subLVDS/CMOS Pin Buffers - CBB: AA27, AA28, AB27, AB28, AD27, AD28, AC28, AC27/ CBC: AC26, AD26, AA25, Y25, AA26, AB26, AC25, AB25/ CUS: V22, W22, Y22, AB22, AC23, AC22, W21, V21						
Vod	Differential voltage range @ R_L = 100 Ω		100	150	200	mV
Vocm	Common mode voltage range		0.8	0.9	1	V
t_T	Input transition time (Vod rise time, t_R or Vod fall time, t_F evaluated between 20% and 80% at PAD)		200		500	ps
Standard LVCMOS Pin Buffers						
V_{IH} (4)	High-level input voltage (Standard LVCMOS)		0.65 × vdds		vdds + 0.3	V
V_{IL} (4)	Low-level input voltage (Standard LVCMOS)		- 0.3		0.35 × vdds	V
V_{HYS}	Hysteresis voltage at an input(5)			0.1		V
V_{OH}	High-level output voltage, driver enabled, pullup or pulldown disabled	$I_O = I_{OH}$ or I_O = –2 mA	vdds – 0.45			V
		$I_O = I_{OH}$ < |–2| mA	vdds – 0.40			
V_{OL}	Low-level output voltage with , driver enabled, pullup or pulldown disabled	$I_O = I_{OL}$ or I_O = 2 mA			0.45	V
		$I_O = I_{OL}$ < 2 mA			0.40	
t_T	Input transition time (rise time, t_R or fall time, t_F evaluated between 10% and 90% at PAD)		0		10(6)	ns
I_I	Input current with $V_I = V_I$ max		–1		1	µA
I_{OZ}	Off-state output current for output in high impedance with driver only, driver disabled		–20		20	µA
	Off-state output current for output in high impedance with driver/receiver/pullup only, driver disabled, pullup not inhibited			–100		
	Off-state output current for output in high impedance with driver/receiver/pulldown only, driver disabled, pulldown not inhibited			100		
I_Z	Total leakage current through the PAD connection of a driver/receiver combination that may include a pullup or pulldown. The driver output is disabled and the pullup or pulldown is inhibited.		– 20		20	µA
LVCMOS Open-Drain Pin Buffers Dedicated to I2C IOs - CBB: K21, J21, AF14, AG14, AF15, AE15, AD26, AE26/ CBC: J25, J24, C2, C1, AB4, AC4, AD15, W16, A21, C21/ CUS: K20, K21, AC13, AC12, AC15, AC14, Y16, Y15						
V_{IH}	High level input voltage		0.7 x vdds		vdds + 0.5	V
V_{IL}	Low level input voltage		- 0.5		0.3 x vdds	V
V_{OL}	Low-level output voltage open-drain at 3-mA sink current		0		0.2 x vdds	V
I_I	Input current at each I/O pin with an input voltage between 0.1 x vdds to 0.9 x vdds		- 10		10	µA
C_I	Capacitance for each I/O pin				10	pF

(4) V_{IH}/V_{IL} (Standard LVCMOS) parameters are applicable for sys_altclk input clocks.
(5) V_{hys} is the magnitude of the difference between the positive-going threshold voltage V_{T+} and the negative-going voltage V_{T-}.
(6) This global value may be overridden on a per interface basis if another value is explicitly defined for that interface (for example, I^2C).

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Table 3-4. DC Electrical Characteristics (continued)

PARAMETER			MIN	NOM	MAX	UNIT
T_{OF}	Output fall time from V_{IHmin} to V_{ILmax} with a bus capacitance C_B from 10 pF to 400 pF	Fast mode	20 + 0.1C_B		250	ns
		Standard mode			250	
	Output fall time with a capacitive load from 10 pF to 100 pF at 3-mA sink current	High-speed mode	10		40	
	Output fall time with a capacitive load of 400 pF at 3-mA sink current		20		80	
	Output fall time with a capacitive load of 40 pF (for CBUS compatibility)				20	
LVCMOS Open-Drain Pin Buffers Dedicated in GPIO mode - CBB: AF15, AE15, AF14, AG14, AD26, AE26 / CBC: C2, C1, AB4, AC4, AD15, W16, A21, C21/ CUS: AC15, AC14, AC13, AC12, Y16, Y15						
V_{IH}	High-level input voltage		0.7 x vdds		vdds + 0.5	V
V_{IL}	Low-level input voltage		- 0.5		0.3 x vdds	V
V_{OH}	High-level output voltage at 4-mA sink current		vdds - 0.45			V
V_{OL}	Low-level output voltage at 4-mA sink current				0.45	V

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3.5 Core Voltage Decoupling

For module performance, decoupling capacitors are required to suppress the switching noise generated by high frequency and to stabilize the supply voltage. A decoupling capacitor is most effective when it is close to the device because this minimizes the inductance of the circuit board wiring and interconnects.

Table 3-5 summarizes the power supplies decoupling characteristics.

Table 3-5. Core Voltage Decoupling Characteristics

PARAMETER	MIN	TYP	MAX	UNIT
Cvdd_mpu _iva (1)	50	100	120	nF
Cvdd_core(1)	50	100	120	nF
Cvdds_sram		100		nF
Ccap_vdd_sram_mpu _iva	0.7	1.0	1.3	µF
Ccap_vdd_sram_core	0.7	1.0	1.3	µF
Ccap_vdd_wkup	0.7	1.0	1.3	µF
Cvdds_wkup_bg		100		nF
Cvdds_dpll_dll		100		nF
Cvdds_dpll_per		100		nF
Cvdda_dac		100		nF
Ccap_vdd_d	100		200	nF
Cvdds_mmc1		100		nF
Cvdds_mmc1a		100		nF
Cvdds		100		nF
Cvdds_mem		100		nF

(1) 1 capacitor per 2 to 4 balls

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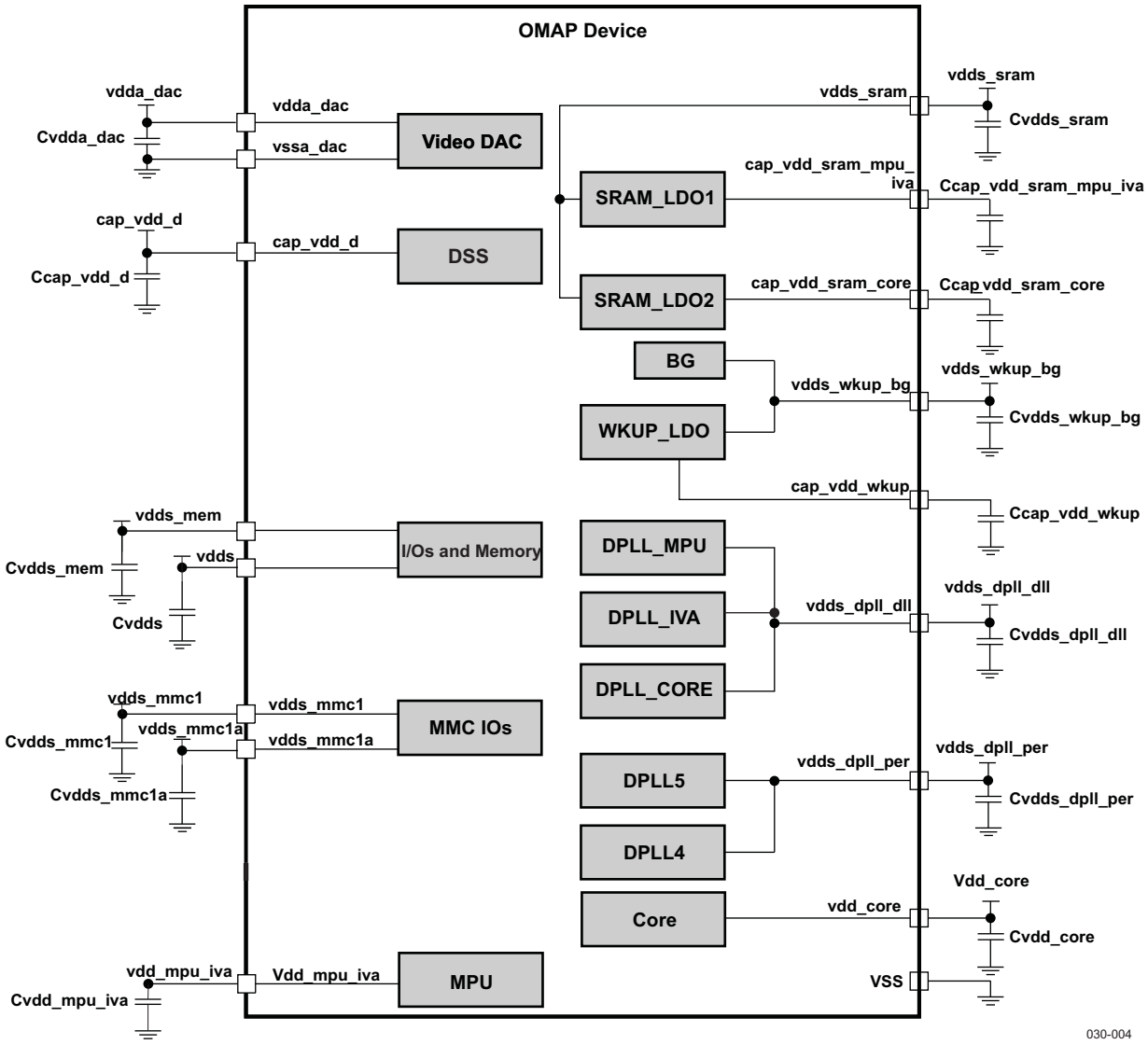
illustrates an example of power supply decoupling.



A. Signals "vdds" and "vdds_mem" are combined with "vdds" on the CBC package.
B. Signals "vdds" and "vdds_mem" are separate on the CBB and CUS packages.

Figure 3-2. Power Supply Decoupling

3.6 Power-up and Power-down

This section provides the timing requirements for the OMAP3530/25 hardware signals.

3.6.1 Power-up Sequence

The following steps give an example of power-up sequence supported by the OMAP3530/25 device.

1. vdds and vdds_mem are ramped ensuring a level on the IO domain and sys_nrespwron must be low. At the same time, vdds_sram and vdds_wkup_bg can also be ramped.
2. Once vdds_wkup_bg rail is stabilized, vdd_core can be ramped.
3. Once vdd_core is stabilized, then vdd_mpu _iva can be ramped.
4. vdds_dpll_dll and vdds_dpll_per rails can be ramped at any time during the above sequence.
5. sys_nrespwron can be released as soon as the vdds_pll_dll rail is stabilized, and sys_xtalin and sys_32k clocks are stabilized.
6. During the whole sequence above, sys_nreswarm is held low by OMAP3530/25. sys_nreswarm is released after the eFuse check has been performed; that is, after sys_nrespwron is released.
7. The other power supplies can then be turned on upon software request.

shows the power-up sequence.

Notes:

- If an external square clock is provided, it could be started after sys_nrespwron release provided it is clean: no glitch, stable frequency, and duty cycle.
- Higher voltage can be used. OPP voltage values may change following the silicon characterization result.

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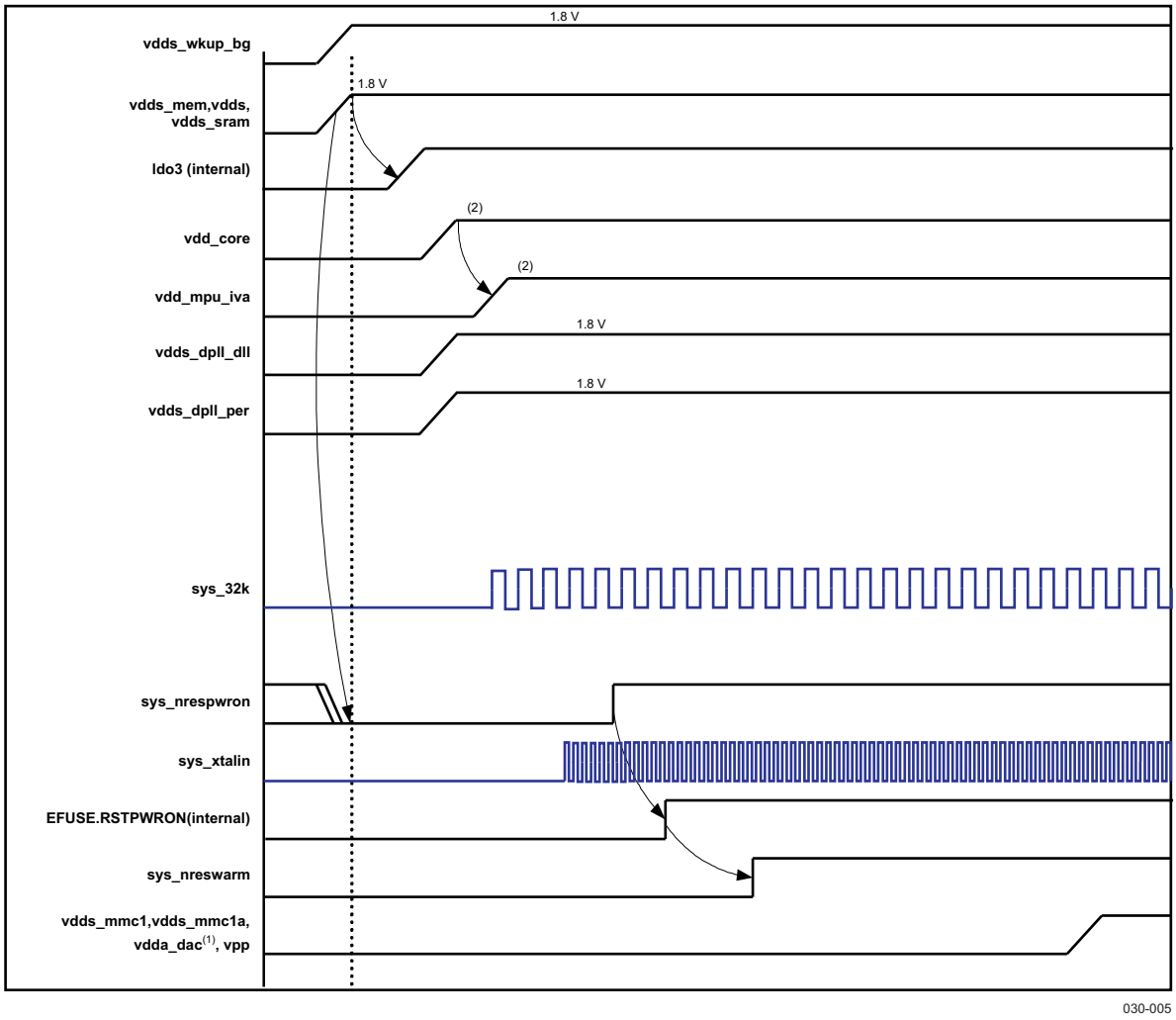

Figure 3-3. Power-up Sequence

3.6.2 Power-down Sequence

The following steps give an example of the power-down sequence supported by the OMAP3530/25 device.

1. Reset OMAP3530/25 device.
2. Stop all signals driven to OMAP3530/25 balls.
3. Option 1: Power down all domains simutaneously.
4. Option 2: If all domains cannot be powered down simultaneously, follow the below sequence:
   (a) Power off all complex I/O domains (vdds_mmc1, vdds_mmc1a, vdda_dac)
   (b) Power off all core domains (vdd_core, vdd_mpu _iva)
   (c) Power off all PLL domains (vdds_dpll_dll, vdds_dpll_per)
   (d) Power off all SRAM LDOs (vdds_sram)
   (e) Power off all reference domains (vdds_wkup_bg)
   (f) Power off all standard I/O domains (vdds, vdds_mem)

The OMAP3530/25 device proceeds with the power-down sequence shown in .

Note: Another possible power-down sequence:

- vdd_mpu _iva shuts down before vdd_core.
- vdds_sram, vdds_wkup_bg, vdds, and vdds_mem shut down simultaneously.
- vdds_dpll_dll and vdds_dpll_per shut down anytime between all complex IO domains shut down and vdds_sram shuts down.

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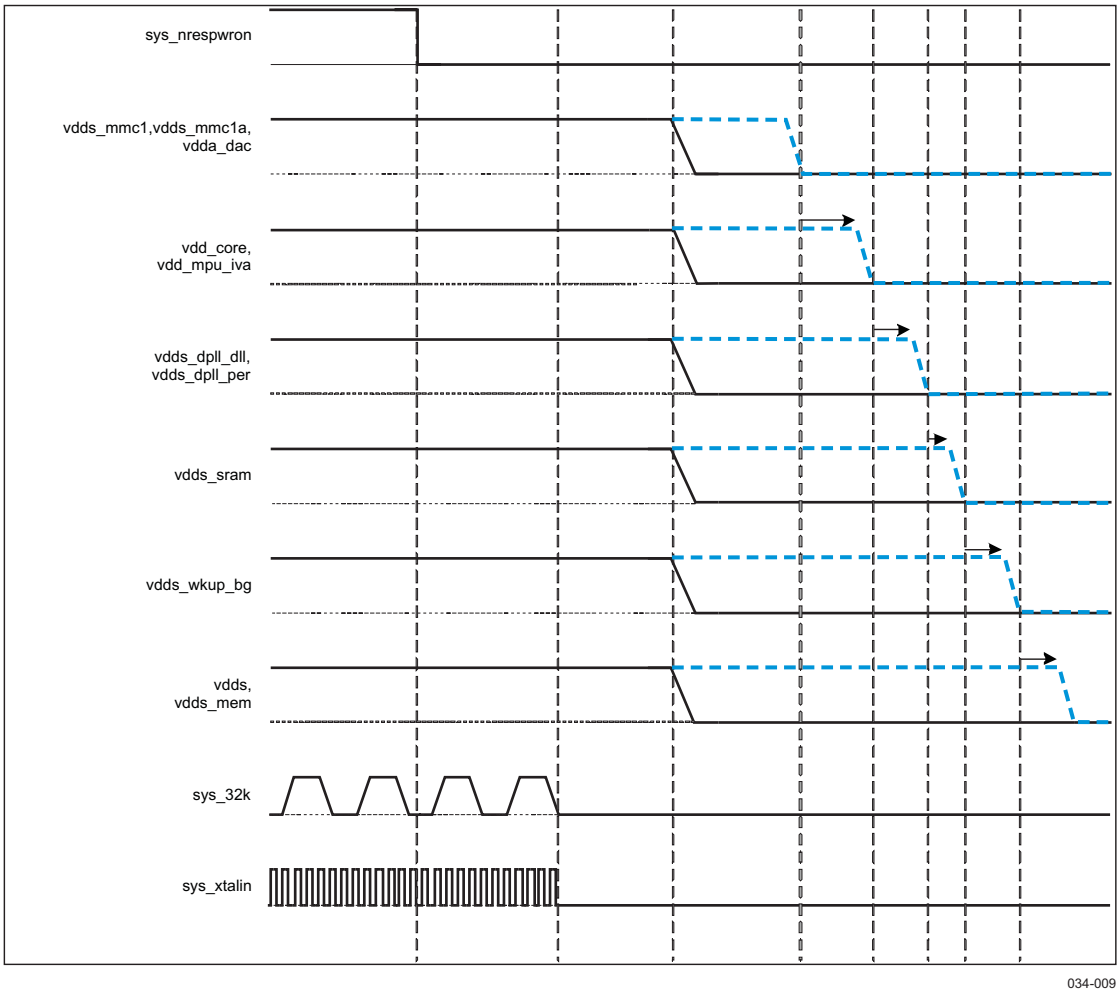

Figure 3-4. Power-down Sequence

4 CLOCK SPECIFICATIONS

The OMAP3530/25 device has three external input clocks, a low frequency (sys_32k), a high frequency (sys_xtalin), and an optional (sys_altclk). The OMAP3530/25 device has two configurable output clocks, sys_clkout1 and sys_clkout2.

Figure 4-1 shows the interface to the external clock sources and clock outputs.

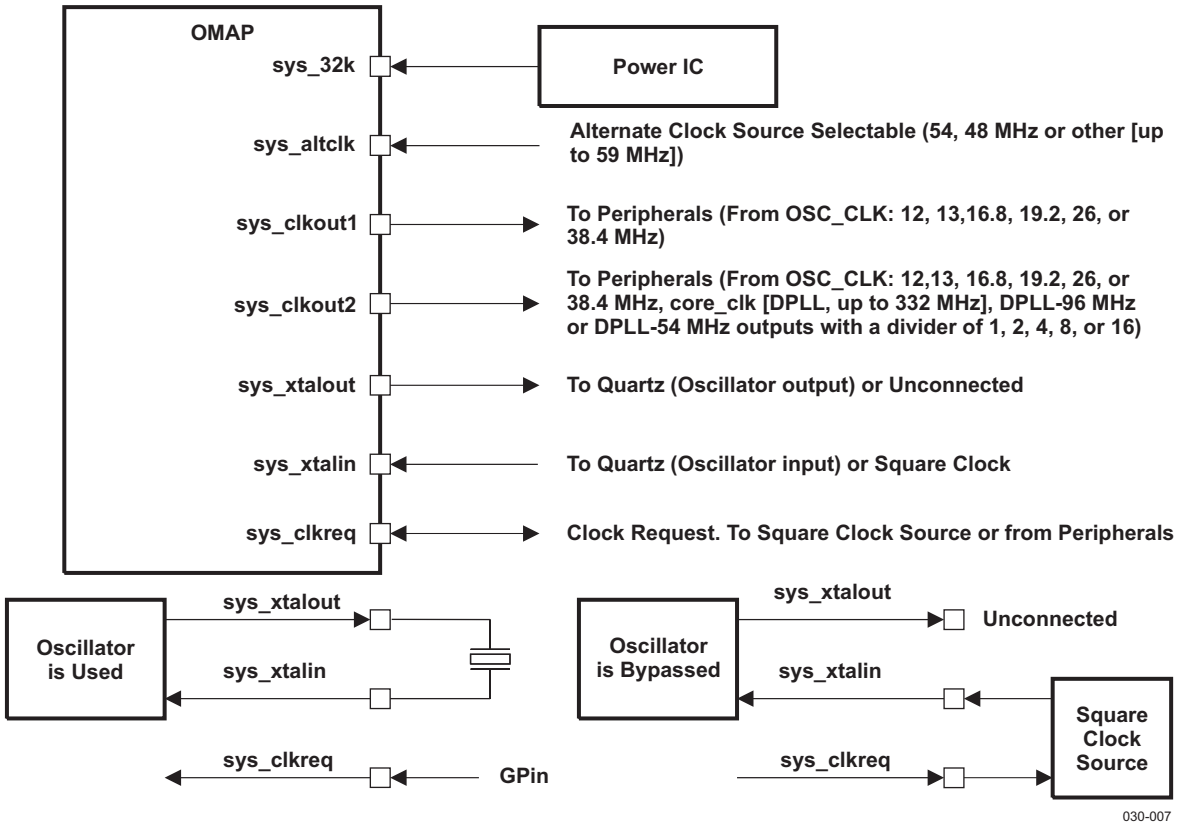

Figure 4-1. Clock Interface

The OMAP3530/25 device operation requires the following three input clocks:

- The 32-kHz frequency is used for low frequency operation. It supplies the wake-up domain for operation in lowest power mode (off mode). This clock is provided through the sys_32k pin.
- The system alternative clock can be used (through the sys_altclk pin) to provide alternative 48 or 54 MHz or other clock source (up to 59 MHz).
- The system clock input (12, 13, 16.8, 19.2, 26, or 38.4 MHz) is used to generate the main source clock of the OMAP3530/25 device. It supplies the DPLLs as well as several OMAP modules. The system clock input can be connected to either:
  - A crystal oscillator clock managed by sys_xtalin and sys_xtalout. In this case, the sys_clkreq is used as an input (GPIN).
  - A CMOS digital clock through the sys_xtalin pin. In this case, the sys_clkreq is used as an output to request the external system clock.

The OMAP3530/25 outputs externally two clocks:

- sys_clkout1 can output the oscillator clock (12, 13, 16.8, 19.2, 26, or 38.4 MHz) at any time. It can be controlled by software or externally using sys_clkreq control. When the device is in the off state, the sys_clkreq can be asserted to enable the oscillator and activate the sys_clkout1 without waking up the device. The off state polarity of sys_clkout1 is programmable.

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- sys_clkout2 can output the oscillator clock (12, 13, 16.8, 19.2, 26, or 38.4 MHz), core_clk (core DPLL output), 96 MHz or 54 MHz. It can be divided by 2, 4, 8, or 16 and its off state polarity is programmable. This output is active only when the core power domain is active.

For more information on the OMAP3530/25 Applications Processor clocking structure, see the Power, Reset, and Clock management (PRCM) chapter of the *OMAP35x Applications Processor TRM* (literature number SPRUFA5).

4.1 Input Clock Specifications

The clock system accepts three input clock sources:

- 32-kHz digital CMOS clock
- Crystal oscillator clock or CMOS digital clock (12, 13, 16.8, 19.2, 26, or 38.4 MHz)
- Alternate clock (48 or 54 MHz, or other up to 59 MHz)

4.1.1 Clock Source Requirements

Table 4-1 illustrates the requirements to supply a clock to the OMAP3530/25 device.

Table 4-1. Clock Source Requirements

PAD	CLOCK FREQUENCY		STABILITY	DUTY CYCLE	JITTER	TRANSITION
sys_xtalout sys_xtalin	12, 13, 16.8, or 19.2 MHz	Crystal	± 25 ppm	na	na	na
	12, 13, 16.8, 19.2, 26, or 38.4 MHz	Square	± 50 ppm	45% to 55%	< 1%	< 3.6 ns
sys_altclk	48,54 or up to 59 MHz		± 50 ppm	40% to 60%	< 1%	< 5 ns

4.1.2 External Crystal Description

To supply a 12-, 13-, 16.8-, or 19.2-MHz clock to the OMAP3530/25, an external crystal can be connected to the sys_xtalin and sys_xtalout pins. Figure 4-2 describes the crystal implementation.

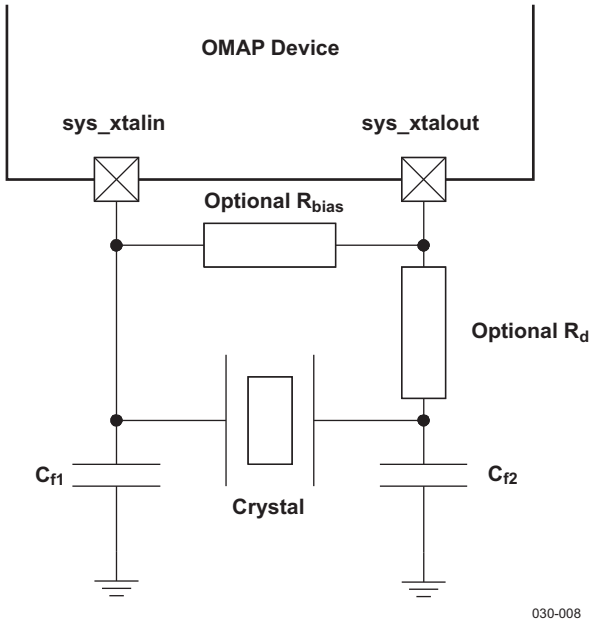

Figure 4-2. Crystal Implementation(1) (2) (3) (4)

(1) On the PCB, the oscillator components (crystal, foot capacitors, optional R_{bias} and R_d) must be located close to the package. All these components must be routed first with the lowest possible number of board vias.

(2) An optional resistor R_d can be added in series with the crystal to debug or filter the harmonics; a footprint must be reserved on the PCB for use with 10-MHz crystals and feature low-drive levels.

(3) A 120-kΩ internal bias resistor R_{bias} is used. The feedback resistor R_{bias} provides negative feedback to the oscillator to put it in the

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linear operating region; thus oscillation begins when power is applied.

(4) C_{f1} and C_{f2} represent the total capacitance of the PCB and components excluding the power IC and crystal. Their values in fact depend on the crystal datasheet. In the datasheet of the crystal, the frequency is specified at a specific load capacitor value which is the equivalent capacitor of the two capacitors C_{f1} and C_{f2} connected to sys_xtalin and sys_xtalout. The frequency of the oscillations depends on the value of the capacitors (10 pF corresponds to a load capacitor of 5 pF for the crystal).

The crystal must be in the fundamental mode of operation and parallel resonant. Table 4-2 summarizes the required electrical constraints.

Table 4-2. Crystal Electrical Characteristics

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
f_p	Parallel resonance crystal frequency(1)	12, 13, 16.8, or 19.2			MHz
C_L	Load capacitance for crystal parallel resonance	5		20	pF
ESR12&13	Crystal ESR (12 and 13 MHz)(1)			80	Ω
ESR16.8&19.2	Crystal ESR (16.8 and 19.2 MHz)(2)			50	Ω
C_o	Crystal shunt capacitance	1		7	pF
L_m	Crystal motional inductance for f_p = 12 MHz			35	mH
C_m	Crystal motional capacitance	5		100	fF
DL	Crystal drive level			0.5	mW
R_{bias}	Internal bias resistor	30	120	300	kΩ

(1) Measured with the load capacitance specified by the crystal manufacturer. This load is defined by the foot capacitances tied in series. If C_L = 20 pF, then both foot capacitors will be $C_{f1} = C_{f2}$ = 40 pF. Parasitic capacitance from package and board must also be taken in account.

(2) Measured with the load capacitance specified by the crystal manufacturer. This load is defined by the foot capacitances tied in series. If C_L = 20 pF, then both foot capacitors will be $C_{f1} = C_{f2}$ = 40 pF. Parasitic capacitance from package and board must also be taken in account.

$$ESR = R_m \left(1 + \frac{C_0}{C_L}\right)^2$$

When selecting a crystal, the system design must take into account the temperature and aging characteristics of a crystal versus the user environment and expected lifetime of the system. Table 4-3 details the switching characteristics of the oscillator and the input requirements of the 12-, 13-, 16.8-, or 19.2-MHz input clock.

Table 4-3. Base Oscillator Switching Characteristics

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
f_p	Oscillation frequency	12, 13, 16.8, or 19.2			MHz
t_{sx}	Start-up time(1) (2)	8			ms

(1) Start-up time defined as time interval between oscillator control signal release and sys_xtalin amplitude at 50% of its final value (vdd and vdds supplies ramped and stable). The start-up time can be performed in function of the crystal characteristics. 8-ms minimum only when using the internal oscillator; it is programmable after reset for wake-up. At power-on reset, the time is adjustable using the pin itself. The reset must be released when the oscillator or clock source is stable. Before the processor boots up and the oscillator is set to bypass mode, there is a start-up time when the internal oscillator is in application mode and receives a square wave. The start-up time in this case is about 100 µs.

(2) For f_p = 12 or 13 MHz: C_L = 13.5 pF and L_m = 35 mH
For f_p = 16.8 or 19.2 MHz: C_L = 9 pF and L_m = 15 mH

4.1.3 Clock Squarer Input Description

A 1.8-V CMOS clock squarer is another source that can supply a 12-, 13-, 16.8-, 19.2-, 26-, or 38.4-MHz clock to the OMAP3530/25. An analog clock squarer function converts a low-amplitude sinusoidal clock into a low-jitter digital signal. It can be connected to input pin sys_xtalin (sys_xtalout unconnected). Figure 4-3 illustrates the effective connections.

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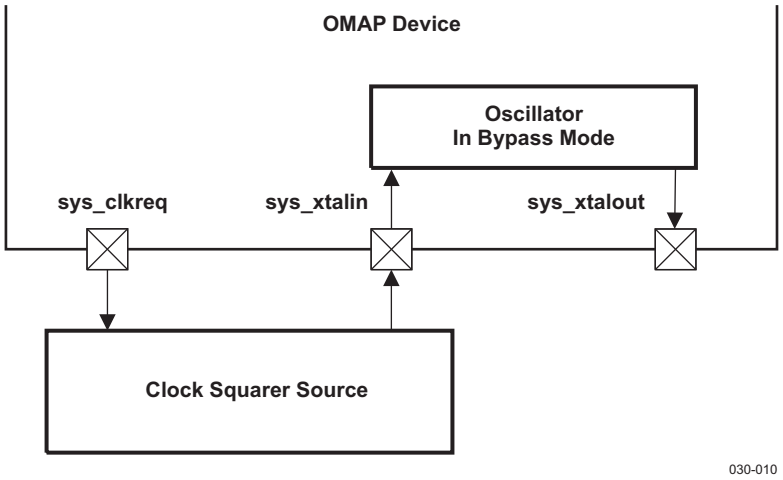

Figure 4-3. Clock Squarer Source Connection

To connect a digital clock source, the oscillator is configured in bypass mode. The sys_clkreq pin is an OMAP3530/25 output which can be used to switch the clock source on or off.

1. Pin sys_xtalout is not used in this mode. It must be left unconnected.
2. Once the system is powered up, the clock squarer source or crystal oscillator source can be applied; however, this affects the performance. The input source must be configured after power up to attain the desired system requirements.

Table 4-4 summarizes the electrical constraints required by the clock squarer used in the fundamental mode of operation.

Note: There is an internal pulldown resistor of 5k Ω (max.) on sys_xtalin when the oscillator is disabled.

Table 4-4. Base Oscillator Electrical Characteristics (in Bypass Mode)

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
f	Frequency(1)	12, 13, 16.8, 19.2, 26, or 38.4			MHz
t_{sx}	Start-up time		(2)		ms
I_{DDQ}	Current consumption on VDDS when sys_xtalin = 0 and in power-down mode			1	µA

(1) Measured with the load capacitance specified by the manufacturer. Parasitic capacitance from package and board must also be taken in account.
(2) Before the processor boots up and the oscillator is set to bypass mode, there is a start-up time when the internal oscillator is in application mode and receives a square wave. The start-up time in this case is about 100 µs.

Table 4-5 details the input requirements of the 12-, 13-, 16.8-, 19.2-, 26-, or 38.4-MHz input clock.

Table 4-5. 12-, 13-, 16.8-, 19.2-, 26-, or 38.4-MHz Input Clock Squarer Timing Requirements

NAME	DESCRIPTION		MIN	TYP	MAX	UNIT
OCS0	1 / $t_{c(xtalin)}$	Frequency, sys_xtalin	12, 13, 16.8, 19.2, 26, or 38.4			MHz
OCS1	$t_{w(xtalin)}$	Pulse duration, sys_xtalin low or high	0.45 * $t_{c(xtalin)}$		0.55 * $t_{c(xtalin)}$	ns
OCS2	$t_{J(xtalin)}$	Peak-to-peak jitter(1), sys_xtalin	–1%		1%	
OCS3	$t_{R(xtalin)}$	Rise time, sys_xtalin			3.6	ns
OCS4	$t_{F(xtalin)}$	Fall time, sys_xtalin			3.6	ns
OCS5	$t_{J(xtalin)}$	Frequency stability, sys_xtalin			±25	ppm

(1) Peak-to-peak jitter is defined as the difference between the maximum and the minimum output periods on a statistical population of 300 period samples. The sinusoidal noise is added on top of the vdds supply voltage.

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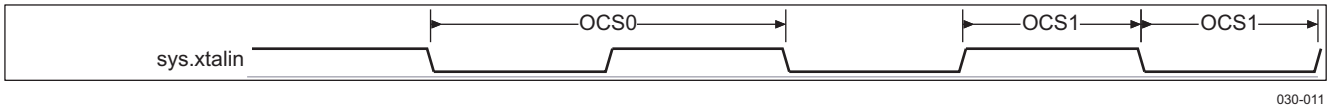

Figure 4-4. Crystal Oscillator in Bypass Mode

4.1.4 External 32-kHz CMOS Input Clock

A 32.768-kHz clock signal (often abbreviated to 32-kHz) can be supplied by an external 1.8-V CMOS signal on pin sys_32k.

Table 4-6 summarizes the electrical constraints imposed to the clock source.

Table 4-6. 32-kHz Input Clock Source Electrical Characteristics

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
f	Frequency	32.768			kHz
C_I	Input capacitance		0.44		pF
R_I	Input resistance	0.25		10^6	GΩ

Table 4-7 details the input requirements of the 32-kHz input clock.

Table 4-7. 32-kHz Input Clock Source Timing Requirements(1)

NAME	DESCRIPTION		MIN	TYP	MAX	UNIT
CK0	1 / $t_{c(32k)}$	Frequency, sys_32k		32.768		kHz
CK3	$t_{R(32k)}$	Rise time, sys_32k			20	ns
CK4	$t_{F(32k)}$	Fall time, sys_32k			20	ns
CK5	$t_{J(32k)}$	Frequency stability, sys_32k			±200	ppm

(1) See Table 3-4, *Electrical Characteristics*, Standard LVCMOS IOs part for sys_32k V_{IH}/V_{IL} parameters.

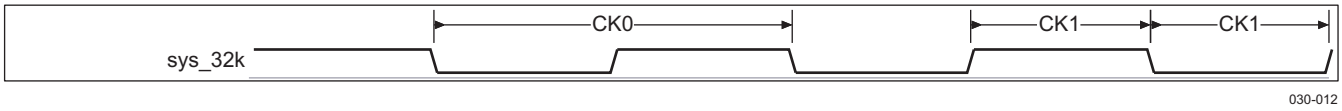

Figure 4-5. 32-kHz CMOS Clock

4.1.5 External sys_altclk CMOS Input Clock

A 48-, 54-, or up to 59- MHz clock signal can be supplied by an external 1.8-V CMOS signal on pin sys_altclk.

Table 4-8 summarizes the electrical constraints imposed by the clock source.

Table 4-8. 48-, 54-, or up to 59- MHz Input Clock Source Electrical Characteristics

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
f	Frequency , sys_altclk	48-, 54-, or up to 59- MHz			MHz
C_I	Input capacitance		0.74		pF
R_I	Input resistance	0.25		10^6	GΩ

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Table 4-9 details the input requirements of the input clock.

Table 4-9. 48- or 54-MHz Input Clock Source Timing Requirements(1) (2)

NAME	DESCRIPTION		MIN	TYP	MAX	UNIT
ALT0	$1 / t_{c(altclk)}$	Frequency, sys_altclk	48-, 54-, or up to 59- MHz			MHz
ALT1	$t_{w(altclk)}$	Pulse duration, sys_altclk low or high	0.40 * $t_{c(altclk)}$		0.60 * $t_{c(altclk)}$	ns
ALT2	$t_{J(altclk)}$	Peak-to-peak jitter(1), sys_altclk	–1%		1%	
ALT3	$t_{R(altclk)}$	Rise time, sys_altclk			10	ns
ALT4	$t_{F(altclk)}$	Fall time, sys_altclk			10	ns
ALT5	$t_{J(altclk)}$	Frequency stability, sys_altclk			± 50	ppm

(1) Peak-to-peak jitter is defined as the difference between the maximum and the minimum output periods on a statistical population of 300 period samples. The sinusoidal noise is added on top of the vdds supply voltage.
(2) See Table 3-4, *Electrical Characteristics*, for sys_altclk V_{IH}/V_{IL} parameters.

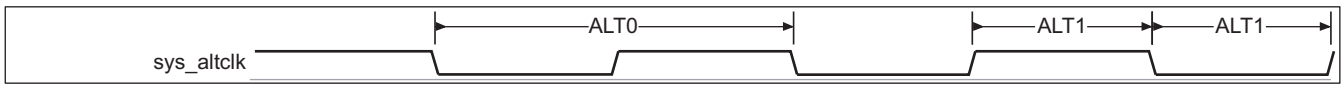

Figure 4-6. Alternate CMOS Clock

4.2 Output Clock Specifications

Two output clocks (pin sys_clkout1 and pin sys_clkout2) are available:

- sys_clkout1 can output the oscillator clock (12, 13, 16.8, 19.2, 26, or 38.4 MHz) at any time. It can be controlled by software or externally using sys_clkreq control. When the device is in the off state, the sys_clkreq can be asserted to enable the oscillator and activate the sys_clkout1 without waking up the device. The off state polarity of sys_clkout1 is programmable.
- sys_clkout2 can output sys_clk (12, 13, 16.8, 19.2, 26, or 38.4 MHz), CORE_CLK (core DPLL output, 332 MHz maximum), APLL-96 MHz, or APLL-54 MHz. It can be divided by 2, 4, 8, or 16 and its off state polarity is programmable. This output is active only when the core domain is active.

Table 4-10 summarizes the sys_clkout1 output clock electrical characteristics.

Table 4-10. sys_clkout1 Output Clock Electrical Characteristics

NAME	DESCRIPTION		MIN	TYP	MAX	UNIT
f	Frequency			12, 13, 16.8, 19.2, 26, or 38.4		MHz
C_I	Load capacitance(1)	f(max) = 38.4 MHz		37		pF
		f(max) = 26 MHz		50		

(1) The load capacitance is adapted to a frequency.

Table 4-11 details the sys_clkout1 output clock timing characteristics.

Table 4-11. sys_clkout1 Output Clock Switching Characteristics

NAME	DESCRIPTION		MIN	TYP	MAX	UNIT
f	1 / CO0	Frequency	12, 13, 16.8, 19.2, 26, or 38.4			MHz
CO1	$t_{w(CLKOUT1)}$	Pulse duration, sys_clkout1 low or high	0.40 * $t_{c(CLKOUT1)}$		0.60 * $t_{c(CLKOUT1)}$	ns
CO2	$t_{R(CLKOUT1)}$	Rise time, sys_clkout1(1)			5.5	ns
CO3	$t_{F(CLKOUT1)}$	Fall time, sys_clkout1(1)			5.5	ns

(1) With a load capacitance of 50 pF.

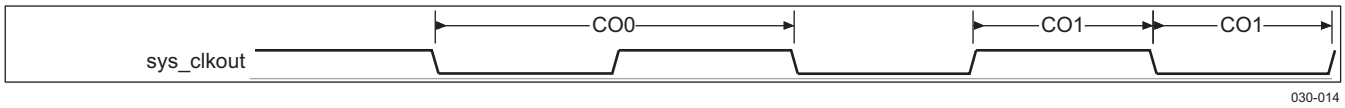

Figure 4-7. sys_clkout1 System Output Clock

Table 4-12 summarizes the sys_clkout2 output clock electrical characteristics.

Table 4-12. sys_clkout2 Output Clock Electrical Characteristics

NAME	DESCRIPTION		MIN	TYP	MAX	UNIT
f	Frequency, sys_clkout2				322	MHz
C_L	Load capacitance(1)	f(max) = 166 MHz	2	8	12	pF

(1) The load capacitance is adapted to a frequency.

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Table 4-13 details the sys_clkout2 output clock timing characteristics.

Table 4-13. sys_clkout2 Output Clock Switching Characteristics

NAME	DESCRIPTION		MIN	TYP	MAX	UNIT
f	1 / CO0	Frequency			322	MHz
CO1	$t_{w(CLKOUT2)}$	Pulse duration, sys_clkout2 low or high	0.40 * $t_{c(CLKOUT2)}$		0.60 * $t_{c(CLKOUT2)}$	ns
CO2	$t_{R(CLKOUT2)}$	Rise time, sys_clkout2 (1)			3.7	ns
CO3	$t_{F(CLKOUT2)}$	Fall time, sys_clkout2 (1)			4.3	ns

(1) With a load capacitance of 12 pF.

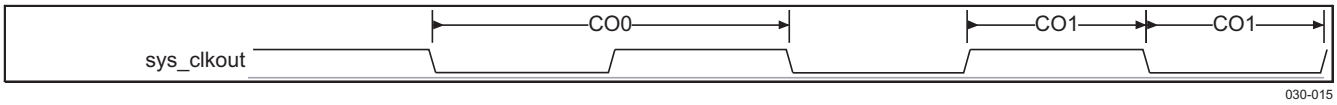


Figure 4-8. sys_clkout2 System Output Clock

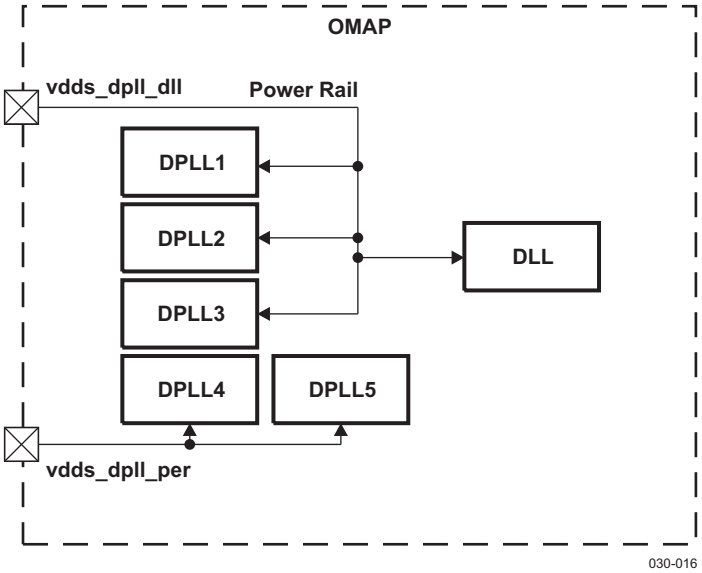
4.3 DPLL and DLL Specifications

The OMAP3530/25 integrates seven DPLLs and a DLL. The PRM and CM drive five of them, while the sixth (not supported) and the seventh (not supported) are controlled by the display subsystem.

The five main DPLLs are:

- DPLL1 (MPU)
- DPLL2 (IVA2)
- DPLL3 (Core)
- DPLL4 (Peripherals)
- DPLL5 (Second Peripherals DPLL)

Figure 4-9 illustrates the DLL and DPLL implementation.



(1) **Figure 4-9. DPLL and DLL Implementation**

For more information on the OMAP3530/25 Applications Processor DPLLs and clocking structure, see the Power, Reset, and Clock management (PRCM) chapter of the *OMAP35x Applications Processor TRM* (literature number SPRUFA5).

4.3.1 Digital Phase-Locked Loop (DPLL)

The DPLL provides all interface clocks and some functional clocks (such as the processor clocks) of the OMAP3530/25 device.

DPLL1 and DPLL2 get an always-on clock used to produce the synthesized clock. They get a high-speed bypass clock used to switch the DPLL output clock on this high-speed clock during bypass mode.

The high-speed bypass clock is an L3 divided clock (programmable by 1 or 2) that saves DPLL processor power consumption when the processor does not need to run faster than the L3 clock speed, or optimizes performance during frequency scaling.

Each DPLL synthesized frequency is set by programming M (multiplier) and N (divider) factors. In addition, all DPLL outputs can be controlled by an independent divider (M2 to M6).

The clock generating DPLLs of the OMAP3530/25 device have following features:

- Independent power domain per DPLL
- Controlled by clock-manager (CM)
- Fed with always-on system clock with independent gating control per DPLL

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- Analog part supplied through dedicated power supply (1.8 V) and an embedded LDO to get rid of 1-MHz noise
- Up to five independent output dividers for simultaneous generation of multiple clock frequencies

4.3.1.1 DPLL1 (MPU)

DPLL1 is located in the MPU subsystem and supplies all clocks of the subsystem. All MPU subsystem clocks are internally generated in the subsystem. When the core domain is on, it can use the DPLL3 (CORE DPLL) output as a high-frequency bypass input clock.

4.3.1.2 DPLL2 (IVA2)

DPLL2 is located in the IVA subsystem and supplies all clocks of the subsystem. All IVA subsystem clocks are internally generated in the subsystem. When the core domain is on, it can use the DPLL3 (CORE DPLL) output as a high-frequency bypass input clock.

4.3.1.3 DPLL3 (CORE)

DPLL3 supplies all interface clocks and also a few module functional clocks. It can be also source of the emulation trace clock. It is located in the core domain area. All interface clocks and a few module functional clocks are generated in the CM. When the core domain is on, it can be used as a bypass input to DPLL1 and DPLL2.

4.3.1.4 DPLL4 (Peripherals)

DPLL4 generates clocks for the peripherals. It supplies five clock sources: 96-MHz functional clocks to subsystems and peripherals, 54 MHz to TV DAC, display functional clock, camera sensor clock, and emulation trace clock. It is located in the core domain area. All interface clocks and few module functional clocks are generated in the CM. Its outputs to the DSS, PER, and EMU domains are propagated with always-on clock trees.

4.3.1.5 DPLL5 (Second peripherals DPLL)

DPLL5 supplies the 120-MHz functional clock to the CM.

4.3.2 Delay-Locked Loops (DLL)

The SDRC includes analog-controlled delay technology for interfacing high-speed mobile DDR memory components. For more information, see the SDRC-GPMC chapter of the *OMAP35x Technical Reference Manual (TRM)* [literature number SPRUF98]. A DLL is a calibration module used on dynamic track of voltage and temperature variations, as well as to compensate the silicon process dispersion.

The SDRC DLL has four modes of operation:

1. APPLICATION MODE 0: used to generate 72° delay
2. APPLICATION MODE 1: used to generate 90° delay
3. MODEMAXDELAY: used for low frequency operation where we do not have the requirement of accurate 72° or 90° phase shift
4. IDLE MODE: a low-power state that allows the DLL to gain lock quickly on exit from this mode

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4.3.3 DPLLs and DLL Characteristics

Several specifications characterize the seven DPLLs.

Table 4-14 summarizes the DPLL characteristics and assumes testing over recommended operating conditions.

Table 4-14. DPLL Characteristics

NAME	PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS(1)
vdds_dpll_per		1.71	1.8	1.89	V	At ball level (+5%, +10%)
vdds_dpll_dll		1.71	1.8	1.89	V	
T_J	Junction temperature	–40	25	105	°C	Will not unlock after lock over this range for slow temperature drifts
f_{input}	Input reference frequency(2)	0.75		65	MHz	FINP
$f_{internal}$	Internal reference frequency	0.75		2.1	MHz	FREQSEL3 = 0; FINT = FINP/(N+1)
		7.5		21	MHz	FREQSEL3 = 1; FINT = FINP/(N+1)
f_{output}	CLKOUT output frequency	25		900	MHz	
$f_{output*2}$	CLKOUTx2 output frequency	50		1800	MHz	
t_{lock}	Frequency lock time(3)	71.4		200	µs	150 FINT cycles; FREQSEL3 = 0
		37.1		104	µs	780 FINT cycles; FREQSEL3 = 1
p_{lock}	Phase lock time	166.7		466.7	µs	350 FINT cycles; FREQSEL3 = 0
		46.7		130.7	µs	980 FINT cycles; FREQSEL3 = 1
t_{relock}	Relock time – frequency lock(4)	4.8		13.3	µs	10 FINT cycles
						Lowcurrstby = 0; FREQSEL3 = 0
		4.8		13.3	µs	100 FINT cycles
						Lowcurrstby = 0; FREQSEL3 = 1
		19		53.3	µs	40 FINT cycles
						Lowcurrstby = 1; FREQSEL3 = 0
		19		53.3	µs	400 FINT cycles
						Lowcurrstby = 1; FREQSEL3 = 1
p_{relock}	Relock time – Phase lock(4)	71.4		200	µs	150 FINT cycles
						Lowcurrstby = 0; FREQSEL3 = 0
		11.9		33.3	µs	250 FINT cycles
						Lowcurrstby = 0; FREQSEL3 = 1
		95.2		266.7	µs	200 FINT cycles
						Lowcurrstby = 1; FREQSEL3 = 0
		26.7		74.7	µs	560 FINT cycles
						Lowcurrstby = 1; FREQSEL3 = 1

(1) f_{reqsel} needs to be programmed accordingly to reference clock and DPLL divider (register setting), Lowcurrstdby depends on the targeted DPLL power state (dynamic).
Lowcurrstdby = 0 then DPLL is in normal mode
Lowcurrstdby = 1 then DPLL is in low-power mode
(2) Input frequencies below 0.75 MHz are possible with performance penalty.
(3) Maximum frequency for nominal conditions. Speed binning possible above fmax.
(4) Relock time assumes typical operating conditions, 4°C maximum temperature drift (see the Functional Specification for more detailed information).

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and Table 4-16 show the DPLL1 and DPLL2 clock frequency ranges.

Note: The DPLL1 and DPLL2 clock frequency ranges depend on the V_{DD1} (vdd_mpu _iva) operating point.

Table 4-15. DPLL1 Clock Frequency Ranges

Clock Signal	Description		Max	Unit
ARM_CLK	DPLL1 output clock.	OPP6(1)	720	MHz
		OPP5	600	MHz
		OPP4	550	MHz
		OPP3	500	MHz
		OPP2	250	MHz
		OPP1(2)	125	MHz

(1) OPP6 frequency range is only supported on high-speed grade OMAP3530/25 devices.
(2) Cannot boot in OPP1. If OPP1 is desired, boot in higher OPP then switch to OPP1.

Table 4-16. DPLL2 Clock Frequency Ranges

Clock Signal	Description		Max	Unit
IVA2_CLK	Generated from DPLL2 output clock.	OPP6(1)	520	MHz
		OPP5	430	MHz
		OPP4	400	MHz
		OPP3	360	MHz
		OPP2	180	MHz
		OPP1(2)	90	MHz

(1) OPP6 frequency range is only supported on high-speed grade OMAP3530/25 devices.
(2) Cannot boot in OPP1. If OPP1 is desired, boot in higher OPP then switch to OPP1.

Table 4-17 through Table 4-19 show the DPLL3 clock frequency ranges.

Note: The DPLL3 clock frequency ranges depend on the VDD2 (vdd_core) operating point and the L3 clock speed configuration.

Table 4-17. DPLL3 Clock Frequency Ranges, VDD2 OPP3

		Config 1 (166 MHz)		Config 2 (133 MHz)		Unit
Clock Signal	Description	Min	Max	Min	Max	
CM: CORE_CLK	Output of clock manager (CM), generated directly from DPLL3.	-	332	-	266	MHz
CM: L3_ICLK	Output of clock manager (CM), generated using DPLL3.	-	166	-	133	MHz
CM: L4_ICLK	Output of clock manager (CM), generated using CM L3_ICLK and divider.	-	83	-	66.5	MHz
SGX	SGX input clock, taken from CM CORE_CLK.	-	110.67	-	88.67	MHz
SDRC	SDRC input clock, taken from CM L3_ICLK.	-	166	-	133	MHz
GPMC	GPMC input clock, taken from CM L3_ICLK.	-	83	-	66.5	MHz

Table 4-18. DPLL3 Clock Frequency Ranges, VDD2 OPP2

		Config 1 (83 MHz)		Config 2 (100 MHz)		Unit
Clock Signal	Description	Min	Max	Min	Max	
CM: CORE_CLK	Output of clock manager (CM), generated directly from DPLL3.	-	166	-	200	MHz
CM: L3_ICLK	Output of clock manager (CM), generated using DPLL3.	-	83	-	100	MHz

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Table 4-18. DPLL3 Clock Frequency Ranges, VDD2 OPP2 (continued)

		Config 1 (83 MHz)		Config 2 (100 MHz)		Unit
Clock Signal	Description	Min	Max	Min	Max	
CM: L4_ICLK	Output of clock manager (CM), generated using CM L3_ICLK and divider.	-	41.5	-	50	MHz
SGX	SGX input clock, taken from CM CORE_CLK.	-	55.53	-	66.67	MHz
SDRC	SDRC input clock, taken from CM L3_ICLK.	-	83	-	100	MHz
GPMC	GPMC input clock, taken from CM L3_ICLK.	-	41.5	-	50	MHz

Table 4-19. DPLL3 Clock Frequency Ranges, VDD2 OPP1 (1)

		Config 1 (40 MHz)		Config 2 (50 MHz)		Unit
Clock Signal	Description	Min	Max	Min	Max	
CM: CORE_CLK	Output of clock manager (CM), generated directly from DPLL3.	-	83	-	100	MHz
CM: L3_ICLK	Output of clock manager (CM), generated using DPLL3.	-	41.5	-	50	MHz
CM: L4_ICLK	Output of clock manager (CM), generated using CM L3_ICLK and divider.	-	20.75	-	25	MHz
SGX	SGX input clock, taken from CM CORE_CLK.	-	N/A	-	N/A	MHz
SDRC	SDRC input clock, taken from CM L3_ICLK.	-	41.5	-	50	MHz
GPMC	GPMC input clock, taken from CM L3_ICLK.	-	41.5	-	25	MHz

(1) Cannot boot in OPP1. If OPP1 is desired, boot in higher OPP then switch to OPP1.

Table 4-20 summarizes the DLL characteristics.

Table 4-20. DLL Characteristics

PARAMETER	MIN	NOM	MAX	UNIT	COMMENTS
Supply voltage vdds_dpll_dll	1.71	1.8	1.89	V	
Junction operating temperature	–40	25	105	°C	
Input clock frequency	66	120	133	MHz	APPLICATION MODE 0
	83	120	166		APPLICATION MODE 1
Input load (1)			15	fF	
Lock time (2)			500	Clocks	
Relock time			500	ns	IDLE to MODEMAXDELAY
(Mode transitions through idle mode)		150	372	Clocks	IDLE to APPLICATION MODE 1 or 0
		1	2	µs	IDLE to APPLICATION MODE @133 MHz
		1	1.5	µs	IDLE to APPLICATION MODE @166 MHz

(1) This parameter is design goal and is not tested on silicon.
(2) Lock signal would go high from power down within 500 clocks. Lock signal switches to low state when the input clock is switched off after 3 µs.

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4.3.4 DPLL and DLL Noise Isolation

The DPLL and DLL require dedicated power supply pins to isolate the core analog circuit from the switching noise generated by the core logic that can cause jitter on the clock output signal. Guard rings are added to the cell to isolate it from substrate noise injection.

The vdd supplies are the most sensitive to noise; decoupling capacitance is recommended below the supply rails. The maximum input noise level allowed is 30 mV_{PP} for frequencies below 1 MHz.

Figure 4-10 illustrates an example of a noise filter.

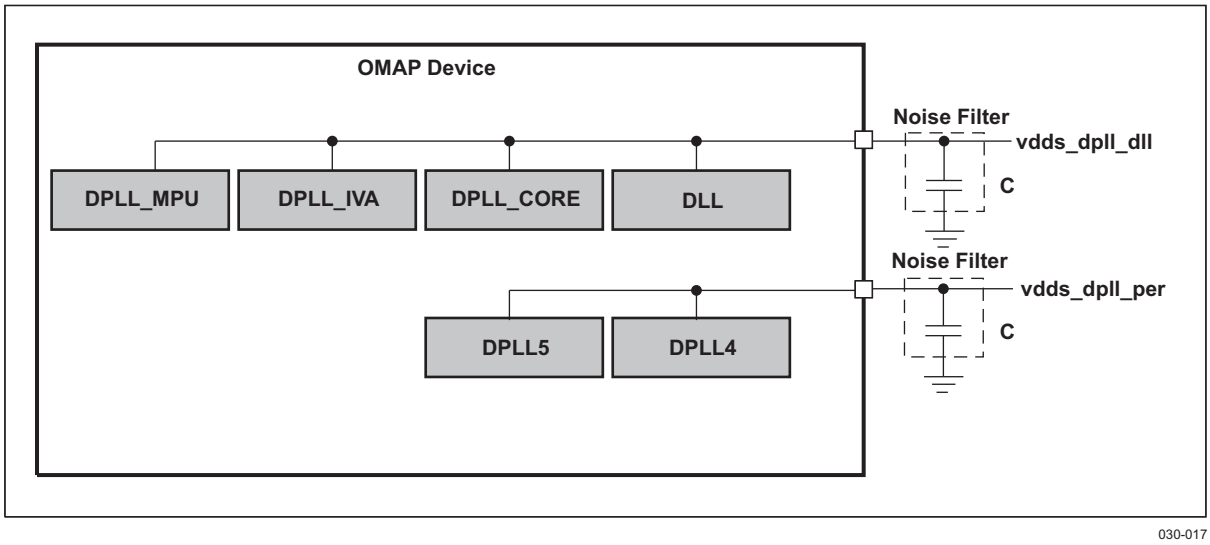

Figure 4-10. DPLL and DLL Noise Filter

Table 4-21 specifies the noise filter requirements.

Table 4-21. DPLL and DLL Noise Filter Requirements

NAME	MIN	TYP	MAX	UNIT
Filtering capacitor		100		nF

(1) The capacitors must be inserted between power and ground as close as possible.

(2) This circuit is provided only as an example.

(3) The filter must be located as close as possible to the device.

(4) No filtering required if noise is below 10 mV_{PP}.

5 VIDEO DAC SPECIFICATIONS

A dual-display interface equips the OMAP3530/25 processor. This display subsystem provides the necessary control signals to interface the memory frame buffer directly to the external displays (TV-set). Two (one per channel) 10-bit current steering DACs are inserted between the DSS and the TV set to generate the video analog signal. One of the video DACs also includes TV detection and power-down mode. Figure 5-1 illustrates the OMAP3530/25 DAC architecture. For more information, see the DSS chapter of the *OMAP35x Technical Reference Manual (TRM)* [literature number SPRUF98].

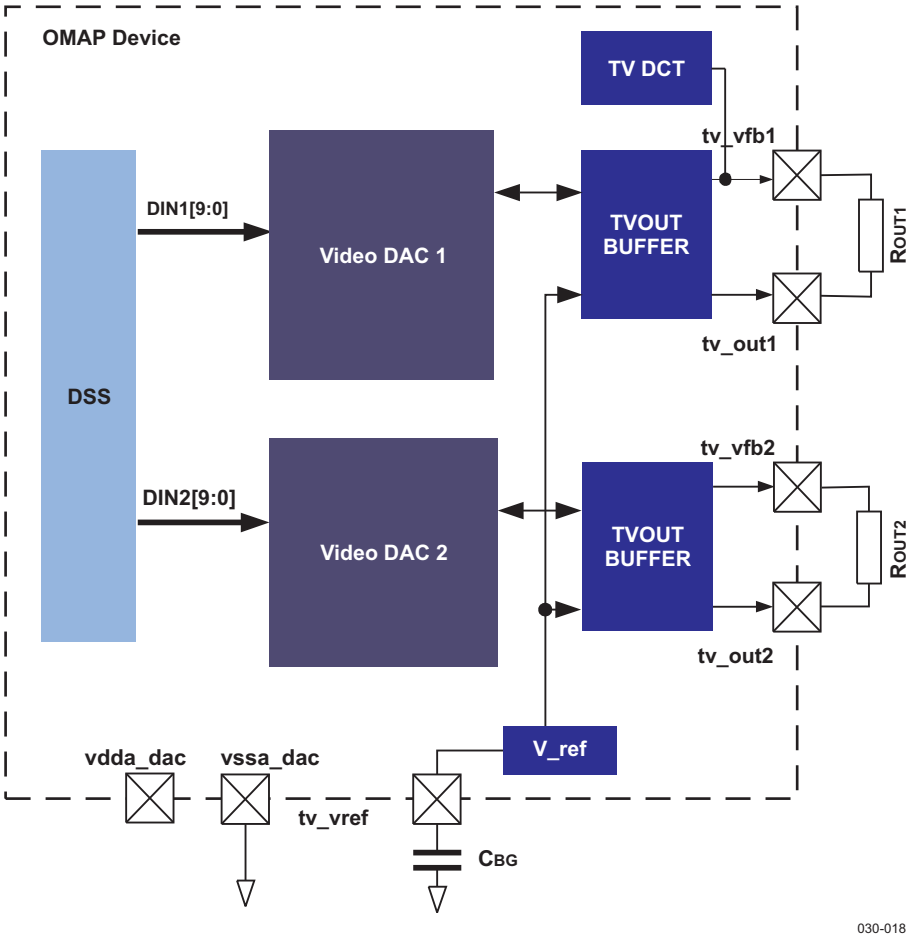

Figure 5-1. Video DAC Architecture

The following paragraphs detail the 10-bit DAC interface pinout, static and dynamic specifications, and noise requirements. The operating conditions and absolute maximum ratings are detailed in Table 5-2 and Table 5-4.

5.1 Interface Description

Table 5-1 summarizes the external pins of the video DAC.

Table 5-1. External Pins of 10-bit Video DAC

PIN NAME	I/O	DESCRIPTION	
tv_out1	O	TV analog output composite	DAC1 video output. An external resistor is connected between this node and tv_vfb1. The nominal value of ROUT1 is 1650 Ω. Finally, note that this is the output node that drives the load (75 Ω).

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Table 5-1. External Pins of 10-bit Video DAC (continued)

PIN NAME	I/O	DESCRIPTION	
tv_out2	O	TV analog output S-VIDEO	DAC2 video output. An external resistor is connected between this node and tv_vfb2. The nominal value of ROUT2 is 1650 Ω. Finally, note that this is the output node that drives the load (75 Ω).
tv_vref	I	Reference output voltage from internal bandgap	A decoupling capacitor (CBG) needs to be connected for optimum performance.
tv_vfb1	O	Amplifier feedback node	Amplifier feedback node. An external resistor is connected between this node and tv_out1. The nominal value of ROUT1 is 1650 Ω (1%).
tv_vfb2	O	Amplifier feedback node	Amplifier feedback node. An external resistor is connected between this node and tv_out2. The nominal value of ROUT2 is 1650 Ω (1%).

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5.2 Electrical Specifications Over Recommended Operating Conditions

(T_{MIN} to T_{MAX}, vdda_dac = 1.8 V, $R_{OUT1/2}$ = 1650 Ω, R_{LOAD} = 75 Ω, unless otherwise noted)

Table 5-2. DAC – Static Electrical Specification

PARAMETER		CONDITIONS/ASSUMPTIONS	MIN	TYP	MAX	UNIT
R	Resolution			10		Bits
DC ACCURACY						
INL (1)	Integral nonlinearity		–1		1	LSB
DNL (2)	Differential nonlinearity		–1		1	LSB
ANALOG OUTPUT						
-	Full-scale output voltage	R_{LOAD} = 75 Ω	0,7	0.88	1	V
-	Output offset voltage			50		mV
-	Output offset voltage drift			20		mV/°C
-	Gain error		–17		19	% FS
R_{VOUT}	Output impedance		67.5	75	82.5	Ω
REFERENCE						
V_{REF}	Reference voltage range		0.525	0.55	0.575	V
-	Reference noise density	100-kHz reference noise bandwidth		129		
R_{SET}	Full-scale current adjust resistor		3700	4000	4200	Ω
P_{SRR}	Reference PSRR (3) (Up to 6 MHz)			40		dB
POWER CONSUMPTION						
$I_{vdda-up}$	Analog Supply Current (4)	2 channels, no load		8		mA
-	Analog supply driving a 75-Ω load (RMS)	2 channels		50		mA
$I_{vdda-up}$ (peak)	Peak analog supply current:	Lasts less than 1 ns		60		mA
I_{vdd-up}	Digital supply current (5)	Measured at f_{CLK} = 54 MHz, f_{OUT} = 2 MHz sine wave, vdd = 1.3 V		2		mA
$I_{vdd-up\ (peak)}$	Peak digital supply current (6)	Lasts less than 1 ns		2.5		mA
$I_{vdda-down}$	Analog power at power-down	T = 30°C, vdda = 1.8 V		1.5		mA
$I_{vdd-down}$	Digital power at power-down	T = 30°C, vdd = 1.3 V		1		mA

(1) The INL is measured at the output of the DAC (accessible at an external pin during bypass mode).
(2) The DNL is measured at the output of the DAC (accessible at an external pin during bypass mode).
(3) Assuming a capacitor of 0.1 µF at the tv_ref node.
(4) The analog supply current I_{vdda} is directly proportional to the full-scale output current IFS and is insensitive to f_{CLK}
(5) The digital supply current I_{VDD} is dependent on the digital input waveform, the DAC update rate f_{CLK}, and the digital supply VDD.
(6) The peak digital supply current occurs at full-scale transition for duration less than 1 ns.

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(T_{MIN} to T_{MAX}, vdda_dac = 1.8 V, $R_{OUT1/2}$ = 1650 Ω, R_{LOAD} = 75 Ω, unless otherwise noted)

Table 5-3. Video DAC – Dynamic Electrical Specification

PARAMETER		CONDITIONS/ASSUMPTIONS	MIN	TYP	MAX	UNIT
f_{CLK} (1)	Output update rate	Equal to input clock frequency		54		MHz
	Clock jitter	rms clock jitter required in order to assure 10-bit accuracy			40	ps
	Attenuation at 5.1 MHz	Corner frequency for signal	0.1	0.5	1.5	dB
	Attenuation at 54 MHz (1)	Image frequency	25	30	33	dB
t_{ST}	Output settling time	Time from the start of the output transition to output within ± 1 LSB of final value.		85		ns
t_{Rout}	Output rise time	Measured from 10% to 90% of full-scale transition		25		ns
t_{Fout}	Output fall time	Measured from 10% to 90% of full-scale transition		25		ns
BW	Signal bandwidth			6		MHz
	Differential gain (2)			1.5%		
	Differential phase (2)			1		deg.
SFDR	Within bandwidth	f_{CLK} = 54 MHz, f_{OUT} = 1 MHz		45		dB
SNR	Signal-to-noise ratio 1 kHz to 6 MHz bandwidth	f_{CLK} = 54 MHz, f_{OUT} = 1 MHz		55 (3)		dB
PSRR	Power supply rejection ratio	Up to 6 MHz		20 (4)		dB
Crosstalk	Between the two video channels			–50	–40	dB

(1) For internal input clock information, For more information, see the DSS chapter of the *OMAP35x Technical Reference Manual (TRM)* [literature number SPRUF98].
(2) The differential gain and phase value is for dc coupling. Note that there is degradation for the ac coupling.
(3) The SNR value is for dc coupling. Note that there is a 6-dB degradation for ac coupling.
(4) The PSSR value is for dc coupling. Note that there is a 10-dB degradation for ac coupling.

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5.3 Analog Supply (vdda_dac) Noise Requirements

In order to assure 10-bit accuracy of the DAC analog output, the analog supply vdda_dac has to meet the noise requirements stated in this section.

The DAC Power Supply Rejection Ratio is defined as the relative variation of the full-scale output current divided by the supply variation. Thus, it is expressed in percentage of Full-Scale Range (FSR) per volt of supply variation as shown in the following equation:

$$PSRR_{DAC} = \frac{100 \cdot \frac{\Delta I_{OUT}}{I_{OUTFS}}}{V_{AC}} \qquad \left[\%\ FSR/V\right]$$

Depending on frequency, the PSRR is defined in Table 5-4.

Table 5-4. Video DAC – Power Supply Rejection Ratio

Supply Noise Frequency	PSRR % FSR/V
0 to 100 kHz	1
> 100 kHz	The rejection decreases 20 dB/dec. Example: at 1 MHz the PSRR is 10% of FSR/V

A graphic representation is shown in Figure 5-2.

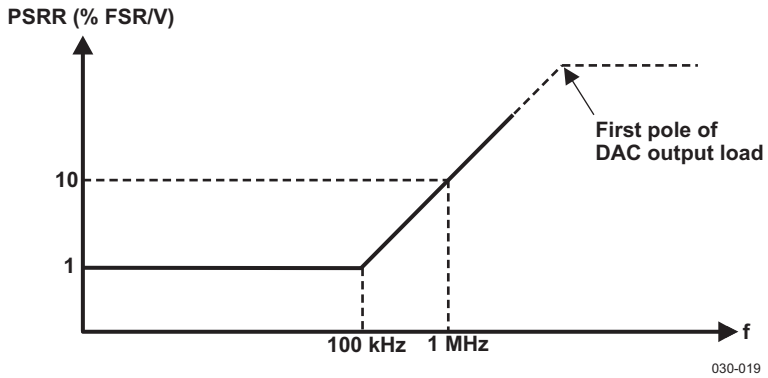

Figure 5-2. Video DAC – Power Supply Rejection Ratio

To ensure that the DAC SFDR specification is met, the PSRR values and the clock jitter requirements translate to the following limits on vdda_dac (for the Video DAC).

The maximum peak-to-peak noise on vdda (ripple) is defined in Table 5-5:

Table 5-5. Video DAC – Maximum Peak-to-Peak Noise on vdda_dac

Tone Frequency	Maximum Peak-to-Peak Noise on vdda_dac
0 to 100 kHz	< 30 mVpp
> 100 kHz	Decreases 20 dB/dec. Example: at 1 MHz the maximum is 3 mVpp

The maximum noise spectral density (white noise) is defined in Table 5-6:

Table 5-6. Video DAC – Maximum Noise Spectral Density

Supply Noise Bandwidth	Maximum Supply Noise Density
0 to 100 kHz	< 20 µV / $\sqrt{Hz}$
> 100 kHz	Decreases 20 dB/dec. Example: at 1 MHz the maximum noise density is 2 µ / $\sqrt{Hz}$

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Because the DAC PSRR deteriorates at a rate of 20 dB/dec after 100 kHz, it is highly recommended to have vdda_dac low pass filtered (proper decoupling) (see the illustrated application: Section 5.4, *External Component Value Choice*).

5.4 External Component Value Choice

The full-scale output voltage V_{OUTMAX} is regulated by the reference amplifier, and is set by an internal resistor R_{SET}. I_{OUTMAX} can be expressed as:

$I_{OUTMAX} = I_{REF} /8 * (63 + 15/16)$ (1)

Where:

$V_{REF} = 0.55V$ (2)

$I_{REF} = V_{REF}/ (2* R_{SET})$ (3)

The output current I_{OUT} appearing at DAC output is a function of both the input code and I_{OUTMAX} and can be expressed as:

$I_{OUT} = (DAC_CODE/1023) * I_{OUTMAX}$ (4)

Where:

DAC_CODE = 0 to 1023 is the DAC input code in decimal. (5)

The output voltage is:

$V_{OUT} = I_{OUT} *N* R_{CABLE}$ (6)

Where:

(N = amplifier gain = 21) (7)

R_{CABLE} = 75 Ω (cable typical impedance) (8)

The TV-out buffer requires a per channel external resistors: $R_{OUT1/2}$. The equation below can be used to select different resistor values (if necessary):

$R_{OUT} = (N+1) R_{CABLE} = 1650$ Ω (9)

Recommended parameter values are:

Table 5-7. Video DAC – Recommended External Components Values

	Recommended Value	UNIT
C_{BG}	100	nF
$R_{OUT1/2}$	1650	Ω

In order to limit the reference noise bandwidth and to suppress transients on V_{REF}, it is necessary to connect a large decoupling capacitor ©$_{BG}$) between the tv_vref and vssa_dac pins.

6 TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

6.1 Timing Test Conditions

All timing requirements and switching characteristics are valid over the recommended operating conditions of , unless otherwise specified.

6.2 Interface Clock Specifications

6.2.1 Interface Clock Terminology

The Interface clock is used at the system level to sequence the data and/or control transfers accordingly with the interface protocol.

6.2.2 Interface Clock Frequency

The two interface clock characteristics are:

- The maximum clock frequency
- The maximum operating frequency

The interface clock frequency documented in this document is the maximum clock frequency, which corresponds to the maximum frequency programmable on this output clock. This frequency defines the maximum limit supported by the OMAP3530/25 IC and doesn't take into account any system consideration (PCB, peripherals).

The system designer will have to consider these system considerations and OMAP3530/25 IC timings characteristics as well, to define properly the maximum operating frequency, which corresponds to the maximum frequency supported to transfer the data on this interface.

6.2.3 Clock Jitter Specifications

Jitter is a phase noise, which may alter different characteristics of a clock signal. The jitter specified in this document is the time difference between the typical cycle period and the actual cycle period affected by noise sources on the clock. The cycle (or period) jitter terminology identifies this type of jitter.

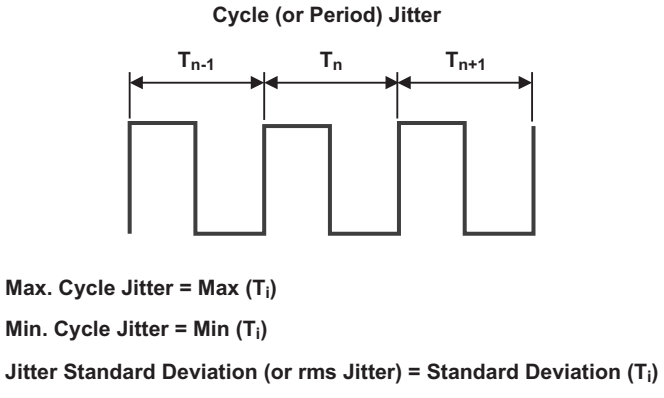

Figure 6-1. Cycle (or Period) Jitter

6.2.4 Clock Duty Cycle Error

The duty cycle error is the ratio between either the high-level pulse duration or the low-level pulse duration and the cycle time of a clock signal.

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6.3 Timing Parameters

The timing parameter symbols used in the timing requirement and switching characteristic tables are created in accordance with JEDEC Standard 100. To shorten the symbols, some pin names and other related terminologies have been abbreviated as follows:

Table 6-1. Timing Parameters

LOWERCASE SUBSCRIPTS	
Symbols	**Parameter**
c	Cycle time (period)
d	Delay time
dis	Disable time
en	Enable time
h	Hold time
su	Setup time
START	Start bit
t	Transition time
v	Valid time
w	Pulse duration (width)
X	Unknown, changing, or don't care level
H	High
L	Low
V	Valid
IV	Invalid
AE	Active Edge
FE	First Edge
LE	Last Edge
Z	High impedance

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6.4 External Memory Interfaces

The OMAP3530/25 processor includes the following external memory interfaces:

- General-purpose memory controller (GPMC)
- SDRAM controller (SDRC)

6.4.1 General-Purpose Memory Controller (GPMC)

The GPMC is the OMAP3530/25 unified memory controller used to interface external memory devices such as:

- Asynchronous SRAM-like memories and ASIC devices
- Asynchronous page mode and synchronous burst NOR flash
- NAND flash

6.4.1.1 GPMC/NOR Flash Interface Synchronous Timing

Table 6-3 and Table 6-4 assume testing over the recommended operating conditions (see Figure 6-2 through Figure 6-5) and electrical characteristic conditions.

Table 6-2. GPMC/NOR Flash Synchronous Mode Timing Conditions

TIMING CONDITION PARAMETER		VALUE	UNIT
Input Conditions			
t_R	Input signal rise time	1.8	ns
t_F	Input signal fall time	1.8	ns
Output Conditions			
C_{LOAD}	Output load capacitance	15.94	pF

Table 6-3. GPMC/NOR Flash Interface Timing Requirements – Synchronous Mode(1)

NO.	PARAMETER		OPP3		OPP2		OPP1(2)		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
F12	$t_{su(DV-CLKH)}$	Setup time, read gpmc_d[15:0] valid before gpmc_clk high	1.9		1.9		3.2		ns
F13	$t_{h(CLKH-DV)}$	Hold time, read gpmc_d[15:0] valid after gpmc_clk high	1.9		1.9		1.9		ns
F21	$t_{su(WAITV-CLKH)}$	Setup time, gpmc_waitx(3) valid before gpmc_clk high	1.9		1.9		3.2		ns
F22	$t_{h(CLKH-WAITV)}$	Hold Time, gpmc_waitx(3) valid after gpmc_clk high	2.5		2.5		2.5		ns

(1) For VDD2 (vdd_core) OPP voltages, see Section 3.3, *Recommended Operating Conditions*.
(2) Cannot boot in OPP1. If OPP1 is desired, boot in higher OPP then switch to OPP1.
(3) Wait monitoring support is limited to a WaitMonitoringTime value > 0. For a full description of wait monitoring feature, see the *OMAP35x Technical Reference Manual* (literature number SPRUF988).

Table 6-4. GPMC/NOR Flash Interface Switching Characteristics – Synchronous Mode

NO.	PARAMETER		1.15 V		1.0 V		0.9 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
F0	$t_{c(CLK)}$	Cycle time(15), output clock gpmc_clk period	10		12.05		25		ns
F1	$t_{w(CLKH)}$	Typical pulse duration, output clock gpmc_clk high	0.5 P(12)	0.5 P(12)	0.5 P(12)	0.5 P(12)	0.5 P(12)	0.5 P(12)	ns
F1	$t_{w(CLKL)}$	Typical pulse duration, output clock gpmc_clk low	0.5 P(12)	0.5 P(12)	0.5 P(12)	0.5 P(12)	0.5 P(12)	0.5 P(12)	ns
	$t_{dc(CLK)}$	Duty cycle error, output clk gpmc_clk	–500	500	–602	602	–1250	1250	ps

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Table 6-4. GPMC/NOR Flash Interface Switching Characteristics – Synchronous Mode (continued)

NO.	PARAMETER			1.15 V		1.0 V		0.9 V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
	$t_{j(CLK)}$	Jitter standard deviation(16), output clock gpmc_clk			33.3		33.3		33.3	ps
	$t_{R(CLK)}$	Rise time, output clock gpmc_clk			1.6		2		2	ns
	$t_{F(CLK)}$	Fall time, output clock gpmc_clk			1.6		2		2	ns
	$t_{R(DO)}$	Rise time, output data			2		2		2	ns
	$t_{F(DO)}$	Fall time, output data			2		2		2	ns
F2	$t_{d(CLKH-nCSV)}$	Delay time, gpmc_clk rising edge to gpmc_ncsx(11) transition		F(6) – 1.9	F(6) + 3.3	F(6) – 1.8	F(6) + 4.1	F(6) – 2.6	F(6) + 4.9	ns
F3	$t_{d(CLKH-nCSIV)}$	Delay time, gpmc_clk rising edge to gpmc_ncsx(11) invalid		E(5) – 1.9	E(5) + 3.3	E(5) – 1.8	E(5) + 4.1	E(5) – 2.6	E(5) + 4.9	ns
F4	$t_{d(ADDV-CLK)}$	Delay time, address bus valid to gpmc_clk first edge		B(2) – 4.1	B(2) + 2.1	B(2) – 4.1	B(2) + 2.1	B(2) – 4.9	B(2) + 2.6	ns
F5	$t_{d(CLKH-ADDIV)}$	Delay time, gpmc_clk rising edge to gpmc_a[16:1] invalid		–2.1		–2.1		–2.6		ns
F6	$t_{d(nBEV-CLK)}$	Delay time, gpmc_nbe0_cle, gpmc_nbe1 valid to gpmc_clk first edge		B(2) – 1.1	B(2) + 2.1	B(2) – 0.9	B(2) + 1.9	B(2) – 2.6	B(2) + 2.6	ns
F7	$t_{d(CLKH-nBEIV)}$	Delay time, gpmc_clk rising edge to gpmc_nbe0_cle, gpmc_nbe1 invalid		D(4) – 2.1	D(4) + 1.1	D(4) – 1.9	D(4) + 0.9	D(4) – 2.6	D(4) + 2.6	ns
F8	$t_{d(CLKH-nADV)}$	Delay time, gpmc_clk rising edge to gpmc_nadv_ale transition		G(7) – 1.9	G(7) + 4.1	G(7) – 2.1	G(7) + 4.1	G(7) – 2.6	G(7) + 4.9	ns
F9	$t_{d(CLKH-nADVIV)}$	Delay time, gpmc_clk rising edge to gpmc_nadv_ale invalid		D(4) – 1.9	D(4) + 4.1	D(4) – 2.1	D(4) + 4.1	D(4) – 2.6	D(4) + 4.9	ns
F10	$t_{d(CLKH-nOE)}$	Delay time, gpmc_clk rising edge to gpmc_noe transition		H(8) – 2.1	H(8) + 2.1	H(8) – 2.1	H(8) + 2.1	H(8) – 2.6	H(8) + 4.9	ns
F11	$t_{d(CLKH-nOEIV)}$	Delay time, gpcm rising edge to gpmc_noe invalid		E(5) – 2.1	E(5) + 2.1	E(5) – 2.1	E(5) + 2.1	E(5) – 2.6	E(5) + 4.9	ns
F14	$t_{d(CLKH-nWE)}$	Delay time, gpmc_clk rising edge to gpmc_nwe transition		I(9) – 1.9	I(9) + 4.1	I(9) – 2.1	I(9) + 4.1	I(9) – 2.6	I(9) + 4.9	ns
F15	$t_{d(CLKH-Data)}$	Delay time, gpmc_clk rising edge to data bus transition		J(10) – 2.1	J(10) + 1.1	J(10) – 1.9	J(10) + 0.9	J(10) – 2.6	J(10) + 2.6	ns
F17	$t_{d(CLKH-nBE)}$	Delay time, gpmc_clk rising edge to gpmc_nbex_cle transition		J(10) – 2.1	J(10) + 1.1	J(10) – 1.9	J(10) + 0.9	J(10) – 2.6	J(10) + 2.6	ns
F18	$t_{W(nCSV)}$	Pulse duration, gpmc_ncsx(11) low	Read	A(1)		A(1)		A(1)		ns
			Write	A(1)		A(1)		A(1)		ns
F19	$t_{W(nBEV)}$	Pulse duration, gpmc_nbe0_cle, gpmc_nbe1 low	Read	C(3)		C(3)		C(3)		ns
			Write	C(3)		C(3)		C(3)		ns
F20	$t_{W(nADVV)}$	Pulse duration, gpmc_nadv_ale low	Read	K(13)		K(13)		K(13)		ns
			Write	K(13)		K(13)		K(13)		ns

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Table 6-4. GPMC/NOR Flash Interface Switching Characteristics – Synchronous Mode (continued)

NO.	PARAMETER		1.15 V		1.0 V		0.9 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
F23	$t_{d(CLKH-IODIR)}$	Delay time, gpmc_clk rising edge to gpmc_io_dir high (IN direction)	H(8) – 2.1	H(8) + 4.1	H(8) – 2.1	H(8) + 4.1	H(8) – 2.6	H(8) + 4.9	ns
F24	$t_{d(CLKH-IODIV)}$	Delay time, gpmc_clk rising edge to gpmc_io_dir low (OUT direction)	M(17) – 2.1	M(17) + 4.1	M(17) – 2.1	M(17) + 4.1	M(17) – 2.6	M(17) + 4.9	ns

(1) **For single read:** A = (CSRdOffTime – CSOnTime) * (TimeParaGranularity + 1) * GPMC_FCLK period
For burst read: A = (CSRdOffTime – CSOnTime + (n – 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK period
For burst write: A = (CSWrOffTime – CSOnTime + (n – 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK period
with n being the page burst access number.

(2) B = ClkActivationTime * GPMC_FCLK

(3) **For single read:** C = RdCycleTime * (TimeParaGranularity + 1) * GPMC_FCLK
For burst read: C = (RdCycleTime + (n – 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK
For burst write: C = (WrCycleTime + (n – 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK with n being the page burst access number.

(4) **For single read:** D = (RdCycleTime – AccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK
For burst read: D = (RdCycleTime – AccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK
For burst write: D = (WrCycleTime – AccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK

(5) **For single read:** E = (CSRdOffTime – AccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK
For burst read: E = (CSRdOffTime – AccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK
For burst write: E = (CSWrOffTime – AccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK

(6) **For nCS falling edge (CS activated):**

- **Case GpmcFCLKDivider = 0:**
  - F = 0.5 * CSExtraDelay * GPMC_FCLK
- **Case GpmcFCLKDivider = 1:**
  - F = 0.5 * CSExtraDelay * GPMC_FCLK if (ClkActivationTime and CSOnTime are odd) or (ClkActivationTime and CSOnTime are even)
  - F = (1 + 0.5 * CSExtraDelay) * GPMC_FCLK otherwise
- **Case GpmcFCLKDivider = 2:**
  - F = 0.5 * CSExtraDelay * GPMC_FCLK if ((CSOnTime – ClkActivationTime) is a multiple of 3)
  - F = (1 + 0.5 * CSExtraDelay) * GPMC_FCLK if ((CSOnTime – ClkActivationTime – 1) is a multiple of 3)
  - F = (2 + 0.5 * CSExtraDelay) * GPMC_FCLK if ((CSOnTime – ClkActivationTime – 2) is a multiple of 3)

(7) **For ADV falling edge (ADV activated):**

- **Case GpmcFCLKDivider = 0:**
  - G = 0.5 * ADVExtraDelay * GPMC_FCLK
- **Case GpmcFCLKDivider = 1:**
  - G = 0.5 * ADVExtraDelay * GPMC_FCLK if (ClkActivationTime and ADVOnTime are odd) or (ClkActivationTime and ADVOnTime are even)
  - G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK otherwise
- **Case GpmcFCLKDivider = 2:**
  - G = 0.5 * ADVExtraDelay * GPMC_FCLK if ((ADVOnTime – ClkActivationTime) is a multiple of 3)
  - G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK if ((ADVOnTime – ClkActivationTime – 1) is a multiple of 3)
  - G = (2 + 0.5 * ADVExtraDelay) * GPMC_FCLK if ((ADVOnTime – ClkActivationTime – 2) is a multiple of 3)

For ADV rising edge (ADV deactivated) in Reading mode:

- **Case GpmcFCLKDivider = 0:**
  - G = 0.5 * ADVExtraDelay * GPMC_FCLK
- **Case GpmcFCLKDivider = 1:**
  - G = 0.5 * ADVExtraDelay * GPMC_FCLK if (ClkActivationTime and ADVRdOffTime are odd) or (ClkActivationTime and ADVRdOffTime are even)
  - G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK otherwise
- Case GpmcFCLKDivider = 2:
  - G = 0.5 * ADVExtraDelay * GPMC_FCLK if ((ADVRdOffTime – ClkActivationTime) is a multiple of 3)
  - G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK if ((ADVRdOffTime – ClkActivationTime – 1) is a multiple of 3)
  - G = (2 + 0.5 * ADVExtraDelay) * GPMC_FCLK if ((ADVRdOffTime – ClkActivationTime – 2) is a multiple of 3)

For ADV rising edge (ADV deactivated) in Writing mode:

- **Case GpmcFCLKDivider = 0:**
  - G = 0.5 * ADVExtraDelay * GPMC_FCLK
- **Case GpmcFCLKDivider = 1:**
  - G = 0.5 * ADVExtraDelay * GPMC_FCLK if (ClkActivationTime and ADVWrOffTime are odd) or (ClkActivationTime and ADVWrOffTime are even)
  - G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK otherwise
- **Case GpmcFCLKDivider = 2:**

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- G = 0.5 * ADVExtraDelay * GPMC_FCLK if ((ADVWrOffTime – ClkActivationTime) is a multiple of 3)
- G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK if ((ADVWrOffTime – ClkActivationTime – 1) is a multiple of 3)
- G = (2 + 0.5 * ADVExtraDelay) * GPMC_FCLK if ((ADVWrOffTime – ClkActivationTime – 2) is a multiple of 3)

(8) **For OE falling edge (OE activated) / IO DIR rising edge (Data Bus input direction):**

- **Case GpmcFCLKDivider = 0:**
  - H = 0.5 * OEExtraDelay * GPMC_FCLK
- **Case GpmcFCLKDivider = 1:**
  - H = 0.5 * OEExtraDelay * GPMC_FCLK if (ClkActivationTime and OEOnTime are odd) or (ClkActivationTime and OEOnTime are even)
  - H = (1 + 0.5 * OEExtraDelay) * GPMC_FCLK otherwise
- **Case GpmcFCLKDivider = 2:**
  - H = 0.5 * OEExtraDelay * GPMC_FCLK if ((OEOnTime – ClkActivationTime) is a multiple of 3)
  - H = (1 + 0.5 * OEExtraDelay) * GPMC_FCLK if ((OEOnTime – ClkActivationTime – 1) is a multiple of 3)
  - H = (2 + 0.5 * OEExtraDelay) * GPMC_FCLK if ((OEOnTime – ClkActivationTime – 2) is a multiple of 3)

For OE rising edge (OE deactivated):

- **GpmcFCLKDivider = 0:**
  - H = 0.5 * OEExtraDelay * GPMC_FCLK
- **Case GpmcFCLKDivider = 1:**
  - H = 0.5 * OEExtraDelay * GPMC_FC if (ClkActivationTime and OEOffTime are odd) or (ClkActivationTime and OEOffTime are even)
  - H = (1 + 0.5 * OEExtraDelay) * GPMC_FCLK otherwise
- **Case GpmcFCLKDivider = 2:**
  - H = 0.5 * OEExtraDelay * GPMC_FCLK if ((OEOffTime – ClkActivationTime) is a multiple of 3)
  - H = (1 + 0.5 * OEExtraDelay) * GPMC_FCLK if ((OEOffTime – ClkActivationTime – 1) is a multiple of 3)
  - H = (2 + 0.5 * OEExtraDelay) * GPMC_FCLK if ((OEOffTime – ClkActivationTime – 2) is a multiple of 3)

(9) **For WE falling edge (WE activated):**

- **Case GpmcFCLKDivider = 0:**
  - I = 0.5 * WEExtraDelay * GPMC_FCLK
- **Case GpmcFCLKDivider = 1:**
  - I = 0.5 * WEExtraDelay * GPMC_FCLK if (ClkActivationTime and WEOnTime are odd) or (ClkActivationTime and WEOnTime are even)
  - I = (1 + 0.5 * WEExtraDelay) * GPMC_FCLK otherwise
- **Case GpmcFCLKDivider = 2:**
  - I = 0.5 * WEExtraDelay * GPMC_FCLK if ((WEOnTime – ClkActivationTime) is a multiple of 3)
  - I = (1 + 0.5 * WEExtraDelay) * GPMC_FCLK if ((WEOnTime – ClkActivationTime – 1) is a multiple of 3)
  - I = (2 + 0.5 * WEExtraDelay) * GPMC_FCLK if ((WEOnTime – ClkActivationTime – 2) is a multiple of 3)

For WE rising edge (WE deactivated):

- **Case GpmcFCLKDivider = 0:**
  - I = 0.5 * WEExtraDelay * GPMC_FCLK
- **Case GpmcFCLKDivider = 1:**
  - I = 0.5 * WEExtraDelay * GPMC_FCLK if (ClkActivationTime and WEOffTime are odd) or (ClkActivationTime and WEOffTime are even)
  - I = (1 + 0.5 * WEExtraDelay) * GPMC_FCLK otherwise
- **Case GpmcFCLKDivider = 2:**
  - I = 0.5 * WEExtraDelay * GPMC_FCLK if ((WEOffTime – ClkActivationTime) is a multiple of 3)
  - I = (1 + 0.5 * WEExtraDelay) * GPMC_FCLK if ((WEOffTime – ClkActivationTime – 1) is a multiple of 3)
  - I = (2 + 0.5 * WEExtraDelay) * GPMC_FCLK if ((WEOffTime – ClkActivationTime – 2) is a multiple of 3)

(10) J = GPMC_FCLK period

(11) In gpmc_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7. In gpmc_waitx, x is equal to 0, 1, 2, or 3.

(12) P = gpmc_clk period

(13) **For read:** K = (ADVRdOffTime – ADVOnTime) * (TimeParaGranularity + 1) * GPMC_FCLK
For write: K = (ADVWrOffTime – ADVOnTime) * (TimeParaGranularity + 1) * GPMC_FCLK

(14) GPMC_FCLK is General-Purpose Memory Controller internal functional clock.

(15) Related to the gpmc_clk output clock maximum and minimum frequencies programmable in the I/F module by setting the GPMC_CONFIG1_CSx configuration register bit field GpmcFCLKDivider.

(16) The jitter probability density can be approximated by a Gaussian function.

(17) M = (RdCycleTime - AccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK
Above M parameter expression is given as one example of GPMC programming. IO DIR signal will go from IN to OUT after both RdCycleTime and BusTurnAround completion. Behavior of IO direction signal does depend on kind of successive Read/Write accesses performed to Memory and multiplexed or non-multiplexed memory addressing scheme, bus keeping feature enabled or not. IO DIR behavior is automatically handled by GPMC controller. For a full description of the gpmc_io_dir feature, see the *OMAP35x Technical Reference Manual (TRM)* [literature number SPRUF98].

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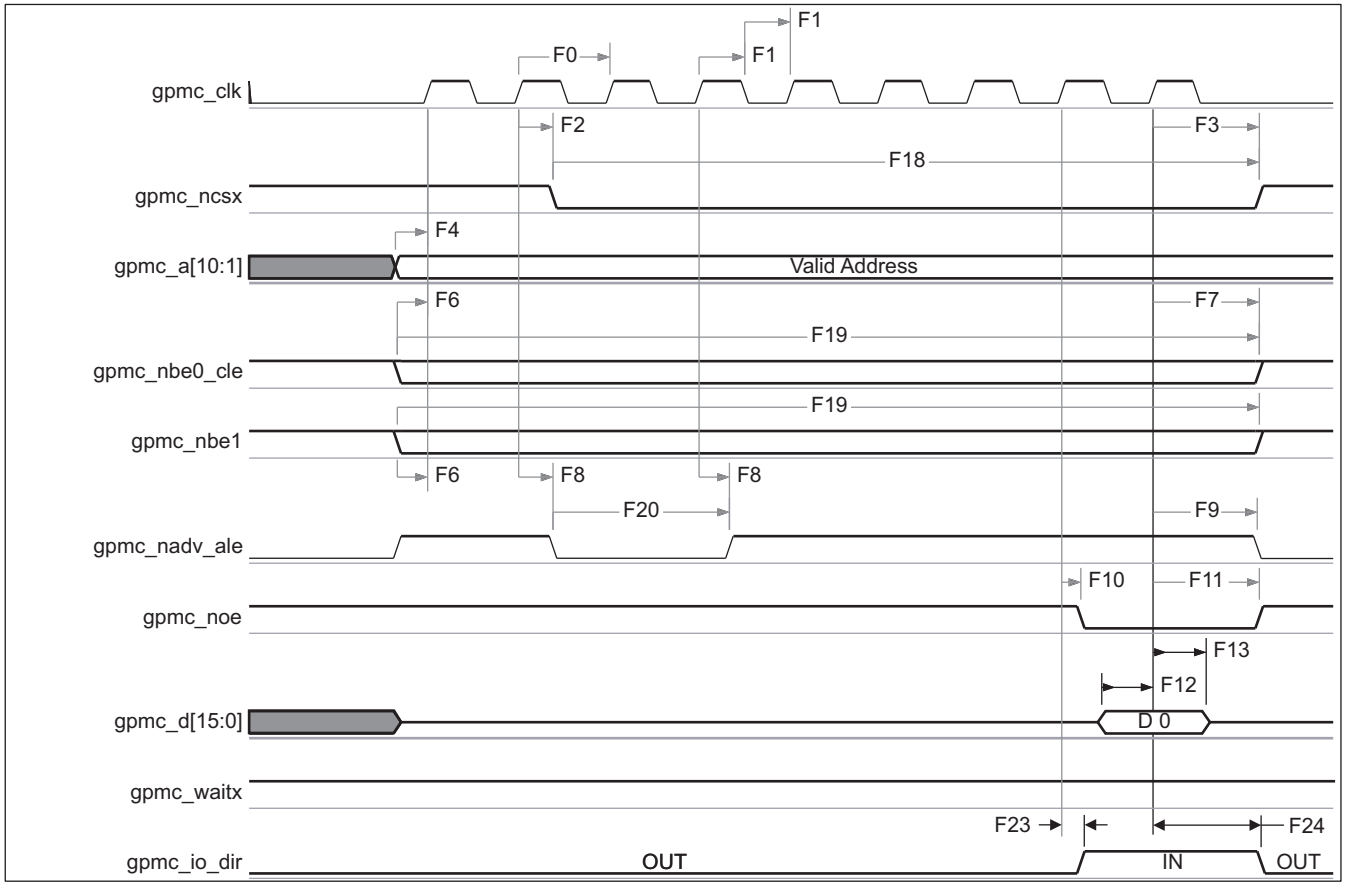

In gpmc_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7. In gpmc_waitx, x is equal to 0, 1, 2, or 3.

Figure 6-2. GPMC/NOR Flash – Synchronous Single Read – (GpmcFCLKDivider = 0)

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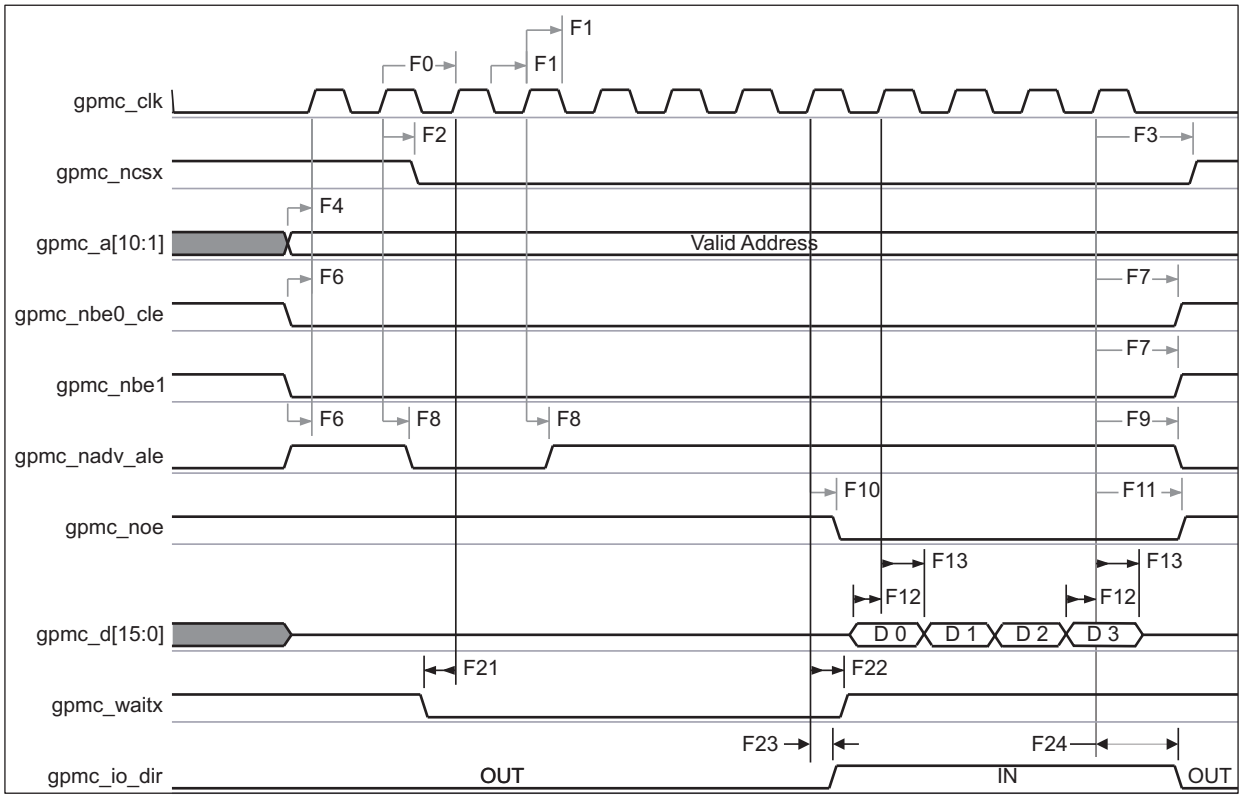
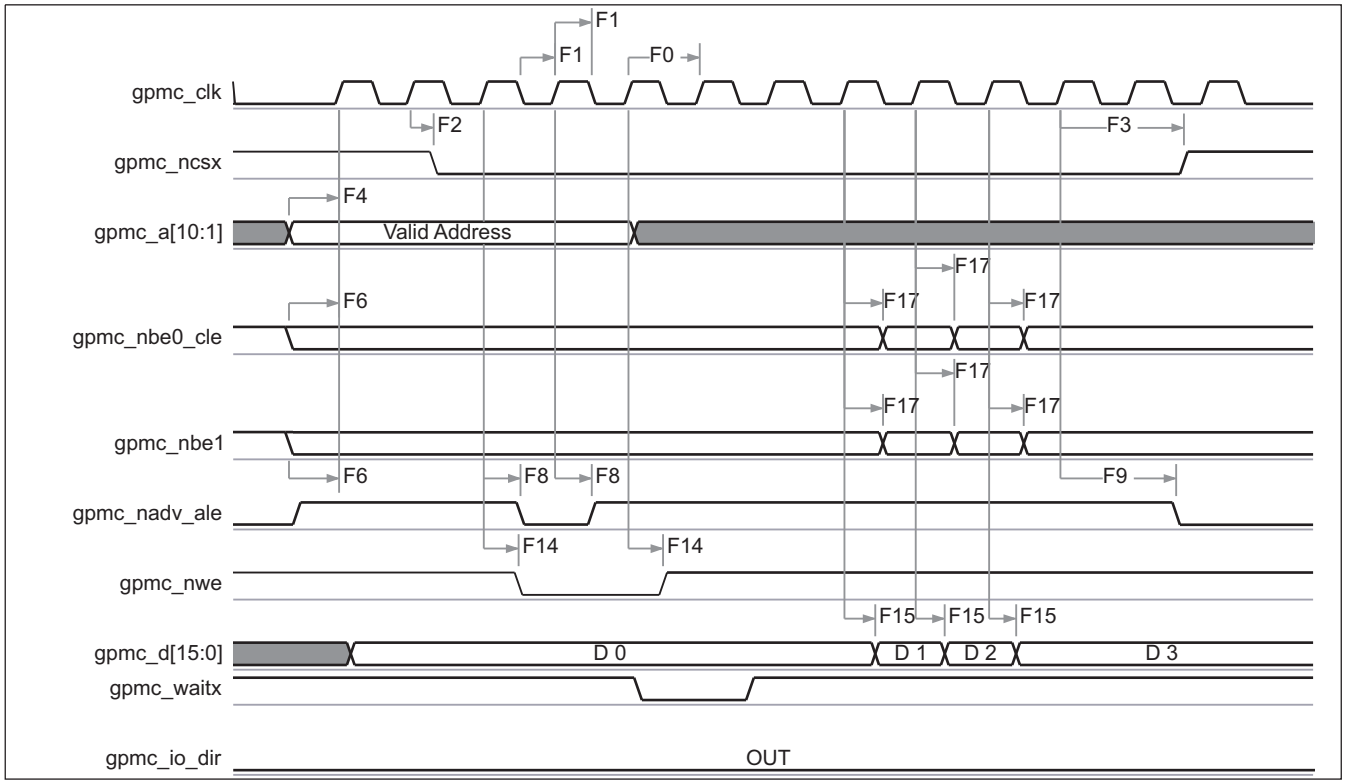


In gpmc_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7. In gpmc_waitx, x is equal to 0, 1, 2, or 3.

Figure 6-3. GPMC/NOR Flash – Synchronous Burst Read – 4x16-bit (GpmcFCLKDivider = 0)



In gpmc_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7. In gpmc_waitx, x is equal to 0, 1, 2, or 3.

Figure 6-4. GPMC/NOR Flash – Synchronous Burst Write – (GpmcFCLKDivider = 0)

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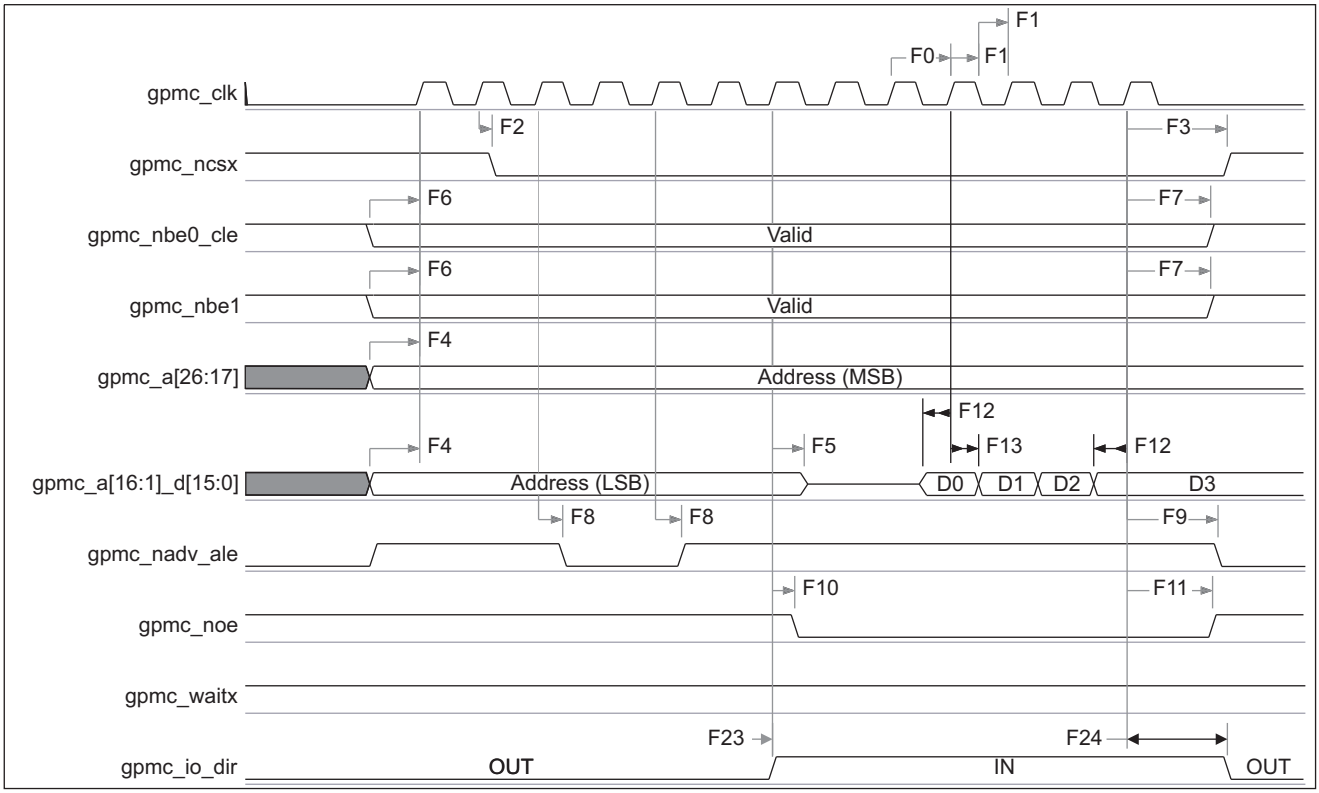
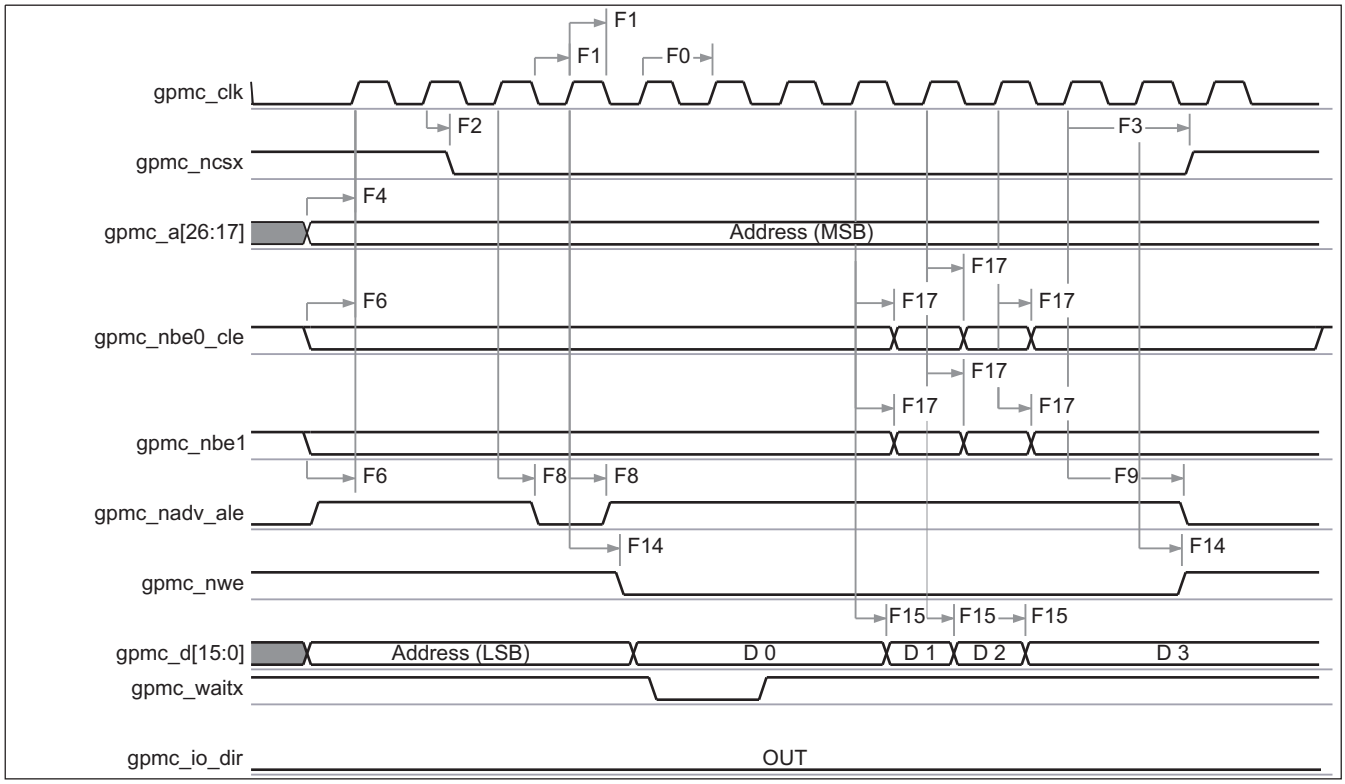


In gpmc_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7. In gpmc_waitx, x is equal to 0, 1, 2, or 3.

Figure 6-5. GPMC/Multiplexed NOR Flash – Synchronous Burst Read



In gpmc_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7. In gpmc_waitx, x is equal to 0, 1, 2, or 3.

Figure 6-6. GPMC/Multiplexed NOR Flash – Synchronous Burst Write

6.4.1.2 GPMC/NOR Flash Interface Asynchronous Timing

Table 6-7 and Table 6-8 assume testing over the recommended operating conditions (see Figure 6-7 through Figure 6-12) and electrical characteristic conditions.

Table 6-5. GPMC/NOR Flash Asynchronous Mode Timing Conditions

TIMING CONDITION PARAMETER		VALUE	UNIT
Input Conditions			
t_R	Input signal rise time	1.8	ns
t_F	Input signal fall time	1.8	ns
Output Conditions			
C_{LOAD}	Output load capacitance	15.94	pF

Table 6-6. GPMC/NOR Flash Interface Asynchronous Timing – Internal Parameters(1) (2)

NO.	PARAMETER	1.15 V		1.0 V		0.9 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
FI1	Maximum output data generation delay from internal functional clock		6.5		9.1		13.7	ns
FI2	Maximum input data capture delay by internal functional clock		4		5.6		8.1	ns
FI3	Maximum device select generation delay from internal functional clock		6.5		9.1		13.7	ns
FI4	Maximum address generation delay from internal functional clock		6.5		9.1		13.7	ns

(1) The internal parameters table must be used to calculate Data Access Time stored in the corresponding CS register bit field.
(2) Internal parameters are referred to the GPMC functional internal clock which is not provided externally.

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Table 6-6. GPMC/NOR Flash Interface Asynchronous Timing – Internal Parameters[1] [2] (continued)

NO.	PARAMETER	1.15 V		1.0 V		0.9 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
FI5	Maximum address valid generation delay from internal functional clock		6.5		9.1		13.7	ns
FI6	Maximum byte enable generation delay from internal functional clock		6.5		9.1		13.7	ns
FI7	Maximum output enable generation delay from internal functional clock		6.5		9.1		13.7	ns
FI8	Maximum write enable generation delay from internal functional clock		6.5		9.1		13.7	ns
FI9	Maximum functional clock skew		100		170		200	ps

Table 6-7. GPMC/NOR Flash Interface Timing Requirements – Asynchronous Mode

NO.	PARAMETER		1.15 V		1.0 V		0.9 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
FA5[1]	$t_{acc(DAT)}$	Data maximum access time		H[2]		H[2]		H[2]	GPMC_FCLK cycles
FA20[3]	$t_{acc1-pgmode(DAT)}$	Page mode successive data maximum access time		P[4]		P[4]		P[4]	GPMC_FCLK cycles
FA21[5]	$t_{acc2-pgmode(DAT)}$	Page mode first data maximum access time		H[2]		H[2]		H[2]	GPMC_FCLK cycles

(1) The FA5 parameter illustrates the amount of time required to internally sample input Data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input Data is internally sampled by active functional clock edge. FA5 value must be stored inside the AccessTime register bit field.
(2) H = AccessTime * (TimeParaGranularity + 1)
(3) The FA20 parameter illustrates amount of time required to internally sample successive input Page Data. It is expressed in number of GPMC functional clock cycles. After each access to input Page Data, next input Page Data is internally sampled by active functional clock edge after FA20 functional clock cycles. The FA20 value must be stored in the PageBurstAccessTime register bit field.
(4) P = PageBurstAccessTime * (TimeParaGranularity + 1)
(5) The FA21 parameter illustrates amount of time required to internally sample first input Page Data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA21 functional clock cycles, First input Page Data is internally sampled by active functional clock edge. FA21 value must be stored inside the AccessTime register bit field.

Table 6-8. GPMC/NOR Flash Interface Switching Characteristics – Asynchronous Mode

NO.	PARAMETER			1.15 V		1.0 V		0.9 V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
	$t_{R(DO)}$	Rise time, output data			2.0		2.0		2.0	ns
	$t_{F(DO)}$	Fall time, output data			2.0		2.0		2.0	ns
FA0	$t_{W(nBEV)}$	Pulse duration, gpmc_nbe0_cle, gpmc_nbe1 valid time	Read	N(12)		N(12)		N(12)		ns
			Write	N(12)		N(12)		N(12)		ns
FA1	$t_{W(nCSV)}$	Pulse duration, gpmc_ncsx(13) v low	Read	A(1)		A(1)		A(1)		ns
			Write	A(1)		A(1)		A(1)		ns
FA3	$t_{d(nCSV-nADVIV)}$	Delay time, gpmc_ncsx(13) valid to gpmc_nadv_ale invalid	Read	B(2) – 0.2	B(2) + 2.0	B(2) – 0.2	B(2) + 2.6	B(2) – 0.2	B(2) + 3.7	ns
			Write	B(2) – 0.2	B(2) + 2.0	B(2) – 0.2	B(2) + 2.6	B(2) – 0.2	B(2) + 3.7	ns
FA4	$t_{d(nCSV-nOEIV)}$	Delay time, gpmc_ncsx(13) valid to gpmc_noe invalid (Single read)		C(3) – 0.2	C(3) + 2.0	C(3) – 0.2	C(3) + 2.6	C(3) – 0.2	C(3) + 3.7	ns
FA9	$t_{d(AV-nCSV)}$	Delay time, address bus valid to gpmc_ncsx(13) valid		J(9) – 0.2	J(9) + 2.0	J(9) – 0.2	J(9) + 2.6	J(9) – 0.2	J(9) + 3.7	ns

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Table 6-8. GPMC/NOR Flash Interface Switching Characteristics – Asynchronous Mode (continued)

NO.	PARAMETER		1.15 V		1.0 V		0.9 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
FA10	$t_{d(nBEV-nCSV)}$	Delay time, gpmc_nbe0_cle, gpmc_nbe1 valid to gpmc_ncsx(13) valid	J(9) – 0.2	J(9) + 2.0	J(9) – 0.2	J(9) + 2.6	J(9) – 0.2	J(9) + 3.7	ns
FA12	$t_{d(nCSV-nADVV)}$	Delay time, gpmc_ncsx(13) valid to gpmc_nadv_ale valid	K(10) – 0.2	K(10) + 2.0	K(10) – 0.2	K(10) + 2.6	K(10) – 0.2	K(10) + 3.7	ns
FA13	$t_{d(nCSV-nOEV)}$	Delay time, gpmc_ncsx(13) valid to gpmc_noe valid	L(11) – 0.2	L(11) + 2.0	L(11) – 0.2	L(11) + 2.6	L(11) – 0.2	L(11) + 3.7	ns
FA14	$t_{d(nCSV-IODIR)}$	Delay time, gpmc_ncsx(13) valid to gpmc_io_dir high	L(11) – 0.2	L(11) + 2.0	L(11) – 0.2	L(11) + 2.6	L(11) – 0.2	L(11) + 3.7	ns
FA15	$t_{d(nCSV-IODIR)}$	Delay time, gpmc_ncsx(13) valid to gpmc_io_dir low	M(14) – 0.2	M(14) + 2.0	M(14) – 0.2	M(14) + 2.6	M(14) – 0.2	M(14) + 3.7	ns
FA16	$t_{w(AIV)}$	Address invalid duration between 2 successive R/W accesses	G(7)		G(7)		G(7)		ns
FA18	$t_{d(nCSV-nOEIV)}$	Delay time, gpmc_ncsx(13) valid to gpmc_noe invalid (Burst read)	I(8) – 0.2	I(8) + 2.0	I(8) – 0.2	I(8) + 2.6	I(8) – 0.2	I(8) + 3.7	ns
FA20	$t_{w(AV)}$	Pulse duration, address valid – 2nd, 3rd, and 4th accesses	D(4)		D(4)		D(4)		ns
FA25	$t_{d(nCSV-nWEV)}$	Delay time, gpmc_ncsx(13) valid to gpmc_nwe valid	E(5) – 0.2	E(5) + 2.0	E(5) – 0.2	E(5) + 2.6	E(5) – 0.2	E(5) + 3.7	ns
FA27	$t_{d(nCSV-nWEIV)}$	Delay time, gpmc_ncsx(13) valid to gpmc_nwe invalid	F(6) – 0.2	F(6) + 2.0	F(6) – 0.2	F(6) + 2.6	F(6) – 0.2	F(6) + 3.7	ns
FA28	$t_{d(nWEV-DV)}$	Delay time, gpmc_ new valid to data bus valid		2.0		2.6		3.7	ns
FA29	$t_{d(DV-nCSV)}$	Delay time, data bus valid to gpmc_ncsx(13) valid	J(9) – 0.2	J(9) + 2.0	J(9) – 0.2	J(9) + 2.6	J(9) – 0.2	J(9) + 3.7	ns
FA37	$t_{d(nOEV-AIV)}$	Delay time, gpmc_noe valid to gpmc_a[16:1]_d[15:0] address phase end		2.0		2.6		3.7	ns

(1) **For single read:** A = (CSRdOffTime – CSOnTime) * (TimeParaGranularity + 1) * GPMC_FCLK
For single write: A = (CSWrOffTime – CSOnTime) * (TimeParaGranularity + 1) * GPMC_FCLK
For burst read: A = (CSRdOffTime – CSOnTime + (n – 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK
For burst write: A = (CSWrOffTime – CSOnTime + (n – 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK with n being the page burst access number

(2) **For reading:** B = ((ADVRdOffTime – CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (ADVExtraDelay – CSExtraDelay)) * GPMC_FCLK
For writing: B = ((ADVWrOffTime – CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (ADVExtraDelay – CSExtraDelay)) * GPMC_FCLK

(3) C = ((OEOffTime – CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (OEExtraDelay – CSExtraDelay)) * GPMC_FCLK

(4) D = PageBurstAccessTime * (TimeParaGranularity + 1) * GPMC_FCLK

(5) E = ((WEOnTime – CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (WEExtraDelay – CSExtraDelay)) * GPMC_FCLK

(6) F = ((WEOffTime – CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (WEExtraDelay – CSExtraDelay)) * GPMC_FCLK

(7) G = Cycle2CycleDelay * GPMC_FCLK

(8) I = ((OEOffTime + (n – 1) * PageBurstAccessTime – CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (OEExtraDelay – CSExtraDelay)) * GPMC_FCLK

(9) J = (CSOnTime * (TimeParaGranularity + 1) + 0.5 * CSExtraDelay) * GPMC_FCLK

(10) K = ((ADVOnTime – CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (ADVExtraDelay – CSExtraDelay)) * GPMC_FCLK

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(11) L = ((OEOnTime – CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (OEExtraDelay – CSExtraDelay)) * GPMC_FCLK

(12) **For single read:** N = RdCycleTime * (TimeParaGranularity + 1) * GPMC_FCLK
For single write: N = WrCycleTime * (TimeParaGranularity + 1) * GPMC_FCLK
For burst read: N = (RdCycleTime + (n – 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK
For burst write: N = (WrCycleTime + (n – 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK

(13) In gpmc_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7.

(14) M = ((RdCycleTime - CSOnTime) * (TimeParaGranularity + 1) - 0.5 * CSExtraDelay) * GPMC_FCLK
Above M parameter expression is given as one example of GPMC programming. IO DIR signal will go from IN to OUT after both RdCycleTime and BusTurnAround completion. Behavior of IO direction signal does depend on kind of successive Read/Write accesses performed to Memory and multiplexed or non-multiplexed memory addressing scheme, bus keeping feature enabled or not. IO DIR behavior is automatically handled by GPMC controller. For a full description of the gpmc_io_dir feature, see the *OMAP35x Technical Reference Manual (TRM)* [literature number SPRUF98].

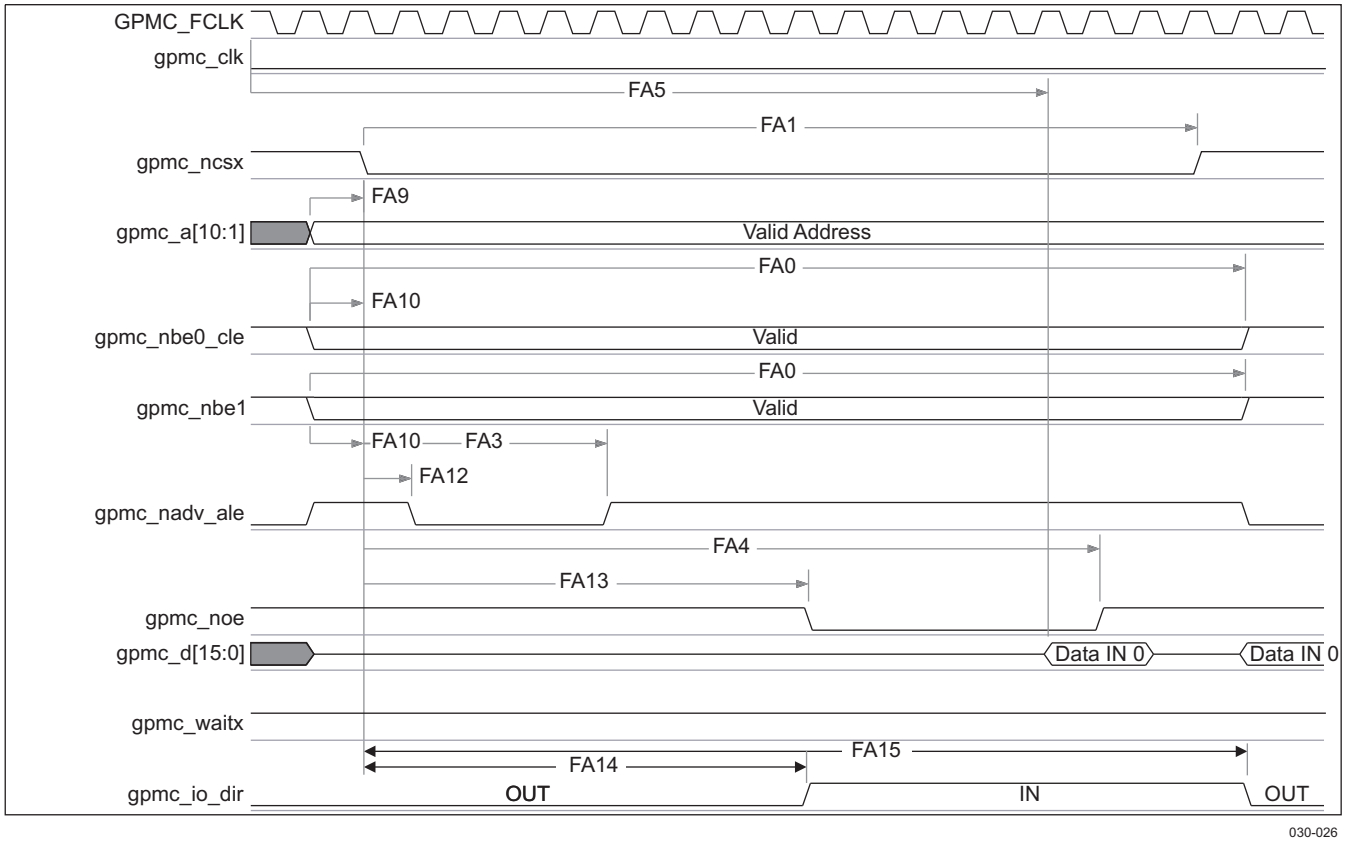

Figure 6-7. GPMC/NOR Flash – Asynchronous Read – Single Word Timing(1) (2) (3)

(1) In gpmc_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7. In gpmc_waitx, x is equal to 0, 1, 2, or 3.

(2) FA5 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data is internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bit field.

(3) GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.

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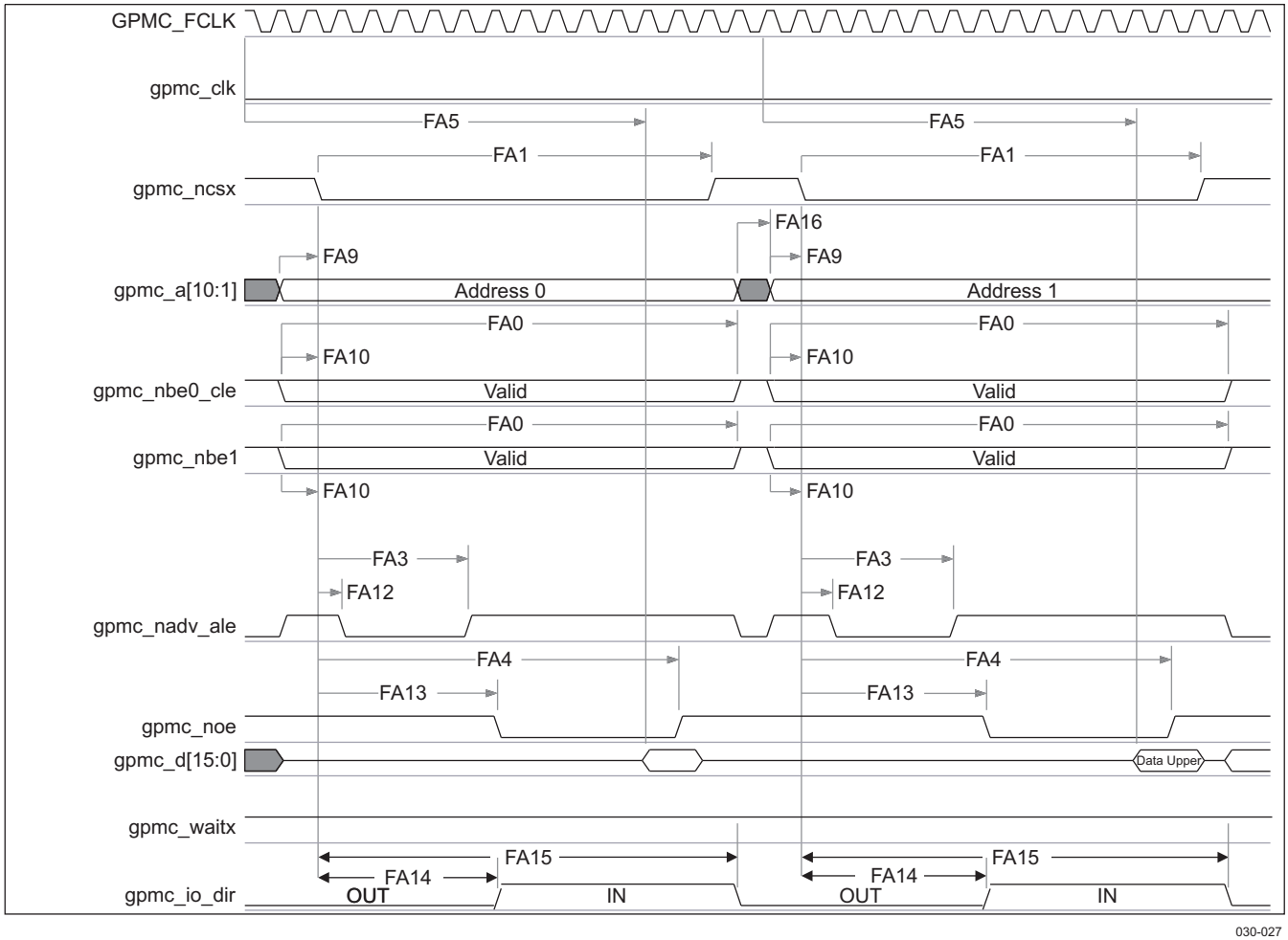

Figure 6-8. GPMC/NOR Flash – Asynchronous Read – 32-bit Timing(1) (2) (3)

(1) In gpmc_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7. In gpmc_waitx, x is equal to 0, 1, 2, or 3.

(2) FA5 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data is internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bit field.

(3) GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.

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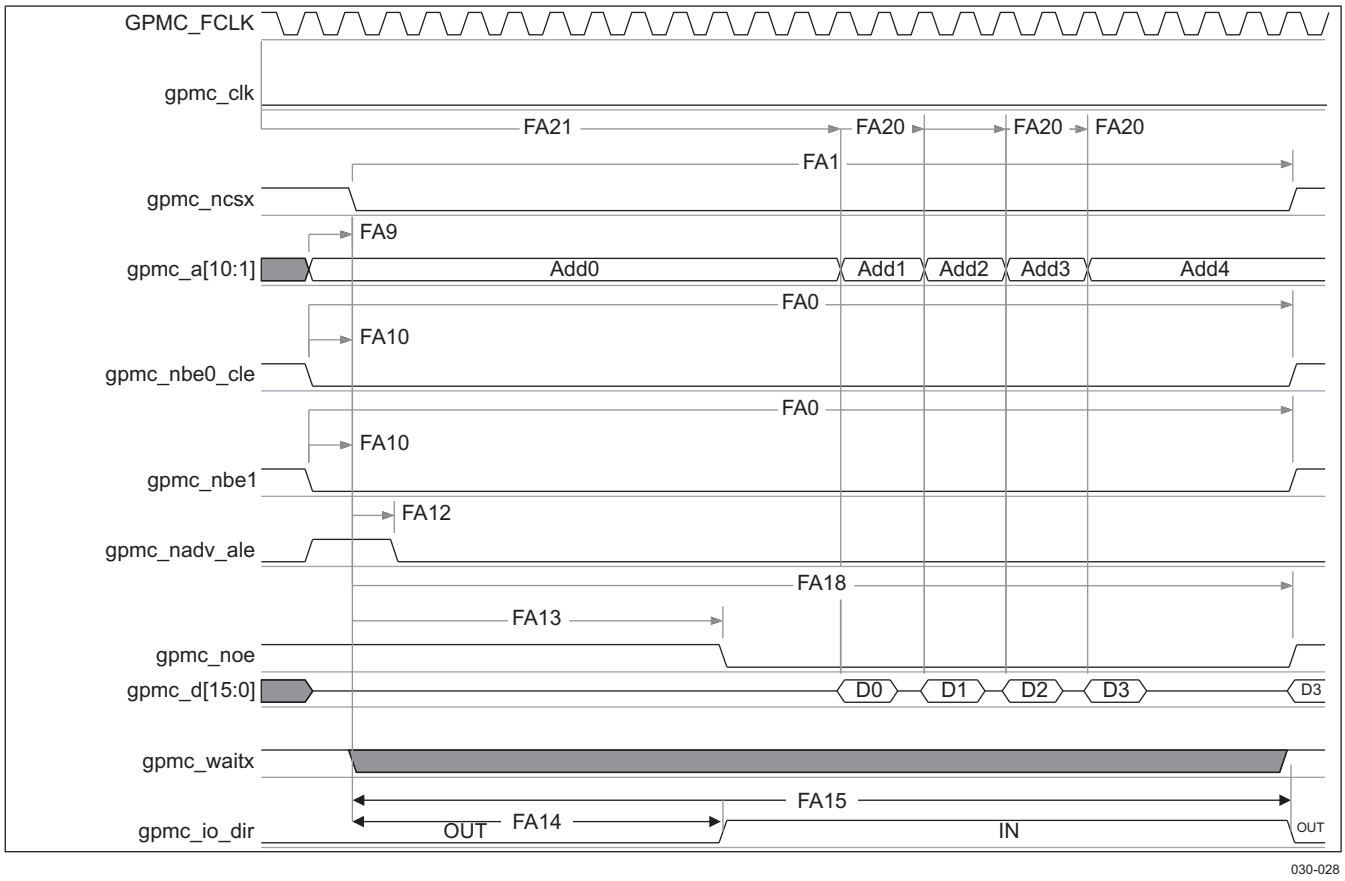

Figure 6-9. GPMC/NOR Flash – Asynchronous Read – Page Mode 4x16-bit Timing(1) (2) (3) (4)

(1) In gpmc_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7. In gpmc_waitx, x is equal to 0, 1, 2, or 3.

(2) FA21 parameter illustrates amount of time required to internally sample first input page data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA21 functional clock cycles, first input page data is internally sampled by active functional clock edge. FA21 value must be stored inside AccessTime register bit field.

(3) FA20 parameter illustrates amount of time required to internally sample successive input page data. It is expressed in number of GPMC functional clock cycles. After each access to input page data, next input page data is internally sampled by active functional clock edge after FA20 functional clock cycles. FA20 is also the duration of address phases for successive input page data (excluding first input page data). FA20 value must be stored in PageBurstAccessTime register bit field.

(4) GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.

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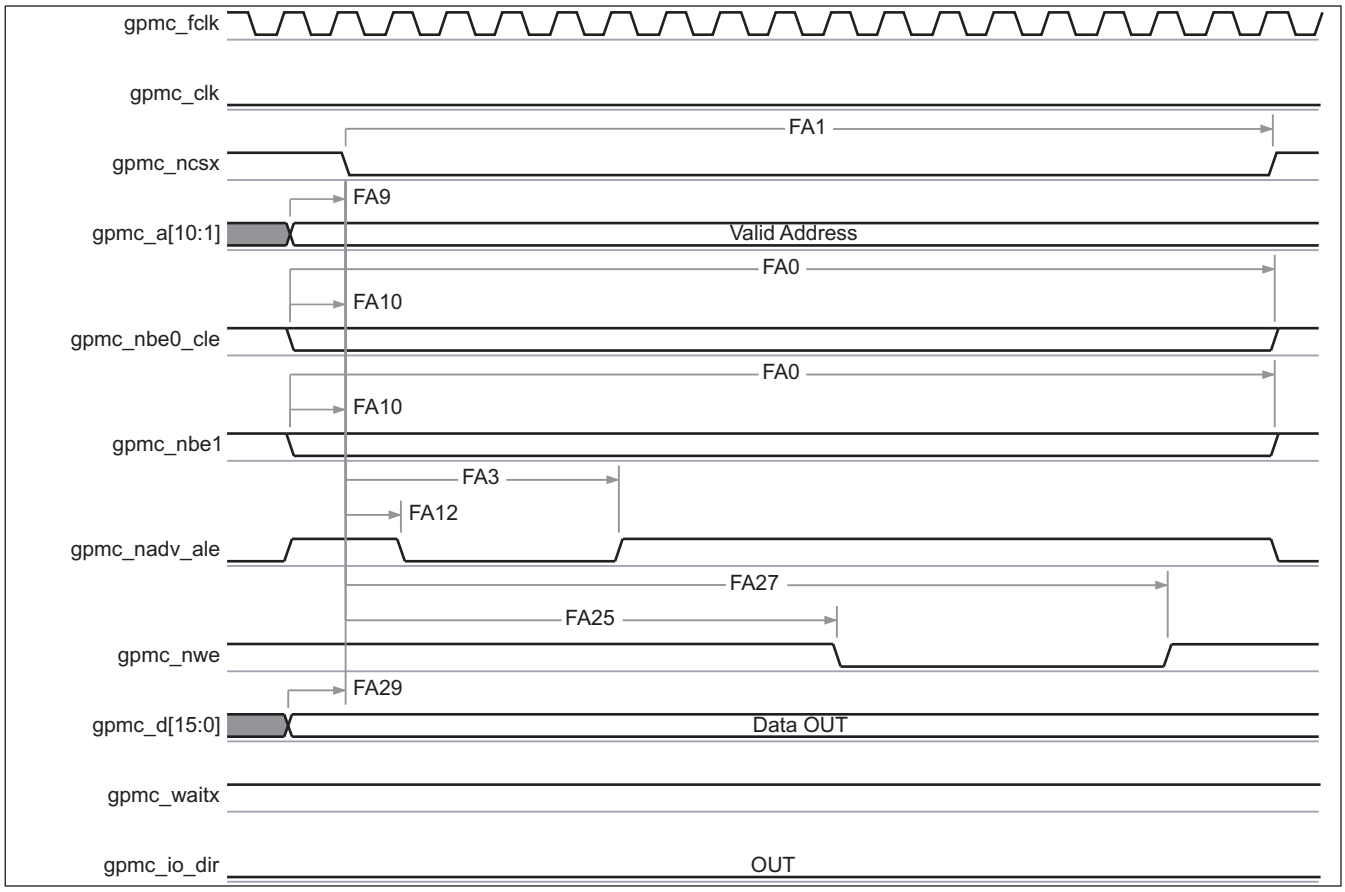

In gpmc_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7. In gpmc_waitx, x is equal to 0, 1, 2, or 3.

Figure 6-10. GPMC/NOR Flash – Asynchronous Write – Single Word Timing

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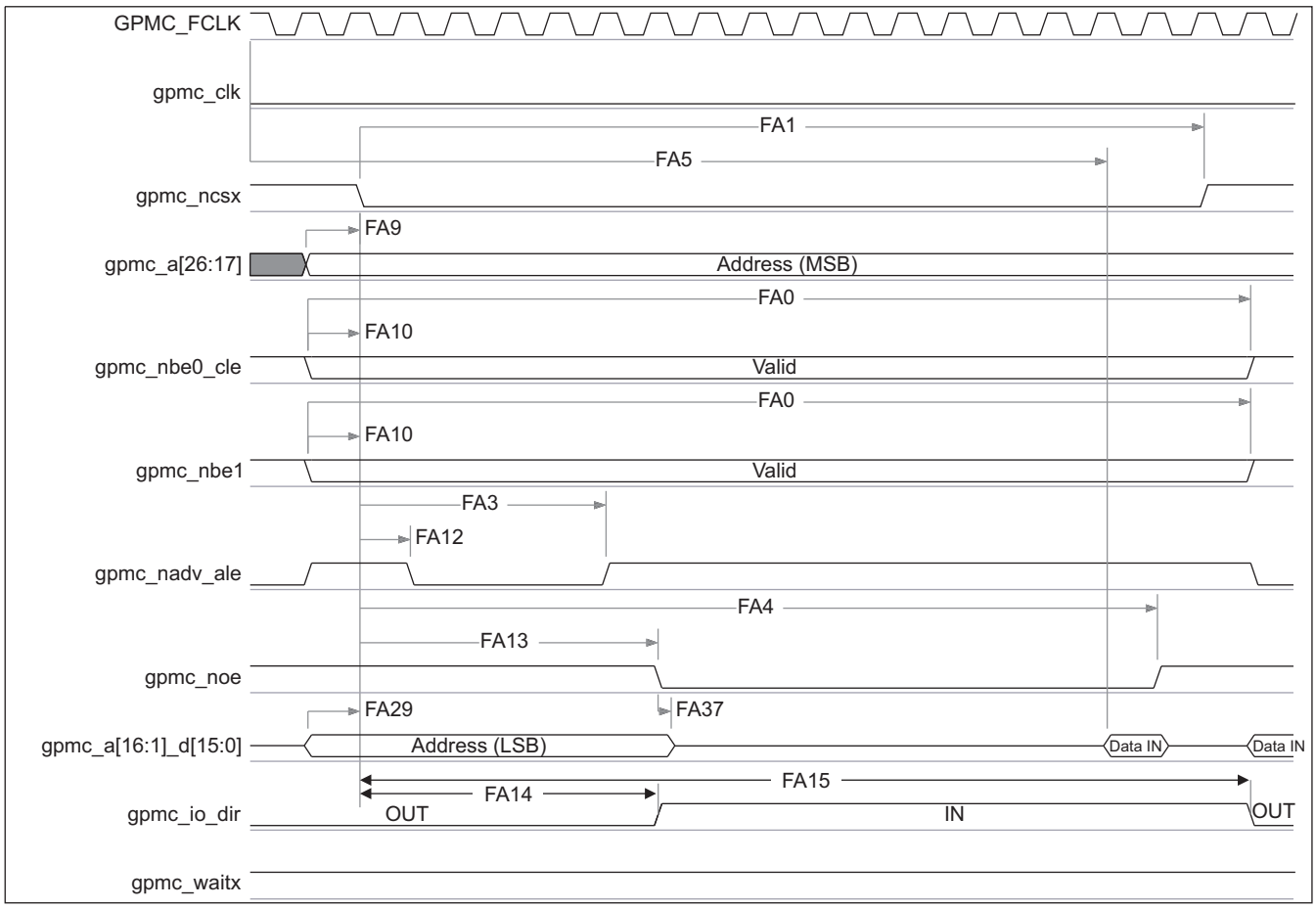

Figure 6-11. GPMC/Multiplexed NOR Flash – Asynchronous Read – Single Word Timing(1) (2) (3)

(1) In gpmc_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7. In gpmc_waitx, x is equal to 0, 1, 2, or 3.

(2) FA5 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data is internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bit field.

(3) GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.

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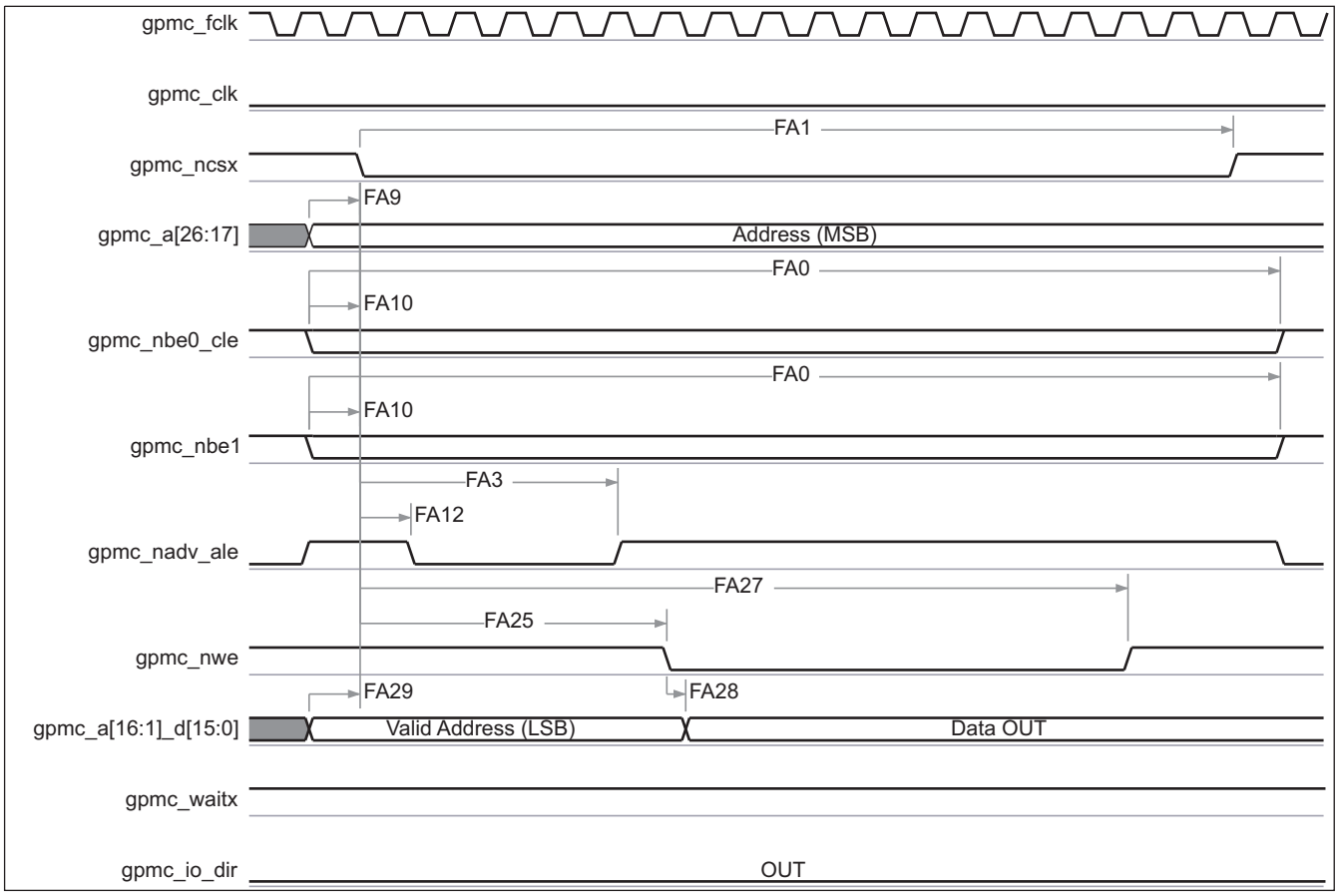

In gpmc_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7. In gpmc_waitx, x is equal to 0, 1, 2, or 3.

Figure 6-12. GPMC/Multiplexed NOR Flash – Asynchronous Write – Single Word Timing

6.4.1.3 GPMC/NAND Flash Interface Timing

Table 6-10 through Table 6-12 assume testing over the recommended operating conditions (see Figure 6-13 through Figure 6-16) and electrical characteristic conditions.

Table 6-9. GPMC/NAND Flash Asynchronous Mode Timing Conditions

TIMING CONDITION PARAMETER		VALUE	UNIT
Input Conditions			
t_R	Input signal rise time	1.8	ns
t_F	Input signal fall time	1.8	ns
Output Conditions			
C_{LOAD}	Output load capacitance	15.94	pF

Table 6-10. GPMC/NAND Flash Interface Asynchronous Timing – Internal Parameters(1) (2)

NO.	PARAMETER	1.15 V		1.0 V		0.9 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
GNFI1	Maximum output data generation delay from internal functional clock		6.5		9.1		13.7	ns
GNFI2	Maximum input data capture delay by internal functional clock		4		5.6		8.1	ns

(1) Internal parameters table must be used to calculate data access time stored in the corresponding CS register bit field.
(2) Internal parameters are referred to the GPMC functional internal clock which is not provided externally.

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Table 6-10. GPMC/NAND Flash Interface Asynchronous Timing – Internal Parameters(1) (2) (continued)

NO.	PARAMETER	1.15 V		1.0 V		0.9 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
GNFI3	Maximum device select generation delay from internal functional clock		6.5		9.1		13.7	ns
GNFI4	Maximum address latch enable generation delay from internal functional clock		6.5		9.1		13.7	ns
GNFI5	Maximum command latch enable generation delay from internal functional clock		6.5		9.1		13.7	ns
GNFI6	Maximum output enable generation delay from internal functional clock		6.5		9.1		13.7	ns
GNFI7	Maximum write enable generation delay from internal functional clock		6.5		9.1		13.7	ns
GNFI8	Maximum functional clock skew		100		170		200	ps

Table 6-11. GPMC/NAND Flash Interface Timing Requirements

NO.	PARAMETER		1.15 V		1.0 V		0.9 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
GNF12(1)	$t_{acc(DAT)}$	Data maximum access time		J(2)		J(2)		J(2)	GPMC_FCLK cycles

(1) The GNF12 parameter illustrates the amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of the read cycle and after GNF12 functional clock cycles, input data is internally sampled by the active functional clock edge. The GNF12 value must be stored inside AccessTime register bit field.
(2) J = AccessTime * (TimeParaGranularity + 1)

Table 6-12. GPMC/NAND Flash Interface Switching Characteristics

NO.	PARAMETER		1.15 V		1.0 V		0.9 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
	$t_{R(DO)}$	Rise time, output data		2.0		2.0		2.0	ns
	$t_{F(DO)}$	Fall time, output data		2.0		2.0		2.0	ns
GNF0	$t_{w(nWEV)}$	Pulse duration, gpmc_nwe valid time	A(1)		A(1)		A(1)		ns
GNF1	$t_{d(nCSV-nWEV)}$	Delay time, gpmc_ncsx(13) valid to gpmc_nwe valid	B(2) – 0.2	B(2) + 2.0	B(2) – 0.2	B(2) + 2.6	B(2) – 0.2	B(2) + 3.7	ns
GNF2	$t_{w(CLEH-nWEV)}$	Delay time, gpmc_nbe0_cle high to gpmc_nwe valid	C(3) – 0.2	C(3) + 2.0	C(3) – 0.2	C(3) + 2.6	C(3) – 0.2	C(3) + 3.7	ns
GNF3	$t_{w(nWEV-DV)}$	Delay time, gpmc_d[15:0] valid to gpmc_nwe valid	D(4) – 0.2	D(4) + 2.0	D(4) – 0.2	D(4) + 2.6	D(4) – 0.2	D(4) + 3.7	ns
GNF4	$t_{w(nWEIV-DIV)}$	Delay time, gpmc_nwe invalid to gpmc_d[15:0] invalid	E(5) – 0.2	E(5) + 2.0	E(5) – 0.2	E(5) + 2.6	E(5) – 0.2	E(5) + 3.7	ns
GNF5	$t_{w(nWEIV-CLEIV)}$	Delay time, gpmc_nwe invalid to gpmc_nbe0_cle invalid	F(6) – 0.2	F(6) + 2.0	F(6) – 0.2	F(6) + 2.6	F(6) – 0.2	F(6) + 3.7	ns

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Table 6-12. GPMC/NAND Flash Interface Switching Characteristics (continued)

NO.	PARAMETER		1.15 V		1.0 V		0.9 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
GNF6	$t_{w(nWEIV-nCSIV)}$	Delay time, gpmc_nwe invalid to gpmc_ncsx(13) invalid	G(7) – 0.2	G(7) + 2.0	G(7) – 0.2	G(7) + 2.6	G(7) – 0.2	G(7) + 3.7	ns
GNF7	$t_{w(ALEH-nWEV)}$	Delay time, gpmc_nadv_ale High to gpmc_nwe valid	C(3) – 0.2	C(3) + 2.0	C(3) – 0.2	C(3) + 2.6	C(3) – 0.2	C(3) + 3.7	ns
GNF8	$t_{w(nWEIV-ALEIV)}$	Delay time, gpmc_nwe invalid to gpmc_nadv_ale invalid	F(6) – 0.2	F(6) + 2.0	F(6) – 0.2	F(6) + 2.6	F(6) – 0.2	F(6) + 3.7	ns
GNF9	$t_{c(nWE)}$	Cycle time, Write cycle time	H(8)		H(8)		H(8)		ns
GNF10	$t_{d(nCSV-nOEV)}$	Delay time, gpmc_ncsx(13) valid to gpmc_noe valid	I(9) – 0.2	I(9) + 2.0	I(9) – 0.2	I(9) + 2.6	I(9) – 0.2	I(9) + 3.7	ns
GNF13	$t_{w(nOEV)}$	Pulse duration, gpmc_noe valid time	K(10)		K(10)		K(10)		ns
GNF14	$t_{c(nOE)}$	Cycle time, Read cycle time	L(11)		L(11)		L(11)		ns
GNF15	$t_{w(nOEIV-nCSIV)}$	Delay time, gpmc_noe invalid to gpmc_ncsx(13) invalid	M(12) – 0.2	M(12) + 2.0	M(12) – 0.2	M(12) + 2.6	M(12) – 0.2	M(12) + 3.7	ns

(1) A = (WEOffTime – WEOnTime) * (TimeParaGranularity + 1) * GPMC_FCLK

(2) B = ((WEOnTime – CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (WEExtraDelay – CSExtraDelay)) * GPMC_FCLK

(3) C = ((WEOnTime – ADVOnTime) * (TimeParaGranularity + 1) + 0.5 * (WEExtraDelay – ADVExtraDelay)) * GPMC_FCLK

(4) D = (WEOnTime * (TimeParaGranularity + 1) + 0.5 * WEExtraDelay) * GPMC_FCLK

(5) E = ((WrCycleTime – WEOffTime) * (TimeParaGranularity + 1) – 0.5 * WEExtraDelay) * GPMC_FCLK

(6) F = ((ADVWrOffTime – WEOffTime) * (TimeParaGranularity + 1) + 0.5 * (ADVExtraDelay – WEExtraDelay)) * GPMC_FCLK

(7) G = ((CSWrOffTime – WEOffTime) * (TimeParaGranularity + 1) + 0.5 * (CSExtraDelay – WEExtraDelay)) * GPMC_FCLK

(8) H = WrCycleTime * (1 + TimeParaGranularity) * GPMC_FCLK

(9) I = ((OEOnTime – CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (OEExtraDelay – CSExtraDelay)) * GPMC_FCLK

(10) K = (OEOffTime – OEOnTime) * (1 + TimeParaGranularity) * GPMC_FCLK

(11) L = RdCycleTime * (1 + TimeParaGranularity) * GPMC_FCLK

(12) M = ((CSRdOffTime – OEOffTime) * (TimeParaGranularity + 1) + 0.5 * (CSExtraDelay – OEExtraDelay)) * GPMC_FCLK

(13) In gpmc_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7.

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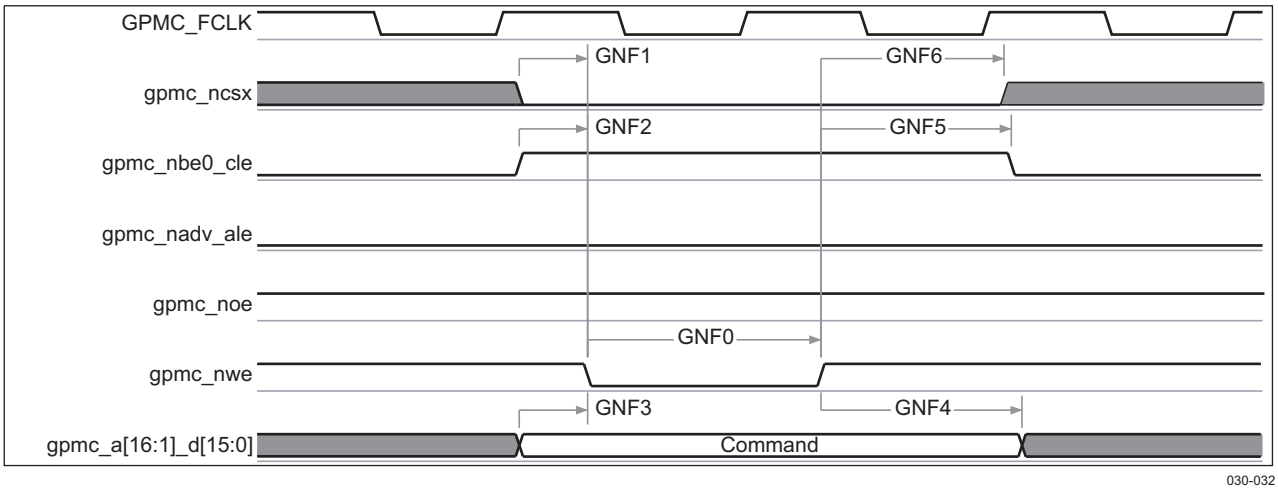
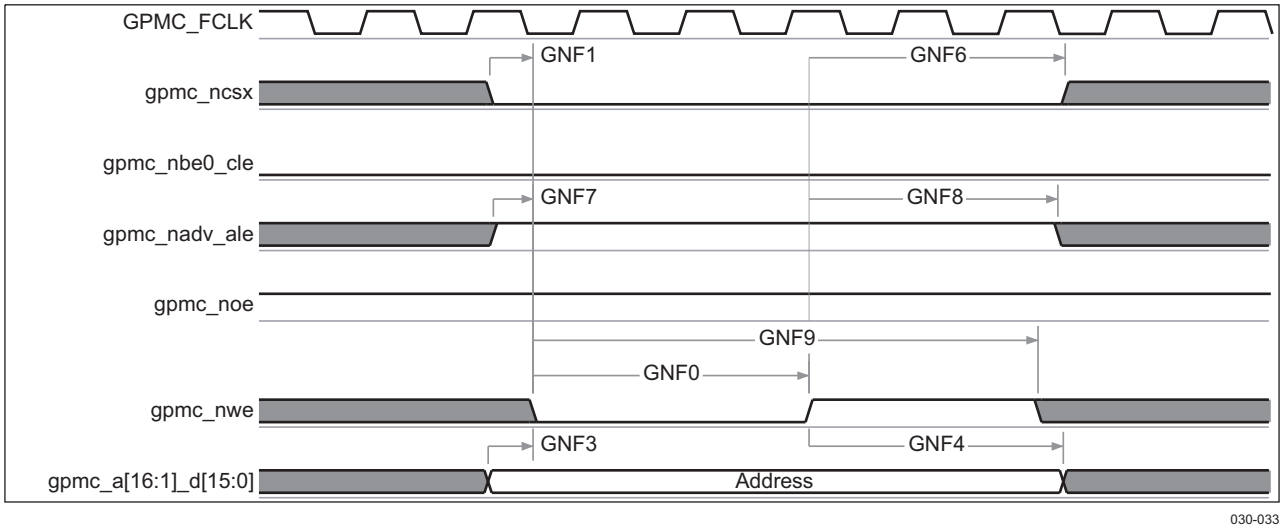


In gpmc_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7.

Figure 6-13. GPMC/NAND Flash – Command Latch Cycle Timing



In gpmc_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7.

Figure 6-14. GPMC/NAND Flash – Address Latch Cycle Timing

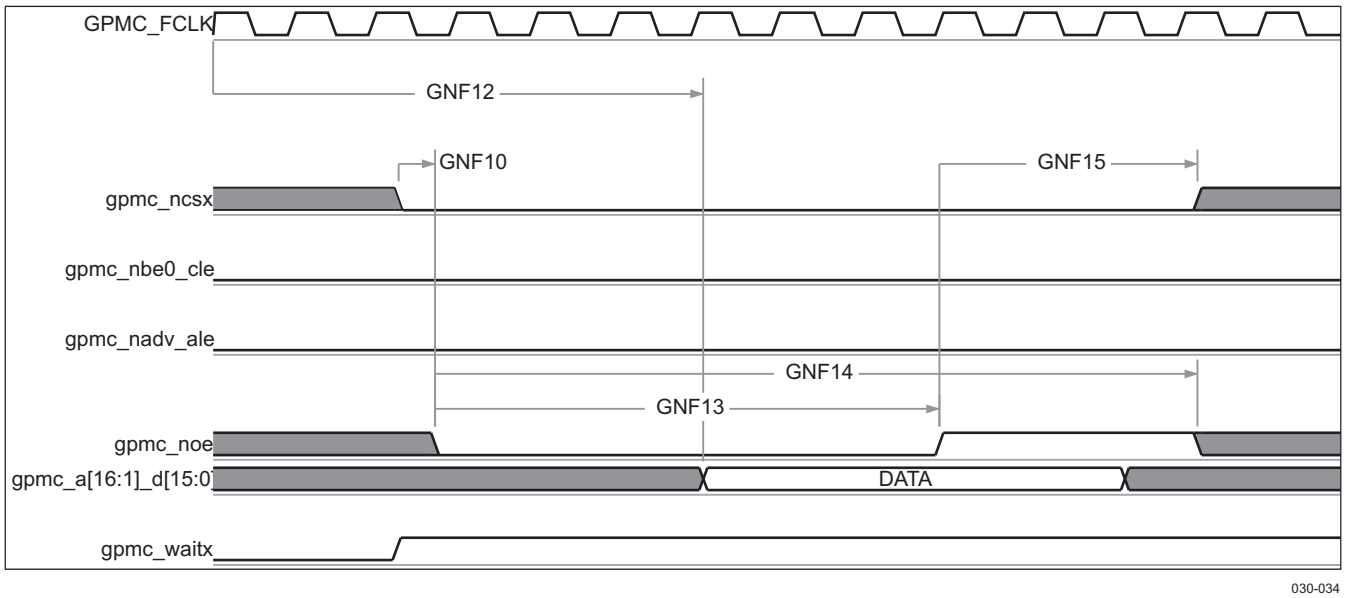
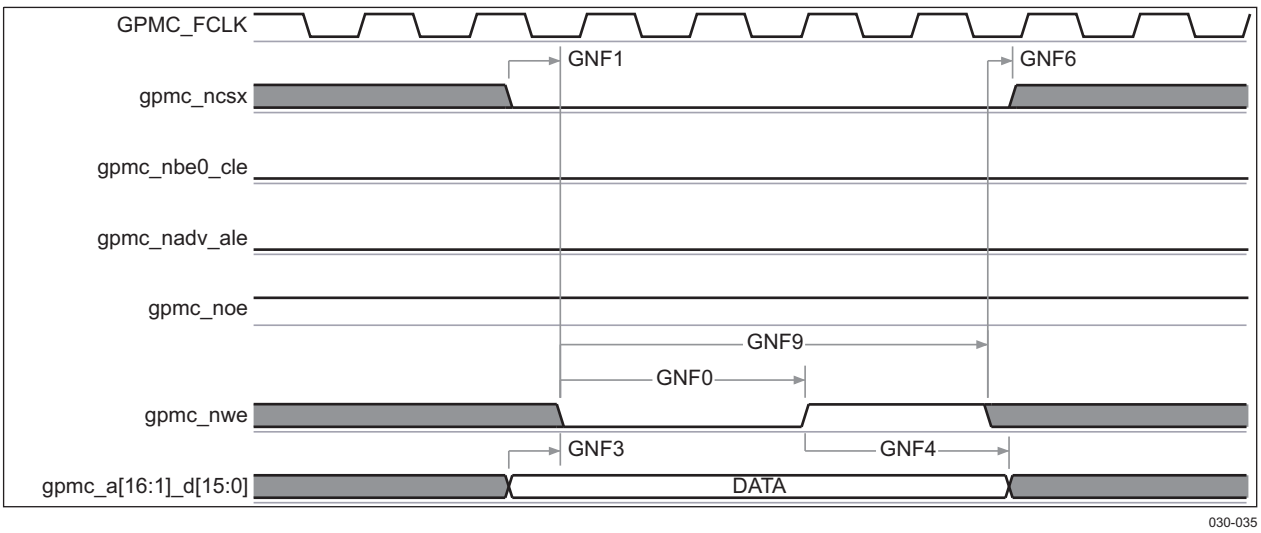


Figure 6-15. GPMC/NAND Flash – Data Read Cycle Timing(1) (2) (3)

(1) The GNF12 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after GNF12 functional clock cycles, input data is internally sampled by active functional clock edge. The GNF12 value must be stored inside AccessTime register bit field.

(2) GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.

(3) In gpmc_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7. In gpmc_waitx, x is equal to 0 ,1, 2, or 3.



In gpmc_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7. In gpmc_waitx, x is equal to 0 or 1.

Figure 6-16. GPMC/NAND Flash – Data Write Cycle Timing

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6.4.2 SDRAM Controller Subsystem (SDRC)

The SDRAM controller subsystem (SDRC) module provides connectivity between the OMAP35x Applications Processor and external DRAM memory components. The SDRC module only supports low-power double-data-rate (LPDDR) SDRAM devices. Memory devices can be interfaced to the SDRC using a stacked-memory approach or through the printed circuit board (PCB). The stacked-memory approach uses the package on package interface pins (available on CBB & CBC package).

6.4.2.1 SDRAM Controller Subsystem Device-Specific Information

The approach to specifying interface timing for the SDRC memory bus is different than on other interfaces such as the general-purpose memory controller (GPMC) and the multi-channel buffered serial ports (McBSPs). For these other interfaces the device timing was specified in terms of data manual specifications and I/O buffer information specification (IBIS) models.

For the SDRC memory bus, the approach is to specify compatible memory devices and provide the printed circuit board (PCB) solution and guidelines directly to the user. Texas Instruments (TI) has performed the simulation and system characterization to ensure all interface timings in this solution are met.

6.4.2.2 LPDDR Interface

The LPDDR interface is balled out on the bottom side of all OMAP35x packages and on the top side of OMAP35x POP packages. The LPDDR interface on the top of the POP package has been designed for compatibility any POP LPDDR device with a matching footprint and compliance with the JEDEC LPDDR-266 specification.

This section provides the timing specification for the bottom-side LPDDR interface as a PCB design and manufacturing specification. The design rules constrain PCB trace length, PCB trace skew, signal integrity, cross-talk, and signal timing. These rules, when followed, result in a reliable LPDDR memory system without the need for a complex timing closure process. For more information regarding guidelines for using this LPDDR specification, see the *Understanding TI's PCB Routing Rule-Based DDR Timing Specification* Application Report (literature number SPRAAV0).

6.4.2.2.1 LPDDR Interface Schematic

Figure 6-17 and Figure 6-18 show the LPDDR interface schematics for a LPDDR memory system. The 1 x16 LPDDR system schematic is identical to Figure 6-17 except that the high word LPDDR device is deleted.

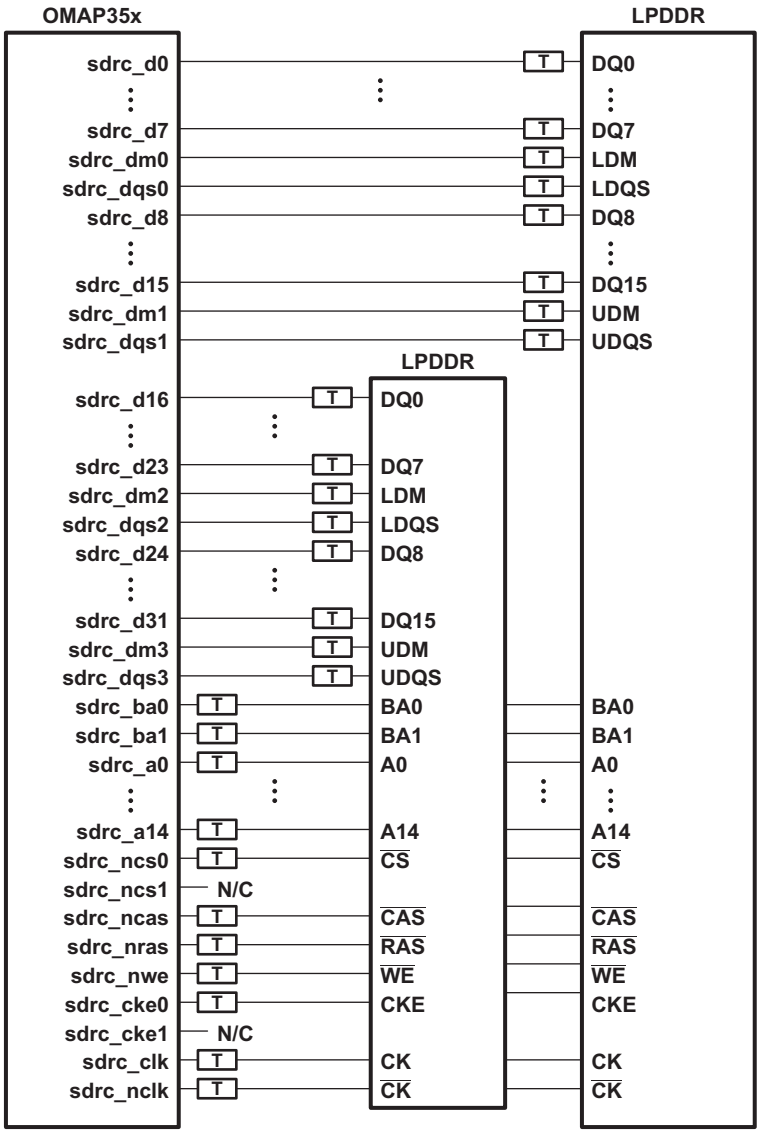

Figure 6-17. OMAP35x LPDDR High Level Schematic (x16 memories)

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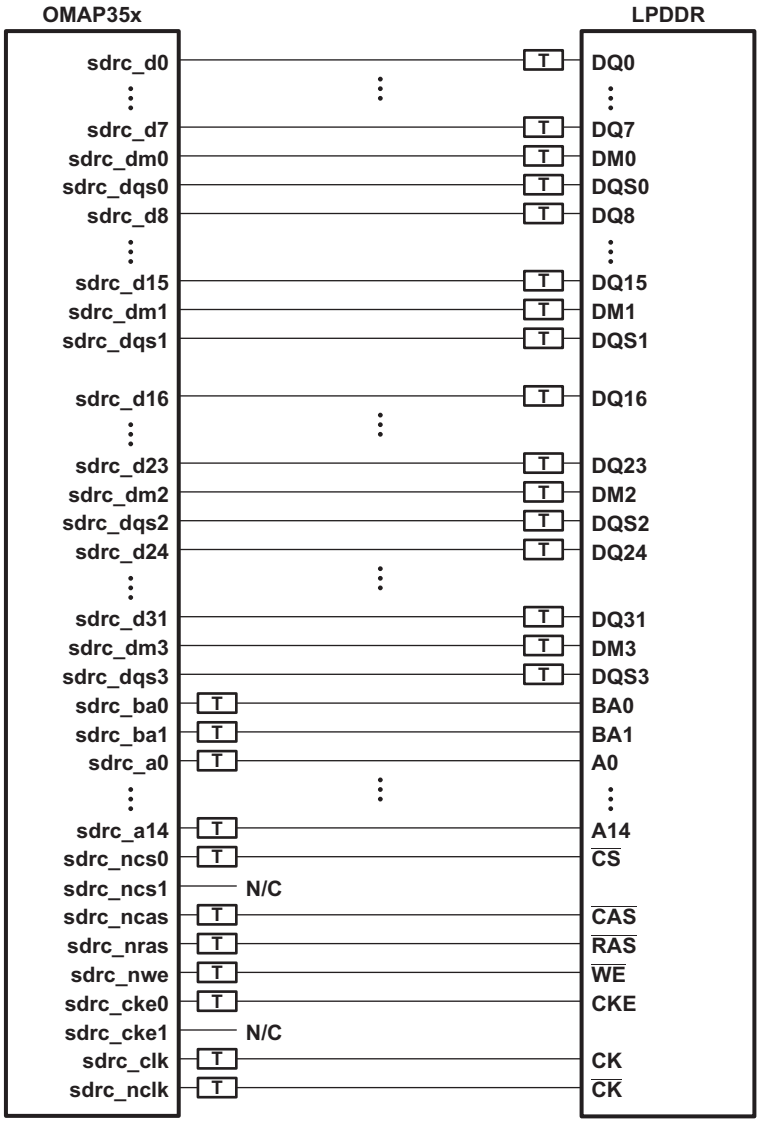

Figure 6-18. OMAP35x LPDDR High Level Schematic (x32 memory)

6.4.2.2.2 Compatible JEDEC LPDDR Devices

Table 6-13 shows the parameters of the JEDEC LPDDR devices that are compatible with this interface. Generally, the LPDDR interface is compatible with x16 and x32 LPDDR266 and LPDDR333 speed grade LPDDR devices.

Table 6-13. Compatible JEDEC LPDDR Devices

NO.	PARAMETER	MIN	MAX	UNIT	NOTES
1	JEDEC LPDDR Device Speed Grade	LPDDR-266			See Note (1)
2	JEDEC LPDDR Device Bit Width	16	32	Bits	
3	JEDEC LPDDR Device Count	1	2	Devices	See Note (2)
4	JEDEC LPDDR Device Ball Count	60	90	Balls	

(1) Higher LPDDR speed grades are supported due to inherent JEDEC LPDDR backwards compatibility.
(2) 1 x16 LPDDR device is used for 16 bit LPDDR memory system. 1x32 or 2x16 LPDDR devices are used for a 32-bit LPDDR memory system.

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6.4.2.2.3 PCB Stackup

The minimum stackup required for routing the OMAP35x is a six layer stack as shown in Table 6-14. Additional layers may be added to the PCB stack up to accommodate other circuity or to reduce the size of the PCB footprint.

Table 6-14. OMAP35x Minimum PCB Stack Up

LAYER	TYPE	DESCRIPTION
1	Signal	Top Routing Mostly Horizontal
2	Plane	Ground
3	Plane	Power
4	Signal	Internal Routing
5	Plane	Ground
6	Signal	Bottom Routing Mostly Vertical

Table 6-15. PCB Stack Up Specifications

NO.	PARAMETER	MIN	TYP	MAX	UNIT	NOTES
1	PCB Routing/Plane Layers	6				
2	Signal Routing Layers	3				
3	Full ground layers under LPDDR routing region	2				
4	Number of ground plane cuts allowed within LPDDR routing region			0		
5	Number of ground reference planes required for each LPDDR routing 1 layer	1				
6	Number of layers between LPDDR routing layer and reference ground 0 plane			0		
7	PCB Routing Feature Size		4		Mils	
8	PCB Trace Width w		4		Mils	
9	PCB BGA escape via pad size		18		Mils	
10	PCB BGA escape via hole size		8		Mils	
11	Device BGA Pad Size					See Note(1)
12	LPDDR Device BGA Pad Size					See Note(2)
13	Single Ended Impedance, ZO	50		75	Ω	
14	Impedance Control	Z-5	Z	Z + 5	Ω	See Note(3)

(1) Please see the *Flip Chip Ball Grid Array Package* Reference Guide (literature number SPRU811) for device BGA pad size.
(2) Please see the LPDDR device manufacturer documentation for the LPDDR device BGA pad size.
(3) Z is the nominal singled ended impedance selected for the PCB specified by item 12.

6.4.2.3 Placement

Figure 6-19 shows the required placement for the OMAP35x device as well as the LPDDR devices. The dimensions for Figure 6-19 are defined in Table 6-16. The placement does not restrict the side of the PCB that the devices are mounted on. The ultimate purpose of the placement is to limit the maximum trace lengths and allow for proper routing space. For 1x16 and 1x32 LPDDR memory systems, the second LPDDR device is omitted from the placement.

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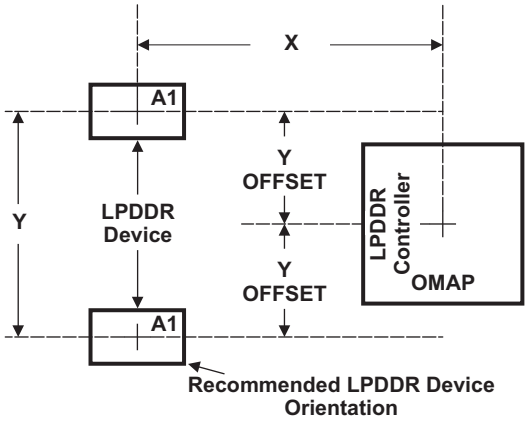


Figure 6-19. OMAP35x and LPDDR Device Placement

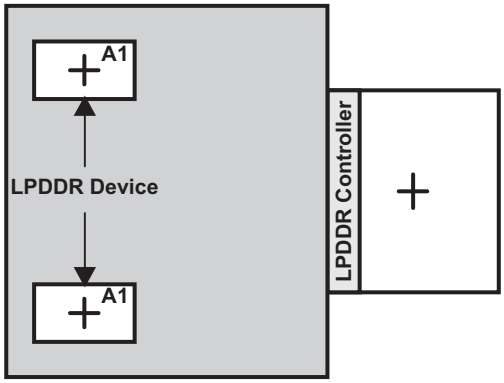
Table 6-16. Placement Specifications

NO.	PARAMETER	MIN	MAX	UNIT	NOTES
1	X		1440	Mils	See Notes(1), (2)
2	Y		1030	Mils	See Notes(1), (2)
3	Y Offset		525	Mils	See Notes(1),(2),(3)
4	LPDDR Keepout Region				See Note(4)
5	Clearance from non-LPDDR signal to LPDDR Keepout Region	4		w	See Note(5)

(1) See Figure 6-17 for dimension definitions.
(2) Measurements from center of device to center of LPDDR device.
(3) For 16 bit memory systems it is recommended that Y Offset be as small as possible.
(4) LPDDR keepout region to encompass entire LPDDR routing area.
(5) Non-LPDDR signals allowed within LPDDR keepout region provided they are separated from LPDDR routing layers by a ground plane.

6.4.2.4 LPDDR Keep Out Region

The region of the PCB used for the LPDDR circuitry must be isolated from other signals. The LPDDR keep out region is defined for this purpose and is shown in Figure 6-20. The size of this region varies with the placement and LPDDR routing. Additional clearances required for the keep out region are shown in Table 6-16.



Region should encompass all LPDDR circuitry and varies depending on placement. Non-LPDDR signals should not be routed on the LPDDR signal layers within the LPDDR keep out region. Non-LPDDR signals may be routed in the region provided they are routed on layers separated from LPDDR signal layers by a ground layer. No breaks should be allowed in the reference ground layers in this region. In addition, the 1.8 V power plane should cover the entire keep out region.

Figure 6-20. LPDDR Keepout Region

6.4.2.5 Net Classes

Table 6-17 lists the clock net classes for the LPDDR interface. Table 6-18 lists the signal net classes, and associated clock net classes, for the signals in the LPDDR interface. These net classes are used for the termination and routing rules that follow.

Table 6-17. Clock Net Class Definitions

CLOCK NET CLASS	OMAP PIN NAMES
CK	sdrc_clk/sdrc_nclk
DQS0	sdrc_dqs0
DQS1	sdrc_dqs1
DQS2	sdrc_dqs2
DQS3	sdrc_dqs3

Table 6-18. Signal Net Class Definitions

CLOCK NET CLASS	ASSOCIATED CLOCK NET CLASS	OMAP PIN NAMES
ADDR_CTRL	CK	sdrc_ba, sdrc_a, sdrc_ncs0, sdrc_ncas, sdrc_nras, sdrc_nwe, sdrc_cke0
DQ0	DQS0	sdrc_d, sdrc_dm0
DQ1	DQS1	sdrc_d, sdrc_dm1
DQ2	DQS2	sdrc_d, sdrc_dm2
DQ3	DQS3	sdrc_d, sdrc_dm3

6.4.2.6 LPDDR Signal Termination

No terminations of any kind are required in order to meet signal integrity and overshoot requirements. Serial terminators are permitted, if desired, to reduce EMI risk; however, serial terminations are the only type permitted. Table 6-19 shows the specifications for the series terminators.

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Table 6-19. LPDDR Signal Terminations

NO.	PARAMETER	MIN	TYP	MAX	UNIT	NOTES
1	CK Net Class	0		10	Ω	See Note (1)
2	ADDR_CTRL Net Class	0	22	Zo	Ω	See Notes (1), (2), (3)
3	Data Byte Net Classes (DQS0-DQS3, DQ0-DQ3)	0	22	Zo	Ω	See Notes (1), (2), (3)

(1) Only series termination is permitted, parallel or SST specifically disallowed.
(2) Terminator values larger than typical only recommended to address EMI issues.
(3) Termination value should be uniform across net class.

6.4.2.7 LPDDR CK and ADDR_CTRL Routing

Figure 6-21 shows the topology of the routing for the CK and ADDR_CTRL net classes. The route is a balanced T as it is intended that the length of segments B and C be equal. In addition, the length of A should be maximized.

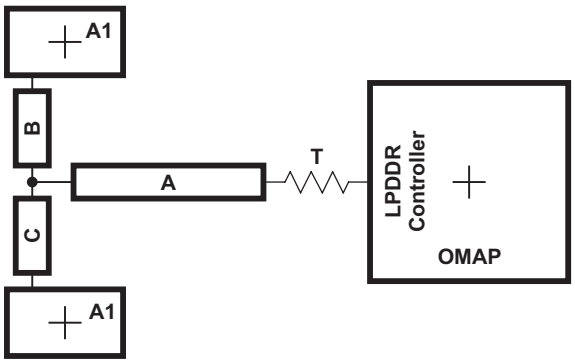

Figure 6-21. CK and ADDR_CTRL Routing and Topology

Table 6-20. CK and ADDR_CTRL Routing Specification

NO.	PARAMETER	MIN	TYP	MAX	UNIT	NOTES
1	Center to Center CK-CK spacing			2w		
2	CK A to B/A to C Skew Length Mismatch			25	Mils	See Note (1)
3	CK B to C Skew Length Mismatch			25	Mils	
4	Center to Center CK to other LPDDR trace spacing	4w				See Note (2)
5	CK/ADDR_CTRL nominal trace length	CACLM-50	CACLM	CACLM+50	Mils	See Note (3)
6	ADDR_CTRL to CK Skew Length Mismatch			100	Mils	
7	ADDR_CTRL to ADDR_CTRL Skew Length Mismatch			100	Mils	
8	Center to Center ADDR_CTRL to other LPDDR trace 4w spacing	4w				See Note (2)
9	Center to Center ADDR_CTRL to other ADDR_CTRL 3w trace spacing	3w				See Note (2)
10	ADDR_CTRL A to B/A to C Skew Length Mismatch			100	Mils	See Note (1)
11	ADDR_CTRL B to C Skew Length Mismatch			100	Mils	

(1) Series terminator, if used, should be located closest to device.
(2) Center to center spacing is allowed to fall to minimum (w) for up to 500 mils of routed length to accommodate BGA escape and routing congestion.
(3) CACLM is the longest Manhattan distance of the CK and ADDR_CTRL net classes.

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Figure 6-22 shows the topology and routing for the DQS and DQ net classes; the routes are point to point. Skew matching across bytes is not needed nor recommended.

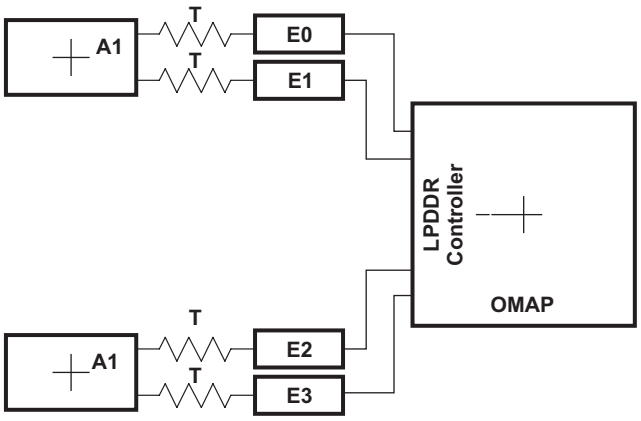

Figure 6-22. DQS and DQ Routing and Topology

Table 6-21. DQS and DQ Routing Specification(1)

NO.	PARAMETER	MIN	TYP	MAX	UNIT	NOTES
2	DQS E Skew Length Mismatch			25	Mils	
3	Center to Center DQS to other LPDDR trace spacing	4w				See Note(2)
4	DQS/DQ nominal trace length	DQLM - 50	DQLM	DQLM + 50	Mils	See Note(3)
5	DQ to DQS Skew Length Mismatch			100	Mils	
6	DQ to DQ Skew Length Mismatch			100	Mils	
7	Center to Center DQ to other LPDDR trace spacing	4w				See Note(2)
8	Center to Center DQ to other DQ trace spacing	3w				See Note(2),(4)
9	DQ E Skew Length Mismatch			100	Mils	

(1) Series terminator, if used, should be located closest to LPDDR.
(2) Center to center spacing is allowed to fall to minimum (w) for up to 500 mils of routed length to accommodate BGA escape and routing congestion.
(3) Center to center spacing is allowed to fall to minimum (w) for up to 500 mils of routed length to accommodate BGA escape and routing congestion.
(4) DQLM is the longest Manhattan distance of the DQS and DQ net classes.

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6.5 Video Interfaces

6.5.1 Camera Interface

The camera subsystem provides the system interfaces and the processing capability to connect supported YCbCr Interfaces to the OMAP3530/25 device. The camera subsystem supports up to two simultaneous pixel flows but only one of them can use supported video processing hardware:

- PARALLEL: the parallel interface data must go through the video processing hardware.

6.5.1.1 Parallel Camera Interface Timing

The parallel camera interface is a 12-bit interface which can be used in two modes:

1. SYNC mode: progressive and interlaced image sensor modules for 8-, 10-, 11-, and 12-bit data. The pixel clock can be up to 75 MHz in 12-bit mode. The pixel clock can be up to 130 MHz in 8-bit packed mode.
2. ITU mode provides an ITU-R BT 656 compatible data stream with progressive image sensor modules only in 8- and 10-bit configurations. The pixel clock can be up to 75 MHz.

6.5.1.1.1 SYNC Normal Mode

6.5.1.1.1.1 12-Bit SYNC Normal – Progressive Mode

Table 6-23 and Table 6-24 assume testing over the recommended operating conditions and electrical chaDSI Timing Conditionsracteristic conditions (see Figure 6-23).

Table 6-22. ISP Timing Conditions – 12-Bit SYNC Normal – Progressive Mode

TIMING CONDITION PARAMETER		VALUE	UNIT
Input Conditions			
t_R	Input signal rise time	2.7	ns
t_F	Input signal fall time	2.7	ns
Output Condition			
C_{LOAD}	Output load capacitance	8.6	pF

Table 6-23. ISP Timing Requirements – 12-Bit SYNC Normal – Progressive Mode(1)

NO.	PARAMETER		1.15 V		1.0 V		UNIT
			MIN	MAX	MIN	MAX	
ISP17	$t_{c(pclk)}$	Cycle time(2), cam_pclk period	13.3		22.2		ns
ISP18	$t_{W(pclkH)}$	Typical pulse duration, cam_pclk high	0.5*P(3)		0.5*P(3)		ns
ISP18	$t_{W(pclkL)}$	Typical pulse duration, cam_pclk low	0.5*P(3)		0.5*P(3)		ns
	$t_{dc(pclk)}$	Duty cycle error, cam_pclk		667		1111	ps
	$t_{j(pclk)}$	Cycle jitter(4), cam_pclk		133		200	ps
ISP19	$t_{su(dV-pclkH)}$	Setup time, cam_d[11:0] valid before cam_pclk rising edge	1.82		3.25		ns
ISP20	$t_{h(pclkH-dV)}$	Hold time, cam_d[11:0] valid after cam_pclk rising edge	1.82		3.25		ns
ISP21	$t_{su(dV-vsH)}$	Setup time, cam_vs valid before cam_pclk rising edge	1.82		3.25		ns
ISP22	$t_{h(pclkH-vsV)}$	Hold time, cam_vs valid after cam_pclk rising edge	1.82		3.25		ns
ISP23	$t_{su(dV-hsH)}$	Setup time, cam_hs valid before cam_pclk rising edge	1.82		3.25		ns

(1) The timing requirements are assured for the cycle jitter and duty cycle error conditions specified.
(2) Related with the input maximum frequency supported by the ISP module.
(3) P = cam_pclk period in ns
(4) Maximum cycle jitter supported by cam_pclk input clock.

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Table 6-23. ISP Timing Requirements – 12-Bit SYNC Normal – Progressive Mode[1] (continued)

NO.	PARAMETER		1.15 V		1.0 V		UNIT
			MIN	MAX	MIN	MAX	
ISP24	$t_{h(pclkH-hsV)}$	Hold time, cam_hs valid after cam_pclk rising edge	1.82		3.25		ns
ISP25	$t_{su(dV-hsH)}$	Setup time, cam_wen valid before cam_pclk rising edge	1.82		3.25		ns
ISP26	$t_{h(pclkH-hsV)}$	Hold time, cam_wen valid after cam_pclk rising edge	1.82		3.25		ns

Table 6-24. ISP Switching Characteristics – 12-Bit SYNC Normal – Progressive Mode

NO.	PARAMETER		1.15 V		1.0 V		UNIT
			MIN	MAX	MIN	MAX	
ISP15	$t_{c(xclk)}$	Cycle time[1], cam_xclk period	4.6		4.6		ns
ISP16	$t_{W(xclkH)}$	Typical pulse duration, cam_xclk high	0.5*PO[2]		0.5*PO[2]		ns
ISP16	$t_{W(xclkL)}$	Typical pulse duration, cam_xclk low	0.5*PO[2]		0.5*PO[2]		ns
	$t_{dc(xclk)}$	Duty cycle error, cam_xclk		231		231	ps
	$t_{j(xclk)}$	Jitter standard deviation[3], cam_xclk		33		33	ps
	$t_{R(xclk)}$	Rise time, cam_xclk		0.93		0.93	ns
	$t_{F(xclk)}$	Fall time, cam_xclk		0.93		0.93	ns

(1) Related with the cam_xclk maximum and minimum frequencies programmable in the ISP module.
Warning: The camera sensor or the camera module must be disabled to change the frequency configuration. For more information, see the *OMAP35x Technical Reference Manual (TRM)* [literature number SPRUF98]
(2) PO = cam_xclk period in ns
(3) The jitter probability density can be approximated by a Gaussian function.

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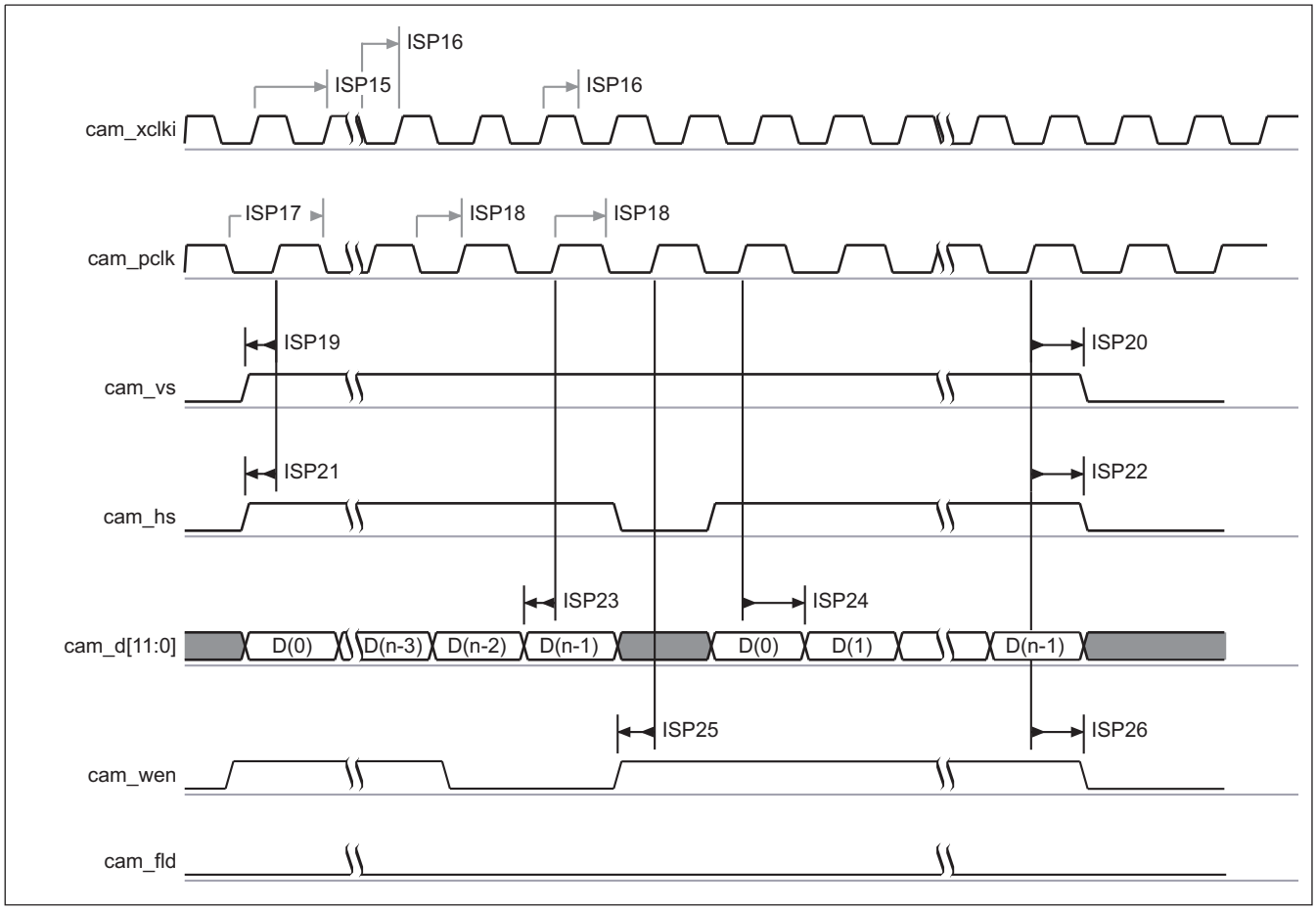

Figure 6-23. ISP – 12-Bit SYNC Normal – Progressive Mode(1) (2) (3) (4) (5) (6) (7) (8)

(1) The polarity of cam_pclk, cam_fld, cam_vs, and cam_hs are configurable. If the cam_hs, cam_vs, and cam_fld signals are output, the signal length can be set.

(2) The parallel camera in SYNC mode supports progressive image sensor modules and 8-, 10-, 11-, or 12-bit data.

(3) When the image sensor has fewer than 12 data lines, it must be connected to the lower data lines and the unused lines must be grounded.

(4) However, it is possible to shift the data to 0, 2, or 4 data internal lanes.

(5) The bit configurations are: cam_d[11:4] or cam_d[7:0] in 8-bit mode, cam_d[11:2] or cam_d[9:0] in 10-bit mode, cam_d[10:0] in 11-bit mode, and cam_d[11:0] in 12-bit mode.

(6) Optionally, the data write to memory can be qualified by the external cam_wen signal.

(7) The cam_wen signal can be used as a external memory write-enable signal. The data is stored to memory only if cam_hs, cam_vs, and cam_wen signals are asserted.

(8) In cam_xclki; I is equal to a or b.

6.5.1.1.1.2 8-bit Packed SYNC – Progressive Mode

Table 6-26 and Table 6-27 assume testing over the recommended operating conditions and electrical characteristic conditions (see Figure 6-24).

Table 6-25. ISP Timing Conditions – 8-bit Packed SYNC – Progressive Mode

TIMING CONDITION PARAMETER		VALUE	UNIT
Input Conditions			
t_R	Input signal rise time	2.5	ns
t_F	Input signal fall time	2.5	ns

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Table 6-25. ISP Timing Conditions – 8-bit Packed SYNC – Progressive Mode (continued)

TIMING CONDITION PARAMETER		VALUE	UNIT
Output Conditions			
C_{LOAD}	Output load capacitance	8.6	pF

Table 6-26. ISP Timing Requirements – 8-bit Packed SYNC – Progressive Mode(1)

NO.	PARAMETER		1.15 V		1.0 V		UNIT
			MIN	MAX	MIN	MAX	
ISP3	$t_{c(pclk)}$	Cycle time(2), cam_pclk period	7.7		15.4		ns
ISP4	$t_{W(pclkH)}$	Typical pulse duration, cam_pclk high	0.5*P(3)		0.5*P(3)		ns
ISP4	$t_{W(pclkL)}$	Typical pulse duration, cam_pclk low	0.5*P(3)		0.5*P(3)		ns
	$t_{dc(pclk)}$	Duty cycle error, cam_pclk		385		769	ps
	$t_{j(pclk)}$	Cycle jitter(4), cam_pclk		83		167	ps
ISP5	$t_{su(dV-pclkH)}$	Setup time, cam_d[11:0] valid before cam_pclk rising edge	1.08		2.27		ns
ISP6	$t_{h(pclkH-dV)}$	Hold time, cam_d[11:0] valid after cam_pclk rising edge	1.08		2.27		ns
ISP7	$t_{su(dV-vsH)}$	Setup time, cam_vs valid before cam_pclk rising edge	1.08		2.27		ns
ISP8	$t_{h(pclkH-vsV)}$	Hold time, cam_vs valid after cam_pclk rising edge	1.08		2.27		ns
ISP9	$t_{su(dV-hsH)}$	Setup time, cam_hs valid before cam_pclk rising edge	1.08		2.27		ns
ISP10	$t_{h(pclkH-hsV)}$	Hold time, cam_hs valid after cam_pclk rising edge	1.08		2.27		ns
ISP11	$t_{su(dV-hsH)}$	Setup time, cam_wen valid before cam_pclk rising edge	1.08		2.27		ns
ISP12	$t_{h(pclkH-hsV)}$	Hold time, cam_wen valid after cam_pclk rising edge	1.08		2.27		ns

(1) The timing requirements are assured for the cycle jitter and duty cycle error conditions specified.
(2) Related with the input maximum frequency supported by the ISP module.
(3) P = cam_pclk period in ns.
(4) Maximum cycle jitter supported by cam_pclk input clock.

Table 6-27. ISP Switching Characteristics – 8-bit packed SYNC – Progressive Mode

NO.	PARAMETER		1.15 V		1.0 V		UNIT
			MIN	MAX	MIN	MAX	
ISP1	$t_{c(xclk)}$	Cycle time(1), cam_xclk period	4.6		4.6		ns
ISP2	$t_{W(xclkH)}$	Typical pulse duration, cam_xclk high	0.5*PO(2)		0.5*PO(2)		ns
ISP2	$t_{W(xclkL)}$	Typical pulse duration, cam_xclk low	0.5*PO(2)		0.5*PO(2)		ns
	$t_{dc(xclk)}$	Duty cycle error, cam_xclk		231		231	ps
	$t_{j(xclk)}$	Jitter standard deviation(3), cam_xclk		67		67	ps
	$t_{R(xclk)}$	Rise time, cam_xclk		0.93		0.93	ns
	$t_{F(xclk)}$	Fall time, cam_xclk		0.93		0.93	ns

(1) Related with the cam_xclk maximum and minimum frequencies programmable in the ISP module.
Warning: You must disable the camera sensor or the camera module to change the frequency configuration. For more information, see the *OMAP35x Technical Reference Manual (TRM)* [literature number SPRUF98]
(2) PO = cam_xclk period in ns
(3) The jitter probability density can be approximated by a Gaussian function.

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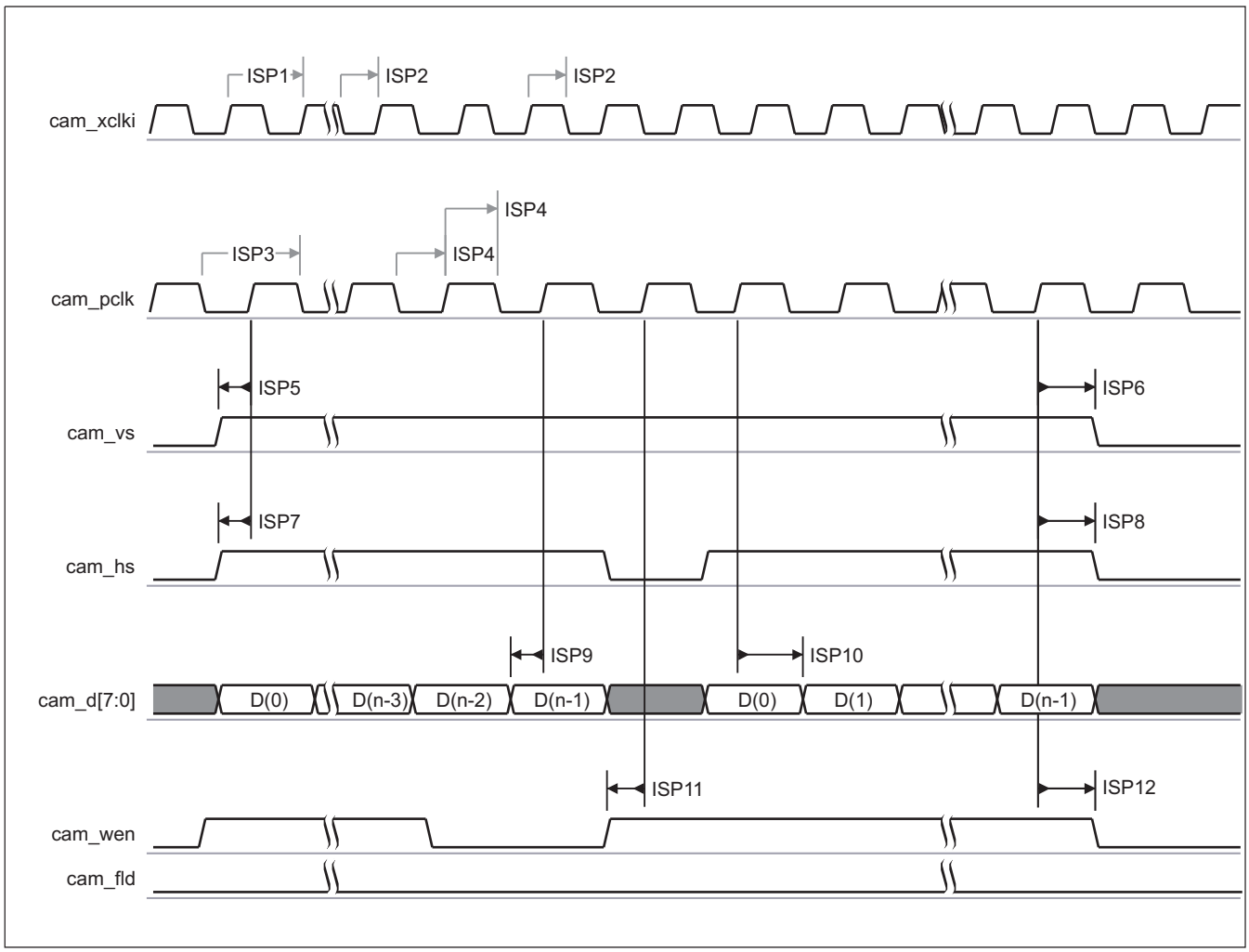

Figure 6-24. ISP – 8-bit Packed SYNC – Progressive Mode(1) (2) (3) (4) (5)

(1) The polarity of cam_pclk, cam_fld, cam_vs, and cam_hs are configurable.

(2) The image sensor must be connected to the lower data lines and the unused lines must be grounded. However, it is possible to shift the data to 0, 2, or 4 data internal lanes. The bit configurations are: cam_d[11:4] or cam_d[7:0] in 8-bit packed mode.

(3) Optionally, the data write to memory can be qualified by the external cam_wen signal. The cam_wen signal can be used as a external memory write-enable signal. The data is stored to memory only if cam_hs, cam_vs, and cam_wen signals are asserted. The polarity of cam_fld is programmable.

(4) The camera module can pack 8-bit data into 16 bits. It doubles the maximum pixel clock. This mode can be particularly useful to transfer a YCbCr data stream or compressed stream to memory at very high speed.

(5) In cam_xclki; I is equal to a or b.

6.5.1.1.1.3 12-Bit SYNC Normal – Interlaced Mode

Table 6-29 and Table 6-30 assume testing over the recommended operating conditions and electrical characteristic conditions (see Figure 6-25).

Table 6-28. ISP Timing Conditions – 12-Bit SYNC Normal – Interlaced Mode

TIMING CONDITION PARAMETER		VALUE	UNIT
Input Conditions			
t_R	Input signal rise time	2.7	ns
t_F	Input signal fall time	2.7	ns

Table 6-28. ISP Timing Conditions – 12-Bit SYNC Normal – Interlaced Mode (continued)

TIMING CONDITION PARAMETER		VALUE	UNIT
Output Conditions			
C_{LOAD}	Output load capacitance	8.6	pF

Table 6-29. ISP Timing Requirements – 12-Bit SYNC Normal – Interlaced Mode(1)

NO.	PARAMETER		1.15 V		1.0 V		UNIT
			MIN	MAX	MIN	MAX	
ISP17	$t_{c(pclk)}$	Cycle time(2), cam_pclk period	13.3		22.2		ns
ISP18	$t_{W(pclkH)}$	Typical pulse duration, cam_pclk high	0.5*P(3)		0.5*P(3)		ns
ISP18	$t_{W(pclkL)}$	Typical pulse duration, cam_pclk low	0.5*P(3)		0.5*P(3)		ns
	$t_{dc(pclk)}$	Duty cycle error, cam_pclk		667		1111	ps
	$t_{j(pclk)}$	Cycle jitter(4), cam_pclk		133		200	ps
ISP19	$t_{su(dV-pclkH)}$	Setup time, cam_d[11:0] valid before cam_pclk rising edge	1.82		3.25		ns
ISP20	$t_{h(pclkH-dV)}$	Hold time, cam_d[11:0] valid after cam_pclk rising edge	1.82		3.25		ns
ISP21	$t_{su(dV-vsH)}$	Setup time, cam_vs valid before cam_pclk rising edge	1.82		3.25		ns
ISP22	$t_{h(pclkH-vsV)}$	Hold time, cam_vs valid after cam_pclk rising edge	1.82		3.25		ns
ISP23	$t_{su(dV-hsH)}$	Setup time, cam_hs valid before cam_pclk rising edge	1.82		3.25		ns
ISP24	$t_{h(pclkH-hsV)}$	Hold time, cam_hs valid after cam_pclk rising edge	1.82		3.25		ns
ISP25	$t_{su(dV-hsH)}$	Setup time, cam_wen valid before cam_pclk rising edge	1.82		3.25		ns
ISP26	$t_{h(pclkH-hsV)}$	Hold time, cam_wen valid after cam_pclk rising edge	1.82		3.25		ns
ISP27	$t_{su(dV-fldH)}$	Setup time, cam_fld valid before cam_pclk rising edge	1.82		3.25		ns
ISP28	$t_{h(pclkH-fldV)}$	Hold time, cam_fld valid after cam_pclk rising edge	1.82		3.25		ns

(1) The timing requirements are assured for the cycle jitter and duty cycle error conditions specified.
(2) Related with the input maximum frequency supported by the ISP module.
(3) P = cam_lclk period in ns.
(4) Maximum cycle jitter supported by cam_pclk input clock.

Table 6-30. ISP Switching Characteristics – 12-Bit SYNC Normal – Interlaced Mode

NO.	PARAMETER		1.15 V		1.0 V		UNIT
			MIN	MAX	MIN	MAX	
ISP15	$t_{c(xclk)}$	Cycle time(1), cam_xclk period	4.6		4.6		ns
ISP16	$t_{W(xclkH)}$	Typical pulse duration, cam_xclk high	0.5*PO(2)		0.5*PO(2)		ns
ISP16	$t_{W(xclkL)}$	Typical pulse duration, cam_xclk low	0.5*PO(2)		0.5*PO(2)		ns
	$t_{dc(xclk)}$	Duty cycle error, cam_xclk		231		231	ps
	$t_{j(xclk)}$	Jitter standard deviation(3), cam_xclk		33		33	ps
	$t_{R(xclk)}$	Rise time, cam_xclk		0.93		0.93	ns
	$t_{F(xclk)}$	Fall time, cam_xclk		0.93		0.93	ns

(1) Related with the cam_xclk maximum and minimum frequencies programmable in the ISP module.
Warning: You must disable the camera sensor or the camera module to change the frequency configuration. For more information, see the *OMAP35x Technical Reference Manual (TRM)* [literature number SPRUF98]
(2) PO = cam_xclk period in ns.
(3) The jitter probability density can be approximated by a Gaussian function.

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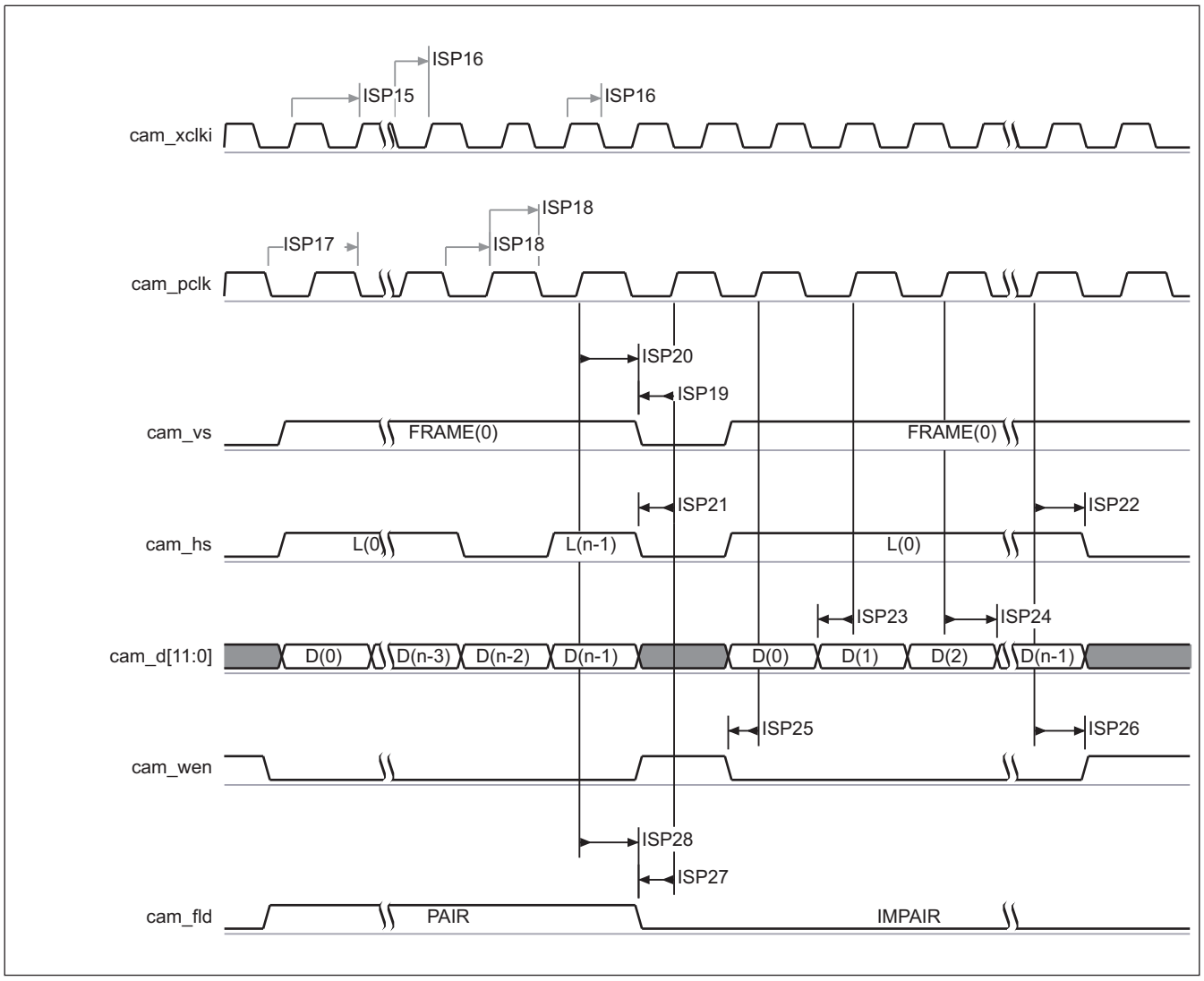

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Figure 6-25. ISP – 12-Bit SYNC Normal – Interlaced Mode(1) (2) (3) (4) (5) (6) (7) (8)

(1) The polarity of cam_pclk, cam_fld, cam_vs, and cam_hs are configurable. If the cam_hs, cam_vs, and cam_fld signals are output, the signal length can be set.

(2) The parallel camera in SYNC mode supports interlaced image sensor modules and 8-, 10-, 11-, or 12-bit data.

(3) When the image sensor has fewer than 12 data lines, it must be connected to the lower data lines and the unused lines must be grounded.

(4) It is possible to shift the data to 0, 2, or 4 data internal lanes.

(5) The bit configurations are: cam_d[11:4] or cam_d[7:0] in 8-bit mode, cam_d[11:2] or cam_d[9:0] in 10-bit mode, cam_d[10:0] in 11-bit mode, and cam_d[11:0] in 12-bit mode.

(6) Optionally, the data write to memory can be qualified by the external cam_wen signal.

(7) The cam_wen signal can be used as a external memory write-enable signal. The data is stored to memory only if cam_hs, cam_vs, and cam_wen signals are asserted.

(8) In cam_xclki; I is equal to a or b.

6.5.1.1.1.4 8-bit Packed SYNC – Interlaced Mode

Table 6-32 and Table 6-33 assume testing over the recommended operating conditions and electrical characteristic conditions (see Figure 6-26).

Table 6-31. ISP Timing Conditions – 8-bit Packed SYNC – Interlaced Mode

TIMING CONDITION PARAMETER		VALUE	UNIT
Input Conditions			
t_R	Input signal rise time	2.5	ns
t_F	Input signal fall time	2.5	ns
Output Conditions			
C_{LOAD}	Output load capacitance	8.6	pF

Table 6-32. ISP Timing Requirements – 8-bit Packed SYNC – Interlaced Mode(1)

NO.	PARAMETER		1.15 V		1.0 V		UNIT
			MIN	MAX	MIN	MAX	
ISP3	$t_{c(pclk)}$	Cycle time(2), cam_pclk period	7.7		15.4		ns
ISP4	$t_{W(pclkH)}$	Typical pulse duration, cam_pclk high	0.5*P(3)		0.5*P(3)		ns
ISP4	$t_{W(pclkL)}$	Typical pulse duration, cam_pclk low	0.5*P(3)		0.5*P(3)		ns
	$t_{dc(pclk)}$	Duty cycle error, cam_pclk		385		769	ps
	$t_{j(pclk)}$	Cycle jitter(4), cam_pclk		83		167	ps
ISP5	$t_{su(dV-pclkH)}$	Setup time, cam_d[11:0] valid before cam_pclk rising edge	1.08		2.27		ns
ISP6	$t_{h(pclkH-dV)}$	Hold time, cam_d[11:0] valid after cam_pclk rising edge	1.08		2.27		ns
ISP7	$t_{su(dV-vsH)}$	Setup time, cam_vs valid before cam_pclk rising edge	1.08		2.27		ns
ISP8	$t_{h(pclkH-vsV)}$	Hold time, cam_vs valid after cam_pclk rising edge	1.08		2.27		ns
ISP9	$t_{su(dV-hsH)}$	Setup time, cam_hs valid before cam_pclk rising edge	1.08		2.27		ns
ISP10	$t_{h(pclkH-hsV)}$	Hold time, cam_hs valid after cam_pclk rising edge	1.08		2.27		ns
ISP11	$t_{su(dV-hsH)}$	Setup time, cam_wen valid before cam_pclk rising edge	1.08		2.27		ns
ISP12	$t_{h(pclkH-hsV)}$	Hold time, cam_wen valid after cam_pclk rising edge	1.08		2.27		ns
ISP13	$t_{su(dV-fldH)}$	Setup time, cam_fld valid before cam_pclk rising edge	1.08		2.27		ns
ISP14	$t_{h(pclkH-fldV)}$	Hold time, cam_fld valid after cam_pclk rising edge	1.08		2.27		ns

(1) The timing requirements are assured for the cycle jitter and duty cycle error conditions specified.
(2) Related with the input maximum frequency supported by the ISP module.
(3) P = cam_lclk period in ns.
(4) Maximum cycle jitter supported by cam_pclk input clock.

Table 6-33. ISP Switching Characteristics – 8-bit Packed SYNC – Interlaced Mode

NO.	PARAMETER		1.15 V		1.0 V		UNIT
			MIN	MAX	MIN	MAX	
ISP16	$t_{c(xclk)}$	Cycle time(1), cam_xclk period	4.6		4.6		ns
ISP2	$t_{W(xclkH)}$	Typical pulse duration, cam_xclk high	0.5*PO(2)		0.5*PO(2)		ns
ISP2	$t_{W(xclkL)}$	Typical pulse duration, cam_xclk low	0.5*PO(2)		0.5*PO(2)		ns
	$t_{dc(xclk)}$	Duty cycle error, cam_xclk		231		231	ps
	$t_{j(xclk)}$	Jitter standard deviation(3), cam_xclk		67		67	ps
	$t_{R(xclk)}$	Rise time, cam_xclk		0.93		0.93	ns
	$t_{F(xclk)}$	Fall time, cam_xclk		0.93		0.93	ns

(1) Related with the cam_xclk maximum and minimum frequencies programmable in the ISP module.
Warning: You must disable the camera sensor or the camera module to change the frequency configuration. For more information, see the *OMAP35x Technical Reference Manual (TRM)* [literature number SPRUF98]
(2) PO = cam_xclk period in ns.
(3) The jitter probability density can be approximated by a Gaussian function.

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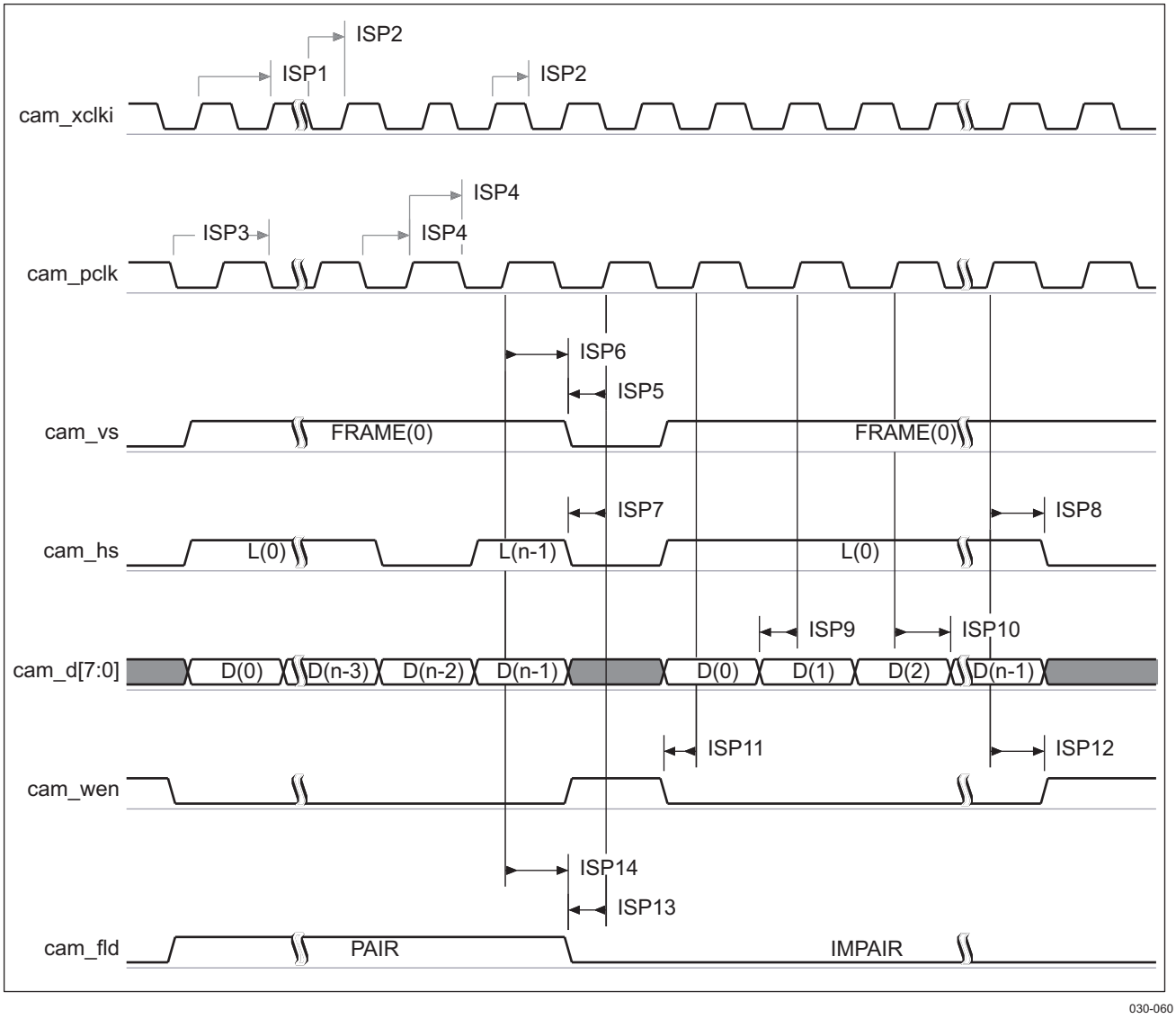

Figure 6-26. ISP – 8-bit Packed SYNC – Interlaced Mode(1) (2) (3) (4) (10)

(1) The polarity of cam_pclk, cam_fld, cam_vs, and cam_hs are configurable.

(2) The image sensor must be connected to the lower data lines and the unused lines must be grounded. However, it is possible to shift the data to 0, 2, or 4 data internal lanes. The bit configurations are: cam_d[11:4] or cam_d[7:0] in 8-bit packed mode.

(3) Optionally, the data write to memory can be qualified by the external cam_wen signal. The cam_wen signal can be used as a external memory write-enable signal. The data is stored to memory only if cam_hs, cam_vs, and cam_wen signals are asserted.

(4) The camera module can pack 8-bit data into 16 bits. It doubles the maximum pixel clock. This mode can be particularly useful to transfer a YCbCr data stream or compressed stream to memory at very high speed.

(5) In cam_xclki; I is equal to a or b.

6.5.1.1.2 ITU Mode

Table 6-35 and Table 6-36 assume testing over the recommended operating conditions and electrical characteristic conditions (see Figure 6-27).

Table 6-34. ISP Timing Conditions – ITU Mode

TIMING CONDITION PARAMETER		VALUE	UNIT
Input Conditions			
t_R	Input signal rise time	2.7	ns

Table 6-34. ISP Timing Conditions – ITU Mode (continued)

TIMING CONDITION PARAMETER		VALUE	UNIT
t_F	Input signal fall time	2.7	ns
Output Conditions			
C_{LOAD}	Output load capacitance	8.6	pF

Table 6-35. ISP Timing Requirements – ITU Mode(1)

NO.	PARAMETER		1.15 V		1.0 V		UNIT
			MIN	MAX	MIN	MAX	
ISP17	$t_{c(pclk)}$	Cycle time(2), cam_pclk period	13.3		22.2		ns
ISP18	$t_{W(pclkH)}$	Typical pulse duration, cam_pclk high	0.5*P(3)		0.5*P(3)		ns
ISP18	$t_{W(pclkL)}$	Typical pulse duration, cam_pclk low	0.5*P(3)		0.5*P(3)		ns
	$t_{dc(pclk)}$	Duty cycle error, cam_pclk		667		1111	ps
	$t_{j(pclk)}$	Cycle jitter(4), cam_pclk		133		200	ps
ISP23	$t_{su(dV-pclkH)}$	Setup time, cam_d[9:0] valid before cam_pclk rising edge	1.82		3.25		ns
ISP24	$t_{h(pclkH-dV)}$	Hold time, cam_d[9:0] valid after cam_pclk rising edge	1.82		3.25		ns

(1) The timing requirements are assured for the cycle jitter and duty cycle error conditions specified.
(2) Related with the input maximum frequency supported by the ISP module.
(3) P = cam_lclk period in ns.
(4) Maximum cycle jitter supported by cam_lclk input clock.

Table 6-36. ISP Switching Characteristics – ITU Mode

NO.	PARAMETER		1.15 V		1.0 V		UNIT
			MIN	MAX	MIN	MAX	
ISP15	$t_{c(xclk)}$	Cycle time(1), cam_xclk period	4.6		4.6		ns
ISP16	$t_{W(xclkH)}$	Typical pulse duration, cam_xclk high	0.5*PO(2)		0.5*PO(2)		ns
ISP16	$t_{W(xclkL)}$	Typical pulse duration, cam_xclk low	0.5*PO(2)		0.5*PO(2)		ns
	$t_{dc(xclk)}$	Duty cycle error, cam_xclk		231		231	ps
	$t_{j(xclk)}$	Jitter standard deviation(3), cam_xclk		33		33	ps
	$t_{R(xclk)}$	Rise time, cam_xclk		0.93		0.93	ns
	$t_{F(xclk)}$	Fall time, cam_xclk		0.93		0.93	ns

(1) Related with the cam_xclk maximum and minimum frequencies programmable in the ISP module.
Warning: The camera sensor or the camera module must be disabled to change the frequency configuration. For more information, see the *OMAP35x Technical Reference Manual (TRM)* [literature number SPRUF98]
(2) PO = cam_xclk period in ns
(3) The jitter probability density can be approximated by a Gaussian function.

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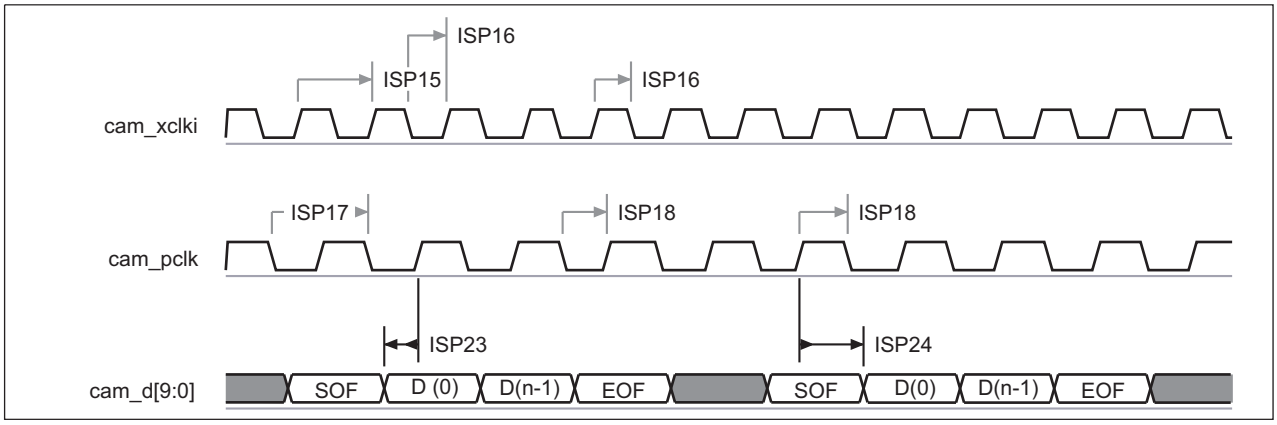

Figure 6-27. ISP – ITU Mode(1) (2)

(1) The unused lines must be grounded and the data bus must be connected to the lower data lines. It is possible to shift the data to 0, 2, or 4 data internal lanes. The different configurations are: cam_d[11:4] or cam_d[7:0] in 8-bit mode and cam_d[11:2] or cam_d[9:0] in 10-bit mode.

(2) The parallel camera in ITU mode supports progressive camera modules.

6.5.2 Display Subsystem (DSS)

The display subsystem (DSS) provides the logic to display the video frame from external (SDRAM) or internal (SRAM) memory on an LCD panel or a TV set. The DSS integrates a display controller, a remote frame buffer module (RFBI), and a TV-out module. It can be used in two configurations:

- LCD display in:
  - Bypass mode (RFBI module bypassed)
  - RFBI mode (through RFBI module)
- TV display (not discussed in this document because of its analog IO signals)

The two displays can be active at the same time.

NOTE

For more information, see Display Subsystem / Display Subsystem Functional Description section of the *OMAP35x Technical Reference Manual (TRM)* [literature number SPRUF98].

6.5.2.1 LCD Display in Bypass Mode

Two types of LCD panel are supported:

- Thin film transistor (TFT) or active matrix technology
- Supertwisted nematic (STN) or passive matrix technology

Both configurations are discussed in the following paragraphs.

6.5.2.1.1 LCD Display in TFT Mode

6.5.2.1.1.1 LCD Display in TFT Mode – HDTV Application

Table 6-37 assumes testing over the recommended operating conditions (see Figure 6-28).

Table 6-37. LCD Display Switching Characteristics in TFT Mode – HDTV Application(3) (4)

NO.	PARAMETER		OPP3		OPP2		UNIT
			MIN	MAX	MIN	MAX	
DL0	$t_{d(PCLKA-HSYNCT)}$	Delay time, dss_pclk active edge to dss_hsync transition	–4.2	4.2	–4.7	4.7	ns
DL1	$t_{d(PCLKA-VSYNCT)}$	Delay time, dss_pclk active edge to dss_vsync transition	–4.2	4.2	–4.7	4.7	ns
DL2	$t_{d(PCLKA-ACBIASA)}$	Delay time, dss_pclk active edge to dss_acbias active level	–4.2	4.2	–4.7	4.7	ns
DL3	$t_{d(PCLKA-DATAV)}$	Delay time, dss_pclk active edge to dss_data bus valid	–4.2	4.2	–4.7	4.7	ns
DL4	$t_{c(PCLK)}$	Cycle time(2), dss_pclk	13.468		15.152		ns
DL5	$t_{w(PCLK)}$	Pulse duration, dss_pclk low or high	0.45*P(1)	0.55*P(1)	0.45*P(1)	0.55*P(1)	ns

(1) P = dss_pclk period.

(2) The pixel clock frequency is software programmable via the pixel clock divider configuration from 1 to 255 division range in the DISPC_DIVISOR register.

(3) The capacitive load is equivalent to 25 pF at 1.15 V and 30 pF at 1.0 V.

(4) For more information, see the DSS chapter in the *OMAP35x Technical Reference Manual (TRM)* [literature number SPRUF98].

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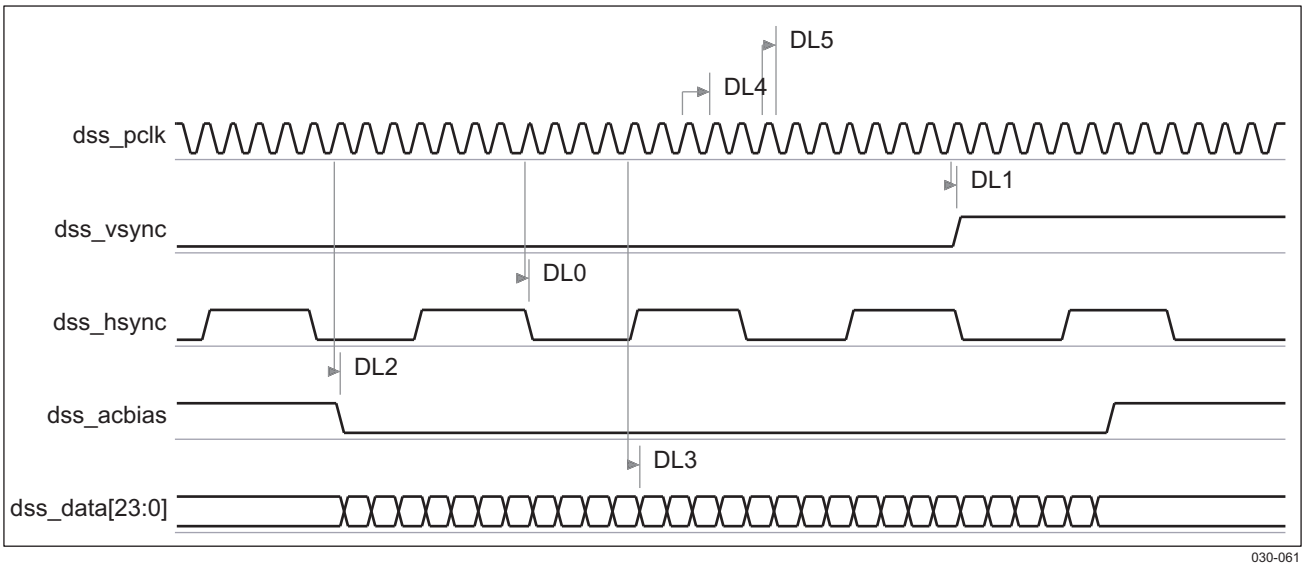

Figure 6-28. LCD Display in TFT Mode – HDTV Application(1) (2) (3) (4)

(1) The pixel data bus depends on the use of 8-, 9-, 12-, 16-, 18-, or 24-bit per pixel data output pins.

(2) The pixel clock frequency is programmable.

(3) All timings not illustrated in the waveform are programmable by software, control signal polarity, and driven edge of dss_pclk.

(4) For more information, see the DSS chapter in the *OMAP35x Technical Reference Manual (TRM)* [literature number SPRUF98].

6.5.2.1.2 LCD Display in STN Mode

Table 6-38 assumes testing over the recommended operating conditions (see Figure 6-29).

Table 6-38. LCD Display Switching Characteristics in STN Mode(3) (4) (5)

NO.	PARAMETER		OPP3		OPP2		UNIT
			MIN	MAX	MIN	MAX	
DL3	$t_{d(PCLKA-DATAV)}$	Delay time, dss_pclk active edge to dss_data bus valid	–6.9	6.9	–6.9	6.9	ns
DL4	$t_{c(PCLK)}$	Cycle time(2), dss_pclk	22.727		22.727		ns
DL5	$t_{w(PCLK)}$	Pulse duration, dss_pclk low or high	0.45*P(1)	0.55*P(1)	0.45*P(1)	0.55*P(1)	ns

(1) P = dss_pclk period.

(2) The pixel clock frequency is software programmable via the pixel clock divider configuration from 1 to 255 division range in the DISPC_DIVISOR register.

(3) The DSS in STN mode is used with 4 or 8 pins only; unused pixel data bits always remain low.

(4) The capacitive load is equivalent to 40 pF.

(5) For more information, see the DSS chapter in the *OMAP35x Technical Reference Manual (TRM)* [literature number SPRUF98].

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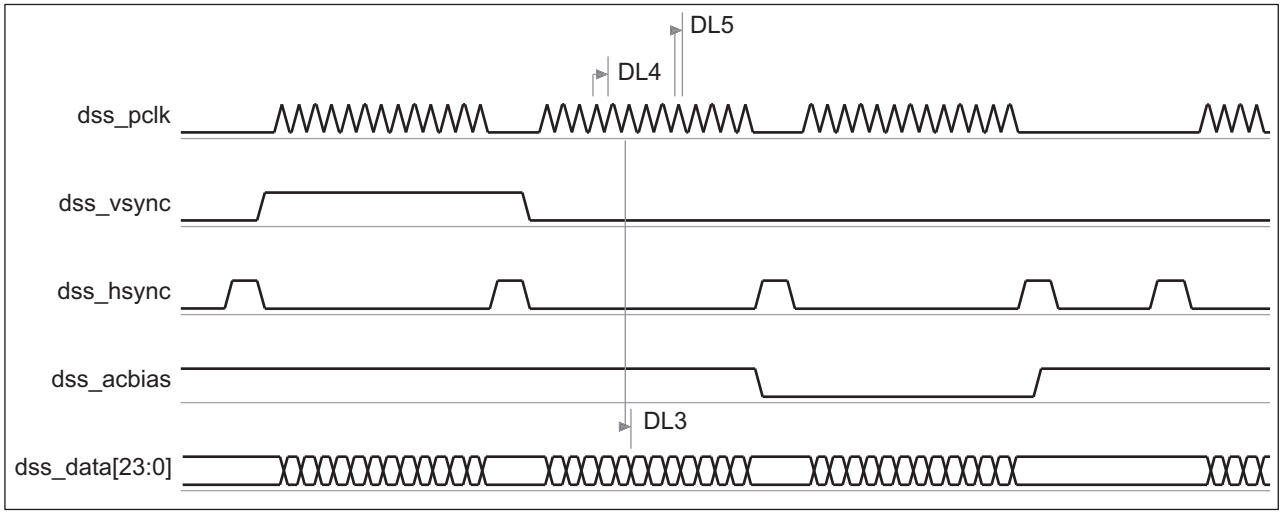

Figure 6-29. LCD Display in STN Mode(1) (2) (3) (4) (5)

(1) The pixel data bus depends on the use 4-, 8-, 12-, 16-, 18-, or 24-bit per pixel data output pins.

(2) All timings not illustrated in the waveform are programmable by software, control signal polarity, and driven edge of dss_pclk.

(3) dss_vsync width must be programmed to be as small as possible.

(4) The pixel clock frequency is programmable.

(5) For more information, see the DSS chapter in the *OMAP35x Technical Reference Manual (TRM)* [literature number SPRUF98].

6.5.2.2 LCD Display in RFBI Mode

Table 6-40 and Table 6-41 assume testing over the recommended operating conditions (see Figure 6-30 through Figure 6-32).

Table 6-39. LCD Timing Conditions – RFBI Mode

TIMING CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rise time		15	ns
t_F	Input signal fall time		15	ns
Output Conditions				
C_{LOAD}	Output load capacitance		30	pF

Table 6-40. LCD Display Timing Requirements in RFBI Mode

NO.	PARAMETER		OPP3		OPP2		OPP1(1)		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
DR0	$t_{su(DAV-RDH)}$	Setup time, rfbi_da[15:0] valid to rfbi_rd high	7.0		9.0				ns
DR1	$t_{h(RDH-DAIV)}$	Hold time, rfbi_rd high to rfbi_da[15:0] invalid	5.0		5.0				ns
	$t_{d(Data\ sampled)}$	rfbi_da[15:0] are sampled at the end off the access time	N(2)		N(2)				ns

(1) Cannot boot in OPP1. If OPP1 is desired, boot in higher OPP then switch to OPP1.

(2) N = (AccessTime) * (TimeParaGranularity + 1) * L4CLK

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Table 6-41. LCD Display Switching Characteristics in RFBI Mode

PARAMETER		OPP3		OPP2		OPP1[1]		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{w(rfbi_wrH)}$	Pulse duration, rfbi_wr high	A[2]		A[2]				ns
$t_{w(rfbi_wrL)}$	Pulse duration, rfbi_wr low	B[3]		B[3]				ns
$t_{d(rfbi_a0\text{-}rfbi_wrL)}$	Delay time, rfbi_a0 transition to rfbi_wr low	C[4]		C[4]				ns
$t_{d(rfbi_wrH\text{-}rfbi_a0)}$	Delay time, rfbi_wr high to rfbi_a0 transition	D[5]		D[5]				ns
$t_{d(rfbi_csx\text{-}rfbi_wrL)}$	Delay time, rfbi_csx[15] low to rfbi_wr low	E[6]		E[6]				ns
$t_{d(rfbi_wrH\text{-}rfbi_csxH)}$	Delay time, rfbi_wr high to rfbi_csx[15] high	F[7]		F[7]				ns
$t_{d(dataV)}$	rfbi_da[15:0] valid	G[8]		G[8]				ns
$t_{d(rfbi_a0H\text{-}rfbi_rdL)}$	Delay time, rfbi_a0 high to rfbi_rd low	H[9]		H[9]				ns
$t_{d(rfbi_rdlH\text{-}rfbi_a0)}$	Delay time, rfbi_rd high to rfbi_a0 transition	I[10]		I[10]				ns
$t_{w(rfbi_rdH)}$	Pulse duration, rfbi_rd high	J[11]		J[11]				ns
$t_{w(rfbi_rdL)}$	Pulse duration, rfbi_rd low	K[12]		K[12]				ns
$t_{d(rfbi_rdL\text{-}rfbi_csxL)}$	Delay time, rfbi_rd low to rfbi_csx[15] low	L[13]		L[13]				ns
$t_{d(rfbi_rdH\text{-}rfbi_csxH)}$	Delay time, rfbi_rd high to rfbi_csx[15] high	M[14]		M[14]				ns
$t_{R(rfbi_wr)}$	Rise time, rfbi_wr		10		10			ns
$t_{F(rfbi_wr)}$	Fall time, rfbi_wr		10		10			ns
$t_{R(rfbi_a0)}$	Rise time, rfbi_a0		10		10			ns
$t_{F(rfbi_a0)}$	Fall time, rfbi_a0		10		10			ns
$t_{R(rfbi_csx)}$	Rise time, rfbi_csx[15]		10		10			ns
$t_{F(rfbi_csx)}$	Fall time, rfbi_csx[15]		10		10			ns
$t_{R(rfbi_da[15:0])}$	Rise time, rfbi_da[15:0]		10		10			ns
$t_{F(rfbi_da[15:0])}$	Fall time, rfbi_da[15:0]		10		10			ns
$t_{R(rfbi_rd)}$	Rise time, rfbi_rd		10		10			ns
$t_{F(rfbi_rd)}$	Fall time, rfbi_rd		10		10			ns

(1) Cannot boot in OPP1. If OPP1 is desired, boot in higher OPP then switch to OPP1.

(2) A = (WECycleTime – WEOffTime) * (TimeParaGranularity + 1) * L4CLK

(3) B = (WEOffTime – WEOntime) * (TimeParaGranularity + 1) * L4CLK

(4) C = WEOnTime * (TimeParaGranularity + 1) * L4CLK

(5) D = (WECycleTime + CSPulseWidth – WEOffTime) * (TimeParaGranularity + 1) * L4CLK if mode Write to Read or Read to Write is enabled

(6) E = (WEOnTime – CSOnTime) * (TimeParaGranularity + 1) * L4CLK

(7) F = (CSOffTime – WEOffTime) * (TimeParaGranularity + 1) * L4CLK

(8) G = (WECycleTime) * (TimeParaGranularity + 1) * L4CLK

(9) H = (REOnTime) * (TimeParaGranularity + 1) * L4CLK

(10) I = (RECycleTime + CSPulseWidth – REOffTime) * (TimeParaGranularity + 1) * L4CLK if mode Write to Read or Read to Write is enabled

(11) J = (RECycleTime – REOffTime) * (TimeParaGranularity + 1) * L4CLK

(12) K = (REOffTime – REOntime) * (TimeParaGranularity + 1) * L4CLK

(13) L = (REOnTime – CSOnTime) * (TimeParaGranularity + 1) * L4CLK

(14) M = (CSOffTime – REOffTime) * (TimeParaGranularity + 1) * L4CLK

(15) In rfbi_csx, x stands for 0 or 1.

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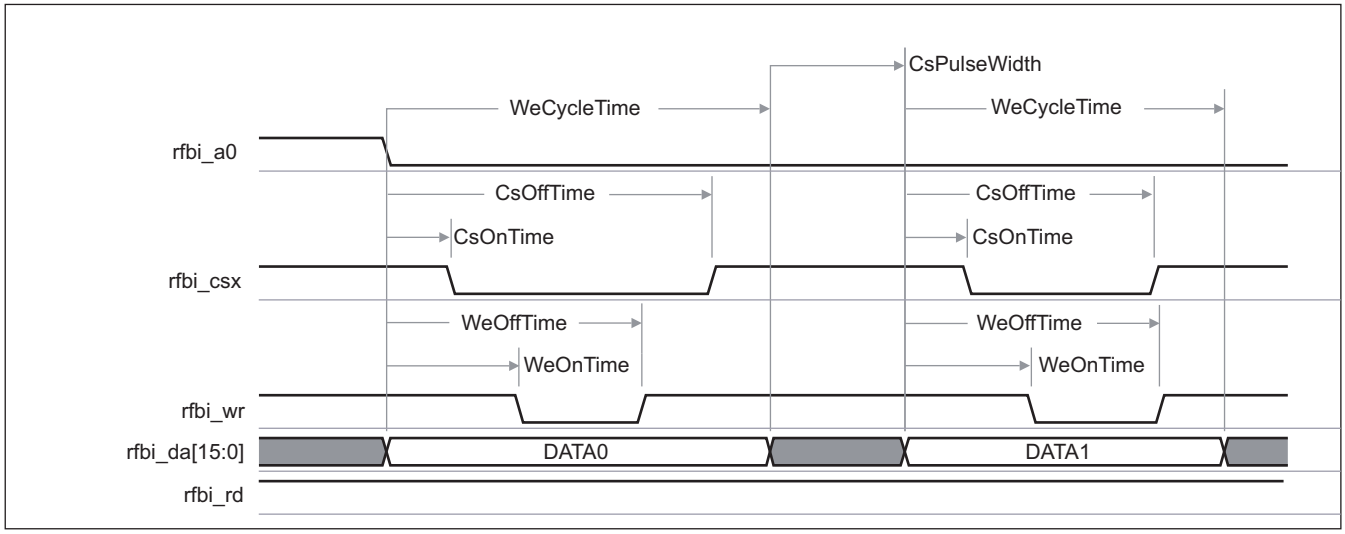

Figure 6-30. LCD Display in RFBI Mode – Command / Data Write Mode(1) (2)

(1) In rfbi_csx, x is equal to 0 or 1.

(2) For more information, see the DSS chapter in the *OMAP35x Technical Reference Manual (TRM)* [literature number SPRUF98] .

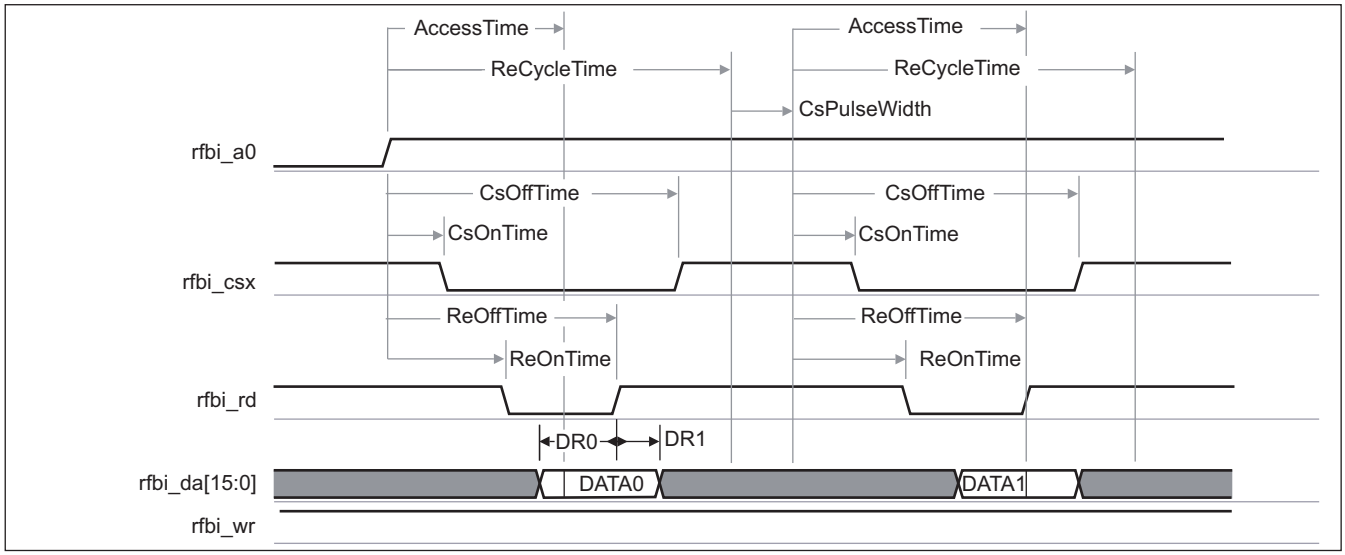

Figure 6-31. LCD Display in RFBI Mode – Data Read Mode(1) (2)

(1) In rfbi_csx, x is equal to 0 or 1.

(2) For more information, see the DSS chapter in the *OMAP35x Technical Reference Manual (TRM)* [literature number SPRUF98].

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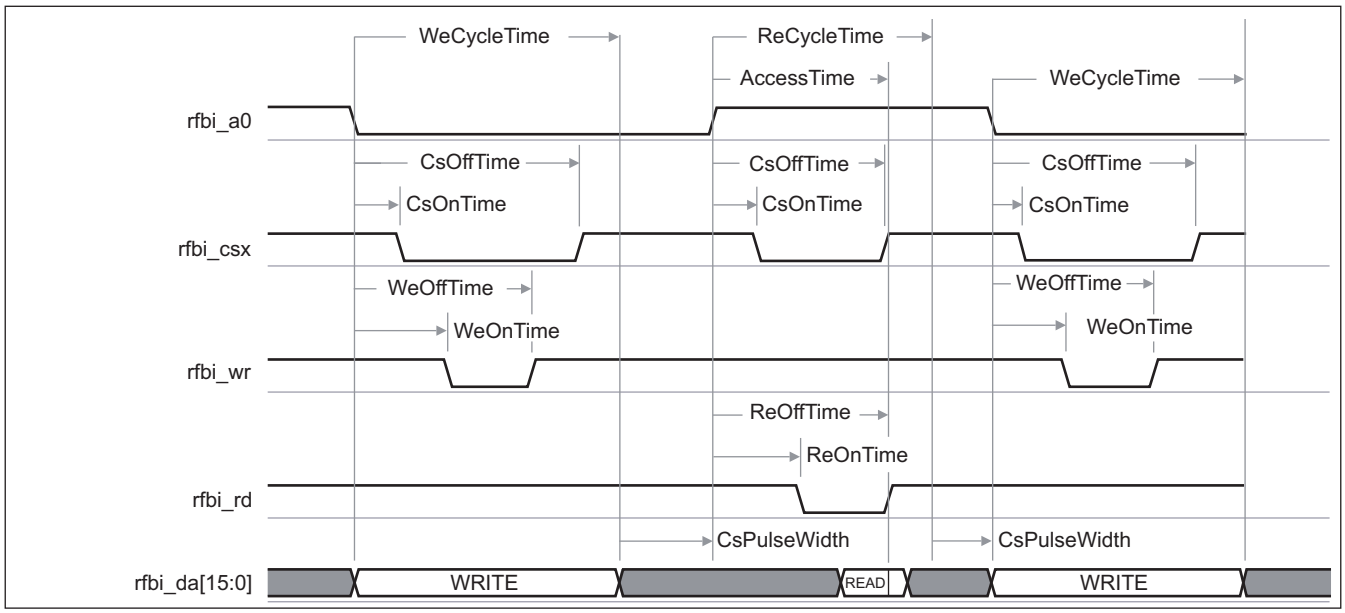

Figure 6-32. LCD Display in RFBI Mode – Command / Data Write-to-Read and Read-to-Write Timing Modes(1) (2)

(1) In rfbi_csx, x is equal to 0 or 1.

(2) For more information, see the DSS chapter in the *OMAP35x Technical Reference Manual (TRM)* [literature number SPRUF98].

6.6 Serial Communications Interfaces

6.6.1 Multichannel Buffered Serial Port (McBSP) Timing

There are five McBSP modules called McBSP1 through McBSP5. McBSP provides a full-duplex, direct serial interface between the OMAP3530/25 device and other devices in a system such as other application devices or codecs. It can accommodate a wide range of peripherals and clocked frame-oriented protocols (I2S, PCM, and TDM) due to its high level of versatility.

The McBSP1-5 modules may support two types of data transfer at the system level:

- The full-cycle mode, for which one clock period is used to transfer the data, generated on one edge and captured on the same edge (one clock period later).
- The half-cycle mode, for which one half clock period is used to transfer the data, generated on one edge and captured on the opposite edge (one half clock period later). Note that a new data is generated only every clock period, which secures the required hold time.

The interface clock (CLKX/CLKR) activation edge (data/frame sync capture and generation) has to be configured accordingly with the external peripheral (activation edge capability) and the type of data transfer required at the system level.

The OMAP3530/25 McBSP1-5 timing characteristics are described for both rising and falling activation edges. McBSP1 supports:

- 6-pin mode: dx and dr as data pins; clkx, clkr, fsx, and fsr as control pins.
- 4-pin mode: dx and dr as data pins; clkx and fsx pins as control pins. The clkx and fsx pins are internally looped back via software configuration, respectively, to the clkr and fsr internal signals for data receive.

McBSP2, 3, 4, and 5 support only the 4-pin mode.

The following sections describe the timing characteristics for applications in normal mode (that is, OMAP3530/25 McBSPx connected to one peripheral) and TDM applications in multipoint mode.

6.6.1.1 McBSP in Normal Mode

Table 6-42. McBSP Timing Conditions—Normal Mode

TIMING CONDITION PARAMETER		VALUE	UNIT
Input Conditions			
t_R	Input signal rise time	2	ns
t_F	Input signal fall time	2	ns
Output Conditions			
C_{LOAD}	Output load capacitance	10	pF

Table 6-43. McBSP Output Clock Pulse Duration

NO.	PARAMETER			OPP3		OPP2		UNIT
				MIN	MAX	MIN	MAX	
Inputs and Outputs								
McBSP1	$t_{c(CLK)}$	Cycle time, mcbsp1_clkx / mcbsp1_clkr (multiplexing mode 0)		20.83		41.67		ns
McBSP2	$t_{c(CLK)}$	Cycle time, mcbsp2_clkx (multiplexing mode 0)		20.83		41.67		ns
McBSP3	$t_{c(CLK)}$	Cycle time, mcbsp3_clkx	IO set 1 (multiplexing mode 0)	31.25		62.50		ns
			IO set 2 (multiplexing mode 1)	20.83		41.67		
			IO set 3 (multiplexing mode 2)	20.83		41.67		
McBSP4	$t_{c(CLK)}$	Cycle time, mcbsp4_clkx	IO set 1 (multiplexing mode 0)	20.83		41.67		ns
			IO set 2 (multiplexing mode 2)	31.25		62.50		
McBSP5	$t_{c(CLK)}$	Cycle time, mcbsp5_clkx (multiplexing mode 1)		31.25		62.50		ns

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Table 6-43. McBSP Output Clock Pulse Duration (continued)

NO.	PARAMETER		OPP3		OPP2		UNIT
			MIN	MAX	MIN	MAX	
Outputs							
	$t_{w(CLKH)}$	Typical pulse duration, mcbsp1_clkr / mcbspx_clkx high(2)	0.5*P(1)		0.5*P(1)		ns
	$t_{w(CLKL)}$	Typical pulse duration, mcbsp1_clkr / mcbspx_clkx low(2)	0.5*P(1)		0.5*P(1)		ns
	$t_{dc(CLK)}$	Duty cycle error, mcbsp1_clkr / mcbspx_clkx(2)	–0.75	0.75	–0.75	0.75	ns

(1) P = mcbsp1_clkr / mcbspx_clkx clock period.

(2) In mcbspx, x identifies the McBSP number: 1, 2, 3, 4, or 5.

6.6.1.1.1 Receive Timing with Rising Edge as Activation Edge

Table 6-44 through Table 6-49 assume testing over the recommended operating conditions (see Figure 6-33 through Figure 6-34).

Table 6-44. McBSP1, 2, and 3 (Sets #2 and #3) Timing Requirements – Rising Edge and Receive Mode(1)

NO.	PARAMETER			1.15 V		1.0 V		UNIT
				MIN	MAX	MIN	MAX	
B3	$t_{su(DRV-CLKAE)}$	Setup time, mcbspx_dr valid before mcbsp1_clkr / mcbspx_clkx active edge	Master	3.5		7.7		ns
			Slave	3.7		7.9		ns
B4	$t_{h(CLKAE-DRV)}$	Hold time, mcbspx_dr valid after mcbsp1_clkr / mcbspx_clkx active edge	Master	1		1		ns
			Slave	0.4		0.4		ns
B5	$t_{su(FSV-CLKAE)}$	Setup time, mcbsp1_fsr / mcbspx_fsx valid before mcbsp1_clkr / mcbspx_clkx active edge		3.7		7.9		ns
B6	$t_{h(CLKAE-FSV)}$	Hold time, mcbsp1_fsr / mcbspx_fsx valid after mcbsp1_clkr / mcbspx_clkx active edge		0.5		0.5		ns

(1) In mcbspx, x identifies the McBSP number: 1, 2, or 3. Note that for the McBSP3, these timings concern only Set #2 (multiplexing mode on UART pins) and Set #3 (multiplexing mode on McBSP1 pins).

Table 6-45. McBSP1, 2, and 3 (Sets #2 and #3) Switching Characteristics – Rising Edge and Receive Mode(1)

NO.	PARAMETER		1.15 V		1.0 V		UNIT
			MIN	MAX	MIN	MAX	
B2	$t_{d(CLKAE-FSV)}$	Delay time, mcbsp1_clkr / mcbspx_clkx active edge to mcbsp1_fsr / mcbspx_fsx valid	0.7	14.8	0.7	29.6	ns

(1) In mcbspx, x identifies the McBSP number: 1, 2, or 3. Note that for the McBSP3, these timings concern only Set #2 (multiplexing mode on UART pins) and Set #3 (multiplexing mode on McBSP1 pins).

Table 6-46. McBSP4 (Set #1) Timing Requirements – Rising Edge and Receive Mode(1)

NO.	PARAMETER			1.15 V		1.0 V		UNIT
				MIN	MAX	MIN	MAX	
B3	$t_{su(DRV-CLKXAE)}$	Setup time, mcbspx_dr valid before mcbspx_clkx active edge	Master	2.7		7.7		ns
			Slave	3.7		7.9		ns
B4	$t_{h(CLKXAE-DRV)}$	Hold time, mcbspx_dr valid after mcbspx_clkx active edge	Master	1		1		ns
			Slave	0.4		0.4		ns
B5	$t_{su(FSXV-CLKXAE)}$	Setup time mcbspx_fsx valid before mcbspx_clkx active edge		3.7		7.9		ns
B6	$t_{h(CLKXAE-FSXV)}$	Hold Time mcbspx_fsx valid after mcbspx_clkx active edge		0.5		0.5		ns

(1) In mcbspx, x identifies the McBSP number: 4. Note that for the McBSP4, these timings concern only Set #1: multiplexing mode by default. The McBSP4 is also multiplexed on GPMC pins (Set #2): the corresponding timings are specified in Table 6-48 and Table 6-49

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Table 6-47. McBSP4 (Set #1) Switching Characteristics – Rising Edge and Receive Mode(1)

NO.	PARAMETER		1.15 V		1.0 V		UNIT
			MIN	MAX	MIN	MAX	
B2	$t_{d(CLKXAE-FSXV)}$	Delay time, mcbspx_clkx active edge to mcbspx_fsx valid	0.7	16.6	0.7	33.1	ns

(1) In mcbspx, x identifies the McBSP number: 4. Note that for the McBSP4, these timings concern only Set #1: multiplexing mode by default. The McBSP4 is also multiplexed on GPMC pins (Set #2): the corresponding timings are specified in Table 6-48 and Table 6-49

Table 6-48. McBSP3 (Set #1), 4 (Set #2), and 5 Timing Requirements – Rising Edge and Receive Mode(1)

NO.	PARAMETER			1.15 V		1.0 V		UNIT
				MIN	MAX	MIN	MAX	
B3	$t_{su(DRV-CLKXAE)}$	Setup time, mcbspx_dr valid before mcbspx_clkx active edge	Master	5.6		12		ns
			Slave	5.8		12.2		ns
B4	$t_{h(CLKXAE-DRV)}$	Hold time, mcbspx_dr valid after mcbspx_clkx active edge	Master	1		1		ns
			Slave	0.4		0.4		ns
B5	$t_{su(FSXV-CLKXAE)}$	Setup time, mcbspx_fsx valid before mcbspx_clkx active edge		5.8		12.2		ns
B6	$t_{h(CLKXAE-FSXV)}$	Hold time, mcbspx_fsx valid after mcbspx_clkx active edge		0.5		0.5		ns

(1) In mcbspx, x identifies the McBSP number: 3, 4, or 5. Note that for the McBSP3, these timings concern only Set #1: multiplexing mode by default. The McBSP3 is also multiplexed on UART pins (Set #2) and on McBSP1 pins (Set #3): the corresponding timings are specified in Table 6-46 and Table 6-47.
For the McBSP4, these timings concern only Set #2 (multiplexing mode on GPMC pins).

Table 6-49. McBSP3 (Set #1), 4 (Set #2), and 5 Switching Requirements – Rising Edge and Receive Mode(1)

NO.	PARAMETER		1.15 V		1.0 V		UNIT
			MIN	MAX	MIN	MAX	
B2	$t_{d(CLKXAE-FSXV)}$	Delay time, mcbspx_clkx active edge to mcbspx_fsx valid	0.7	22.2	0.7	44.4	ns

(1) In mcbspx, x identifies the McBSP number: 3, 4, or 5. Note that for the McBSP3, these timings concern only Set #1: multiplexing mode by default. The McBSP3 is also multiplexed on UART pins (Set #2) and on McBSP1 pins (Set #3): the corresponding timings are specified in Table 6-46 and Table 6-47.
For the McBSP4, these timings concern only Set #2 (multiplexing mode on GPMC pins).

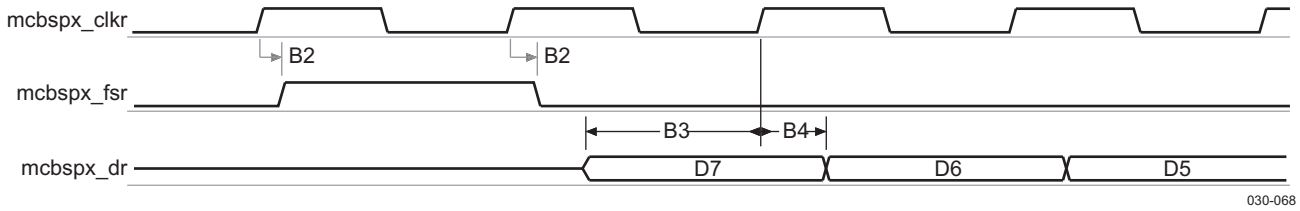

Figure 6-33. McBSP Rising Edge Receive Timing in Master Mode

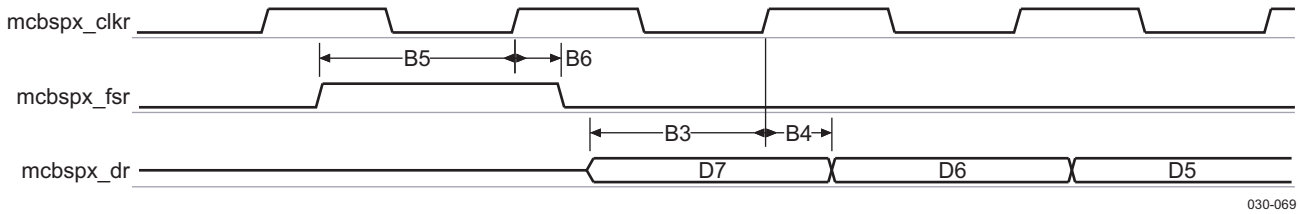

Figure 6-34. McBSP Rising Edge Receive Timing in Slave Mode

6.6.1.1.2 Transmit Timing with Rising Edge as Activation Edge

Table 6-50 through Table 6-55 assume testing over the recommended operating conditions (see Figure 6-35 and Figure 6-36).

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Table 6-50. McBSP1, 2, and 3 (Sets #2 and #3) Timing Requirements – Rising Edge and Transmit Mode(1)

NO.	PARAMETER		1.15 V		1.0 V		UNIT
			MIN	MAX	MIN	MAX	
B5	$t_{su(FSXV-CLKXAE)}$	Setup time, mcbspx_fsx valid before mcbspx_clkx active edge	3.7		7.9		ns
B6	$t_{h(CLKXAE-FSXV)}$	Hold time, mcbspx_fsx valid after mcbspx_clkx active edge	0.5		0.5		ns

(1) In mcbspx, x identifies the McBSP number: 1, 2, or 3. Note that for the McBSP3, these timings concern only Set #2 (multiplexing mode on UART pins) and Set #3 (multiplexing mode on McBSP1 pins).

Table 6-51. McBSP1, 2, and 3 (Sets #2 and #3) Switching Characteristics – Rising Edge and Transmit Mode(1)

NO.	PARAMETER			1.15 V		1.0 V		UNIT
				MIN	MAX	MIN	MAX	
B2	$t_{d(CLKXAE-FSXV)}$	Delay time, mcbspx_clkx active edge to mcbspx_fsx valid		0.7	14.8	0.7	29.6	ns
B8	$t_{d(CLKXAE-DXV)}$	Delay time, mcbspx_clkx active edge to mcbspx_dx valid	Master	0.6	14.8	0.6	29.6	ns
			Slave	0.6	14.8	0.6	29.6	ns

(1) In mcbspx, x identifies the McBSP number: 1, 2, or 3. Note that for the McBSP3, these timings concern only Set #2 (multiplexing mode on UART pins) and Set #3 (multiplexing mode on McBSP1 pins).

Table 6-52. McBSP4 (Set #1) Timing Requirements – Rising Edge and Transmit Mode(1)

NO.	PARAMETER		1.15 V		1.0 V		UNIT
			MIN	MAX	MIN	MAX	
B5	$t_{su(FSXV-CLKXAE)}$	Setup time, mcbspx_fsx valid before mcbspx_clkx active edge	3.7		7.9		ns
B6	$t_{h(CLKXAE-FSXV)}$	Hold time, mcbspx_fsx valid after mcbspx_clkx active edge	0.5		0.5		ns

(1) In mcbspx, x identifies the McBSP number: 4. Note that for the McBSP4, these timings concern only Set #1: multiplexing mode by default. The McBSP4 is also multiplexed on GPMC pins (Set #2): the corresponding timings are specified in Table 6-54.

Table 6-53. McBSP4 (Set #1) Switching Characteristics – Rising Edge and Transmit Mode(1)

NO.	PARAMETER			1.15 V		1.0 V		UNIT
				MIN	MAX	MIN	MAX	
B2	$t_{d(CLKXAE-FSXV)}$	Delay time, mcbspx_clkx active edge to mcbspx_fsx valid		0.7	16.6	0.7	33.1	ns
B8	$t_{d(CLKXAE-DXV)}$	Delay time, mcbspx_clkx active edge to mcbspx_dx valid	Master	0.6	16.6	0.6	33.1	ns
			Slave	0.6	17.3	0.6	33.1	ns

(1) In mcbspx, x identifies the McBSP number: 4. Note that for the McBSP4, these timings concern only Set #1: multiplexing mode by default. The McBSP4 is also multiplexed on GPMC pins (Set #2): the corresponding timings are specified in Table 6-54.

Table 6-54. McBSP3 (Set #1), 4 (Set #2), and 5 Timing Requirements – Rising Edge and Transmit Mode(1)

NO.	PARAMETER		1.15 V		1.0 V		UNIT
			MIN	MAX	MIN	MAX	
B5	$t_{su(FSXV-CLKXAE)}$	Setup time, mcbspx_fsx valid before mcbspx_clkx active edge	5.8		12.2		ns
B6	$t_{h(CLKXAE-FSXV)}$	Hold time, mcbspx_fsx valid after mcbspx_clkx active edge	0.5		0.5		ns

(1) In mcbspx, x identifies the McBSP number: 4. Note that for the McBSP4, these timings concern only Set #1: multiplexing mode by default. The McBSP4 is also multiplexed on GPMC pins (Set #2): the corresponding timings are specified in Table 6-54.

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Table 6-55. McBSP 3 (Set #1), 4 (Set #2), and 5 Switching Requirements – Rising Edge and Transmit Mode(1)

NO.	PARAMETER			1.15 V		1.0 V		UNIT
				MIN	MAX	MIN	MAX	
B2	$t_{d(CLKXAE-FSXV)}$	Delay time, mcbspx_clkx active edge to mcbspx_fsx valid		0.7	22.2	0.7	44.4	ns
B8	$t_{d(CLKXAE-DXV)}$	Delay time, mcbspx_clkx active edge to mcbspx_dx valid	Master	0.6	22.2	0.6	44.4	ns
			Slave	0.6	22.2	0.6	44.4	ns

(1) In mcbspx, x identifies the McBSP number: 3, 4 or 5. Note that for the McBSP3, these timings concern only Set #1: multiplexing mode by default. The McBSP3 is also multiplexed on UART pins (Set #2) and on McBSP1 pins (Set #3): the corresponding timings are specified in the table above. For the McBSP4, these timings concern only Set #2 (multiplexing mode on GPMC pins).

Figure 6-35. McBSP Rising Edge Transmit Timing in Master Mode

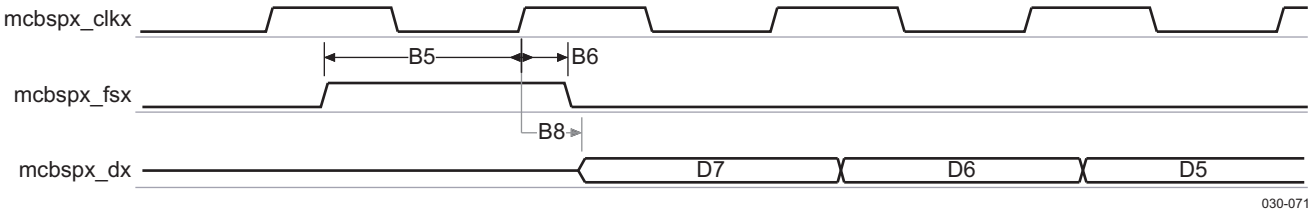

Figure 6-36. McBSP Rising Edge Transmit Timing in Slave Mode

6.6.1.1.3 Receive Timing with Falling Edge as Activation Edge

Table 6-56 through Table 6-61 assume testing over the recommended operating conditions (see Figure 6-37 and Figure 6-38).

Table 6-56. McBSP1, 2, and 3 (Sets #2 and #3) Timing Requirements – Falling Edge and Receive Mode(1)

NO.	PARAMETER			1.15 V		1.0 V		UNIT
				MIN	MAX	MIN	MAX	
B3	$t_{su(DRV-CLKAE)}$	Setup time, mcbspx_dr valid before mcbsp1_clkr / mcbspx_clkx active edge	Master	3.5		7.7		ns
			Slave	3.7		7.9		ns
B4	$t_{h(CLKAE-DRV)}$	Hold time, mcbspx_dr valid after mcbsp1_clkr / mcbspx_clkx active edge	Master	1		1		ns
			Slave	0.4		0.4		ns
B5	$t_{su(FSV-CLKAE)}$	Setup time, mcbsp1_fsr / mcbspx_fsx valid before mcbsp1_clkr /mcbspx_clkx active edge		3.7		7.9		ns
B6	$t_{h(CLKAE-FSV)}$	Hold time, mcbsp1_fsr / mcbspx_fsx valid after mcbsp1_clkr /mcbspx_clkx active edge		0.5		0.5		ns

(1) In mcbspx, x identifies the McBSP number: 1, 2, or 3. Note that for the McBSP3, these timings concern only Set #2 (multiplexing mode on UART pins) and Set #3 (multiplexing mode on McBSP1 pins).

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Table 6-57. McBSP1, 2, and 3 (Sets #2 and #3) Switching Characteristics – Falling Edge and Receive Mode(1)

NO.	PARAMETER		1.15 V		1.0 V		UNIT
			MIN	MAX	MIN	MAX	
B2	$t_{d(CLKAE-FSV)}$	Delay time, mcbsp1_clkr / mcbspx_clkx active edge to mcbsp1_fsr / mcbspx_fsx valid	0.7	14.8	0.7	29.6	ns

(1) In mcbspx, x identifies the McBSP number: 1, 2, or 3. Note that for the McBSP3, these timings concern only Set #2 (multiplexing mode on UART pins) and Set #3 (multiplexing mode on McBSP1 pins).

Table 6-58. McBSP4 (Set #1) Timing Requirements – Falling Edge and Receive Mode(1)

NO.	PARAMETER			1.15 V		1.0 V		UNIT
				MIN	MAX	MIN	MAX	
B3	$t_{su(DRV-CLKXAE)}$	Setup time, mcbspx_dr valid before mcbspx_clkx active edge	Master	2.7		7.7		ns
			Slave	3.7		7.9		ns
B4	$t_{h(CLKXAE-DRV)}$	Hold time, mcbspx_dr valid after mcbspx_clkx active edge	Master	1		1		ns
			Slave	0.4		0.4		ns
B5	$t_{su(FSXV-CLKXAE)}$	Setup time mcbspx_fsx valid before mcbspx_clkx active edge		3.7		7.9		ns
B6	$t_{h(CLKXAE-FSXV)}$	Hold time mcbspx_fsx valid after mcbspx_clkx active edge		0.5		0.5		ns

(1) In mcbspx, x identifies the McBSP number: 4. Note that for the McBSP4, these timings concern only Set #1: multiplexing mode by default. The McBSP4 is also multiplexed on GPMC pins (Set #2): the corresponding timings are specified in Table 6-60

Table 6-59. McBSP4 (Set #1) Switching Characteristics – Falling Edge and Receive Mode(1)

NO.	PARAMETER		1.15 V		1.0 V		UNIT
			MIN	MAX	MIN	MAX	
B2	$t_{d(CLKXAE-FSXV)}$	Delay time, mcbspx_clkx active edge to mcbspx_fsx valid	0.7	16.6	0.7	33.1	ns

(1) In mcbspx, x identifies the McBSP number: 4. Note that for the McBSP4, these timings concern only Set #1: multiplexing mode by default. The McBSP4 is also multiplexed on GPMC pins (Set #2): the corresponding timings are specified in Table 6-60

Table 6-60. McBSP3 (Set #1), 4 (Set #2), and 5 Timing Requirements – Falling Edge and Receive Mode(1)

NO.	PARAMETER			1.15 V		1.0 V		UNIT
				MIN	MAX	MIN	MAX	
B3	$t_{su(DRV-CLKXAE)}$	Setup time, mcbspx_dr valid before mcbspx_clkx active edge	Master	5.6		12		ns
			Slave	5.8		12.2		ns
B4	$t_{h(CLKXAE-DRV)}$	Hold time, mcbspx_dr valid after mcbspx_clkx active edge	Master	1		1		ns
			Slave	0.4		0.4		ns
B5	$t_{su(FSXV-CLKXAE)}$	Setup time, mcbspx_fsx valid before mcbspx_clkx active edge		5.8		12.2		ns
B6	$t_{h(CLKXAE-FSXV)}$	Hold time, mcbspx_fsx valid after mcbspx_clkx active edge		0.5		0.5		ns

(1) In mcbspx, x identifies the McBSP number: 3, 4, or 5. Note that for the McBSP3, these timings concern only Set #1: multiplexing mode by default. The McBSP3 is also multiplexed on UART pins (Set #2) and on McBSP1 pins (Set #3): the corresponding timings are specified in the table above. For the McBSP4, these timings concern only Set #2 (multiplexing mode on GPMC pins).

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Table 6-61. McBSP3 (Set #1), 4 (Set #2), and 5 Switching Requirements – Falling Edge and Receive Mode(1)

NO.	PARAMETER		1.15 V		1.0 V		UNIT
			MIN	MAX	MIN	MAX	
B2	$t_{d(CLKXAE-FSXV)}$	Delay time, mcbspx_clkx active edge to mcbspx_fsx valid	0.7	22.2	0.7	44.4	ns

(1) In mcbspx, x identifies the McBSP number: 3, 4, or 5. Note that for the McBSP3, these timings concern only Set #1: multiplexing mode by default. The McBSP3 is also multiplexed on UART pins (Set #2) and on McBSP1 pins (Set #3): the corresponding timings are specified in the table above. For the McBSP4, these timings concern only Set #2 (multiplexing mode on GPMC pins).

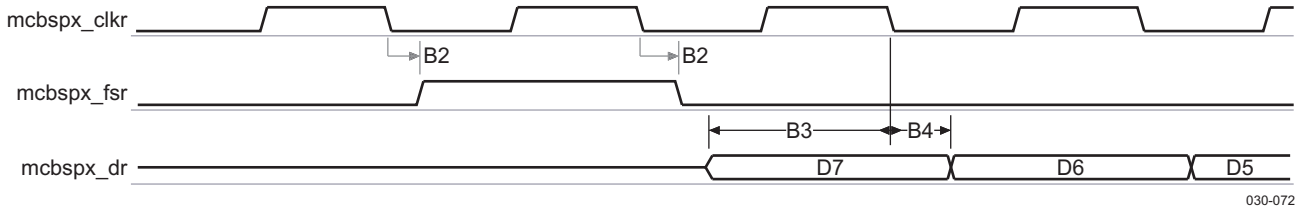

Figure 6-37. McBSP Falling Edge Receive Timing in Master Mode

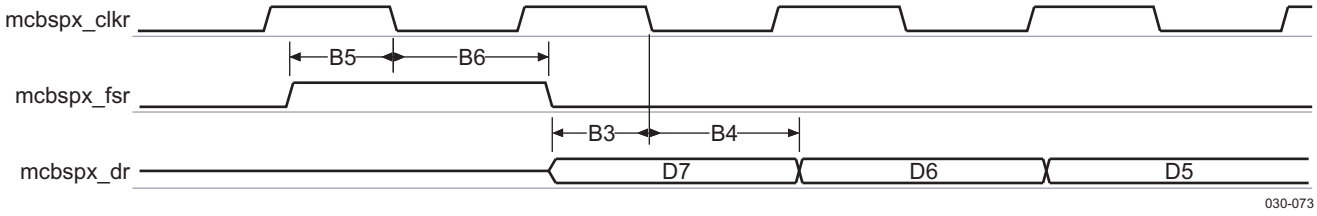

Figure 6-38. McBSP Falling Edge Receive Timing in Slave Mode

6.6.1.1.4 Transmit Timing with Falling Edge as Activation Edge

Table 6-62 through Table 6-67 assume testing over the recommended operating conditions (see Figure 6-39 and Figure 6-40).

Table 6-62. McBSP1, 2, and 3 (Sets #2 and #3) Timing Requirements – Falling Edge and Transmit Mode(1)

NO.	PARAMETER		1.15 V		1.0 V		UNIT
			MIN	MAX	MIN	MAX	
B5	$t_{su(FSXV-CLKXAE)}$	Setup time, mcbspx_fsx valid before mcbspx_clkx active edge	3.7		7.9		ns
B6	$t_{h(CLKXAE-FSXV)}$	Hold time, mcbspx_fsx valid after mcbspx_clkx active edge	0.5		0.5		ns

(1) In mcbspx, x identifies the McBSP number: 1, 2, or 3. Note that for the McBSP3, these timings concern only Set #2 (multiplexing mode on UART pins) and Set #3 (multiplexing mode on McBSP1 pins).

Table 6-63. McBSP1, 2, and 3 (Sets #2 and #3) Switching Characteristics – Falling Edge and Transmit Mode(1)

NO.	PARAMETER			1.15 V		1.0 V		UNIT
				MIN	MAX	MIN	MAX	
B2	$t_{d(CLKXAE-FSXV)}$	Delay time, mcbspx_clkx active edge to mcbspx_fsx valid		0.7	14.8	0.7	29.6	ns
B8	$t_{d(CLKXAE-DXV)}$	Delay time, mcbspx_clkx active edge to mcbspx_dx valid	Master	0.6	14.8	0.6	29.6	ns
			Slave	0.6	14.8	0.6	29.6	ns

(1) In mcbspx, x identifies the McBSP number: 1, 2, or 3. Note that for the McBSP3, these timings concern only Set #2 (multiplexing mode on UART pins) and Set #3 (multiplexing mode on McBSP1 pins).

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Table 6-64. McBSP4 (Set #1) Timing Requirements – Falling Edge and Transmit Mode(1)

NO.	PARAMETER		1.15 V		1.0 V		UNIT
			MIN	MAX	MIN	MAX	
B5	$t_{su(FSXV-CLKXAE)}$	Setup time, mcbspx_fsx valid before mcbspx_clkx active edge	3.7		7.9		ns
B6	$t_{h(CLKXAE-FSXV)}$	Hold time, mcbspx_fsx valid after mcbspx_clkx active edge	0.5		0.5		ns

(1) In mcbspx, x identifies the McBSP number: 4. Note that for the McBSP4, these timings concern only Set #1: multiplexing mode by default. The McBSP4 is also multiplexed on GPMC pins (Set #2): the corresponding timings are specified in Table 6-66.

Table 6-65. McBSP4 (Set #1) Switching Characteristics – Falling Edge and Transmit Mode(1)

NO.	PARAMETER			1.15 V		1.0 V		UNIT
				MIN	MAX	MIN	MAX	
B2	$t_{d(CLKXAE-FSXV)}$	Delay time, mcbspx_clkx active edge to mcbspx_fsx valid		0.7	16.6	0.7	33.1	ns
B8	$t_{d(CLKXAE-DXV)}$	Delay time, mcbspx_clkx active edge to mcbspx_dx valid	Master	0.6	16.6	0.6	33.1	ns
			Slave	0.6	17.3	0.6	33.1	ns

(1) In mcbspx, x identifies the McBSP number: 4. Note that for the McBSP4, these timings concern only Set #1: multiplexing mode by default. The McBSP4 is also multiplexed on GPMC pins (Set #2): the corresponding timings are specified in Table 6-66.

Table 6-66. McBSP3 (Set #1), 4 (Set #2), and 5 Timing Requirements – Falling Edge and Transmit Mode(1)

NO.	PARAMETER		1.15 V		1.0 V		UNIT
			MIN	MAX	MIN	MAX	
B5	$t_{su(FSXV-CLKXAE)}$	Setup time, mcbspx_fsx valid before mcbspx_clkx active edge	5.8		12.2		ns
B6	$t_{h(CLKXAE-FSXV)}$	Hold time, mcbspx_fsx valid after mcbspx_clkx active edge	0.5		0.5		ns

(1) In mcbspx, x identifies the McBSP number: 3, 4, or 5. Note that for the McBSP3, these timings concern only Set #1: multiplexing mode by default. The McBSP3 is also multiplexed on UART pins (Set #2) and on McBSP1 pins (Set #3): the corresponding timings are specified in Table 6-66. For the McBSP4, these timings concern only Set #2 (multiplexing mode on GPMC pins).

Table 6-67. McBSP3 (Set #1), 4 (Set #2), and 5 Switching Requirements – Falling Edge and Transmit Mode(1)

NO.	PARAMETER			1.15 V		1.0 V		UNIT
				MIN	MAX	MIN	MAX	
B2	$t_{d(CLKXAE-FSXV)}$	Delay time, mcbspx_clkx active edge to mcbspx_fsx valid		0.7	22.2	0.7	44.4	ns
B8	$t_{d(CLKXAE-DXV)}$	Delay time, mcbspx_clkx active edge to mcbspx_dx valid	Master	0.6	22.2	0.6	44.4	ns
			Slave	0.6	22.2	0.6	44.4	ns

(1) In mcbspx, x identifies the McBSP number: 3, 4, or 5. Note that for the McBSP3, these timings concern only Set #1: multiplexing mode by default. The McBSP3 is also multiplexed on UART pins (Set #2) and on McBSP1 pins (Set #3): the corresponding timings are specified in Table 6-66. For the McBSP4, these timings concern only Set #2 (multiplexing mode on GPMC pins).

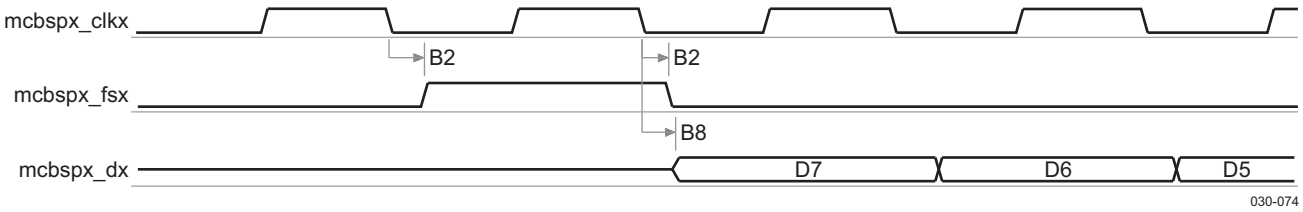

Figure 6-39. McBSP Falling Edge Transmit Timing in Master Mode

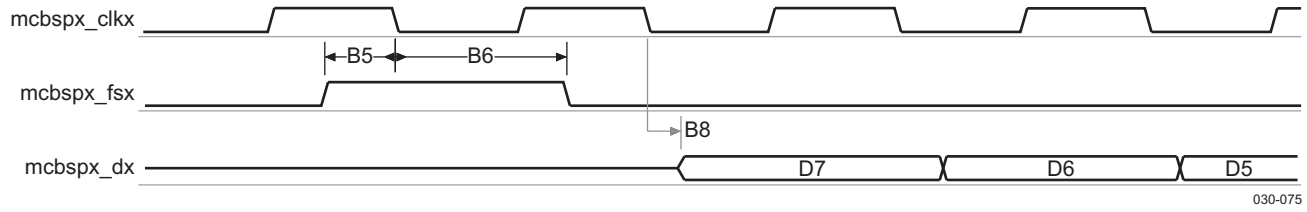

Figure 6-40. McBSP Falling Edge Transmit Timing in Slave Mode

6.6.1.2 McBSP in TDM—Multipoint Mode (McBSP3)

For TDM application in multipoint mode, OMAP3530/25 is considered as a slave. Table 6-69 and Table 6-70 assume testing over the operating conditions and electrical characteristic conditions described below.

Table 6-68. McBSP3 Timing Conditions—TDM in Multipoint Mode

TIMING CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rising time	1.0	8.5	ns
t_F	Input signal falling time	1.0	8.5	ns
Output Conditions				
C_{LOAD}	Output Load Capacitance		40	pF

Table 6-69. McBSP3 Timing Requirements—TDM in Multipoint Mode(1)

NO.	PARAMETER		1.15 V		1.0 V		UNIT
			MIN	MAX	MIN	MAX	
	$t_{W(CLKH)}$	Cycle Time, mcbsp3_clkx	162.8		162.8		ns
	$t_{W(CLKH)}$	Typical Pulse duration, mcbsp3_clkx high	0.5*P(2)		0.5*P(2)		ns
	$t_{W(CLKL)}$	Typical Pulse duration, mcbsp3_clkx low	0.5*P(2)		0.5*P(2)		ns
	$t_{dc(CLK)}$	Duty cycle error, mcbsp3_clkx	–8.14	8.14	–8.14	8.14	ns
B3(3)	$t_{su(DRV-CLKAE)}$	Setup time, mcbsp3_dr valid before mcbsp3_clkx active edge	9		9		ns
B4(3)	$t_{h(CLKAE-DRV)}$	Hold time, mcbsp3_dr valid after mcbsp3_clkx active edge	2.4		2.4		ns
B5(3)	$t_{su(FSV-CLKAE)}$	Setup time, mcbsp3_fsx valid before mcbsp3_clkx active edge	9		9		ns
B6(3)	$t_{h(CLKAE-FSV)}$	Hold time, mcbsp3_fsx valid after mcbsp3_clkx active edge	2.4		2.4		ns

(1) For McBSP3, these timings concern only Set #3 (multiplexing mode in McBSP1 pins).
(2) P = mcbsp3_clkx period in ns
(3) See Section 6.6.1.1, *McBSP in Normal Mode* for corresponding figures.

Table 6-70. McBSP3 Switching Characteristics—TDM in Multipoint Mode(1)

NO.	PARAMETER		1.15 V		1.0 V		UNIT
			MIN	MAX	MIN	MAX	
B8(2)	$t_{d(CLKXAE-DXV)}$	Delay time, mcbsp3_clkx active edge to mcbsp3_dx valid	0.6	16.8	0.6	29.6	ns

(1) For McBSP3, these timings concern only Set #3 (multiplexing mode in McBSP1 pins).
(2) See Section 6.6.1.1, *McBSP in Normal Mode* for corresponding figures.

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6.6.2 Multichannel Serial Port Interface (McSPI) Timing

The multichannel SPI is a master/slave synchronous serial bus. The McSPI1 module supports up to four peripherals and the others (McSPI2, McSPI3, and McSPI4) support up to two peripherals. The following timings are applicable to the different configurations of McSPI in master/slave mode for any McSPI and any channel (n).

6.6.2.1 McSPI in Slave Mode

Table 6-71 and Table 6-72 assume testing over the recommended operating conditions (see Figure 6-41).

Table 6-71. McSPI Interface Timing Requirements – Slave Mode(1) (2)

NO.	PARAMETER		1.15 V		1.0 V		UNIT
			MIN	MAX	MIN	MAX	
1/SS0	$1/t_{c(CLK)}$	Frequency, mcspix_clk		24		12	MHz
	$t_{j(CLK)}$	Cycle jitter(3), mcspix_clk	-200	200	-200	200	ps
SS1	$t_{w(CLK)}$	Pulse duration, mcspix_clk high or low	0.45*P(4)	0.55*P(4)	0.45*P(4)	0.55*P(4)	ns
SS2	$t_{su(SIMOV-CLKAE)}$	Setup time, mcspix_simo valid before mcspix_clk active edge	4.2		9.5		ns
SS3	$t_{h(SIMOV-CLKAE)}$	Hold time, mcspix_simo valid after mcspix_clk active edge	4.6		9.9		ns
SS4	$t_{su(CS0V-CLKFE)}$	Setup time, mcspix_cs0 valid before mcspix_clk first edge	13.8		28.6		ns
SS5	$t_{h(CS0I-CLKLE)}$	Hold time, mcspix_cs0 invalid after mcspix_clk last edge	13.8		28.6		ns

(1) The input timing requirements are given by considering a rise time and a fall time of 4 ns.
(2) In mcspix, x is equal to 1, 2, 3, or 4.
(3) Maximum cycle jitter supported by mcspix_clk input clock.
(4) P = mcspix_clk clock period

Table 6-72. McSPI Interface Switching Requirements(1) (2) (3) (4)

NO.	PARAMETER			1.15 V		1.0 V		UNIT
				MIN	MAX	MIN	MAX	
SS6	$t_{d(CLKAE-SOMIV)}$	Delay time, mcspix_clk active edge to mcspix_somi shifted		1.8	15.9	3.2	31.7	ns
SS7	$t_{d(CS0AE-SOMIV)}$	Delay time, mcspix_cs0 active edge to mcspix_somi shifted	Modes 0 and 2		15.9		31.7	ns

(1) The capacitive load is equivalent to 20 pF.
(2) In mcspix, x is equal to 1, 2, 3, or 4.
(3) The polarity of mcspix_clk and the active edge (rising or falling) on which mcspix_simo is driven and mcspix_somi is latched is all software configurable.
(4) This timing applies to all configurations regardless of mcspix_clk polarity and which clock edges are used to drive output data and capture input data.

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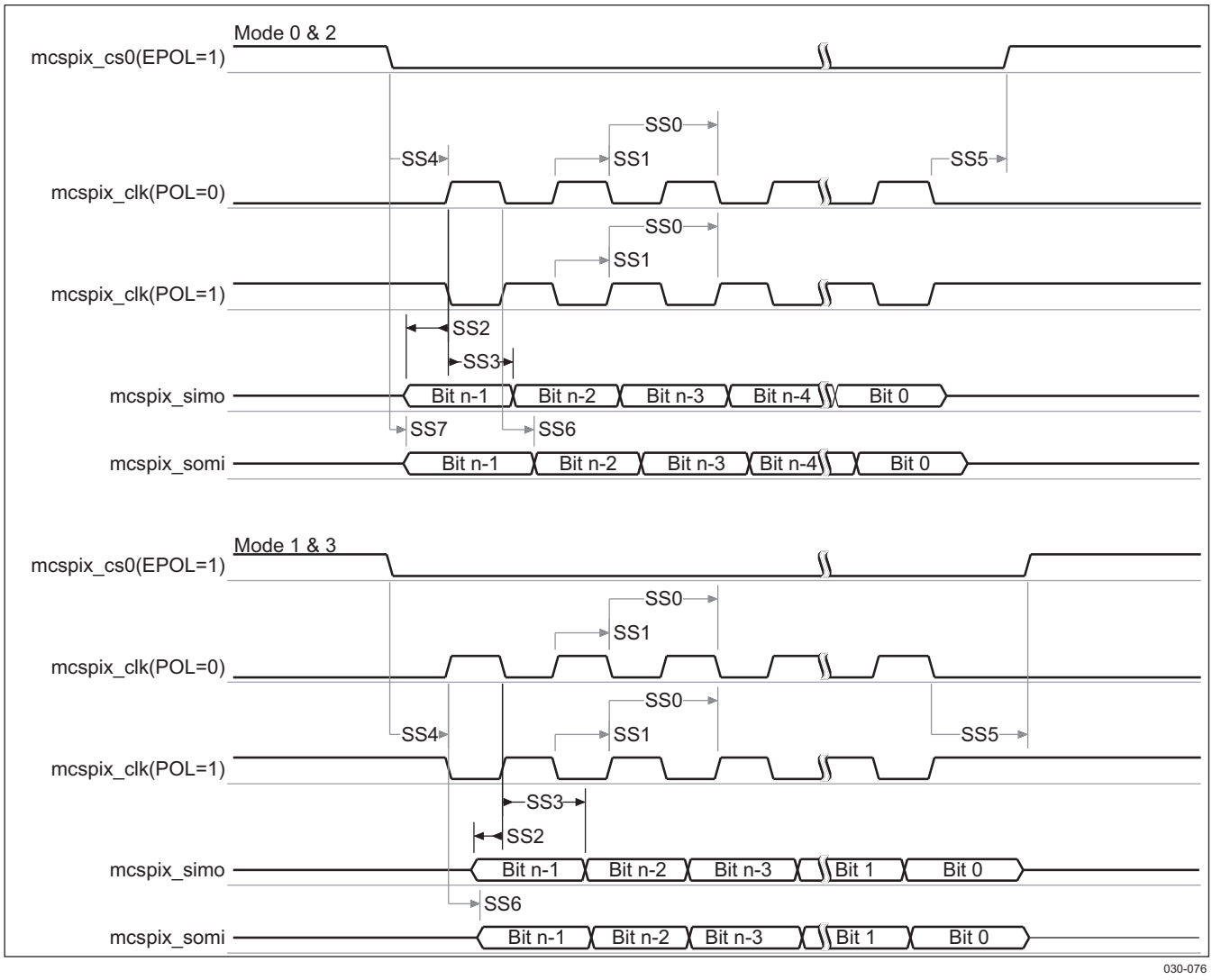

Figure 6-41. McSPI Interface – Transmit and Receive in Slave Mode(1) (2)

(1) The active clock edge (rising or falling) on which mcspi_somi is driven and mcspi_simo data is latched is software configurable with the bit MSPI_CHCONFx[0] = PHA and the bit MSPI_CHCONFx[1] = POL.

(2) The polarity of mcspix_csi is software configurable with the bit MSPI_CHCONFx[6] = EPOL In mcspix, x is equal to 1, 2, 3, or 4.

6.6.2.2 McSPI in Master Mode

Table 6-73 and Table 6-74 assume testing over the recommended operating conditions (see Figure 6-42).

Table 6-73. McSPI1, 2, and 4 Interface Timing Requirements – Master Mode(1) (2)

NO.	PARAMETER		1.15 V		1.0 V		UNIT
			MIN	MAX	MIN	MAX	
SM2	$t_{su(SOMIV-CLKAE)}$	Setup time, mcspix_somi valid before mcspix_clk active edge	1.1		1.5		ns
SM3	$t_{h(SOMIV-CLKAE)}$	Hold time, mcspix_somi valid after mcspix_clk active edge	1.9		2.8		ns

(1) The input timing requirements are given by considering a rise time and a fall time of 4 ns.
(2) In mcspix, x is equal to 1, 2, or 4. In mcspix_csn, n is equal to 0, 1, 2, or 3 for x equal to 1, n is equal to 0 or 1 for x equal to 2 and 4.

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Table 6-74. McSPI1, 2, and 4 Interface Switching Characteristics – Master Mode(1) (2) (3)

NO.	PARAMETER			1.15 V		1.0 V		UNIT
				MIN	MAX	MIN	MAX	
1/SM0	$1/t_{c(CLK)}$	Frequency, mcspix_clk			48		24	MHz
	$t_{j(CLK)}$	Cycle jitter(4), mcspix_clk		-200	200	-200	200	ps
SM1	$t_{w(CLK)}$	Pulse duration, mcspix_clk high or low		0.45*P(5)	0.55*P(5)	0.45*P(5)	0.55*P(5)	ns
SM4	$t_{d(CLKAE-SIMOV)}$	Delay time, mcspix_clk active edge to mcspix_simo shifted		–2.1	5	–2.1	11.3	ns
SM5	$t_{d(CSnA-CLKFE)}$	Delay time, mcspix_csi active to mcspix_clk first edge	Modes 1 and 3	A(6) – 3.1		A(6) – 4.4		ns
			Modes 0 and 2	B(7) – 3.1		B(7) – 4.4		ns
SM6	$t_{d(CLKLE-CSnI)}$	Delay time, mcspix_clk last edge to mcspix_csi inactive	Modes 1 and 3	B(7) – 3.1		B(7) – 4.4		ns
			Modes 0 and 2	A(6) – 3.1		A(6) – 4.4		ns
SM7	$t_{d(CSnAE-SIMOV)}$	Delay time, mcspix_csi active edge to mcspix_simo shifted	Modes 0 and 2		5.0		11.3	ns

(1) Timings are given for a maximum load capacitance of 20 pF for spix_csn signals, 30 pF for spix_clk and spix_simo signals with x = 1 or 2, and 20 pF for spi4_clk and spi4_simo signals.
(2) In mcspix, x is equal to 1, 2, or 4. In mcspix_csn, n is equal to 0, 1, 2, or 3 for x equal to 1, n is equal to 0 or 1 for x equal to 2 and 4.
(3) The polarity of mcspix_clk and the active edge (rising or falling) on which mcspix_simo is driven and mcspix_somi is latched is all software configurable.
(4) Maximum cycle jitter supported by mcspix_clk input clock.
(5) P = mcspix_clk clock period
(6) Case P = 20.8 ns, A = (TCS+0.5)*P(5) (TCS is a bit field of MSPI_CHCONFx[26:25] register). Case P > 20.8 ns, A = TCS*P(5) (TCS is a bitfield of MSPI_CHCONFx[26:25] register). For more information, see the McSPI chapter of the *OMAP35x Technical Reference Manual (TRM)* [literature number SPRUF98].
(7) B = TCS*P (TCS is a bit field of MSPI_CHCONFx[26:25] register). For more information, see the McSPI chapter of the *OMAP35x Technical Reference Manual (TRM)* [literature number SPRUF98].

Table 6-75 and Table 6-76 assume testing over the recommended operating conditions (see Figure 6-42).

Table 6-75. McSPI 3 Interface Timing Requirements – Master Mode(1) (2)

NO.	PARAMETER		1.15 V		1.0 V		UNIT
			MIN	MAX	MIN	MAX	
SM2	$t_{su(SOMIV-CLKAE)}$	Setup time, mcspi3_somi valid before mcspi3_clk active edge	1.5		4.3		ns
SM3	$t_{h(SOMIV-CLKAE)}$	Hold time, mcspi3_somi valid after mcspi3_clk active edge	2.8		5.9		ns

(1) The input timing requirements are given by considering a rise time and a fall time of 4 ns.
(2) In mcspi3_csn, n is equal to 0 or 1. The polarity of mcspi3_clk and the active edge (rising or falling) on which mcspi3_simo is driven and mcspi3_somi is latched is all software configurable.

Table 6-76. McSPI3 Interface Switching Requirements – Master Mode(1) (2) (3)

NO.	PARAMETER		1.15 V		1.0 V		UNIT
			MIN	MAX	MIN	MAX	
1/SM0	$1/t_{c(CLK)}$	Frequency, mcspix_clk		24		12	MHz
	$t_{j(CLK)}$	Cycle jitter(4), mcspix_clk	-200	200	-200	200	ps
SM1	$t_{w(CLK)}$	Pulse duration, mcspix_clk high or low	0.45*P(5)	0.55*P(5)	0.45*P(5)	0.55*P(5)	ns

(1) The capacitive load is equivalent to 20 pF.
(2) In mcspi3_csn, n is equal to 0 or 1. The polarity of mcspi3_clk and the active edge (rising or falling) on which mcspi3_simo is driven and mcspi3_somi is latched is all software configurable.
(3) This timing applies to all configurations regardless of McSPI3_CLK polarity and which clock edges are used to drive output data and capture input data.
(4) Maximum cycle jitter supported by mcspix_clk input clock.
(5) P = mcspi3_clk clock period

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Table 6-76. McSPI3 Interface Switching Requirements – Master Mode(1) (2) (3) (continued)

NO.	PARAMETER			1.15 V		1.0 V		UNIT
				MIN	MAX	MIN	MAX	
SM4	$t_{d(CLKAE-SIMOV)}$	Delay time, mcspix_clk active edge to mcspix_simo shifted		–2.1	11.3	–5.3	23.6	ns
SM5	$t_{d(CSnA-CLKFE)}$	Delay time, mcspix_csi active to mcspix_clk first edge	Modes 1 and 3	–4.4 + A(6)		–10.1 + A(6)		ns
			Modes 0 and 2	–4.4 + B(7)		–10.1 + B(7)		ns
SM6	$t_{d(CLK-CSn)}$	Delay time, mcspix_clk last edge to mcspix_csi inactive	Modes 1 and 3	B – 4.4(7)		B – 10.1(7)		ns
			Modes 0 and 2	A(6) – 4.4		A(6) – 10.1		ns
SM7	$t_{d(CSnAE-SIMOV)}$	Delay time, mcspix_csi active edge to mcspix_simo shifted	Modes 0 and 2		11.3		23.6	ns

(6) Case P = 20.8 ns, A = (TCS + 0.5)*P(5) (TCS is a bit field of MSPI_CHCONFx[26:25] register). Case P > 20.8 ns, A = TCS*P(5) (TCS is a bit field of MSPI_CHCONFx[26:25] register). For more information, see the McSPI chapter of the *OMAP35x Technical Reference Manual (TRM)* [literature number SPRUF98].

(7) B = TCS*P (TCS is a bit field of MSPI_CHCONFx[26:25] register). For more information, see the McSPI chapter of the *OMAP35x Technical Reference Manual (TRM)* [literature number SPRUF98].

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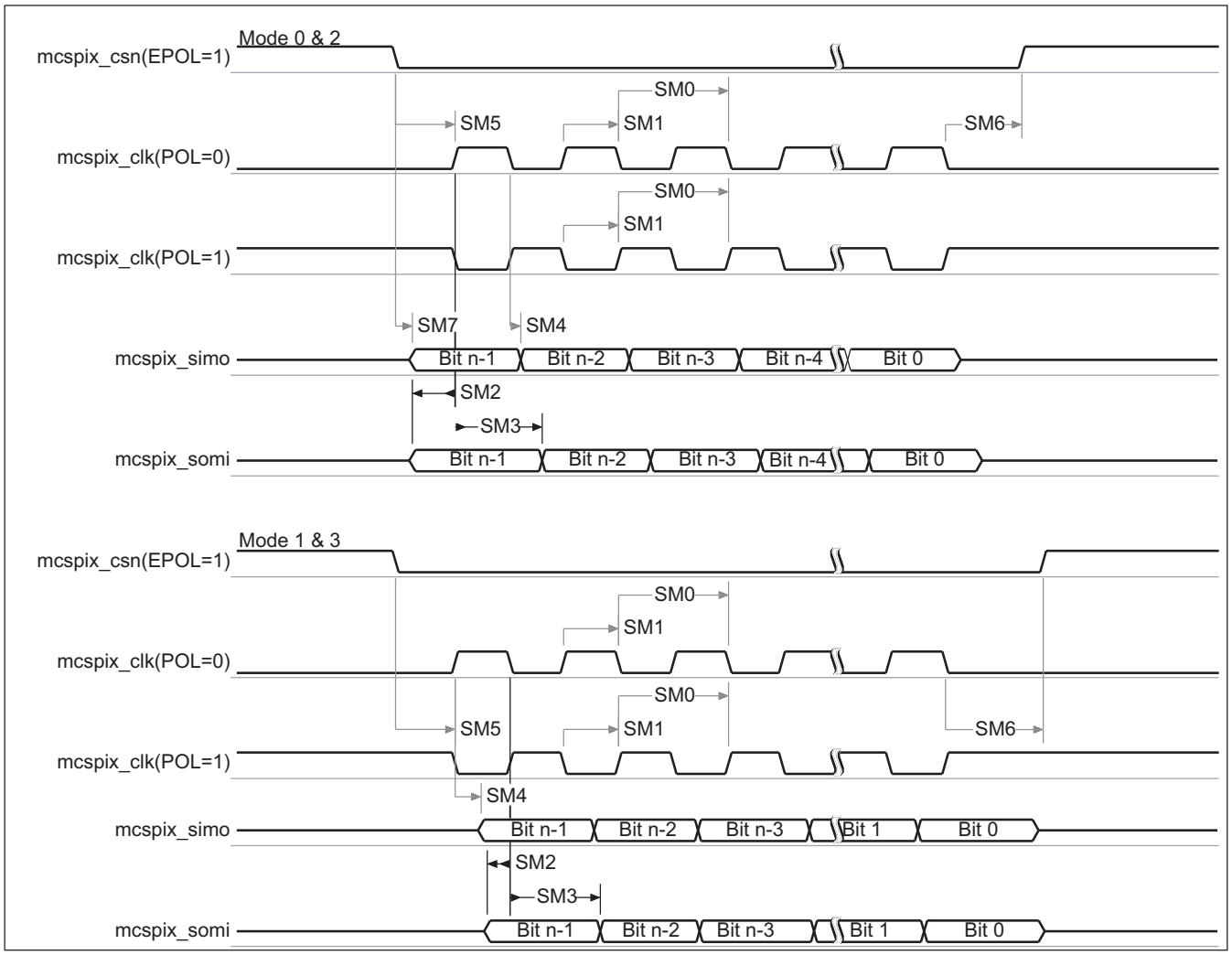

Figure 6-42. McSPI Interface – Transmit and Receive in Master Mode(1) (2) (3)

(1) The active clock edge (rising or falling) on which mcspix_simo is driven and mcspi_somi data is latched is software configurable with the bit MSPI_CHCONFx[0] = PHA and the bit MSPI_CHCONFx[1] = POL.

(2) The polarity of mcspix_csi is software configurable with the bit MSPI_CHCONFx[6] = EPOL.

(3) In mcspix, x is equal to 1. In mcspix_csn, n is equal to 0, 1, 2, or 3.

6.6.3 Multiport Full-Speed Universal Serial Bus (USB) Interface

The OMAP3530/25 processor provides three USB ports working in full- and low-speed data transactions (up to 12Mbit/s).

Connected to either a serial link controller (TLL modes) or a serial PHY (PHY interface modes) it supports:

- 6-pin (Tx: Dat/Se0 or Tx: Dp/Dm) unidirectional mode
- 4-pin bidirectional mode
- 3-pin bidirectional mode

6.6.3.1 Multiport Full-Speed Universal Serial Bus (USB) – Unidirectional Standard 6-pin Mode

Table 6-78 and Table 6-79 assume testing over the recommended operating conditions (see Figure 6-43).

Table 6-77. Low-/Full-Speed USB Timing Conditions – Unidirectional Standard 6-pin Mode

TIMING CONDITION PARAMETER		VALUE	UNIT
Input Conditions			
t_R	Input signal rise time	2.0	ns
t_F	Input signal fall time	2.0	ns
Output Conditions			
C_{LOAD}	Output load capacitance	15.0	pF

Table 6-78. Low-/Full-Speed USB Timing Requirements – Unidirectional Standard 6-pin Mode

NO.	PARAMETER		1.15 V		1.0 V		UNIT
			MIN	MAX	MIN	MAX	
FSU1	$t_{d(Vp,Vm)}$	Time duration, mmx_rxdp and mmx_rxdm low together during transition		14.0		14.0	ns
FSU2	$t_{d(Vp,Vm)}$	Time duration, mmx_rxdp and mmx_rxdm high together during transition		8.0		8.0	ns
FSU3	$t_{d(RCVU0)}$	Time duration, mmx_rrxcv undefine during a single end 0 (mmx_rxdp and mmx_rxdm low together)		14.0		14.0	ns
FSU4	$t_{d(RCVU1)}$	Time duration, mmx_rxrcv undefine during a single end 1 (mmx_rxdp and mmx_rxdm high together)		8.0		8.0	ns

Table 6-79. Low-/Full-Speed USB Switching Characteristics – Unidirectional Standard 6-pin Mode

NO.	PARAMETER		1.15 V		1.0 V		UNIT
			MIN	MAX	MIN	MAX	
FSU5	$t_{d(TXENL-DATV)}$	Delay time, mmx_txen_n low to mmx_txdat valid	81.8	84.8	81.8	84.8	ns
FSU6	$t_{d(TXENL-SE0V)}$	Delay time, mmx_txen_n low to mmx_txse0 valid	81.8	84.8	81.8	84.8	ns
FSU7	$t_{s(DAT-SE0)}$	Skew between mmx_txdat and mmx_txse0 transition		1.5		1.5	ns
FSU8	$t_{d(DATI-TXENH)}$	Delay time, mmx_txdat invalid to mmx_txen_n high	81.8		81.8		ns
FSU9	$t_{d(SE0I-TXENH)}$	Delay time, mmx_txse0 invalid to mmx_txen_n high	81.8		81.8		ns
	$t_{R(do)}$	Rise time, mmx_txen_n		4.0		4.0	ns
	$t_{F(do)}$	Fall time, mmx_txen_n		4.0		4.0	ns
	$t_{R(do)}$	Rise time, mmx_txdat		4.0		4.0	ns
	$t_{F(do)}$	Fall time, mmx_txdat		4.0		4.0	ns
	$t_{R(do)}$	Rise time, mmx_txse0		4.0		4.0	ns
	$t_{F(do)}$	Fall time, mmx_txse0		4.0		4.0	ns

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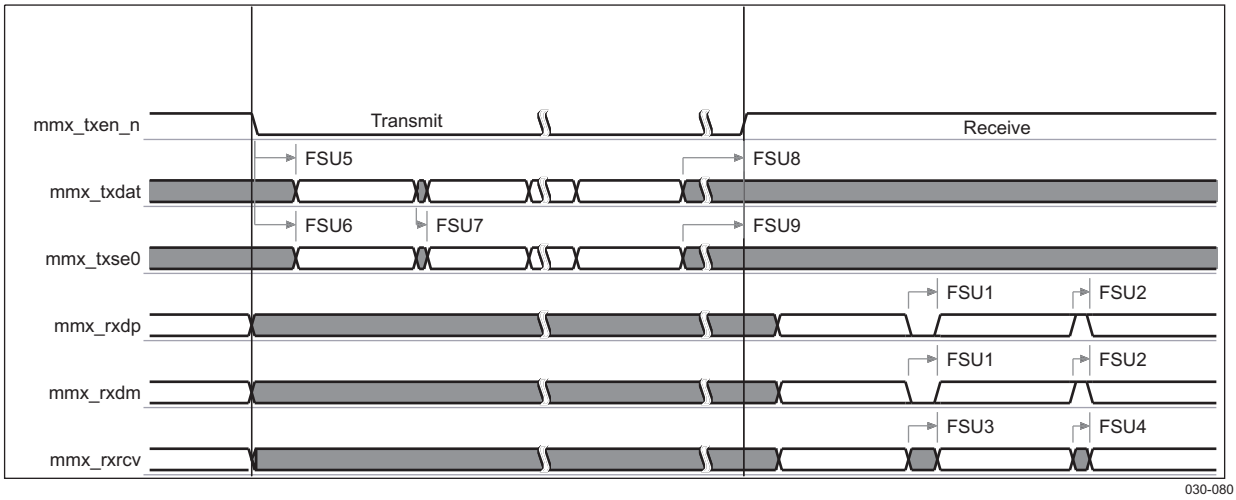

In mmx, x is equal to 0, 1, or 2.

Figure 6-43. Low-/Full-Speed USB – Unidirectional Standard 6-pin Mode

6.6.3.2 Multiport Full-Speed Universal Serial Bus (USB) – Bidirectional Standard 4-pin Mode

Table 6-81 and Table 6-82 assume testing over the recommended operating conditions (see Figure 6-44).

Table 6-80. Low-/Full-Speed USB Timing Conditions – Bidirectional Standard 4-pin Mode

TIMING CONDITION PARAMETER		VALUE	UNIT
Input Conditions			
t_R	Input signal rise time	2.0	ns
t_F	Input signal fall time	2.0	ns
Output Conditions			
C_{LOAD}	Output load capacitance	15.0	pF

Table 6-81. Low-/Full-Speed USB Timing Requirements – Bidirectional Standard 4-pin Mode

NO.	PARAMETER		1.15 V		1.0 V		UNIT
			MIN	MAX	MIN	MAX	
FSU10	$t_{d(DAT,SE0)}$	Time duration, mmx_txdat and mmx_txse0 low together during transition		14.0		14.0	ns
FSU11	$t_{d(DAT,SE0)}$	Time duration, mmx_txdat and mmx_txse0 high together during transition		8.0		8.0	ns
FSU12	$t_{d(RCVU0)}$	Time duration, mmx_rrxcv undefine during a single end 0 (mmx_txdat and mmx_txse0 low together)		14.0		14.0	ns
FSU13	$t_{d(RCVU1)}$	Time duration, mmx_rxrcv undefine during a single end 1 (mmx_txdat and mmx_txse0 high together)		8.0		8.0	ns

Table 6-82. Low-/Full-Speed USB Switching Characteristics – Bidirectional Standard 4-pin Mode

NO.	PARAMETER		1.15 V		1.0 V		UNIT
			MIN	MAX	MIN	MAX	
FSU14	$t_{d(TXENL-DATV)}$	Delay time, mmx_txen_n low to mmx_txdat valid	81.8	84.8	81.8	84.8	ns
FSU15	$t_{d(TXENL-SE0V)}$	Delay time, mmx_txen_n low to mmx_txse0 valid	81.8	84.8	81.8	84.8	ns
FSU16	$t_{s(DAT-SE0)}$	Skew between mmx_txdat and mmx_txse0 transition		1.5		1.5	ns
FSU17	$t_{d(DATV-TXENH)}$	Delay time, mmx_txdat invalid before mmx_txen_n high	81.8		81.8		ns

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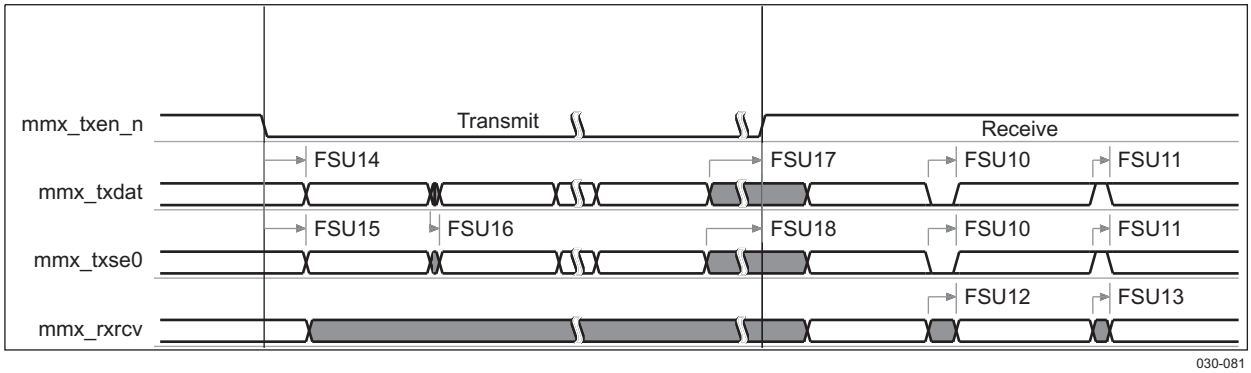
Table 6-82. Low-/Full-Speed USB Switching Characteristics – Bidirectional Standard 4-pin Mode (continued)

NO.	PARAMETER		1.15 V		1.0 V		UNIT
			MIN	MAX	MIN	MAX	
FSU18	$t_{d(SE0V-TXENH)}$	Delay time, mmx_txse0 invalid before mmx_txen_n high	81.8		81.8		ns
	$t_{R(txen)}$	Rise time, mmx_txen_n		4.0		4.0	ns
	$t_{F(txen)}$	Fall time, mmx_txen_n		4.0		4.0	ns
	$t_{R(dat)}$	Rise time, mmx_txdat		4.0		4.0	ns
	$t_{F(dat)}$	Fall time, mmx_txdat		4.0		4.0	ns
	$t_{R(se0)}$	Rise time, mmx_txse0		4.0		4.0	ns
	$t_{F(se0)}$	Fall time, mmx_txse0		4.0		4.0	ns



In mmx, x is equal to 0, 1, or 2.

Figure 6-44. Low-/Full-Speed USB – Bidirectional Standard 4-pin Mode

6.6.3.3 Multiport Full-Speed Universal Serial Bus (USB) – Bidirectional Standard 3-pin Mode

Table 6-84 and Table 6-85 assume testing over the recommended operating conditions below (see Figure 6-45).

Table 6-83. Low-/Full-Speed USB Timing Conditions – Bidirectional Standard 3-pin Mode

TIMING CONDITION PARAMETER		VALUE	UNIT
Input Conditions			
t_R	Input signal rise time	2.0	ns
t_F	Input signal fall time	2.0	ns
Output Conditions			
C_{LOAD}	Output load capacitance	15.0	pF

Table 6-84. Low-/Full-Speed USB Timing Requirements – Bidirectional Standard 3-pin Mode

NO.	PARAMETER		1.15 V		1.0 V		UNIT
			MIN	MAX	MIN	MAX	
FSU19	$t_{d(DAT,SE0)}$	Time duration, mmx_txdat and mmx_txse0 low together during transition		14.0		14.0	ns
FSU20	$t_{d(DAT,SE0)}$	Time duration, mmx_tsdat and mmx_txse0 high together during transition		8.0		8.0	ns

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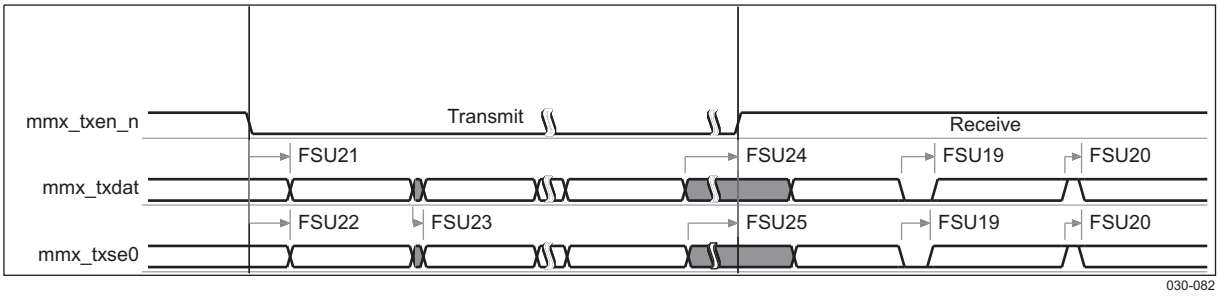
Table 6-85. Low-/Full-Speed USB Switching Characteristics – Bidirectional Standard 3-pin Mode

NO.	PARAMETER		1.15 V		1.0 V		UNIT
			MIN	MAX	MIN	MAX	
FSU21	$t_{d(TXENL-DATV)}$	Delay time, mmx_txen_n low to mmx_txdat valid	81.8	84.8	81.8	84.8	ns
FSU22	$t_{d(TXENL-SE0V)}$	Delay time, mmx_txen_n low to mmx_txse0 valid	81.8	84.8	81.8	84.8	ns
FSU23	$t_{s(DAT-SE0)}$	Skew between mmx_txdat and mmx_txse0 transition		1.5		1.5	ns
FSU24	$t_{d(DATI-TXENH)}$	Delay time, mmx_txdat invalid to mmx_txen_n high	81.8		81.8		ns
FSU25	$t_{d(SE0I-TXENH)}$	Delay time, mmx_txse0 invalid to mmx_txen_n high	81.8		81.8		ns
	$t_{R(do)}$	Rise time, mmx_txen_n		4.0		4.0	ns
	$t_{F(do)}$	Fall time, mmx_txen_n		4.0		4.0	ns
	$t_{R(do)}$	Rise time, mmx_txdat		4.0		4.0	ns
	$t_{F(do)}$	Fall time, mmx_txdat		4.0		4.0	ns
	$t_{R(do)}$	Rise time, mmx_txse0		4.0		4.0	ns
	$t_{F(do)}$	Fall time, mmx_txse0		4.0		4.0	ns



In mmx, x is equal to 0, 1, or 2.

Figure 6-45. Low-/Full-Speed USB – Bidirectional Standard 3-pin Mode

6.6.3.4 Multiport Full-Speed Universal Serial Bus (USB) – Unidirectional TLL 6-pin Mode

Table 6-87 and Table 6-88 assume testing over the recommended operating conditions (see Figure 6-46).

Table 6-86. Low-/Full-Speed USB Timing Conditions – Unidirectional TLL 6-pin Mode

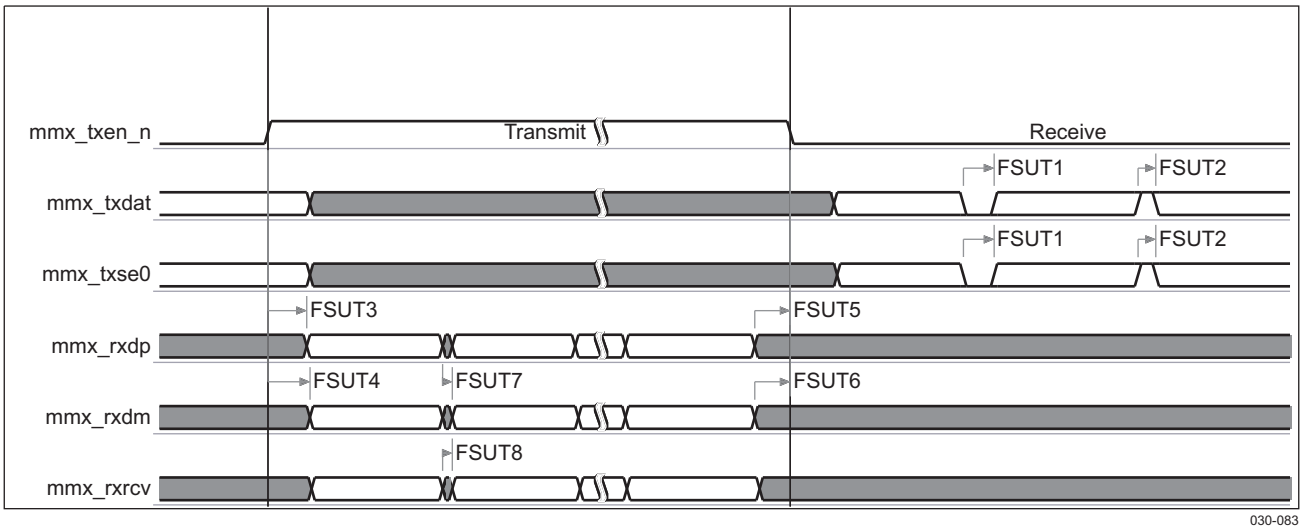
TIMING CONDITION PARAMETER		VALUE	UNIT
Input Conditions			
t_R	Input signal rise time	2	ns
t_F	Input signal fall time	2	ns
Output Conditions			
C_{LOAD}	Output load capacitance	15	pF

Table 6-87. Low-/Full-Speed USB Timing Requirements – Unidirectional TLL 6-pin Mode

NO.	PARAMETER		1.15 V		1.0 V		UNIT
			MIN	MAX	MIN	MAX	
FSUT1	$t_{d(SE0,DAT)}$	Time duration, mmx_txse0 and mmx_txdat low together during transition		14		14	ns
FSUT2	$t_{d(SE0,DAT)}$	Time duration, mmx_txse0 and mmx_txdat high together during transition		8		8	ns

Table 6-88. Low-/Full-Speed USB Switching Characteristics – Unidirectional TLL 6-pin Mode

NO.	PARAMETER		1.15 V		1.0 V		UNIT
			MIN	MAX	MIN	MAX	
FSUT3	$t_{d(TXENH-DPV)}$	Delay time, mmx_txen_n high to mmx_rxdp valid	81.8	84.8	81.8	84.8	ns
FSUT4	$t_{d(TXENH-DMV)}$	Delay time, mmx_txen_n high to mmx_rxdm valid	81.8	84.8	81.8	84.8	ns
FSUT5	$t_{d(DPI-TXENL)}$	Delay time, mmx_rxdp invalid mmx_txen_n low	81.8		81.8		ns
FSUT6	$t_{d(DMI-TXENL)}$	Delay time, mmx_rxdm invalid mmx_txen_n low	81.8		81.8		ns
FSUT7	$t_{s(DP-DM)}$	Skew between mmx_rxdp and mmx_rxdm transition		1.5		1.5	ns
FSUT8	$t_{s(DP,DM-RCV)}$	Skew between mmx_rxdp, mmx_rxdm, and mmx_rxrcv transition		1.5		1.5	ns
	$t_{R(rxrcv)}$	Rise time, mmx_rxrcv		4		4	ns
	$t_{F(rxrcv)}$	Fall time, mmx_rxrcv		4		4	ns
	$t_{R(dp)}$	Rise time, mmx_rxdp		4		4	ns
	$t_{F(dp)}$	Fall time, mmx_rxdp		4		4	ns
	$t_{R(dm)}$	Rise time, mmx_rxdm		4		4	ns
	$t_{F(dm)}$	Fall time, mmx_rxdm		4		4	ns



In mmx, x is equal to 0, 1, or 2.

Figure 6-46. Low-/Full-Speed USB – Unidirectional TLL 6-pin Mode

6.6.3.5 Multiport Full-Speed Universal Serial Bus (USB) – Bidirectional TLL 4-pin Mode

Table 6-90 and Table 6-91 assume testing over the recommended operating conditions (see Figure 6-47).

Table 6-89. Low-/Full-Speed USB Timing Conditions – Bidirectional TLL 4-pin Mode

TIMING CONDITION PARAMETER		VALUE	UNIT
Input Conditions			
t_R	Input signal rise time	2	ns
t_F	Input signal fall time	2	ns
Output Conditions			
C_{LOAD}	Output load capacitance	15	pF

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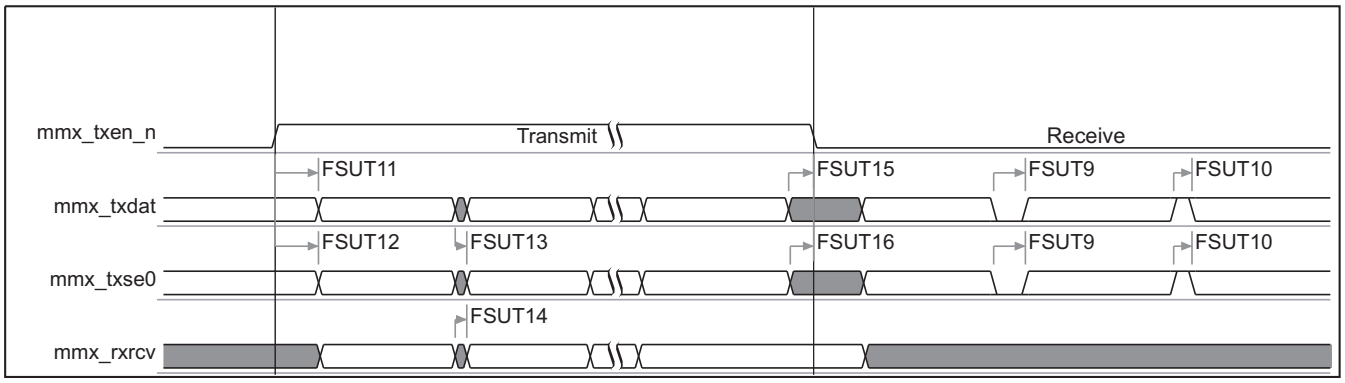
Table 6-90. Low-/Full-Speed USB Timing Requirements – Bidirectional TLL 4-pin Mode

NO.	PARAMETER		1.15 V		1.0 V		UNIT
			MIN	MAX	MIN	MAX	
FSUT9	$t_{d(DAT,SE0)}$	Time duration, mmx_txdat and mmx_txse0 low together during transition		14		14	ns
FSUT10	$t_{d(DAT,SE0)}$	Time duration, mmx_tsdat and mmx_txse0 high together during transition		8		8	ns

Table 6-91. Low-/Full-Speed USB Switching Characteristics – Bidirectional TLL 4-pin Mode

NO.	PARAMETER		1.15 V		1.0 V		UNIT
			MIN	MAX	MIN	MAX	
FSUT11	$t_{d(TXENL-DATV)}$	Delay time, mmx_txen_n active to mmx_txdat valid	81.8	84.8	81.8	84.8	ns
FSUT12	$t_{d(TXENL-SE0V)}$	Delay time, mmx_txen_n active to mmx_txse0 valid	81.8	84.8	81.8	84.8	ns
FSUT13	$t_{s(DAT-SE0)}$	Skew between mmx_txdat and mmx_txse0 transition		1.5		1.5	ns
FSUT14	$t_{s(DP,DM-RCV)}$	Skew between mmx_rxdp, mmx_rxdm, and mmx_rxrcv transition		1.5		1.5	ns
FSUT15	$t_{d(DATI-TXENL)}$	Delay time, mmx_txse0 invalid to mmx_txen_n Low	81.8		81.8		ns
FSUT16	$t_{d(SE0I-TXENL)}$	Delay time, mmx_txdat invalid to mmx_txen_n Low	81.8		81.8		ns
	$t_{R(rcv)}$	Rise time, mmx_rxrcv		4		4	ns
	$t_{F(rcv)}$	Fall time, mmx_rxrcv		4		4	ns
	$t_{R(dat)}$	Rise time, mmx_txdat		4		4	ns
	$t_{F(dat)}$	Fall time, mmx_txdat		4		4	ns
	$t_{R(se0)}$	Rise time, mmx_txse0		4		4	ns
	$t_{F(se0)}$	Fall time, mmx_txse0		4		4	ns



In mmx, x is equal to 0, 1, or 2.

Figure 6-47. Low-/Full-Speed USB – Bidirectional TLL 4-pin Mode

6.6.3.6 Multiport Full-Speed Universal Serial Bus (USB) – Bidirectional TLL 3-pin Mode

Table 6-93 and Table 6-94 assume testing over the recommended operating conditions (see Figure 6-48).

Table 6-92. Low-/Full-Speed USB Timing Conditions – Bidirectional TLL 3-pin Mode

TIMING CONDITION PARAMETER		VALUE	UNIT
Input Conditions			
t_R	Input signal rise time	2	ns
t_F	Input signal fall time	2	ns
Output Conditions			

Table 6-92. Low-/Full-Speed USB Timing Conditions – Bidirectional TLL 3-pin Mode (continued)

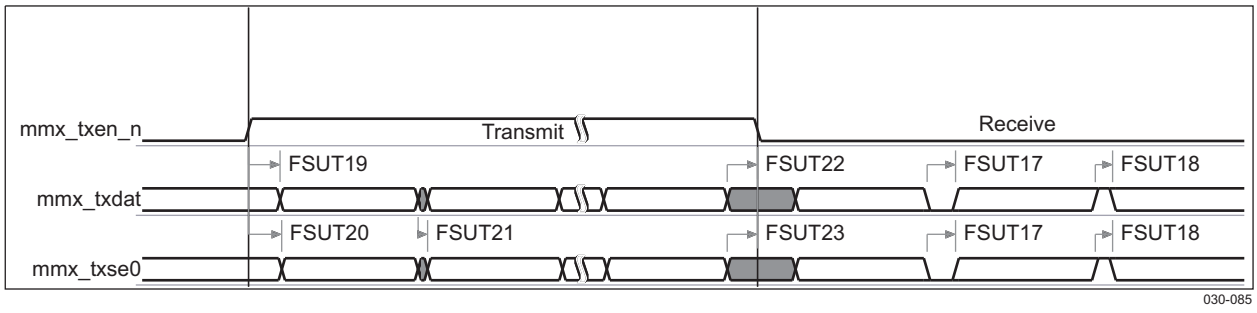
TIMING CONDITION PARAMETER		VALUE	UNIT
C_{LOAD}	Output load capacitance	15	pF

Table 6-93. Low-/Full-Speed USB Timing Requirements – Bidirectional TLL 3-pin Mode

NO.	PARAMETER		1.15 V		1.0 V		UNIT
			MIN	MAX	MIN	MAX	
FSUT17	$t_{d(DAT,SE0)}$	Time duration, mmx_txdat and mmx_txse0 low together during transition		14		14	ns
FSUT18	$t_{d(DAT,SE0)}$	Time duration, mmx_tsdat and mmx_txse0 high together during transition		8		8	ns

Table 6-94. Low-/Full-Speed USB Switching Characteristics – Bidirectional TLL 3-pin Mode

NO.	PARAMETER		1.15 V		1.0 V		UNIT
			MIN	MAX	MIN	MAX	
FSUT19	$t_{d(TXENH-DATV)}$	Delay time, mmx_txen_n high to mmx_txdat valid	81.8	84.8	81.8	84.8	ns
FSUT20	$t_{d(TXENH-SE0V)}$	Delay time, mmx_txen_n high to mmx_txse0 valid	81.8	84.8	81.8	84.8	ns
FSUT21	$t_{s(DAT-SE0)}$	Skew between mmx_txdat and mmx_txse0 transition		1.5		1.5	ns
FSUT22	$t_{d(DATI-TXENL)}$	Delay time, mmx_txdat invalid mmx_txen_n low	81.8		81.8		ns
FSUT23	$t_{d(SE0I-TXENL)}$	Delay time, mmx_txse0 invalid mmx_txen_n low	81.8		81.8		ns
	$t_{R(dat)}$	Rise time, mmx_txdat		4		4	ns
	$t_{F(dat)}$	Fall time, mmx_txdat		4		4	ns
	$t_{R(se0)}$	Rise time, mmx_txse0		4		4	ns
	$t_{F(se0)}$	Fall time, mmx_txse0		4		4	ns
	$t_{R(do)}$	Rise time, mmx_txse0		4		4	ns
	$t_{F(do)}$	Fall time, mmx_txse0		4		4	ns



In mmx, x is equal to 0, 1, or 2.

Figure 6-48. Low-/Full-Speed USB – Bidirectional TLL 3-pin Mode

6.6.4 Multiport High-Speed Universal Serial Bus (USB) Timing

In addition to the full-speed USB controller, a high-speed (HS) USB OTG controller is instantiated inside OMAP3530/25. It allows high-speed transactions (up to 480 Mbit/s) on the USB ports 0, 1, 2, and 3.

- Port 0:
  - 12-bit slave mode (SDR)
- Port 1 and port 2:
  - 12-bit master mode (SDR)
  - 12-bit TLL master mode (SDR)
  - 8-bit TLL master mode (DDR)

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- Port 3:
  - 12-bit TLL master mode (SDR)
  - 8-bit TLL master mode (DDR)

6.6.4.1 High-Speed Universal Serial Bus (USB) on Port 0 – 12-bit Slave Mode

Table 6-96 and Table 6-97 assume testing over the recommended operating conditions (see Figure 6-49).

Table 6-95. High-Speed USB Timing Conditions – 12-bit Slave Mode

TIMING CONDITION PARAMETER		VALUE	UNIT
Input Conditions			
t_r	Input Signal Rising Time	2.00	ns
t_f	Input Signal Falling Time	2.00	ns
Output Conditions			
C_{load}	Output Load Capacitance	3.50	pF

Table 6-96. High-Speed USB Timing Requirements – 12-bit Slave Mode(1)

NO.	PARAMETER		1.15 V		UNIT
			MIN	MAX	
HSU0	$f_{p(CLK)}$	hsusb0_clk clock frequency(2) (3)		60.03	MHz
	$t_{j(CLK)}$	Cycle Jitter(3), hsusb0_clk		500.00	ps
HSU3	$t_{s(DIRV-CLKH)}$	Setup time, hsusb0_dir valid before hsusb0_clk rising edge	6.7		ns
	$t_{s(NXTV-CLKH)}$	Setup time, hsusb0_nxt valid before hsusb0_clk rising edge	6.7		ns
HSU4	$t_{h(CLKH-DIRIV)}$	Hold time, hsusb0_dir valid after hsusb0_clk rising edge	0.0		ns
	$t_{h(CLKH-NXT/IV)}$	Hold time, hsusb0_nxt valid after hsusb0_clk rising edge	0.0		ns
HSU5	$t_{s(DATAV-CLKH)}$	Setup time, hsusb0_data[0:7] valid before hsusb0_clk rising edge	6.7		ns
HSU6	$t_{h(CLKH-DATIV)}$	Hold time, hsusb0_data[0:7] valid after hsusb0_clk rising edge	0.0		ns

(1) The timing requirements are assured for the cycle jitter error condition specified.
(2) Related with the input maximum frequency supported by the I/F module.
(3) Maximum cycle jitter supported by clk input clock.

Table 6-97. High-Speed USB Switching Characteristics – 12-bit Slave Mode

NO.	PARAMETER		1.15 V		UNIT
			MIN	MAX	
HSU1	$t_{d(clkL-STPV)}$	Delay time, hsusb0_clk high to output usb0_stp valid		9.0	ns
	$t_{d(clkL-STPIV)}$	Delay time, hsusb0_clk high to output usb0_stp invalid	0.5		ns
HSU2	$t_{d(clkL-DV)}$	Delay time, hsusb0_clk high to output hsusb0_data[0:7] valid		9.0	ns
	$t_{d(clkL-DIV)}$	Delay time, hsusb0_clk high to output hsusb0_data[0:7] invalid	0.5		ns
	$t_{r(do)}$	Rising time, output signals		2.0	ns
	$t_{f(do)}$	Falling time, output signals		2.0	ns

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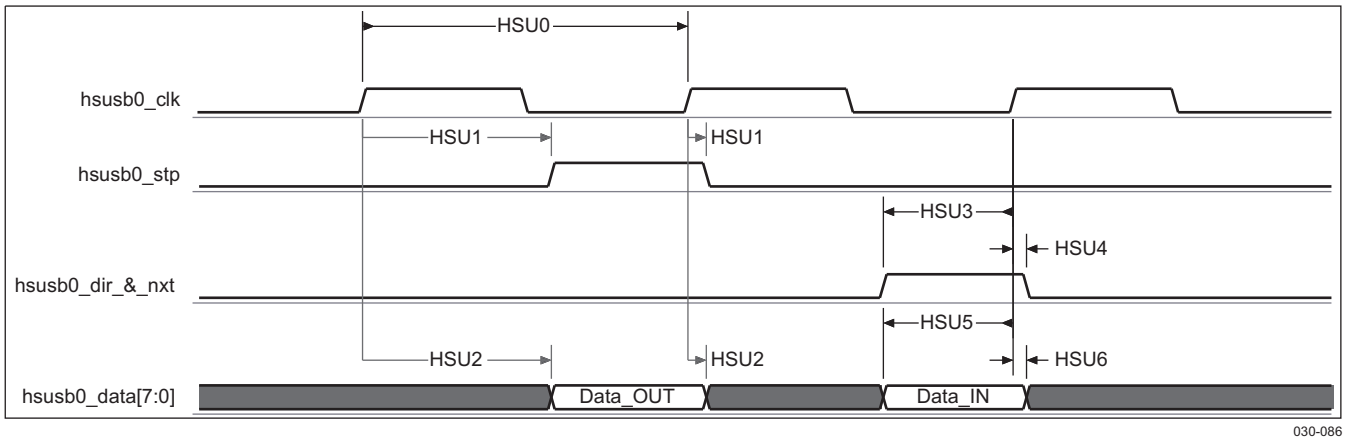

Figure 6-49. High-Speed USB – 12-bit Slave Mode

6.6.4.2 High-Speed Universal Serial Bus (USB) on Ports 1 and 2 – 12-bit Master Mode

Table 6-99 and Table 6-100 assume testing over the recommended operating conditions (see Figure 6-50).

Table 6-98. High-Speed USB Timing Conditions – 12-bit Master Mode

TIMING CONDITION PARAMETER		VALUE	UNIT
Input Conditions			
t_R	Input signal rise time	2	ns
t_F	Input signal fall time	2	ns
Output Conditions			
C_{LOAD}	Output load capacitance	3	pF

Table 6-99. High-Speed USB Timing Requirements – 12-bit Master Mode(1)

NO.	PARAMETER		1.15 V		UNIT
			MIN	MAX	
HSU3	$t_{s(DIRV-CLKH)}$	Setup time, hsusbx_dir valid before hsusbx_clk rising edge	9.3		ns
	$t_{s(NXTV-CLKH)}$	Setup time, hsusbx_nxt valid before hsusbx_clk rising edge	9.3		ns
HSU4	$t_{h(CLKH-DIRIV)}$	Hold time, hsusbx_dir valid after hsusbx_clk rising edge	0.2		ns
	$t_{h(CLKH-NXT/IV)}$	Hold time, hsusbx_nxt valid after hsusbx_clk rising edge	0.2		ns
HSU5	$t_{s(DATAV-CLKH)}$	Setup time, hsusbx_data[0:7] valid before hsusbx_clk rising edge	9.3		ns
HSU6	$t_{h(CLKH-DATIV)}$	Hold time, hsusbx_data[0:7] valid after hsusbx_clk rising edge	0.2		ns

(1) In hsusbx, x is equal to 1 or 2.

Table 6-100. High-Speed USB Switching Characteristics – 12-bit Master Mode(1)

N O.	PARAMETER		1.15 V		UNIT
			MIN	MAX	
HSU0	$f_{p(CLK)}$	hsusbx_clk clock frequency		60	MHz
	$t_{j(CLK)}$	Jitter standard deviation(2), hsusbx_clk		200	ps
HSU1	$t_{d(clkL-STPV)}$	Delay time, hsusbx_clk high to output hsusbx_stp valid		13	ns
	$t_{d(clkL-STPIV)}$	Delay time, hsusbx_clk high to output hsusbx_stp invalid	2		ns
HSU2	$t_{d(clkL-DV)}$	Delay time, hsusbx_clk high to output hsusbx_data[0:7] valid		13	ns

(1) In hsusbx, x is equal to 1 or 2.
(2) The jitter probability density can be approximated by a Gaussian function.

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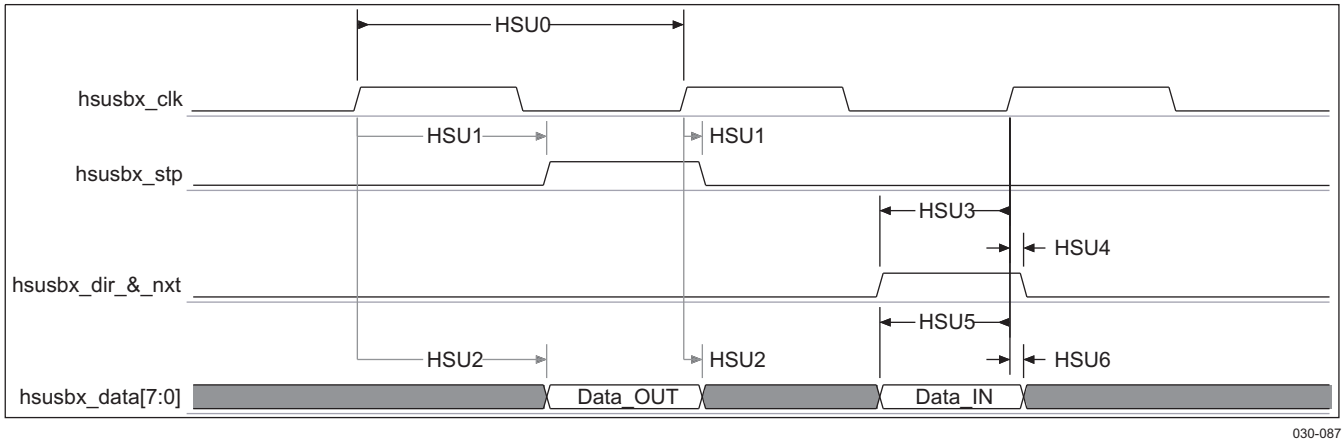
Table 6-100. High-Speed USB Switching Characteristics – 12-bit Master Mode[1] (continued)

N O.	PARAMETER		1.15 V		UNIT
			MIN	MAX	
	$t_{d(clkL-DIV)}$	Delay time, hsusbx_clk high to output hsusbx_data[0:7] invalid	2		ns
	$t_{R(do)}$	Rise time, output signals		2	ns
	$t_{F(do)}$	Fall time, output signals		2	ns



In hsusbx, x is equal to 1 or 2.

Figure 6-50. High-Speed USB – 12-bit Master Mode

6.6.4.3 High-Speed Universal Serial Bus (USB) on Ports 1, 2, and 3 – 12-bit TLL Master Mode

Table 6-102 and Table 6-103 assume testing over the recommended operating conditions (see Figure 6-51).

Table 6-101. High-Speed USB Timing Conditions – 12-bit TLL Master Mode

TIMING CONDITION PARAMETER		VALUE	UNIT
Input Conditions			
t_R	Input signal rise time	2	ns
t_F	Input signal fall time	2	ns
Output Conditions			
C_{LOAD}	Output load capacitance	3	pF

Table 6-102. High-Speed USB Timing Requirements – 12-bit TLL Master Mode[1]

NO.	PARAMETER		1.15 V		UNIT
			MIN	MAX	
HSU2	$t_{s(STPV-CLKH)}$	Setup time, hsusbx_tll_stp valid before hsusbx_tll_clk rising edge	6		ns
HSU3	$t_{s(CLKH-STPIV)}$	Hold time, hsusbx_tll_stp valid after hsusbx_tll_clk rising edge	0		ns
HSU4	$t_{s(DATAV-CLKH)}$	Setup time, hsusbx_tll_data[7:0] valid before hsusbx_tll_clk rising edge	6		ns
HSU5	$t_{h(CLKH-DATIV)}$	Hold time, hsusbx_tll_data[7:0] valid after hsusbx_tll_clk rising edge	0		ns

(1) In hsusbx, x is equal to 1, 2, or 3.

Table 6-103. High-Speed USB Switching Characteristics – 12-bit TLL Master Mode[1]

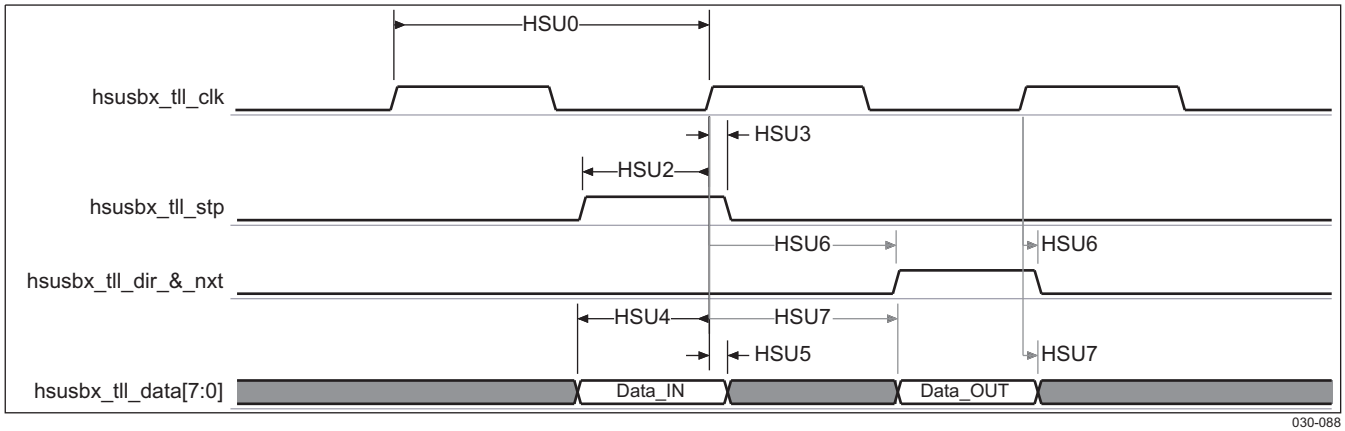
NO.	PARAMETER		1.15 V		UNIT
			MIN	MAX	
HSU0	$f_{p(CLK)}$	hsusbx_tll_clk clock frequency		60	MHz

(1) In hsusbx, x is equal to 1, 2, or 3.

Table 6-103. High-Speed USB Switching Characteristics – 12-bit TLL Master Mode[1] (continued)

NO.	PARAMETER		1.15 V		UNIT
			MIN	MAX	
	$t_{j(CLK)}$	Jitter standard deviation[2], hsusbx_tll_clk		200	ps
HSU6	$t_{d(CLKL-DIRV)}$	Delay time, hsusbx_tll_clk high to output hsusbx_tll_dir valid		9	ns
	$t_{d(CLKL-DIRIV)}$	Delay time, hsusbx_tll_clk high to output hsusbx_tll_dir invalid	0		ns
	$t_{d(CLKL-NXTV)}$	Delay time, hsusbx_tll_clk high to output hsusbx_tll_nxt valid		9	ns
	$t_{d(CLKL-NXTIV)}$	Delay time, hsusbx_tll_clk high to output hsusbx_tll_nxt invalid	0		ns
HSU7	$t_{d(CLKL-DV)}$	Delay time, hsusbx_tll_clk high to output hsusbx_tll_data[7:0] valid		9	ns
	$t_{d(CLKL-DIV)}$	Delay time, hsusbx_tll_clk high to output hsusbx_tll_data[7:0] invalid	0		ns
	$t_{R(do)}$	Rise time, output signals		2	ns
	$t_{F(do)}$	Fall time, output signals		2	ns

(2) The jitter probability density can be approximated by a Gaussian function.



In hsusbx, x is equal to 1, 2, or 3.

Figure 6-51. High-Speed USB – 12-bit TLL Master Mode

6.6.4.4 High-Speed Universal Serial Bus (USB) on Ports 1, 2, and 3 – 8-bit TLL Master Mode

Table 6-105 and Table 6-106 assume testing over the recommended operating conditions (see Figure 6-52).

Table 6-104. High-Speed USB Timing Conditions – 8-bit TLL Master Mode

TIMING CONDITION PARAMETER		VALUE	UNIT
Input Conditions			
t_R	Input signal rise time	2	ns
t_F	Input signal fall time	2	ns
Output Conditions			
C_{LOAD}	Output load capacitance	3	pF

Table 6-105. High-Speed USB Timing Requirements – 8-bit TLL Master Mode[1]

NO.	PARAMETER		1.15 V		UNIT
			MIN	MAX	
HSU2	$t_{s(STPV-CLKH)}$	Setup time, hsusbx_tll_stp valid before hsusbx_tll_clk rising edge	6		ns
HSU3	$t_{s(CLKH-STPIV)}$	Hold time, hsusbx_tll_stp valid after hsusbx_tll_clk rising edge	0		ns
HSU4	$t_{s(DATAV-CLKH)}$	Setup time, hsusbx_tll_data[3:0] valid before hsusbx_tll_clk rising edge	3		ns
HSU5	$t_{h(CLKH-DATIV)}$	Hold time, hsusbx_tll_data[3:0] valid after hsusbx_tll_clk rising edge	–0.8		ns

(1) In hsusbx, x is equal to 1, 2, or 3.

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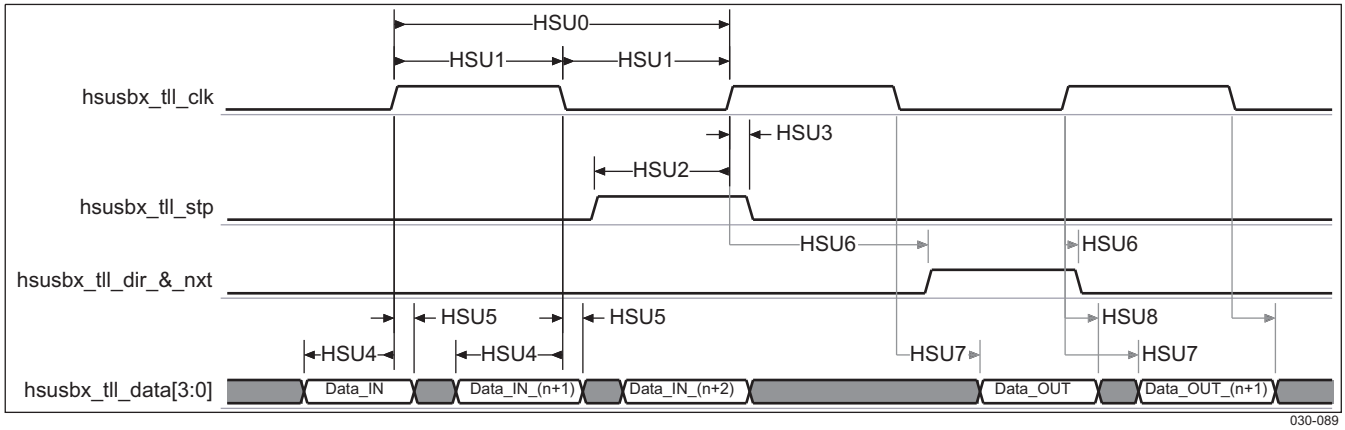
Table 6-106. High-Speed USB Switching Characteristics – 8-bit TLL Master Mode(1)

NO.	PARAMETER		1.15 V		UNIT
			MIN	MAX	
HSU0	$f_{p(CLK)}$	hsusbx_tll_clk clock frequency		60	MHz
	$t_{j(CLK)}$	Jitter standard deviation(2), hsusbx_tll_clk		200	ps
HSU1	$t_{j(CLK)}$	Duty cycle, hsusbx_tll_clk pulse duration (low and high)	47.6%	52.4%	
HSU6	$t_{d(CLKL-DIRV)}$	Delay time, hsusbx_tll_clk high to output hsusbx_tll_dir valid		9	ns
	$t_{d(CLKL-DIRIV)}$	Delay time, hsusbx_tll_clk high to output hsusbx_tll_dir invalid	0		ns
	$t_{d(CLKL-NXTV)}$	Delay time, hsusbx_tll_clk high to output hsusbx_tll_nxt valid		9	ns
	$t_{d(CLKL-NXTIV)}$	Delay time, hsusbx_tll_clk high to output hsusbx_tll_nxt invalid	0		ns
HSU7	$t_{d(CLKL-DV)}$	Delay time, hsusbx_tll_clk high to output hsusbx_tll_data[3:0] valid		4	ns
HSU8	$t_{d(CLKL-DIV)}$	Delay time, hsusbx_tll_clk high to output hsusbx_tll_data[3:0] invalid	0		ns
	$t_{R(do)}$	Rise time, output signals		2	ns
	$t_{F(do)}$	Fall time, output signals		2	ns

(1) In hsusbx, x is equal to 1, 2, or 3.
(2) The jitter probability density can be approximated by a Gaussian function.



In hsusbx, x is equal to 1, 2, or 3.

Figure 6-52. High-Speed USB – 8-bit TLL Master Mode

6.6.5 I²C Interface

The multimaster I²C peripheral provides an interface between two or more devices via an I²C serial bus. The I²C controller supports the multimaster mode which allows more than one device capable of controlling the bus to be connected to it. Each I²C device is recognized by a unique address and can operate as either transmitter or receiver, according to the function of the device. In addition to being a transmitter or receiver, a device connected to the I²C bus can also be considered as master or slave when performing data transfers. This data transfer is carried out via two serial bidirectional wires:

- An SDA data line
- An SCL clock line

The following sections illustrate the data transfer is in master or slave configuration with 7-bit addressing format. The I²C interface is compliant with Philips I²C specification version 2.1. It supports standard mode (up to 100K bits/s), fast mode (up to 400K bits/s) and high-speed mode (up to 3.4Mb/s) .

6.6.5.1 I²C Standard/Fast-Speed Mode

Table 6-107. I²C Standard/Fast-Speed Mode Timings

NO.	PARAMETER(1)		Standard Mode		Fast Mode		UNIT
			MIN	MAX	MIN	MAX	
	f_{SCL}	Clock Frequency, i2cX_scl		100		400	kHz
I1	$t_{w(SCLH)}$	Pulse Duration, i2cX_scl high	4		0.6		µs
I2	$t_{w(SCLL)}$	Pulse Duration, i2cX_scl low	4.7		1.3		µs
I3	$t_{su(SDAV-SCLH)}$	Setup time, i2cX_sda valid before i2cX_scl active level	250		100(2)		ns
I4	$t_{h(SCLH–SDAV)}$	Hold time, i2cX_sda valid after i2cX_scl active level	0(3)	3.45(4)	0(3)	0.9(4)	µs
I5	$t_{su(SDAL-SCLH)}$	Setup time, i2cX_scl high after i2cX_sda low (for a START(5) condition or a repeated START condition)	4.7		0.6		µs
I6	$t_{h(SCLH–SDAH)}$	Hold time, i2cX_sda low level after i2cX_scl high level (STOP condition)	4		0.6		µs
I7	$t_{h(SCLH–RSTART)}$	Hold time, i2cX_sda low level after i2cX_scl high level (for a repeated START condition)	4		0.6		µs
I8	$t_{w(SDAH)}$	Pulse duration, i2cX_sda high between STOP and START conditions	4.7		1.3		µs
	$t_{R(SCL)}$	Rise time, i2cX_scl		1000		300	ns
	$t_{F(SCL)}$	Fall time, i2cX_scl		300		300	ns
	$t_{R(SDA)}$	Rise time, i2cX_sda		1000		300	ns
	$t_{F(SDA)}$	Fall time, i2cX_sda		300		300	ns
	CB	Capacitive load for each bus line		60(6)		60(6)	pF

(1) In i2cX, X is equal to 1, 2, 3, or 4. Note that I2C4 is master transmitter only.
(2) A fast-mode I²C-bus device can be used in a standard-mode I²C-bus system, but the requirement $t_{su(SDAV-SCLH)} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the low period of the i2cx_scl. If such a device does stretch the low period of the i2cx_scl, it must output the next data bit to the i2cx_sda line $t_{r(SDA)}$ max + $t_{su(SDAV-SCLH)}$ = 1000 + 250 = 1250 ns (according to the standard-mode I²C-bus specification) before the i2cx_scl line is released.
(3) The device provides (via the I²C bus) a hold time of at least 300 ns for the i2cx_sda signal (see the fall and rise time of i2cx_scl) to bridge the undefined region of the falling edge of i2cx_scl.
(4) The maximum $t_{h(SCLH-SDA)}$ has only to be met if the device does not stretch the low period of the i2cx_scl signal.
(5) After this time, the first clock is generated.
(6) Maximum reference load for i2c4_scl and i2c4_sda is CB = 15 pF.

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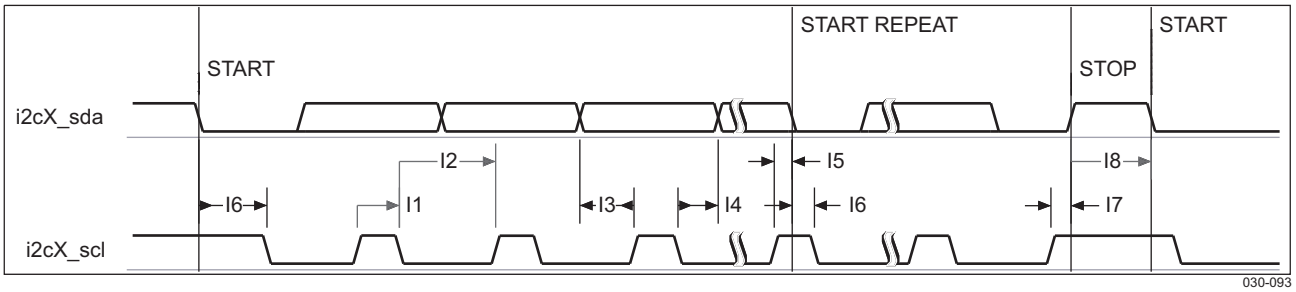

Figure 6-53. I²C – Standard/Fast Mode

6.6.5.2 I²C High-Speed Mode

Table 6-108. I²C HighSpeed Mode Timings(1) (2)

NO.	PARAMETER		CB = 100 pF MAX		CB = 400 pF MAX		UNIT
			MIN	MAX	MIN	MAX	
	f_{SCL}	Clock frequency, i2cX_scl		3.4		1.7	MHz
I1	$t_{w(SCLH)}$	Pulse duration, i2cX_scl high	60(3)		120(3)		µs
I2	$t_{w(SCLL)}$	Pulse duration, i2cX_scl low	160(3)		320(3)		µs
I3	$t_{su(SDAV-SCLH)}$	Setup time, i2cX_sda valid before i2cX_scl active level	10		10		ns
I4	$t_{h(SCLH–SDAV)}$	Hold time, i2cX_sda valid after i2cX_scl active level	0(2)	70	0(2)	150	µs
I5	$t_{su(SDAL-SCLH)}$	Setup time, i2cX_scl high after i2cX_sda low (for a START(4) condition or a repeated START condition)	160		160		µs
I6	$t_{h(SCLH–SDAH)}$	Hold time, i2cX_sda low level after i2cX_scl high level (STOP condition)	160		160		µs
I7	$t_{h(SCLH–RSTART)}$	Hold time, i2cX_sda low level after i2cX_scl high level (for a repeated START condition)	160		160		ns
	$t_{R(SCL)}$	Rise time, i2cX_scl		40		80	ns
	$t_{R(SCL)}$	Rise time, i2cX_scl after a repeated START condition and after a bit acknowledge		80		160	ns
	$t_{F(SCL)}$	Fall time, i2cX_scl		40		80	ns
	$t_{R(SDA)}$	Rise time, i2cX_sda		80		160	ns
	$t_{F(SDA)}$	Fall time, i2cX_sda		80		160	ns
	C_B	Capacitive load for each bus line		60(5)	pF		

(1) In i2cX, X is equal to 1, 2, 3, or 4. Note that I2C4 is master transmitter only.
(2) The device provides (via the I²C bus) a hold time of at least 300 ns for the i2cx_sda signal (see the fall and rise time of i2cx_scl) to bridge the undefined region of the falling edge of i2cx_scl.
(3) HS-mode master devices generate a serial clock signal with a high to low ratio of 1 to 2. $t_{w(SCLL)} > 2 \times t_{w(SCLH)}$.
(4) After this time, the first clock is generated.
(5) Maximum reference load for i2c4_scl and i2c4_sda is C_B = 15 pF.

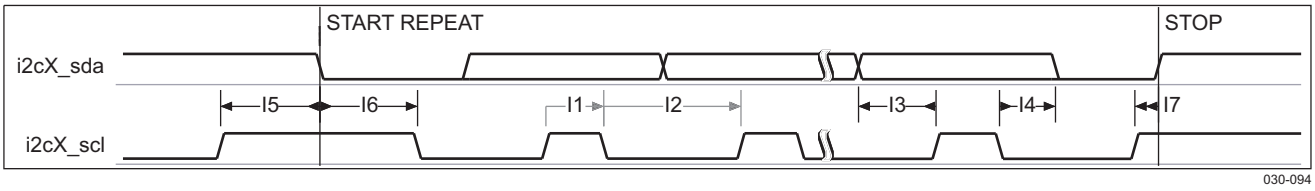

Figure 6-54. I²C – High-Speed Mode(1) (2) (3)

(1) HS-mode master devices generate a serial clock signal with a high-to-low ratio of 1 to 2. $t_{w(SCLL)} > 2 \times t_{w(SCLH)}$.
(2) In i2cX, X is equal to 1, 2, 3, or 4. Note that I2C4 is master transmitter only.
(3) After this time, the first clock is generated.

Table 6-109. Correspondence Standard vs. TI Timing References

	TI-OMAP	STANDARD-I²C	
		S/F Mode	HS Mode
	f_{SCL}	F_{SCL}	F_{SCLH}
I1	$t_{w(SCLH)}$	T_{HIGH}	T_{HIGH}
I2	$t_{w(SCLL)}$	T_{LOW}	T_{LOW}
I3	$t_{su(SDAV-SCLH)}$	$T_{SU;DAT}$	$T_{SU;DAT}$
I4	$t_{h(SCLH-SDAV)}$	$T_{SU;DAT}$	$T_{SU;DAT}$
I5	$t_{su(SDAL-SCLH)}$	$T_{SU;STA}$	$T_{SU;STA}$
I6	$t_{h(SCLH-SDAH)}$	$T_{HD;STA}$	$T_{HD;STA}$

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Table 6-109. Correspondence Standard vs. TI Timing References (continued)

	TI-OMAP	STANDARD-I²C	
		S/F Mode	HS Mode
I7	$t_{h(SCLH-RSTART)}$	$T_{SU;STO}$	$T_{SU;STO}$
I8	$t_{w(SDAH)}$	T_{BUF}	

6.6.6 HDQ / 1-Wire Interfaces

This module is intended to work with both the HDQ and the 1-Wire protocols. The protocols use a single wire to communicate between the master and the slave. The protocols employ an asynchronous return to 1 mechanism where, after any command, the line is pulled high.

6.6.6.1 HDQ Protocol

Table 6-110 and Table 6-111 assume testing over the recommended operating conditions (see Figure 6-55 through Figure 6-58).

Table 6-110. HDQ Timing Requirements

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
t_{CYCD}	Bit window	253		µs
t_{HW1}	Reads 1		68	
t_{HW0}	Reads 0	180		
t_{RSPS}	Command to host respond time(1)			

(1) Defined by software.

Table 6-111. HDQ Switching Characteristics

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
t_B	Break timing		193		µs
t_{BR}	Break recovery		63		
t_{CYCH}	Bit window		253		
t_{DW1}	Sends1 (write)		1.3		
t_{DW0}	Sends0 (write)		101		

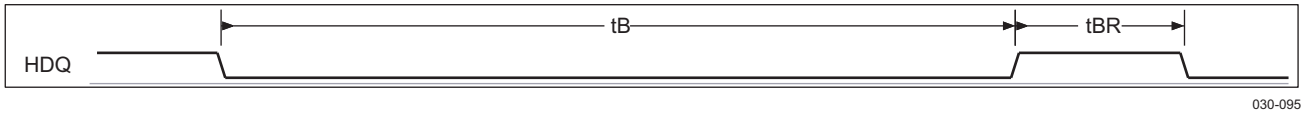

Figure 6-55. HDQ Break (Reset) Timing

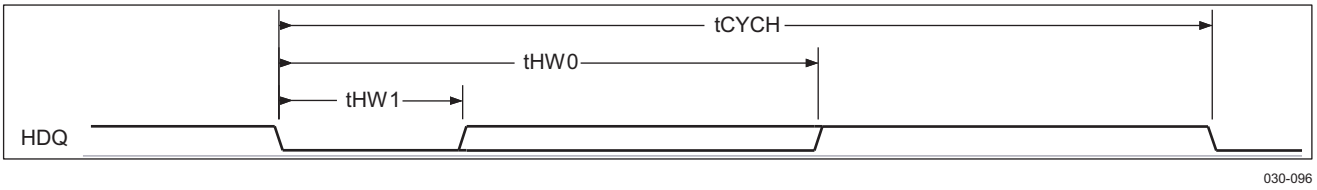

Figure 6-56. HDQ Read Bit Timing (Data)

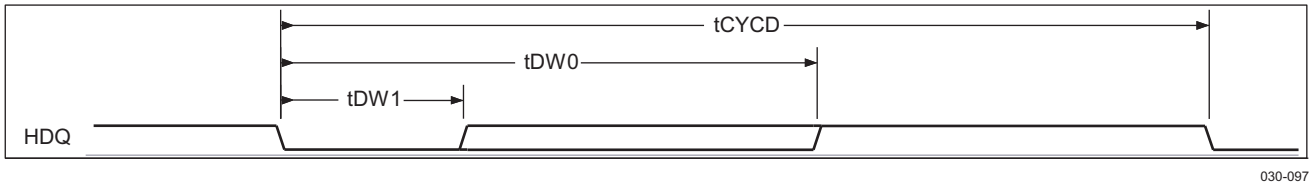

Figure 6-57. HDQ Write Bit Timing (Command/Address or Data)

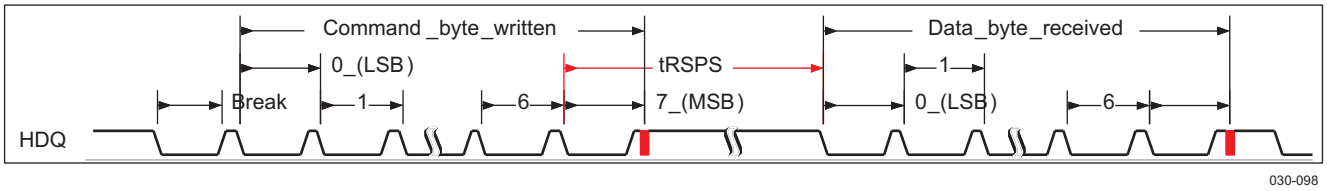

Figure 6-58. HDQ Communication Timing

6.6.6.2 1-Wire Protocol

Table 6-112 and Table 6-113 assume testing over the recommended operating conditions (see Figure 6-59 through Figure 6-61).

Table 6-112. 1-Wire Timing Requirements

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
t_{PDH}	Presence pulse delay high		68	µs
t_{PDL}	Presence pulse delay low	68 – t_{PDH}		
t_{RDV} + t_{REL}	Read bit-zero time		102	

Table 6-113. 1-Wire Switching Characteristics

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{RSTL}	Reset time low		484		µs
t_{RSTH}	Reset time high		484		
t_{SLOT}	Write bit cycle time		102		
t_{LOW1}	Write bit-one time		1.3		
t_{LOW0}	Write bit-zero time		101		
t_{REC}	Recovery time		134		
t_{LOWR}	Read bit strobe time		13		

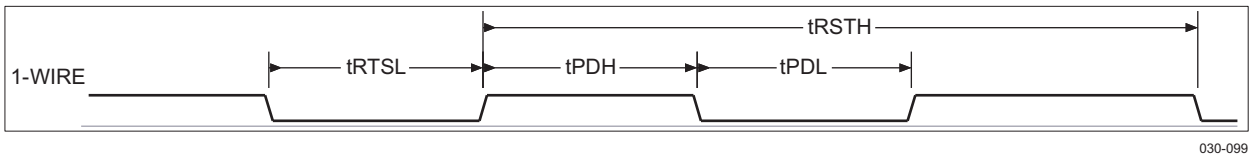

Figure 6-59. 1-Wire Break (Reset) Timing

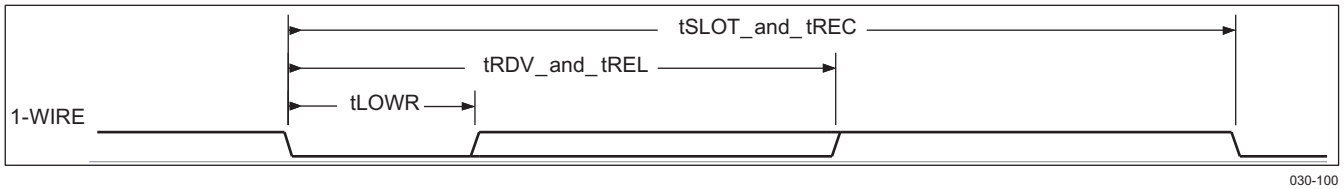

Figure 6-60. 1-Wire Read Bit Timing (Data)

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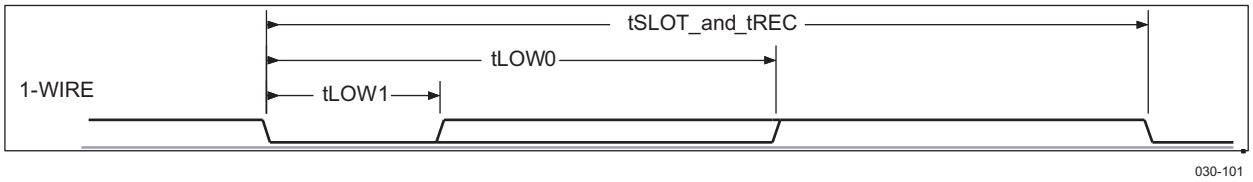

Figure 6-61. 1-Wire Write Bit Timing (Command/Address or Data)

6.6.7 UART IrDA Interface

The IrDA module can operate in three different modes:

- Slow infrared (SIR) (≤115.2 Kbits/s)
- Medium infrared (MIR) (0.576 Mbits/s and 1.152 Mbits/s)
- Fast infrared (FIR) (4 Mbits/s)

For more information about this interface, see the UART/IrDA chapter in the *OMAP35x Technical Reference Manual (TRM)* [literature number SPRUF98].

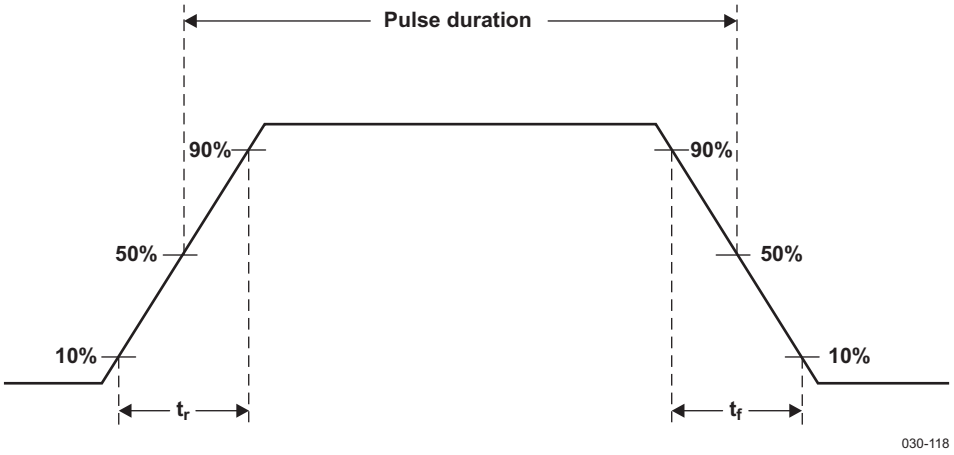

Figure 6-62. UART IrDA Pulse Parameters

6.6.7.1 IrDA—Receive Mode

Table 6-114. UART IrDA—Signaling Rate and Pulse Duration—Receive Mode

SIGNALING RATE	ELECTRICAL PULSE DURATION			UNIT
	MIN	NOMINAL	MAX	
SIR				
2.4 Kbit/s	1.41	78.1	88.55	µs
9.6 Kbit/s	1.41	19.5	22.13	µs
19.2 Kbit/s	1.41	9.75	11.07	µs
38.4 Kbit/s	1.41	4.87	5.96	µs
57.6 Kbit/s	1.41	3.25	4.34	µs
115.2 Kbit/s	1.41	1.62	2.23	µs
MIR				
0.576 Mbit/s	297.2	416	518.8	ns
1.152 Mbit/s	149.6	208	258.4	ns
FIR				
4.0 Mbit/s (Single pulse)	67	125	164	ns

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Table 6-114. UART IrDA—Signaling Rate and Pulse Duration—Receive Mode (continued)

SIGNALING RATE	ELECTRICAL PULSE DURATION			UNIT
	MIN	NOMINAL	MAX	
4.0 Mbit/s (Double pulse)	190	250	289	ns

Table 6-115. UART IrDA—Rise and Fall Time—Receive Mode

	PARAMETER	MAX	UNIT
t_R	Rising time, uart3_rx_irrx	200	ns
t_F	Falling time, uart3_rx_irrx	200	ns

6.6.7.2 IrDA—Transmit Mode

Table 6-116. UART IrDA—Signaling Rate and Pulse Duration—Transmit Mode

SIGNALING RATE	ELECTRICAL PULSE DURATION			UNIT
	MIN	NOMINAL	MAX	
SIR				
2.4 Kbit/s	78.1	78.1	78.1	µs
9.6 Kbit/s	19.5	19.5	19.5	µs
19.2 Kbit/s	9.75	9.75	9.75	µs
38.4 Kbit/s	4.87	4.87	4.87	µs
57.6 Kbit/s	3.25	3.25	3.25	µs
115.2 Kbit/s	1.62	1.62	1.62	µs
MIR				
0.576 Mbit/s	414	416	419	ns
1.152 Mbit/s	206	208	211	ns
FIR				
4.0 Mbit/s (Single pulse)	123	125	128	ns
4.0 Mbit/s (Double pulse)	248	250	253	ns

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6.7 Removable Media Interfaces

6.7.1 High-Speed Multimedia Memory Card (MMC) and Secure Digital IO Card (SDIO) Timing

The MMC/SDIO host controller provides an interface to high-speed and standard MMC, SD memory cards, or SDIO cards. The application interface is responsible for managing transaction semantics. The MMC/SDIO host controller deals with MMC/SDIO protocol at transmission level, packing data, adding CRC, start/end bit, and checking for syntactical correctness.

There are three MMC interfaces on the OMAP3530/25:

- MMC/SD/SDIO Interface 1:
  - 1.8 V/3 V support
  - 8 bits
- MMC/SD/SDIO Interface 2:
  - 1.8 V support
  - 8 bits
  - 4 bits with external transceiver allowing to support 3 V peripherals. Transceiver direction control signals are multiplexed with the upper four data bits.
- MMC/SD/SDIO Interface 3:
  - 1.8 V support
  - 8 bits

6.7.1.1 MMC/SD/SDIO in SD Identification Mode

Table 6-118 and Table 6-119 assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 6-117. MMC/SD/SDIO Timing Conditions – SD Identification Mode

TIMING CONDITION PARAMETER		VALUE	UNIT
SD Identification Mode			
Input Conditions			
t_R	Input signal rise time	10	ns
t_F	Input signal fall time	10	ns
Output Conditions			
C_{LOAD}	Output load capacitance	40	pF

Table 6-118. MMC/SD/SDIO Timing Requirements – SD Identification Mode(1) (2) (3)

NO.	PARAMETER		1.15 V		1.0 V		UNIT
			MIN	MAX	MIN	MAX	
SD Identification Mode							
MMC/SD/SDIO Interface 1 (1.8 V IO)							
HSSD3/SD3	$t_{su(CMDV-CLKIH)}$	Setup time, mmc1_cmd valid before mmc1_clk rising clock edge	1198.4		1198.4		ns
HSSD4/SD4	$t_{su(CLKIH-CMDIV)}$	Hold time, mmc1_cmd valid after mmc1_clk rising clock edge	1249.2		1249.2		ns
MMC/SD/SDIO Interface 1 (3.0 V IO)							
HSSD3/SD3	$t_{su(CMDV-CLKIH)}$	Setup time, mmc1_cmd valid before mmc1_clk rising clock edge	1198.4		1198.4		ns
HSSD4/SD4	$t_{su(CLKIH-CMDIV)}$	Hold time, mmc1_cmd valid after mmc1_clk rising clock edge	1249.2		1249.2		ns
MMC/SD/SDIO Interface 2							

(1) Timing parameters are referred to output clock specified in Table 6-119.
(2) The timing requirements are assured for the cycle jitter and duty cycle error conditions specified in Table 6-119.
(3) Corresponding figures showing timing parameters are common with other interface modes. (See SD and HS SD modes).

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Table 6-118. MMC/SD/SDIO Timing Requirements – SD Identification Mode(1) (2) (3) (continued)

NO.	PARAMETER		1.15 V		1.0 V		UNIT
			MIN	MAX	MIN	MAX	
HSSD3/SD3	$t_{su(CMDV-CLKIH)}$	Setup time, mmc2_cmd valid before mmc2_clk rising clock edge	1198.4		1198.4		ns
HSSD4/SD4	$t_{su(CLKIH-CMDIV)}$	Hold time, mmc2_cmd valid after mmc2_clk rising clock edge	1249.2		1249.2		ns
MMC/SD/SDIO Interface 3							
HSSD3/SD3	$t_{su(CMDV-CLKIH)}$	Setup time, mmc3_cmd valid before mmc3_clk rising clock edge	1198.4		1198.4		ns
HSSD4/SD4	$t_{su(CLKIH-CMDIV)}$	Hold time, mmc3_cmd valid after mmc3_clk rising clock edge	1249.2		1249.2		ns

Table 6-119. MMC/SD/SDIO Switching Characteristics – SD Identification Mode(1)

NO.	PARAMETER		1.15 V		1.0 V		UNIT
			MIN	MAX	MIN	MAX	
SD Identification Mode							
1 / (HSSD1/SD1)	$1/t_{c(clk)}$	Frequency(2), mmcx_ clk (3)		0.4		0.4	MHz
HSSD2/SD2	$t_{W(clkH)}$	Typical pulse duration, output clk high	X(4)*PO(5)		X(4)*PO(5)		ns
HSSD2/SD2	$t_{W(clkL)}$	Typical pulse duration, output clk low	Y(6)*PO(5)		Y(6)*PO(5)		ns
	$t_{dc(clk)}$	Duty cycle error, output clk		125		125	ns
	$t_{j(clk)}$	Jitter standard deviation(7), output clk		200		200	ps
MMC/SD/SDIO Interface 1 (1.8 V IO)							
	$t_{c(clk)}$	Rise time, output clk		10		10	ns
	$t_{W(clkH)}$	Fall time, output clk		10		10	ns
	$t_{W(clkL)}$	Rise time, output data		10		10	ns
	$t_{dc(clk)}$	Fall time, output data		10		10	ns
HSSD5/SD5	$t_{d(CLKOH-CMD)}$	Delay time, mmc1_clk rising clock edge to mmc1_cmd transition	6.3	2492.7	6.3	2492.7	ns
MMC/SD/SDIO Interface 1 (3.0 V IO)							
	$t_{c(clk)}$	Rise time, output clk		10		0	ns
	$t_{W(clkH)}$	Fall time, output clk		10		0	ns
	$t_{W(clkL)}$	Rise time, output data		10		10	ns
	$t_{dc(clk)}$	Fall time, output data		10		10	ns
HSSD5/SD5	$t_{d(CLKOH-CMD)}$	Delay time, mmc1_clk rising clock edge to mmc1_cmd transition	6.3	2492.7	6.3	2492.7	ns
MMC/SD/SDIO Interface 2							
	$t_{c(clk)}$	Rise time, output clk		10		10	ns
	$t_{W(clkH)}$	Fall time, output clk		10		10	ns
	$t_{W(clkL)}$	Rise time, output data		10		10	ns
	$t_{dc(clk)}$	Fall time, output data		10		10	ns
HSSD5/SD5	$t_{d(CLKOH-CMD)}$	Delay time, mmc2_clk rising clock edge to mmc2_cmd transition	6.3	2492.7	6.3	2492.7	ns
MMC/SD/SDIO Interface 3							
	$t_{c(clk)}$	Rise time, output clk		10		10	ns

(1) Corresponding figures showing timing parameters are common with other interface modes (see SD and HS SD modes).
(2) Related with the output clk maximum and minimum frequencies programmable in I/F module.
(3) In mmcx_clk, 'x' is equal to 1, 2, or 3.
(4) The X parameter is defined as shown in Table 6-120.
(5) PO = output clk period in ns.
(6) The Y parameter is defined as shown in Table 6-121.
(7) The jitter probability density can be approximated by a Gaussian function.

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Table 6-119. MMC/SD/SDIO Switching Characteristics – SD Identification Mode[1] (continued)

NO.	PARAMETER		1.15 V		1.0 V		UNIT
			MIN	MAX	MIN	MAX	
	$t_{W(clkH)}$	Fall time, output clk		10		10	ns
	$t_{W(clkL)}$	Rise time, output data		10		10	ns
	$t_{dc(clk)}$	Fall time, output data		10		10	ns
HSSD5/SD5	$t_{d(CLKOH-CMD)}$	Delay time, mmc3_clk rising clock edge to mmc3_cmd transition	6.3	2492.7	6.3	2492.7	ns

Table 6-120. X Parameter

CLKD	X
1 or Even	0.5
Odd	(trunk[CLKD/2]+1)/CLKD

Table 6-121. Y Parameter

CLKD	Y
1 or Even	0.5
Odd	(trunk[CLKD/2])/CLKD

For details about clock division factor CLKD, see the *OMAP35x Technical Reference Manual (TRM)* [literature number SPRUF98].

6.7.1.2 MMC/SD/SDIO in High-Speed MMC Mode

Table 6-123 and Table 6-124 assume testing over the recommended operating conditions and electrical characteristic conditions (see Figure 6-63 and Figure 6-64).

Table 6-122. MMC/SD/SDIO Timing Conditions – High-Speed MMC Mode

TIMING CONDITION PARAMETER		VALUE	UNIT
High-Speed MMC Mode			
Input Conditions			
t_R	Input signal rise time	3	ns
t_F	Input signal fall time	3	ns
Output Conditions			
C_{LOAD}	Output load capacitance	30	pF

Table 6-123. MMC/SD/SDIO Timing Requirements – High-Speed MMC Mode[1] [2] [3] [4]

NO.	PARAMETER		1.15 V		1.0 V		UNIT
			MIN	MAX	MIN	MAX	
High-Speed MMC Mode							
MMC/SD/SDIO Interface 1 (1.8 V IO)							
MMC3	$t_{su(CMDV-CLKIH)}$	Setup time, mmc1_cmd valid before mmc1_clk rising clock edge	5.6		26		ns
MMC4	$t_{su(CLKIH-CMDIV)}$	Hold time, mmc1_cmd valid after mmc1_clk rising clock edge	2.3		1.9		ns
MMC7	$t_{su(DATxV-CLKIH)}$	Setup time, mmc1_datx valid before mmc1_clk rising clock edge	5.6		26		ns
MMC8	$t_{su(CLKIH-DATxIV)}$	Hold time, mmc1_datx valid after mmc1_clk rising clock edge	2.3		1.9		ns

(1) Timing parameters are referred to output clock specified in Table 6-124.
(2) The timing requirements are assured for the cycle jitter and duty cycle error conditions specified in Table 6-124.
(3) Corresponding figures showing timing parameters are common with Standard MMC mode (See Figure 6-63 and Figure 6-64)
(4) In datx, x is equal to 1, 2, 3, 4, 5, 6, or 7.

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Table 6-123. MMC/SD/SDIO Timing Requirements – High-Speed MMC Mode(1) (2) (3) (4) (continued)

NO.	PARAMETER		1.15 V		1.0 V		UNIT
			MIN	MAX	MIN	MAX	
MMC/SD/SDIO Interface 1 (3.0 V IO)							
MMC3	$t_{su(CMDV-CLKIH)}$	Setup time, mmc1_cmd valid before mmc1_clk rising clock edge	5.6		26		ns
MMC4	$t_{su(CLKIH-CMDIV)}$	Hold time, mmc1_cmd valid after mmc1_clk rising clock edge	2.3		1.9		ns
MMC7	$t_{su(DATxV-CLKIH)}$	Setup time, mmc1_datx valid before mmc1_clk rising clock edge	5.6		26		ns
MMC8	$t_{su(CLKIH-DATxIV)}$	Hold time, mmc1_datx valid after mmc1_clk rising clock edge	2.3		1.9		ns
MMC/SD/SDIO Interface 2							
MMC3	$t_{su(CMDV-CLKIH)}$	Setup time, mmc2_cmd valid before mmc2_clk rising clock edge	5.6		26		ns
MMC4	$t_{su(CLKIH-CMDIV)}$	Hold time, mmc2_cmd valid after mmc2_clk rising clock edge	2.3		1.9		ns
MMC7	$t_{su(DATxV-CLKIH)}$	Setup time, mmc2_datx valid before mmc2_clk rising clock edge	5.6		26		ns
MMC8	$t_{su(CLKIH-DATxIV)}$	Hold time, mmc2_datx valid after mmc2_clk rising clock edge	2.3		1.9		ns
MMC/SD/SDIO Interface 3							
MMC3	$t_{su(CMDV-CLKIH)}$	Setup time, mmc3_cmd valid before mmc3_clk rising clock edge	5.6		26		ns
MMC4	$t_{su(CLKIH-CMDIV)}$	Hold time, mmc3_cmd valid after mmc3_clk rising clock edge	2.3		1.9		ns
MMC7	$t_{su(DATxV-CLKIH)}$	Setup time, mmc3_datx valid before mmc3_clk rising clock edge	5.6		26		ns
MMC8	$t_{su(CLKIH-DATxIV)}$	Hold time, mmc3_datx valid after mmc3_clk rising clock edge	2.3		1.9		ns

Table 6-124. MMC/SD/SDIO Switching Characteristics – High-Speed MMC Mode(1)

N O.	PARAMETER		1.15 V		1.0 V		UNIT
			MIN	MAX	MIN	MAX	
High-Speed MMC Mode							
1/MMC1	$1/t_{c(clk)}$	Frequency(2), mmcx_ clk (3)		48		24	MHz
MMC2	$t_{W(clkH)}$	Typical pulse duration, output clk high	X(4)*PO(5)		X(4)*PO(5)		ns
MMC2	$t_{W(clkL)}$	Typical pulse duration, output clk low	Y(6)*PO(5)		Y(6)*PO(5)		ns
	$t_{dc(clk)}$	Duty cycle error, output clk		1041.7		2083.3	ps
	$t_{j(clk)}$	Jitter standard deviation(3), output clk		200		200	ps
MMC/SD/SDIO Interface 1 (1.8 V IO)							
	$t_{c(clk)}$	Rise time, output clk		3		3	ns
	$t_{W(clkH)}$	Fall time, output clk		3		3	ns
	$t_{W(clkL)}$	Rise time, output data		3		3	ns
	$t_{dc(clk)}$	Fall time, output data		3		3	ns
MMC5	$t_{d(CLKOH-CMD)}$	Delay time, mmc1_clk rising clock edge to mmc1_cmd transition	3.7	14.1	4.1	34.5	ns

(1) In datx, x is equal to 1, 2, 3, 4, 5, 6, or 7.
(2) Related with the output clk maximum and minimum frequencies programmable in I/F module.
(3) In mmcx_clk, 'x' is equal to 1, 2, or 3.
(4) The X parameter is defined as shown in Table 6-125.
(5) PO = output clk period in ns.
(6) The Y parameter is defined as shown in Table 6-126.

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Table 6-124. MMC/SD/SDIO Switching Characteristics – High-Speed MMC Mode[1] (continued)

N O.	PARAMETER		1.15 V		1.0 V		UNIT
			MIN	MAX	MIN	MAX	
MMC6	$t_{d(CLKOH-DATx)}$	Delay time, mmc1_clk rising clock edge to mmc1_datx transition	3.7	14.1	4.1	34.5	ns
MMC/SD/SDIO Interface 1 (3.0 V IO)							
	$t_{c(clk)}$	Rise time, output clk		3		3	ns
	$t_{W(clkH)}$	Fall time, output clk		3		3	ns
	$t_{W(clkL)}$	Rise time, output data		3		3	ns
	$t_{dc(clk)}$	Fall time, output data		3		3	ns
MMC5	$t_{d(CLKOH-CMD)}$	Delay time, mmc1_clk rising clock edge to mmc1_cmd transition	3.7	14.1	4.1	34.5	ns
MMC6	$t_{d(CLKOH-DATx)}$	Delay time, mmc1_clk rising clock edge to mmc1_datx transition	3.7	14.1	4.1	34.5	ns
MMC/SD/SDIO Interface 2							
	$t_{c(clk)}$	Rise time, output clk		3		3	ns
	$t_{W(clkH)}$	Fall time, output clk		3		3	ns
	$t_{W(clkL)}$	Rise time, output data		3		3	ns
	$t_{dc(clk)}$	Fall time, output data		3		3	ns
MMC5	$t_{d(CLKOH-CMD)}$	Delay time, mmc2_clk rising clock edge to mmc2_cmd transition	3.7	14.1	4.1	34.5	ns
MMC6	$t_{d(CLKOH-DATx)}$	Delay time, mmc2_clk rising clock edge to mmc2_datx transition	3.7	16.5	4.1	36.9	ns
MMC/SD/SDIO Interface 3							
	$t_{c(clk)}$	Rise time, output clk		3		3	ns
	$t_{W(clkH)}$	Fall time, output clk		3		3	ns
	$t_{W(clkL)}$	Rise time, output data		3		3	ns
	$t_{dc(clk)}$	Fall time, output data		3		3	ns
MMC5	$t_{d(CLKOH-CMD)}$	Delay time, mmc3_clk rising clock edge to mmc3_cmd transition	3.7	14.1	4.1	34.5	ns
MMC6	$t_{d(CLKOH-DATx)}$	Delay time, mmc3_clk rising clock edge to mmc3_datx transition	3.7	14.1	4.1	34.5	ns

Table 6-125. X Parameter

CLKD	X
1 or Even	0.5
Odd	(trunk[CLKD/2]+1)/CLKD

Table 6-126. Y Parameter

CLKD	Y
1 or Even	0.5
Odd	(trunk[CLKD/2])/CLKD

For details about clock division factor CLKD, see the *OMAP35x Technical Reference Manual (TRM)* [literature number SPRUF98].

6.7.1.3 MMC/SD/SDIO in Standard MMC Mode and MMC Identification Mode

Table 6-128 and Table 6-129 assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 6-127. MMC/SD/SDIO Timing Conditions – Standard MMC Mode and MMC Identification Mode

TIMING CONDITION PARAMETER		VALUE	UNIT
Standard MMC Mode and MMC Identification Mode			
Input Conditions			
t_R	Input signal rise time	10	ns
t_F	Input signal fall time	10	ns
Output Conditions			
C_{LOAD}	Output load capacitance	30	pF

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Table 6-128. MMC/SD/SDIO Timing Requirements – Standard MMC Mode and MMC Identification Mode[1] [2]

NO.	PARAMETER		1.15 V		1.0 V		UNIT
			MIN	MAX	MIN	MAX	
Standard MMC Mode and MMC Identification Mode							
MMC/SD/SDIO Interface 1 (1.8 V IO)							
MMC3	$t_{su(CMDV-CLKIH)}$	Setup time, mmc1_cmd valid before mmc1_clk rising clock edge	13.6		65.7		ns
MMC4	$t_{su(CLKIH-CMDIV)}$	Hold time, mmc1_cmd valid after mmc1_clk rising clock edge	8.9		8.9		ns
MMC7	$t_{su(DATxV-CLKIH)}$	Setup time, mmc1_datx valid before mmc1_clk rising clock edge	13.6		65.7		ns
MMC8	$t_{su(CLKIH-DATxIV)}$	Hold time, mmc1_datx valid after mmc1_clk rising clock edge	8.9		8.9		ns
MMC/SD/SDIO Interface 1 (3.0 V IO)							
MMC3	$t_{su(CMDV-CLKIH)}$	Setup time, mmc1_cmd valid before mmc1_clk rising clock edge	13.6		65.7		ns
MMC4	$t_{su(CLKIH-CMDIV)}$	Hold time, mmc1_cmd valid after mmc1_clk rising clock edge	8.9		8.9		ns
MMC7	$t_{su(DATxV-CLKIH)}$	Setup time, mmc1_datx valid before mmc1_clk rising clock edge	13.6		65.7		ns
MMC8	$t_{su(CLKIH-DATxIV)}$	Hold time, mmc1_datx valid after mmc1_clk rising clock edge	8.9		8.9		ns
MMC/SD/SDIO Interface 2							
MMC3	$t_{su(CMDV-CLKIH)}$	Setup time, mmc2_cmd valid before mmc2_clk rising clock edge	13.6		65.7		ns
MMC4	$t_{su(CLKIH-CMDIV)}$	Hold time, mmc2_cmd valid after mmc2_clk rising clock edge	8.9		8.9		ns
MMC7	$t_{su(DATxV-CLKIH)}$	Setup time, mmc2_datx valid before mmc2_clk rising clock edge	13.6		65.7		ns
MMC8	$t_{su(CLKIH-DATxIV)}$	Hold time, mmc2_datx valid after mmc2_clk rising clock edge	8.9		8.9		ns
MMC/SD/SDIO Interface 3							
MMC3	$t_{su(CMDV-CLKIH)}$	Setup time, mmc3_cmd valid before mmc3_clk rising clock edge	13.6		65.7		ns
MMC4	$t_{su(CLKIH-CMDIV)}$	Hold time, mmc3_cmd valid after mmc3_clk rising clock edge	8.9		8.9		ns
MMC7	$t_{su(DATxV-CLKIH)}$	Setup time, mmc3_datx valid before mmc3_clk rising clock edge	13.6		65.7		ns
MMC8	$t_{su(CLKIH-DATxIV)}$	Hold time, mmc3_datx valid after mmc3_clk rising clock edge	8.9		8.9		ns

(1) Timing parameters are referred to output clock specified in Table 6-129.
(2) The timing requirements are assured for the cycle jitter and duty cycle error conditions specified in Table 6-129.

Table 6-129. MMC/SD/SDIO Switching Characteristics – Standard MMC Mode and MMC Identification Mode

NO.	PARAMETER		1.15 V		1.0 V		UNIT
			MIN	MAX	MIN	MAX	
MMC Identification Mode							
1/MMC1	$1/t_{c(clk)}$	Frequency[1], mmcx_ clk [2]		0.4		0.4	MHz
MMC2	$t_{W(clkH)}$	Typical pulse duration, output clk high	X[3]*PO[4]		X[3]*PO[4]		ns

(1) Related with the output clk maximum and minimum frequencies programmable in I/F module.
(2) In mmcx_clk, 'x' is equal to 1, 2, or 3.
(3) The X parameter is defined as shown in Table 6-130.
(4) PO = output clk period in ns.

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Table 6-129. MMC/SD/SDIO Switching Characteristics – Standard MMC Mode and MMC Identification Mode (continued)

NO.	PARAMETER		1.15 V		1.0 V		UNIT
			MIN	MAX	MIN	MAX	
MMC2	$t_{W(clkL)}$	Typical pulse duration, output clk low	Y*PO(4)		Y*PO(4)		ns
	$t_{dc(clk)}$	Duty cycle error, output clk		125		125	ns
	$t_{j(clk)}$	Jitter standard deviation(5), output clk		200		200	ps
Standard MMC Mode							
1/MMC1	$1/t_{c(clk)}$	Frequency(1), mmcx_ clk (2)		19.2		9.6	MHz
MMC2	$t_{W(clkH)}$	Typical pulse duration, output clk high	X(3)*PO(4)		X(3)*PO(4)		ns
MMC2	$t_{W(clkL)}$	Typical pulse duration, output clk low	Y*PO(4)		Y*PO(4)		ns
	$t_{dc(clk)}$	Duty cycle error, output clk		2604.2		5208.3	ps
	$t_{j(clk)}$	Jitter standard deviation(5), output clk		200		200	ps
MMC/SD/SDIO Interface 1 (1.8 V IO)							
	$t_{c(clk)}$	Rise time, output clk		10		10	ns
	$t_{W(clkH)}$	Fall time, output clk		10		10	ns
	$t_{W(clkL)}$	Rise time, output data		10		10	ns
	$t_{dc(clk)}$	Fall time, output data		10		10	ns
MMC5	$t_{d(CLKOH-CMD)}$	Delay time, mmc1_clk rising clock edge to mmc1_cmd transition	4.3	47.8	4.3	99.9	ns
MMC6	$t_{d(CLKOH-DATx)}$	Delay time, mmc1_clk rising clock edge to mmc1_datx transition	4.3	47.8	4.3	99.9	ns
MMC/SD/SDIO Interface 1 (3.0 V IO)							
	$t_{c(clk)}$	Rise time, output clk		10		10	ns
	$t_{W(clkH)}$	Fall time, output clk		10		10	ns
	$t_{W(clkL)}$	Rise time, output data		10		10	ns
	$t_{dc(clk)}$	Fall time, output data		10		10	ns
MMC5	$t_{d(CLKOH-CMD)}$	Delay time, mmc1_clk rising clock edge to mmc1_cmd transition	4.3	47.8	4.3	99.9	ns
MMC6	$t_{d(CLKOH-DATx)}$	Delay time, mmc1_clk rising clock edge to mmc1_datx transition	4.3	47.8	4.3	99.9	ns
MMC/SD/SDIO Interface 2							
	$t_{c(clk)}$	Rise time, output clk		10		10	ns
	$t_{W(clkH)}$	Fall time, output clk		10		10	ns
	$t_{W(clkL)}$	Rise time, output data		10		10	ns
	$t_{dc(clk)}$	Fall time, output data		10		10	ns
MMC5	$t_{d(CLKOH-CMD)}$	Delay time, mmc2_clk rising clock edge to mmc2_cmd transition	4.3	47.8	4.3	99.9	ns
MMC6	$t_{d(CLKOH-DATx)}$	Delay time, mmc2_clk rising clock edge to mmc2_datx transition	4.3	47.8	4.3	99.9	ns
MMC/SD/SDIO Interface 3							
	$t_{c(clk)}$	Rise time, output clk		10		10	ns
	$t_{W(clkH)}$	Fall time, output clk		10		10	ns
	$t_{W(clkL)}$	Rise time, output data		10		10	ns
	$t_{dc(clk)}$	Fall time, output data		10		10	ns
MMC5	$t_{d(CLKOH-CMD)}$	Delay time, mmc3_clk rising clock edge to mmc3_cmd transition	4.3	47.8	4.3	99.9	ns
MMC6	$t_{d(CLKOH-DATx)}$	Delay time, mmc3_clk rising clock edge to mmc3_datx transition	4.3	47.8	4.3	99.9	ns

(5) The jitter probability density can be approximated by a Gaussian function.

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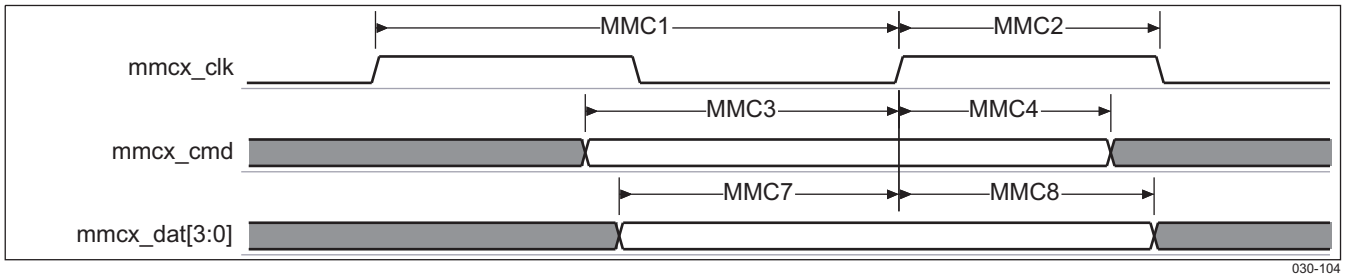
Table 6-130. X Parameter

CLKD	X
1 or Even	0.5
Odd	(trunk[CLKD/2]+1)/CLKD

Table 6-131. Y Parameter

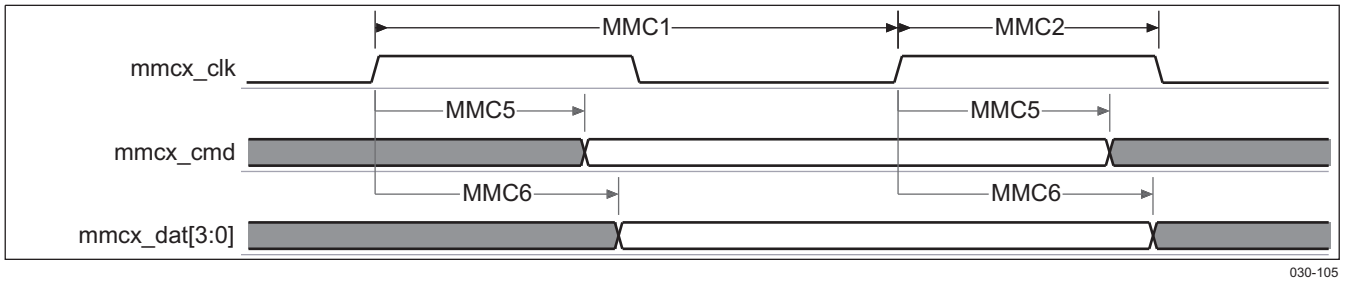
CLKD	Y
1 or Even	0.5
Odd	(trunk[CLKD/2])/CLKD

For details about clock division factor CLKD, see the *OMAP35x Technical Reference Manual (TRM)* [literature number SPRUF98].



In mmcx, x is equal to 1, 2, or 3.

Figure 6-63. MMC/SD/SDIO – High-Speed and Standard MMC Modes – Data/Command Receive



In mmcx, x is equal to 1, 2, or 3.

Figure 6-64. MMC/SD/SDIO – High-Speed and Standard MMC Modes – Data/Command Transmit

6.7.1.4 MMC/SD/SDIO in High-Speed SD Mode

Table 6-133 and Table 6-134 assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 6-132. MMC/SD/SDIO Timing Conditions – High-Speed SD Mode

TIMING CONDITION PARAMETER		VALUE	UNIT
High-Speed SD Mode			
Input Conditions			
t_R	Input signal rise time	3	ns
t_F	Input signal fall time	3	ns
Output Conditions			
C_{LOAD}	Output load capacitance	40	pF

Table 6-133. MMC/SD/SDIO Timing Requirements – High-Speed SD Mode(1) (2) (3)

NO.	PARAMETER		1.15 V		1.0 V		UNIT
			MIN	MAX	MIN	MAX	
High-Speed SD Mode							
MMC/SD/SDIO Interface 1 (1.8 V IO)							
HSSD3	$t_{su(CMDV-CLKIH)}$	Setup time, mmc1_cmd valid before mmc1_clk rising clock edge	5.6		26		ns
HSSD4	$t_{su(CLKIH-CMDIV)}$	Hold time, mmc1_cmd valid after mmc1_clk rising clock edge	2.3		1.9		ns
HSSD7	$t_{su(DATxV-CLKIH)}$	Setup time, mmc1_datx valid before mmc1_clk rising clock edge	5.6		26		ns
HSSD8	$t_{su(CLKIH-DATxIV)}$	Hold time, mmc1_datx valid after mmc1_clk rising clock edge	2.3		1.9		ns
MMC/SD/SDIO Interface 1 (3.0 V IO)							
HSSD3	$t_{su(CMDV-CLKIH)}$	Setup time, mmc1_cmd valid before mmc1_clk rising clock edge	5.6		26		ns
HSSD4	$t_{su(CLKIH-CMDIV)}$	Hold time, mmc1_cmd valid after mmc1_clk rising clock edge	2.3		1.9		ns
HSSD7	$t_{su(DATxV-CLKIH)}$	Setup time, mmc1_datx valid before mmc1_clk rising clock edge	5.6		26		ns
HSSD8	$t_{su(CLKIH-DATxIV)}$	Hold time, mmc1_datx valid after mmc1_clk rising clock edge	2.3		1.9		ns
MMC/SD/SDIO Interface 2							
HSSD3	$t_{su(CMDV-CLKIH)}$	Setup time, mmc2_cmd valid before mmc2_clk rising clock edge	5.6		26		ns
HSSD4	$t_{su(CLKIH-CMDIV)}$	Hold time, mmc2_cmd valid after mmc2_clk rising clock edge	2.3		1.9		ns
HSSD7	$t_{su(DATxV-CLKIH)}$	Setup time, mmc2_datx valid before mmc2_clk rising clock edge	5.6		26		ns
HSSD8	$t_{su(CLKIH-DATxIV)}$	Hold time, mmc2_datx valid after mmc2_clk rising clock edge	2.3		1.9		ns
MMC/SD/SDIO Interface 3							
HSSD3	$t_{su(CMDV-CLKIH)}$	Setup time, mmc3_cmd valid before mmc3_clk rising clock edge	5.6		26		ns
HSSD4	$t_{su(CLKIH-CMDIV)}$	Hold time, mmc3_cmd valid after mmc3_clk rising clock edge	2.3		1.9		ns
HSSD7	$t_{su(DATxV-CLKIH)}$	Setup time, mmc3_datx valid before mmc3_clk rising clock edge	5.6		26		ns
HSSD8	$t_{su(CLKIH-DATxIV)}$	Hold time, mmc3_datx valid after mmc3_clk rising clock edge	2.3		1.9		ns

(1) Timing Parameters are referred to output clock specified in Table 6-134.
(2) The timing requirements are assured for the cycle jitter and duty cycle error conditions specified in Table 6-134.
(3) In datx, x is equal to 1, 2, 3, 4, 5, 6, or 7.

Table 6-134. MMC/SD/SDIO Switching Characteristics – High-Speed SD Mode

NO.	PARAMETER		1.15 V		1.0 V		UNIT
			MIN	MAX	MIN	MAX	
High-Speed SD Mode							
1/HSSD1	$1/t_{c(clk)}$	Frequency(1), mmcx_ clk (2)		48		24	ns
HSSD2	$t_{W(clkH)}$	Typical pulse duration, output clk high	X(3)*PO(4)		X(3)*PO(4)		ns

(1) Related with the output clk maximum and minimum frequencies programmable in I/F module.
(2) In mmcx_clk, 'x' is equal to 1, 2, or 3.
(3) The X parameter is defined as shown in Table 6-135.
(4) PO = output clk period in ns.

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Table 6-134. MMC/SD/SDIO Switching Characteristics – High-Speed SD Mode (continued)

NO.	PARAMETER		1.15 V		1.0 V		UNIT
			MIN	MAX	MIN	MAX	
HSSD2	$t_{W(clkL)}$	Typical pulse duration, output clk low	Y(5)*PO(4)		Y(5)*PO(4)		ns
	$t_{dc(clk)}$	Duty cycle error, output clk		1041.7		2083.3	ps
	$t_{j(clk)}$	Jitter standard deviation(6), output clk		200		200	ps
MMC/SD/SDIO Interface 1 (1.8 V IO)							
	$t_{c(clk)}$	Rise time, output clk		3		3	ns
	$t_{W(clkH)}$	Fall time, output clk		3		3	ns
	$t_{W(clkL)}$	Rise time, output data		3		3	ns
	$t_{dc(clk)}$	Fall time, output data		3		3	ns
HSSD5	$t_{d(CLKOH-CMD)}$	Delay time, mmc1_clk rising clock edge to mmc1_cmd transition	3.7	14.1	4.1	34.5	ns
HSSD6	$t_{d(CLKOH-DATx)}$	Delay time, mmc1_clk rising clock edge to mmc1_datx transition	3.7	14.1	4.1	34.5	ns
MMC/SD/SDIO Interface 1 (3.0 V IO)							
	$t_{c(clk)}$	Rise time, output clk		3		3	ns
	$t_{W(clkH)}$	Fall time, output clk		3		3	ns
	$t_{W(clkL)}$	Rise time, output data		3		3	ns
	$t_{dc(clk)}$	Fall time, output data		3		3	ns
HSSD5	$t_{d(CLKOH-CMD)}$	Delay time, mmc1_clk rising clock edge to mmc1_cmd transition	3.7	14.1	4.1	34.5	ns
HSSD6	$t_{d(CLKOH-DATx)}$	Delay time, mmc1_clk rising clock edge to mmc1_datx transition	3.7	14.1	4.1	34.5	ns
MMC/SD/SDIO Interface 2							
	$t_{c(clk)}$	Rise time, output clk		3		3	ns
	$t_{W(clkH)}$	Fall time, output clk		3		3	ns
	$t_{W(clkL)}$	Rise time, output data		3		3	ns
	$t_{dc(clk)}$	Fall time, output data		3		3	ns
HSSD5	$t_{d(CLKOH-CMD)}$	Delay time, mmc2_clk rising clock edge to mmc2_cmd transition	3.7	14.1	4.1	34.5	ns
HSSD6	$t_{d(CLKOH-DATx)}$	Delay time, mmc2_clk rising clock edge to mmc2_datx transition	3.7	14.1	4.1	34.5	ns
MMC/SD/SDIO Interface 3							
	$t_{c(clk)}$	Rise time, output clk		3		3	ns
	$t_{W(clkH)}$	Fall time, output clk		3		3	ns
	$t_{W(clkL)}$	Rise time, output data		3		3	ns
	$t_{dc(clk)}$	Fall time, output data		3		3	ns
HSSD5	$t_{d(CLKOH-CMD)}$	Delay time, mmc3_clk rising clock edge to mmc3_cmd transition	3.7	14.1	4.1	34.5	ns
HSSD6	$t_{d(CLKOH-DATx)}$	Delay time, mmc3_clk rising clock edge to mmc3_datx transition	3.7	14.1	4.1	34.5	ns

(5) The Y parameter is defined as shown in Table 6-136.
(6) The jitter probability density can be approximated by a Gaussian function.

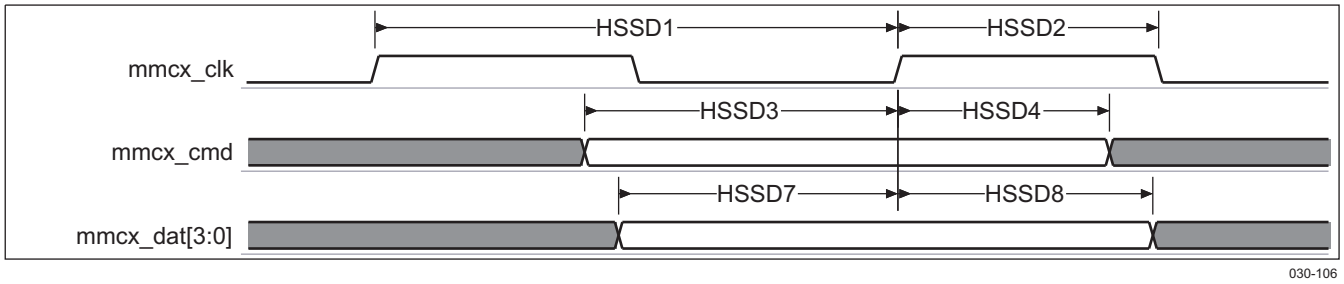
Table 6-135. X Parameters

CLKD	X
1 or Even	0.5
Odd	(trunk[CLKD/2]+1)/CLKD

Table 6-136. Y Parameters

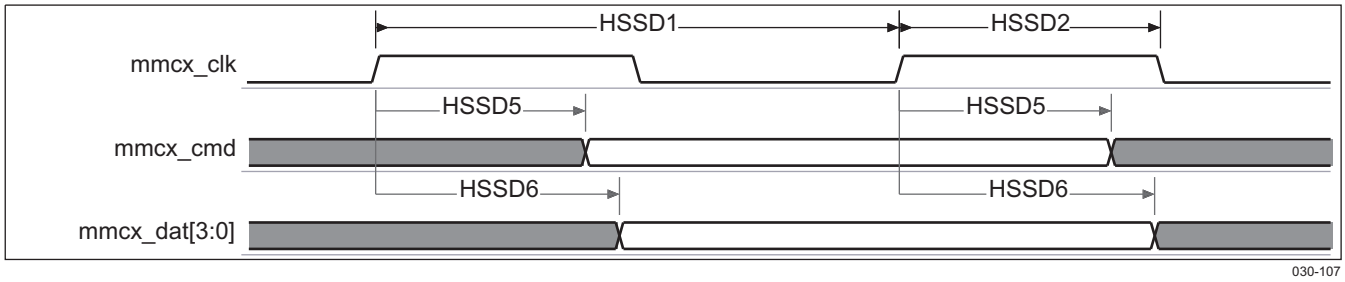
CLKD	Y
1 or Even	0.5
Odd	(trunk[CLKD/2])/CLKD

For details about clock division factor CLKD, see the *OMAP35x Technical Reference Manual (TRM)* [literature number SPRUF98].



In mmcx, x is equal to 1, 2, or 3.

Figure 6-65. MMC/SD/SDIO – High-Speed SD Mode – Data/Command Receive



In mmcx, x is equal to 1, 2, or 3.

Figure 6-66. MMC/SD/SDIO – High-Speed SD Mode – Data/Command Transmit

6.7.1.5 MMC/SD/SDIO in Standard SD Mode

Table 6-138 and Table 6-139 assume testing over the recommended operating conditions and electrical characteristic conditions (see Figure 6-67).

Table 6-137. MMC/SD/SDIO Timing Conditions – Standard SD Mode

TIMING CONDITION PARAMETER		VALUE	UNIT
Standard SD Mode			
Input Conditions			
t_R	Input signal rise time	10	ns
t_F	Input signal fall time	10	ns
Output Conditions			
C_{LOAD}	Output load capacitance	40	pF

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Table 6-138. MMC/SD/SDIO Timing Requirements – Standard SD Mode(1) (2) (3)

NO.	PARAMETER		1.15 V		1.0 V		UNIT
			MIN	MAX	MIN	MAX	
Standard SD Mode							
MMC/SD/SDIO Interface 1 (1.8 V IO)							
SD3	$t_{su(CMDV-CLKIH)}$	Setup time, mmc1_cmd valid before mmc1_clk rising clock edge	6.2		47.7		ns
SD4	$t_{su(CLKIH-CMDIV)}$	Hold time, mmc1_cmd valid after mmc1_clk rising clock edge	19.4		19.2		ns
SD7	$t_{su(DATxV-CLKIH)}$	Setup time, mmc1_datx valid before mmc1_clk rising clock edge	6.2		47.7		ns
SD8	$t_{su(CLKIH-DATxIV)}$	Hold time, mmc1_datx valid after mmc1_clk rising clock edge	19.4		19.2		ns
MMC/SD/SDIO Interface 1 (3.0 V IO)							
SD3	$t_{su(CMDV-CLKIH)}$	Setup time, mmc1_cmd valid before mmc1_clk rising clock edge	6.2		47.7		ns
SD4	$t_{su(CLKIH-CMDIV)}$	Hold time, mmc1_cmd valid after mmc1_clk rising clock edge	19.4		19.2		ns
SD7	$t_{su(DATxV-CLKIH)}$	Setup time, mmc1_datx valid before mmc1_clk rising clock edge	6.2		47.7		ns
SD8	$t_{su(CLKIH-DATxIV)}$	Hold time, mmc1_datx valid after mmc1_clk rising clock edge	19.4		19.2		ns
MMC/SD/SDIO Interface 2							
SD3	$t_{su(CMDV-CLKIH)}$	Setup time, mmc2_cmd valid before mmc2_clk rising clock edge	6.2		47.7		ns
SD4	$t_{su(CLKIH-CMDIV)}$	Hold time, mmc2_cmd valid after mmc2_clk rising clock edge	19.4		19.2		ns
SD7	$t_{su(DATxV-CLKIH)}$	Setup time, mmc2_datx valid before mmc2_clk rising clock edge	6.2		47.7		ns
SD8	$t_{su(CLKIH-DATxIV)}$	Hold time, mmc2_datx valid after mmc2_clk rising clock edge	19.4		19.2		ns
MMC/SD/SDIO Interface 3							
SD3	$t_{su(CMDV-CLKIH)}$	Setup time, mmc3_cmd valid before mmc3_clk rising clock edge	6.2		47.7		ns
SD4	$t_{su(CLKIH-CMDIV)}$	Hold time, mmc3_cmd valid after mmc3_clk rising clock edge	19.4		19.2		ns
SD7	$t_{su(DATxV-CLKIH)}$	Setup time, mmc3_datx valid before mmc3_clk rising clock edge	6.2		47.7		ns
SD8	$t_{su(CLKIH-DATxIV)}$	Hold time, mmc3_datx valid after mmc3_clk rising clock edge	19.4		19.2		ns

(1) Timing parameters are referred to output clock specified in Table 6-139.
(2) The timing requirements are assured for the cycle jitter and duty cycle error conditions specified in Table 6-139.
(3) In datx, x is equal to 1, 2, 3, 4, 5, 6, or 7.

Table 6-139. MMC/SD/SDIO Switching Characteristics – Standard SD Mode

NO.	PARAMETER		1.15 V		1.0 V		UNIT
			MIN	MAX	MIN	MAX	
Standard SD Mode							
1/SD 1	$1/t_{c(clk)}$	Frequency (1), mmcx_clk(2)		24		12	MHz
SD2	$t_{W(clkH)}$	Typical pulse duration, output clk high	X(3)*PO(4)		X(3)*PO(4)		ns

(1) Related with the output clk maximum and minimum frequencies programmable in I/F module.
(2) In mmcx_clk, 'x' is equal to 1, 2, or 3.
(3) The X parameter is defined as shown in Table 6-140.
(4) PO = output clk period in ns.

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Table 6-139. MMC/SD/SDIO Switching Characteristics – Standard SD Mode (continued)

NO.	PARAMETER		1.15 V		1.0 V		UNIT
			MIN	MAX	MIN	MAX	
SD2	$t_{W(clkL)}$	Typical pulse duration, output clk low	Y[5]*PO[4]		Y[5]*PO[4]		ns
	$t_{dc(clk)}$	Duty cycle error, output clk		2083.3		4166.7	ps
	$t_{j(clk)}$	Jitter standard deviation[6], output clk		200		200	ps
MMC/SD/SDIO Interface 1 (1.8 V IO)							
	$t_{c(clk)}$	Rise time, output clk		10		10	ns
	$t_{W(clkH)}$	Fall time, output clk		10		10	ns
	$t_{W(clkL)}$	Rise time, output data		10		10	ns
	$t_{dc(clk)}$	Fall time, output data		10		10	ns
SD5	$t_{d(CLKOH-CMD)}$	Delay time, mmc1_clk rising clock edge to mmc1_cmd transition	6.1	35.5	6.3	77	ns
SD6	$t_{d(CLKOH-DATx)}$	Delay time, mmc1_clk rising clock edge to mmc1_datx transition	6.1	35.5	6.3	77	ns
MMC/SD/SDIO Interface 1 (3.0 V IO)							
	$t_{c(clk)}$	Rise time, output clk		10		10	ns
	$t_{W(clkH)}$	Fall time, output clk		10		10	ns
	$t_{W(clkL)}$	Rise time, output data		10		10	ns
	$t_{dc(clk)}$	Fall time, output data		10		10	ns
SD5	$t_{d(CLKOH-CMD)}$	Delay time, mmc1_clk rising clock edge to mmc1_cmd transition	6.1	35.5	6.3	77	ns
SD6	$t_{d(CLKOH-DATx)}$	Delay time, mmc1_clk rising clock edge to mmc1_datx transition	6.1	35.5	6.3	77	ns
MMC/SD/SDIO Interface 2							
	$t_{c(clk)}$	Rise time, output clk		10		10	ns
	$t_{W(clkH)}$	Fall time, output clk		10		10	ns
	$t_{W(clkL)}$	Rise time, output data		10		10	ns
	$t_{dc(clk)}$	Fall time, output data		10		10	ns
SD5	$t_{d(CLKOH-CMD)}$	Delay time, mmc2_clk rising clock edge to mmc2_cmd transition	6.1	35.5	6.3	77	ns
SD6	$t_{d(CLKOH-DATx)}$	Delay time, mmc2_clk rising clock edge to mmc2_datx transition	6.1	35.5	6.3	77	ns
MMC/SD/SDIO Interface 3							
	$t_{c(clk)}$	Rise time, output clk		10		10	ns
	$t_{W(clkH)}$	Fall time, output clk		10		10	ns
	$t_{W(clkL)}$	Rise time, output data		10		10	ns
	$t_{dc(clk)}$	Fall time, output data		10		10	ns
SD5	$t_{d(CLKOH-CMD)}$	Delay time, mmc3_clk rising clock edge to mmc3_cmd transition	6.1	35.5	6.3	77	ns
SD6	$t_{d(CLKOH-DATx)}$	Delay time, mmc3_clk rising clock edge to mmc3_datx transition	6.1	35.5	6.3	77	ns

(5) The Y parameter is defined as shown in Table 6-141.
(6) The jitter probability density can be approximated by a Gaussian function.

Table 6-140. X Parameter

CLKD	X
1 or Even	0.5
Odd	(trunk[CLKD/2]+1)/CLKD

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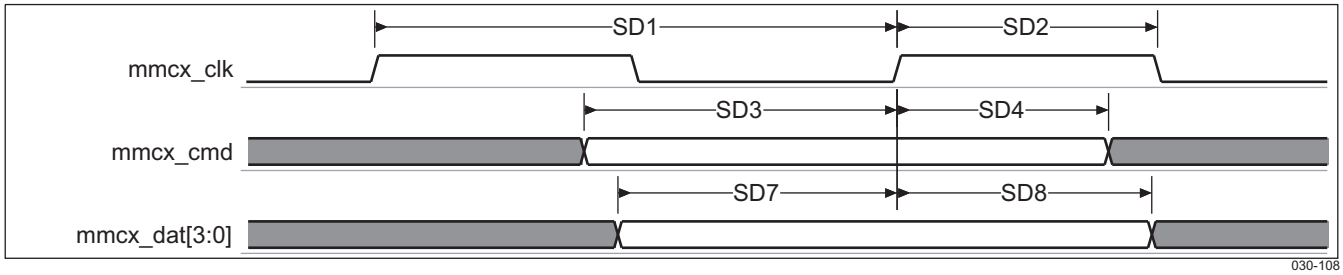
Table 6-141. Y Parameter

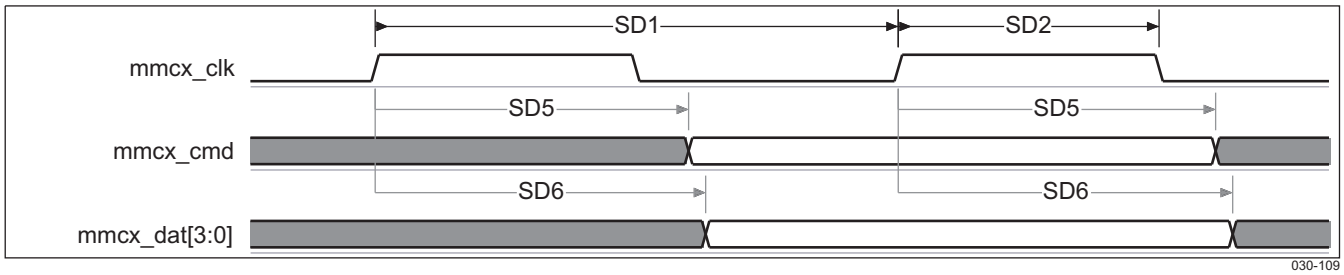
CLKD	Y
1 or Even	0.5
Odd	(trunk[CLKD/2])/CLKD

For details about clock division factor CLKD, see the *OMAP35x Technical Reference Manual (TRM)* [literature number SPRUF98].



In mmcx, x is equal to 1, 2, or 3.

Figure 6-67. MMC/SD/SDIO – Standard SD Mode – Data/Command Receive



In mmcx, x is equal to 1, 2, or 3.

Figure 6-68. MMC/SD/SDIO – Standard SD Mode – Data/Command Transmit

6.8 Test Interfaces

The emulation and trace interfaces allow tracing activities of the following CPUs:

- ARM1136JF-STM through an Embedded Trace Macro-cell (ETM11) dedicated to enable real-time trace of the ARM subsystem operations and a Serial Debug Trace Interface (SDTI)
- IVA2 DSP through a high-speed real-time data exchange (HS-RTDX) controller

All processors can be emulated via JTAG ports.

6.8.1 Embedded Trace Macro Interface (ETM)

Table 6-142 assumes testing over the recommended operating conditions (see Figure 6-69).

Table 6-142. Embedded Trace Macro Interface Switching Characteristics(1)

NO.	PARAMETER		1.15 V		UNIT
			MIN	MAX	
f	$1/t_{c(CLK)}$	Frequency, etk_clk		166	MHz
ETM0	$t_{c(CLK)}$	Cycle time(2), etk_clk	6		ns
ETM1	$t_{W(CLK)}$	Clock pulse width, etk_clk	2.7		ns
ETM2	$t_{d(CLK-CTL)}$	Delay time, etk_clk clock edge to etk_ctl transition	–0.5	0.5	ns
ETM3	$t_{d(CLK-D)}$	Delay time, etk_clk clock high to etk_d[15:0] transition	–0.5	0.5	ns

(1) The capacitive load is equivalent to 25 pF.
(2) Cycle time is given by considering a jitter of 5%.

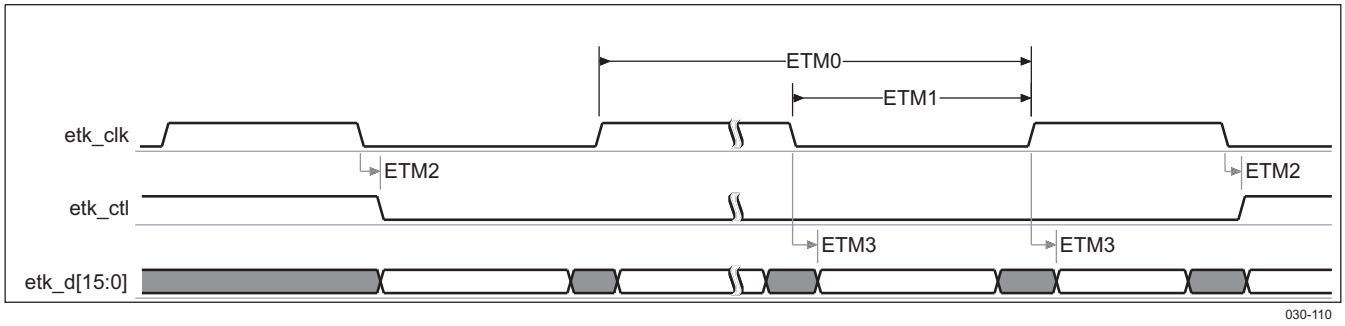


Figure 6-69. Embedded Trace Macro Interface

6.8.2 System Debug Trace Interface (SDTI)

The system debug trace interface (SDTI) module provides real-time software tracing functionality to the OMAP3530/25 device.

The trace interface has four trace data pins and a trace clock pin.

This interface is a dual-edge interface: the data are available on rising and falling edges of sdti_clk but can be also configured in single edge mode where data are available on falling edge of sdti_clk.

Serial interface operates in clock stop regime: serial clock is not free running, when there is no trace data there is no trace clock.

6.8.2.1 System Debug Trace Interface in Dual-Edge Mode

Table 6-144 assumes testing over the recommended operating conditions and electrical characteristic conditions (see Figure 6-70).

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Table 6-143. System Debug Trace Interface Timing Conditions – Dual-Edge Mode

TIMING CONDITION PARAMETER		VALUE	UNIT
Output Conditions			
C_{LOAD}	Output load capacitance	25	pF

Table 6-144. System Debug Trace Interface Switching Characteristics – Dual-Edge Mode

NO.	PARAMETER			1.15 V		1.0 V		UNIT
				MIN	MAX	MIN	MAX	
SD1	$t_{c(CLK)}$	Cycle time, sdti_clk period		29		29		ns
SD2	$t_{w(CLK)}$	Typical pulse duration, sdti_clk high or low		0.5*P (1)		0.5*P (1)		ns
	$t_{dc(CLK)}$	Duty cycle error, sdti_clk		–1.2	1.2	–1.2	1.2	ns
	$t_{R(CLK)}$	Rise time, sdti_clk			5		5	ns
	$t_{F(CLK)}$	Fall time, sdti_clk			5		5	ns
SD3	$t_{d(CLK-TxD)}$	Delay time, sdti_clk transition to sdti_txd[3:0] transition	Multiplexing mode on etk pins	2.3	10.9	2.3	10.9	ns
			Multiplexing mode on jtag_emu pins	2.3	13.9	2.3	13.9	
	$t_{R(CLK)}$	Rise time, sdti_txd[3:0]			5		5	ns
	$t_{F(CLK)}$	Fall time, sdti_txd[3:0]			5		5	ns

(1) P = sdti_clk clock period

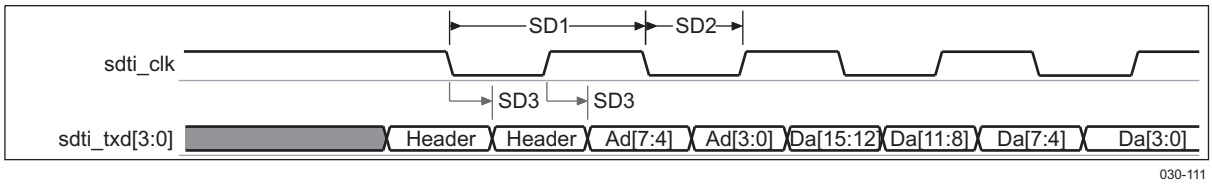

Figure 6-70. System Debug Trace Interface – Dual-Edge Mode

6.8.2.2 System Debug Trace Interface in Single-Edge Mode

Table 6-146 assumes testing over the recommended operating conditions and electrical characteristic conditions (see Figure 6-71).

Table 6-145. System Debug Trace Interface Timing Conditions – Single-Edge Mode

TIMING CONDITION PARAMETER		VALUE	UNIT
Output Conditions			
C_{LOAD}	Output load capacitance	25	pF

Table 6-146. System Debug Trace Interface Switching Characteristics – Single-Edge Mode

NO.	PARAMETER			1.15 V		1.0 V		UNIT
				MIN	MAX	MIN	MAX	
SD1	$t_{c(CLK)}$	Cycle time, sdti_clk period		29		29		ns
SD2	$t_{w(CLK)}$	Typical pulse duration, sdti_clk high or low		0.5*P (1)		0.5*P (1)		ns
	$t_{dc(CLK)}$	Duty cycle error, sdti_clk		–1.2	1.2	–1.2	1.2	ns
	$t_{R(CLK)}$	Rise time, sdti_clk			5		5	ns
	$t_{F(CLK)}$	Fall time, sdti_clk			5		5	ns
SD3	$t_{d(CLK-TxD)}$	Delay time, sdti_clk transition to sdti_txd[3:0] transition	Multiplexing mode on etk pins	2.3	26.5	2.3	26.5	ns
			Multiplexing mode on jtag_emu pins	2.3	33.2	2.3	33.2	
	$t_{R(CLK)}$	Rise time, sdti_txd[3:0]			5		5	ns

(1) P = sdti_clk clock period.

Table 6-146. System Debug Trace Interface Switching Characteristics – Single-Edge Mode (continued)

NO.	PARAMETER		1.15 V		1.0 V		UNIT
			MIN	MAX	MIN	MAX	
	$t_{F(CLK)}$	Fall time, sdti_txd[3:0]		5		5	ns

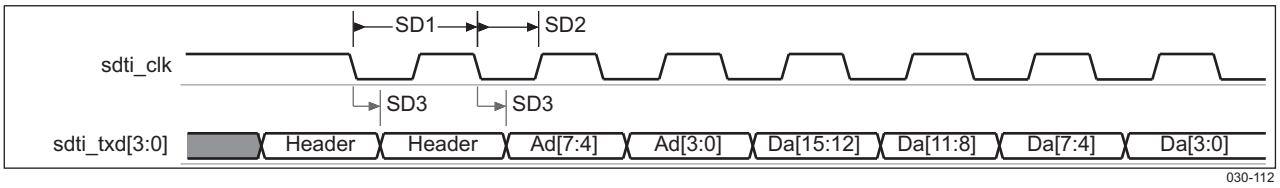

Figure 6-71. System Debug Trace Interface – Single-Edge Mode

6.8.3 JTAG Interfaces

OMAP3530/25 JTAG TAP controller handles standard IEEE JTAG interfaces. The following sections define the timing requirements for several tools used to test the OMAP3530/25 processors as:

- Free running clock tool, like XDS560 and XDS510 tools
- Adaptive clock tool, like RealView® ICE tool and Lauterbach™ tool

6.8.3.1 JTAG – Free Running Clock Mode

Table 6-148 and Table 6-149 assume testing over the recommended operating conditions and electrical characteristic conditions (see Figure 6-72).

Table 6-147. JTAG Timing Conditions – Free Running Clock Mode

TIMING CONDITION PARAMETER		VALUE	UNIT
Input Conditions			
t_R	Input signal rise time	5	ns
t_F	Input signal fall time	5	ns
Output Conditions			
C_{LOAD}	Output load capacitance	30	pF

Table 6-148. JTAG Timing Requirements – Free Running Clock Mode(1)

NO.	PARAMETER		1.15 V		1.0 V		UNIT
			MIN	MAX	MIN	MAX	
JT4	$t_{c(tck)}$	Cycle time(2), jtag_tck period	25		33		ns
JT5	$t_{w(tckL)}$	Typical pulse duration, jtag_tck low	0.5*P(3)		0.5*P(3)		ns
JT6	$t_{w(tckH)}$	Typical pulse duration, jtag_tck high	0.5*P(3)		0.5*P(3)		ns
	$t_{dc(tck)}$	Duty cycle error, jtag_tck	–1250	1250	–1667	1667	ps
	$t_{j(tck)}$	Cycle jitter(4), jtag_tck	–1250	1250	–1667	1667	ps
JT7	$t_{su(tdiV-rtckH)}$	Setup time, jtag_tdi valid before jtag_rtck high	1.8		1.8		ns
JT8	$t_{h(tdiV-rtckH)}$	Hold time, jtag_tdi valid after jtag_rtck high	0.7		1		ns
JT9	$t_{su(tmsV-rtckH)}$	Setup time, jtag_tms valid before jtag_rtck high	1.8		1.8		ns
JT10	$t_{h(tmsV-rtckH)}$	Hold time, jtag_tms valid after jtag_rtck high	0.7		1		ns
JT12	$t_{su(emuxV-rtckH)}$	Setup time, jtag_emux(5) valid before jtag_rtck high	14.6		19.8		ns
JT13	$t_{h(emuxV-rtckH)}$	Hold time,jtag_emux(5) valid after jtag_rtck high	2		2.7		ns

(1) The timing requirements are assured for the cycle jitter and duty cycle error conditions specified.
(2) Related with the input maximum frequency supported by the JTAG module.
(3) P = jtag _tck period in ns.
(4) Maximum cycle jitter supported by jtag _tck input clock.
(5) x = 0 to 1

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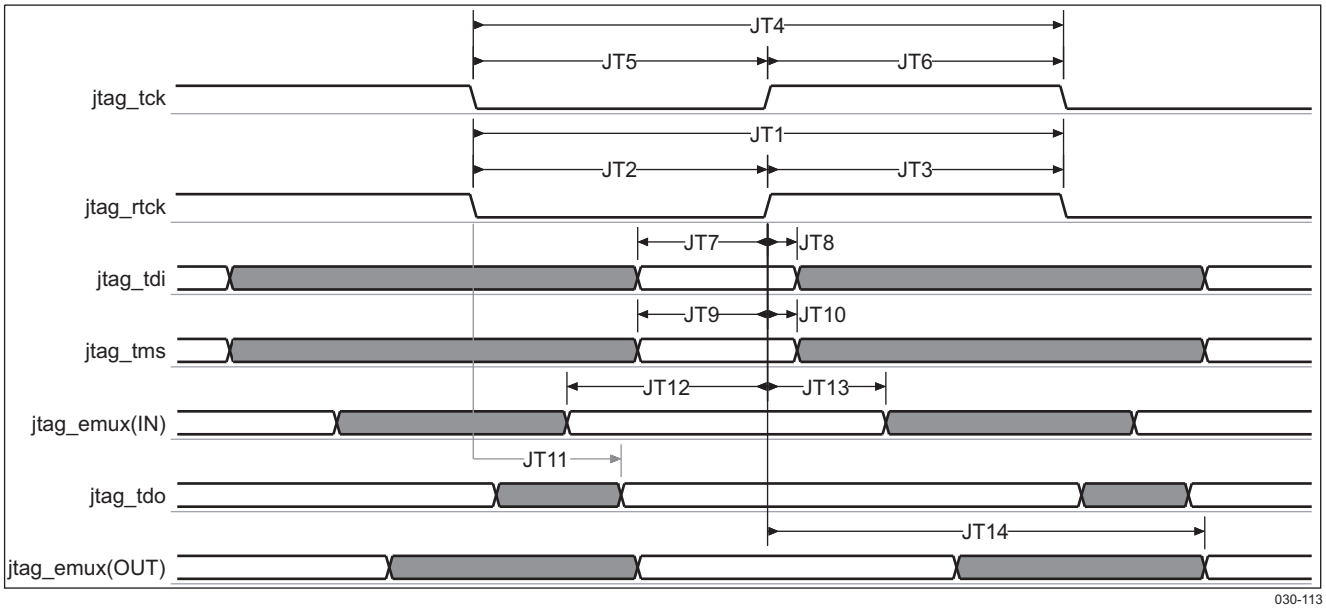
Table 6-149. JTAG Switching Characteristics – Free Running Clock Mode

NO.	PARAMETER		1.15 V		1.0 V		UNIT
			MIN	MAX	MIN	MAX	
JT1	$t_{c(rtck)}$	Cycle time(1), jtag_rtck period	25		33		ns
JT2	$t_{w(rtckL)}$	Typical pulse duration, jtag_rtck low	0.5*PO(2)		0.5*PO(2)		ns
JT3	$t_{w(rtckH)}$	Typical pulse duration, jtag_rtck high	0.5*PO(2)		0.5*PO(2)		ns
	$t_{dc(rtck)}$	Duty cycle error, jtag_rtck	–1250	1250	–1667	1667	ps
	$t_{j(rtck)}$	Jitter standard deviation(3), jtag_rtck		33.3		33.3	ps
	$t_{R(rtck)}$	Rise time, jtag_rtck		4		4	ns
	$t_{F(rtck)}$	Fall time, jtag_rtck		4		4	ns
JT11	$t_{d(rtckL-tdoV)}$	Delay time, jtag_rtck low to jtag_tdo valid	–5.8	5.8	–7.9	7.9	ns
	$t_{R(tdo)}$	Rise time, jtag_tdo		4		4	ns
	$t_{F(tdo)}$	Fall time, jtag_tdo		4		4	ns
JT14	$t_{d(rtckH-emuxV)}$	Delay time, jtag_rtck high to ,jtag_emux(4) valid	2.7	15.1	2.7	20.4	ns
	$t_{R(emux)}$	Rise time, jtag_emux(4)		6		6	ns
	$t_{F(emux)}$	Fall time, jtag_emux(4)		6		6	ns

(1) Related with the jtag_rtck maximum frequency.
(2) PO = jtag _rtck period in ns.
(3) The jitter probability density can be approximated by a Gaussian function.
(4) x = 0 to 1



In jtag_emux, x is equal to 0 to 1.

Figure 6-72. JTAG Interface Timing – Free Running Clock Mode

6.8.3.2 JTAG – Adaptive Clock Mode

Table 6-151 and Table 6-152 assume testing over the recommended operating conditions and electrical characteristic conditions (see Figure 6-73):

Table 6-150. JTAG Timing Conditions – Adaptive Clock Mode

TIMING CONDITION PARAMETER		VALUE	UNIT
Input Conditions			
t_R	Input signal rise time	5	ns
t_F	Input signal fall time	5	ns

Table 6-150. JTAG Timing Conditions – Adaptive Clock Mode (continued)

TIMING CONDITION PARAMETER		VALUE	UNIT
Output Conditions			
C_{LOAD}	Output load capacitance	30	pF

Table 6-151. JTAG Timing Requirements – Adaptive Clock Mode(1)

NO.	PARAMETER		1.15 V		1.0 V		UNIT
			MIN	MAX	MIN	MAX	
JA4	$t_{c(tck)}$	Cycle time(2), jtag_tck period	50		50		ns
JA5	$t_{w(tckL)}$	Typical pulse duration, jtag_tck low	0.5*P(3)		0.5*P(3)		ns
JA6	$t_{w(tckH)}$	Typical pulse duration, jtag_tck high	0.5*P(3)		0.5*P(3)		ns
	$t_{dc(lclk)}$	Duty cycle error, jtag_tck	–2500	2500	–2500	2500	ps
	$t_{j(lclk)}$	Cycle jitter(4), jtag_tck	–1500	1500	–1500	1500	ps
JA7	$t_{su(tdiV-tckH)}$	Setup time, jtag_tdi valid before jtag_tck high	13.8		13.8		ns
JA8	$t_{h(tdiV-tckH)}$	Hold time, jtag_tdi valid after jtag_tck high	13.8		13.8		ns
JA9	$t_{su(tmsV-tckH)}$	Setup time, jtag_tms valid before jtag_tck high	13.8		13.8		ns
JA10	$t_{h(tmsV-tckH)}$	Hold time, jtag_tms valid after jtag_tck high	13.8		13.8		ns

(1) The timing requirements are assured for the cycle jitter and duty cycle error conditions specified.
(2) Related with the input maximum frequency supported by the JTAG module.
(3) P = jtag _tck period in ns.
(4) Maximum cycle jitter supported by jtag _tck input clock.

Table 6-152. JTAG Switching Characteristics – Adaptive Clock Mode

NO.	PARAMETER		1.15 V		1.0 V		UNIT
			MIN	MAX	MIN	MAX	
JA1	$t_{c(rtck)}$	Cycle time(1), jtag_rtck period	50		50		ns
JA2	$t_{w(rtckL)}$	Typical pulse duration, jtag_rtck low	0.5*PO(2)		0.5*PO(2)		ns
JA3	$t_{w(rtckH)}$	Typical pulse duration, jtag_rtck high	0.5*PO(2)		0.5*PO(2)		ns
	$t_{dc(rtck)}$	Duty cycle error, jtag_rtck	–2500	2500	–2500	2500	ps
	$t_{j(rtck)}$	Jitter standard deviation(3), jtag_rtck		33.3		33.3	ps
	$t_{R(rtck)}$	Rise time, jtag_rtck		4		4	ns
	$t_{F(rtck)}$	Fall time, jtag_rtck		4		4	ns
JA11	$t_{d(rtckL-tdoV)}$	Delay time, jtag_rtck low to jtag_tdo valid	–14.6	14.6	–14.6	14.6	ns
	$t_{R(tdo)}$	Rise time, jtag_tdo,		4		4	ns
	$t_{F(tdo)}$	Fall time, jtag_tdo		4		4	ns

(1) Related with the jtag _rtck maximum frequency programmable.
(2) PO = jtag _rtck period in ns.
(3) The jitter probability density can be approximated by a Gaussian function.

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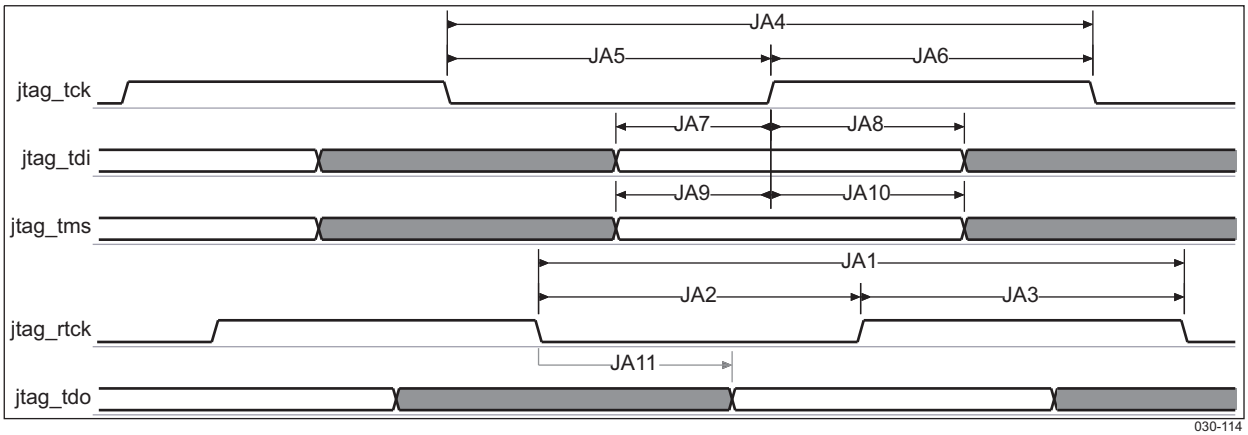

Figure 6-73. JTAG Interface Timing – Adaptive Clock Mode

7 PACKAGE CHARACTERISTICS

7.1 Package Thermal Resistance

Table 7-1 provides the thermal resistance characteristics for the recommended package types used on the OMAP3530/25 Applications Processor.

Table 7-1. OMAP3530/25 Thermal Resistance Characteristics(1) (2)

Package	Power (W)(3)	$R_{\theta JA}$(°C/W)	$R_{\theta JB}$(°C/W)	$R_{\theta JC}$(°C/W)(4)	Board Type
OMAP3530/25 (CBB Pkg.)	0.92871	24.46	10.94	See (5)	2S2P(6)
OMAP3530/25 (CBC Pkg.)	0.92871	21.89	6.23	See (5)	2S2P(6)
OMAP3530/25 (CUS Pkg.)	0.92871	23.69	8.1	2.31	2S2P(6)

(1) $R_{\theta JA}$ (Theta-JA) = Thermal Resistance Junction-to-Ambient, °C/W
(2) This table provides simulation data and may not represent actual use-case values.
$R_{\theta JB}$ (Theta-JB) = Thermal Resistance Junction-to-Board, °C/W
$R_{\theta JC}$ (Theta-JC) = Thermal Resistance Junction-to-Case, °C/W
(3) These numbers are based on simulation results and don't necessarily represent the wattage that the part will take in actual use.
(4) It is recommended to dissipate the heat to the board instead of attempting to remove it from the top of the chip; therefore, top-side heat sinks should not be used for package.
(5) Not applicable if the POP package has a memory package on top; no heat sink can be used.
(6) The board types are defined by JEDEC (reference JEDEC standard JESD51-9, Test Board for Area Array Surface Mount Package Thermal Measurements).

7.2 Device Support

7.2.1 Device and Development-Support Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all OMAP processors and support tools. Each OMAP device has one of three prefixes: X, P, or null (no prefix). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMDX) through fully qualified production devices/tools (TMDS).

Device development evolutionary flow:

X Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow. (TMX definition)

P Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications. (TMP definition)

null Production version of the silicon die that is fully qualified. (TMS definition)

Support tool development evolutionary flow:

TMDX Development support product that has not yet completed Texas Instruments internal qualification testing.

TMDS Fully qualified development support product.

TMX and TMP devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

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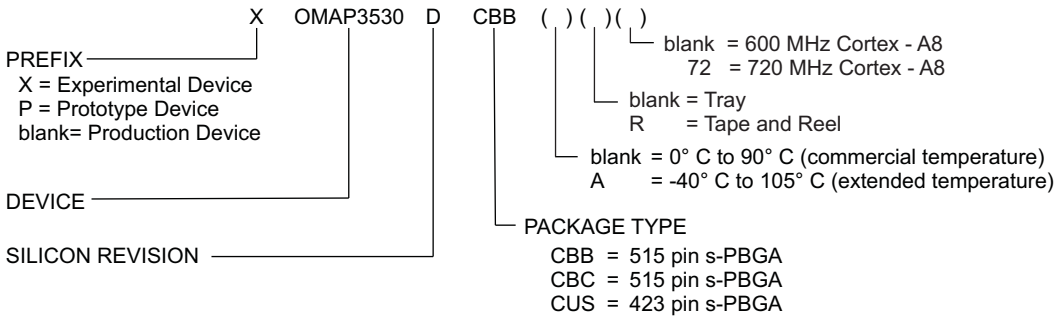
Predictions show that prototype devices (X or P), have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

For additional description of the device nomenclature markings, see the *OMAP3530/25/15/03 Applications Processor Silicon Errata* (literature number SPRZ278).



A. For more information on the silicon revision, please see the *OMAP3530/25/15/03 Applications Processor Silicon Errata* (literature number SPRZ278).

Figure 7-1. Device Nomenclature

7.2.2 Documentation Support

7.2.2.1 Related Documentation from Texas Instruments

The following documents describe the OMAP3530/25 Applications Processor. Copies of these documents are available on the Internet at www.ti.com. Tip: Enter the literature number in the search box provided at www.ti.com.

The current documentation that describes the OMAP3530/25 Applications Processor, related peripherals, and other technical collateral, is available in the product folder at: www.ti.com.

SPRUF98 ***OMAP35x Technical Reference Manual***. Collection of documents providing detailed information on the OMAP3 architecture including power, reset, and clock control, interrupts, memory map, and switch fabric interconnect. Detailed information on the microprocessor unit (MPU) subsystem, the image, video, and audio (IVA2.2) subsystem, as well a functional description of the peripherals supported on OMAP35x devices is also included.

SPRU732 ***TMS320C64x/C64x+ DSP CPU and Instruction Set Reference Guide.*** Describes the CPU architecture, pipeline, instruction set, and interrupts for the TMS320C64x and TMS320C64x+ digital signal processors (DSPs) of the TMS320C6000 DSP family. The C64x/C64x+ DSP generation comprises fixed-point devices in the C6000 DSP platform. The C64x+ DSP is an enhancement of the C64x DSP with added functionality and an expanded instruction set.

SPRU871 ***TMS320C64x+ DSP Megamodule Reference Guide.*** Describes the TMS320C64x+ digital signal processor (DSP) megamodule. Included is a discussion on the internal direct memory access (IDMA) controller, the interrupt controller, the power-down controller, memory protection, bandwidth management, and the memory and cache.

SPRU889 ***High-Speed DSP Systems Design Reference Guide.*** Provides recommendations for meeting the many challenges of high-speed DSP system design. These recommendations include information about DSP audio, video, and communications systems for the C5000 and C6000 DSP platforms.

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7.2.2.2 Related Documentation from Other Sources

The following documents are related to the OMAP3530/25 Applications Processor. Copies of these documents can be obtained directly from the internet or from your Texas Instruments representative.

Cortex™-A8 Technical Reference Manual. This is the technical reference manual for the Cortex-A8 processor. A copy of this document can be obtained via the internet at http://infocenter.arm.com. Please see the *OMAP35x Applications Processor Silicon Errata* (literature number SPRZ278) to determine the revision of the Cortex-A8 core used on your device.

ARM Core Cortex™-A8 (AT400/AT401) Errata Notice. Provides a list of advisories for the different revisions of the Cortex-A8 processor. Contact your TI representative for a copy of this document. Please see the *OMAP35x Applications Processor Silicon Errata* (literature number SPRZ278) to determine the revision of the Cortex-A8 core used on your device.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
3530ECBCAMERCURY	LIFEBUY	POP-FCBGA	CBC	515	119	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	0 to 0	3530ECBC A	
3530ECUSAGRM	ACTIVE	FCBGA	CUS	423	90	Green (RoHS & no Sb/Br)	SNAGCU	Level-4-260C-72 HR	-40 to 105	3530ECUS A	Samples
OMAP3525ECBB	ACTIVE	POP-FCBGA	CBB	515	168	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	0 to 90	3525ECBB	Samples
OMAP3525ECBBA	ACTIVE	POP-FCBGA	CBB	515	168	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 105	3525ECBB A	Samples
OMAP3525ECBC	LIFEBUY	POP-FCBGA	CBC	515	119	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	0 to 0	3525ECBC	
OMAP3525ECBCA	LIFEBUY	POP-FCBGA	CBC	515	119	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	0 to 0	3525ECBC A	
OMAP3525ECUS	ACTIVE	FCBGA	CUS	423	90	Green (RoHS & no Sb/Br)	SNAGCU	Level-4-260C-72 HR	0 to 90	3525ECUS	Samples
OMAP3525ECUSA	ACTIVE	FCBGA	CUS	423	90	Green (RoHS & no Sb/Br)	SNAGCU	Level-4-260C-72 HR	-40 to 105	3525ECUS A	Samples
OMAP3530ECBB	ACTIVE	POP-FCBGA	CBB	515	168	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	0 to 90	3530ECBB	Samples
OMAP3530ECBB72	ACTIVE	POP-FCBGA	CBB	515	168	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	0 to 90	3530ECBB72	Samples
OMAP3530ECBBA	ACTIVE	POP-FCBGA	CBB	515	168	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 105	3530ECBB A	Samples
OMAP3530ECBBALPD	ACTIVE	POP-FCBGA	CBB	515	168	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 105	3530ECBB A	Samples
OMAP3530ECBBAR	ACTIVE	POP-FCBGA	CBB	515	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR		3530ECBB A	Samples
OMAP3530ECBBLPD	ACTIVE	POP-FCBGA	CBB	515	168	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	0 to 90	3530ECBB	Samples
OMAP3530ECBC	LIFEBUY	POP-FCBGA	CBC	515	119	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	0 to 0	3530ECBC	
OMAP3530ECBC72	LIFEBUY	POP-FCBGA	CBC	515	119	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	0 to 0	3530ECBC72	
OMAP3530ECBCA	LIFEBUY	POP-FCBGA	CBC	515	119	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	0 to 0	3530ECBC A	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OMAP3530ECUS	ACTIVE	FCBGA	CUS	423	90	Green (RoHS & no Sb/Br)	SNAGCU	Level-4-260C-72 HR	0 to 90	3530ECUS	Samples
OMAP3530ECUS72	ACTIVE	FCBGA	CUS	423	90	Green (RoHS & no Sb/Br)	SNAGCU	Level-4-260C-72 HR	0 to 90	3530ECUS72	Samples
OMAP3530ECUSA	ACTIVE	FCBGA	CUS	423	90	Green (RoHS & no Sb/Br)	SNAGCU	Level-4-260C-72 HR	-40 to 105	3530ECUS A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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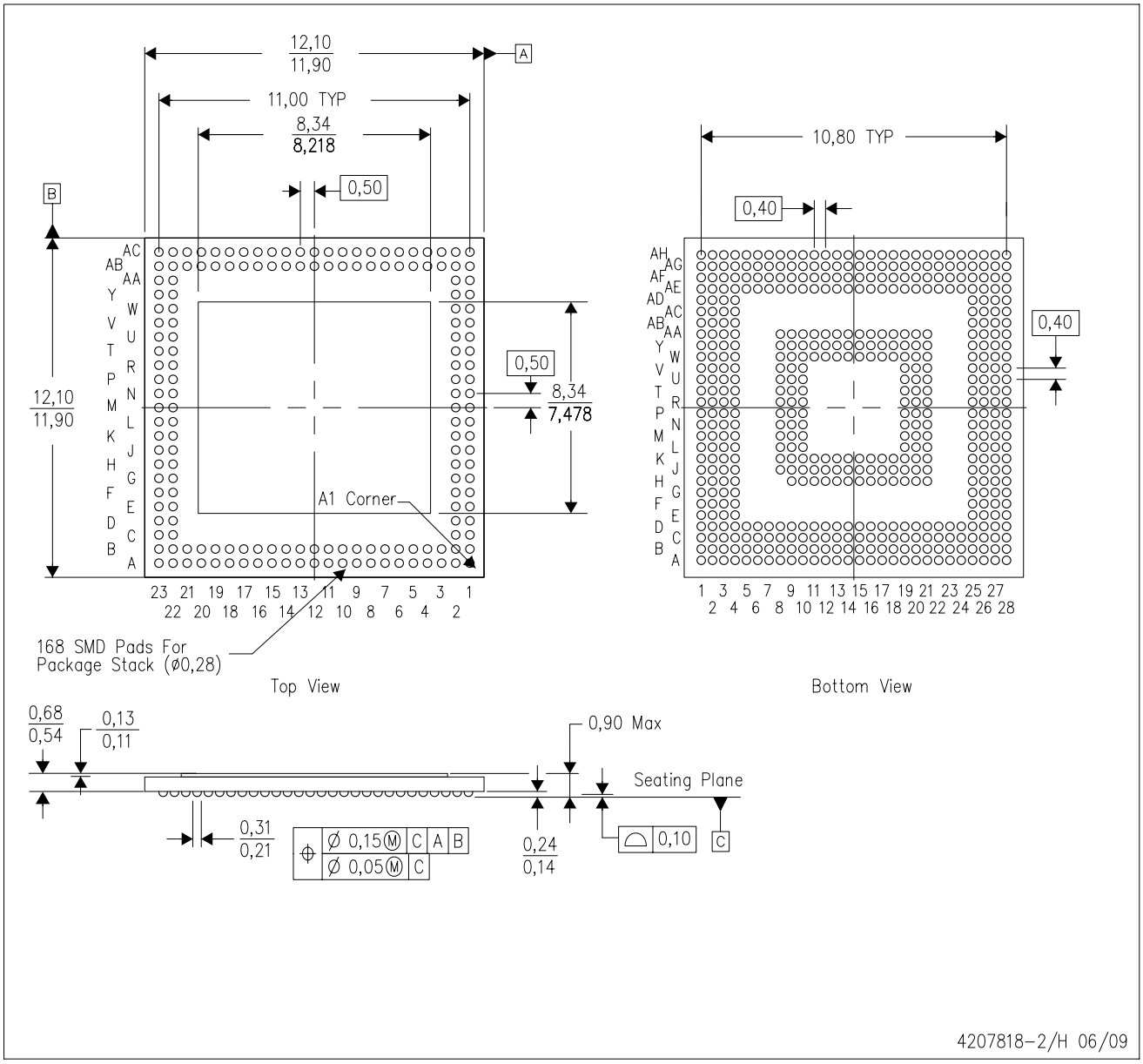
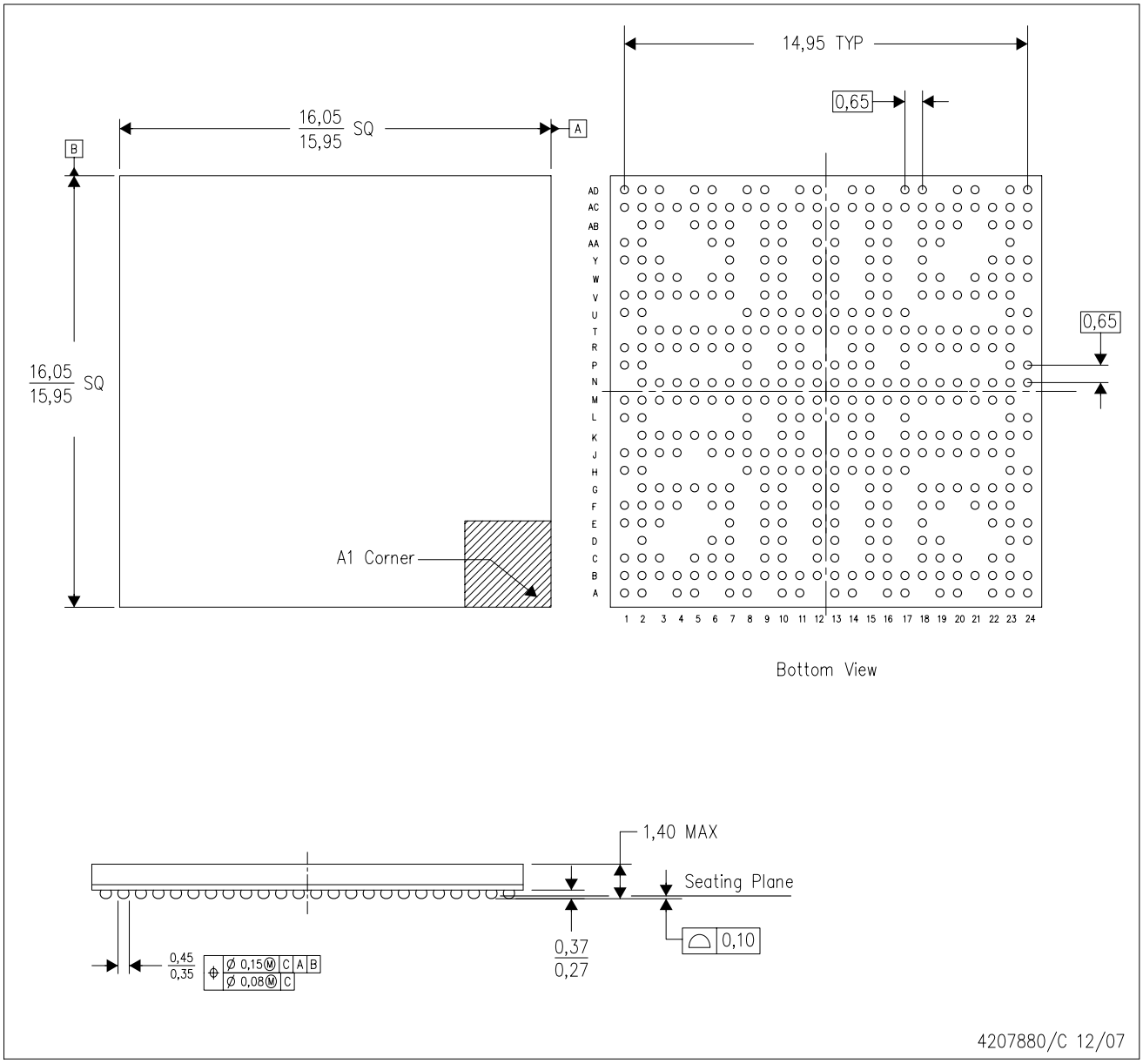
CBB (S–PBGA–N515) PLASTIC BALL GRID ARRAY



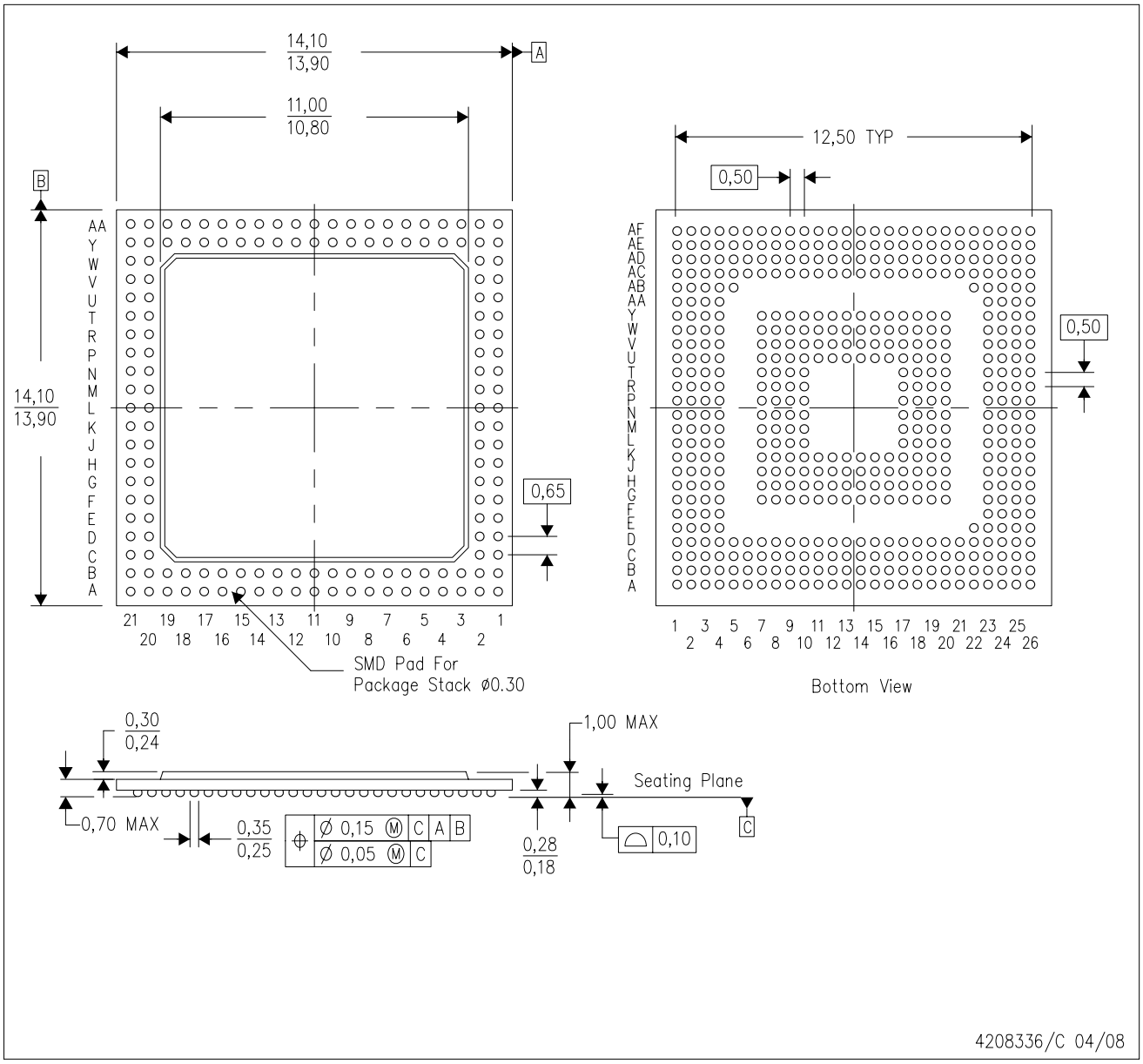
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Flip chip application only.
D. Pb–free die bump and solder ball.

CUS (S–PBGA–N423) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Flip chip application only.
D. Lead–free die bump and solder ball.

CBC (S–PBGA–N515) PLASTIC BALL GRID ARRAY



NOTES:
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B. This drawing is subject to change without notice.
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D. Lead–free die bump and solder ball.

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