# MHT2012N 2400-2500 MHz REFERENCE CIRCUIT

ORDERABLE PART NUMBER: **MHT2012N-2450**

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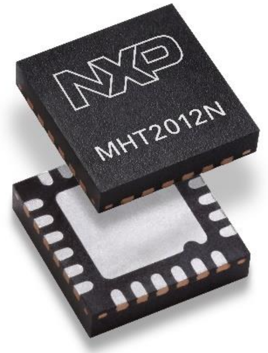
# Introduction

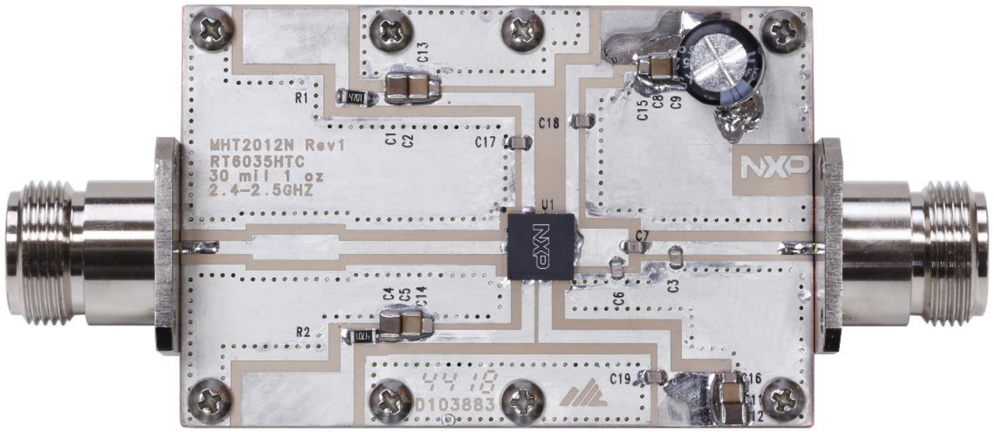
- The NXP MHT2012N is a 2400-2500 MHz, 12.5 W CW RF power LDMOS integrated circuit housed in a PQFN over-molded plastic package. It has 50 ohm input matching, inter-stage matching and no output matching.
  - Further details about the device, including its data sheet, are available here.

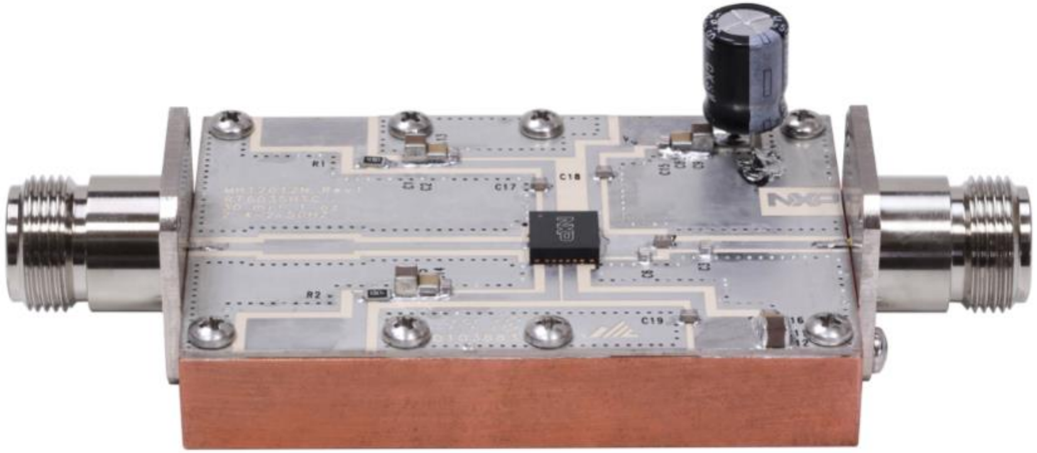
- The following pages describe the 2400-2500 MHz reference circuit (evaluation board).
  Its typical applications are RF Energy and driver for RF cooking.

- The reference circuit can be ordered through NXP's distribution partners and etailers under part number MHT2012N-2450.

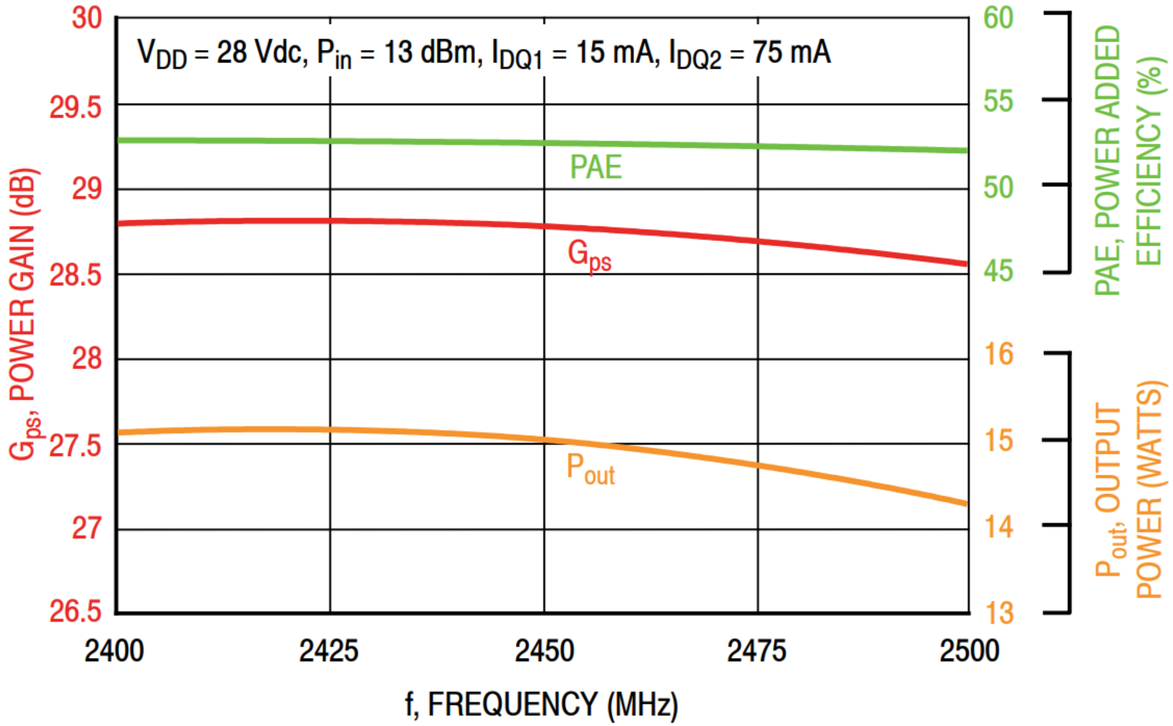


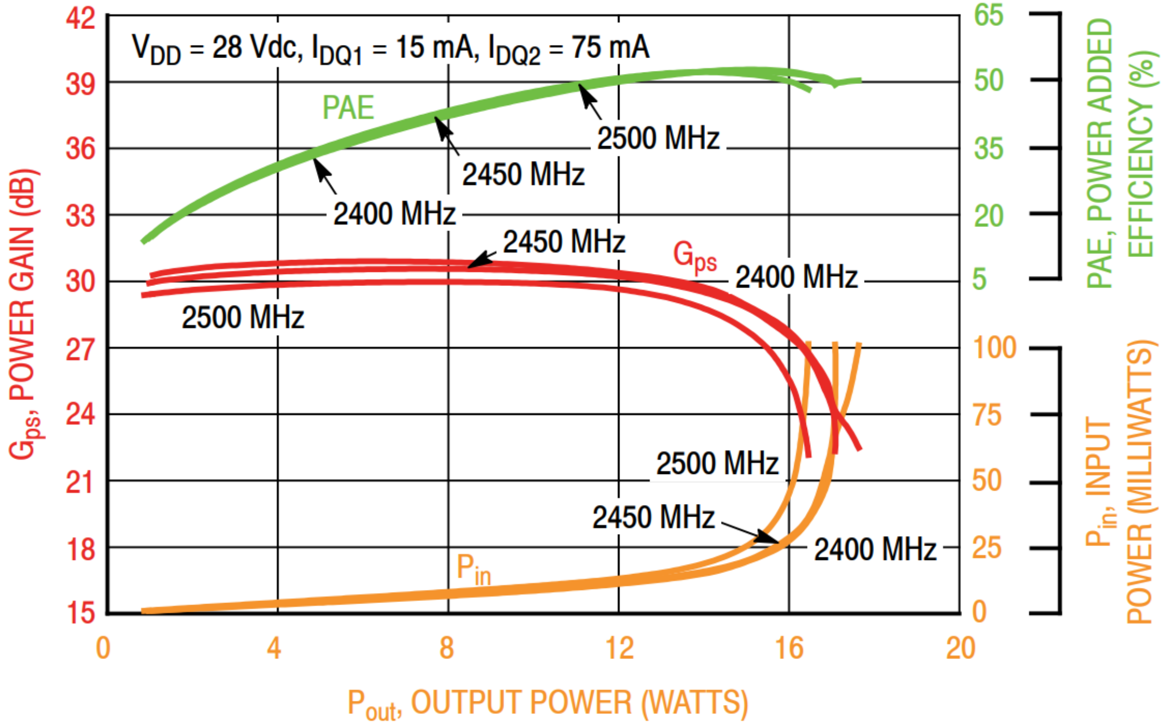
# **Circuit Overview** – 5.08 cm × 7.62 cm (2.0″ × 3.0″)



# Typical CW Performance



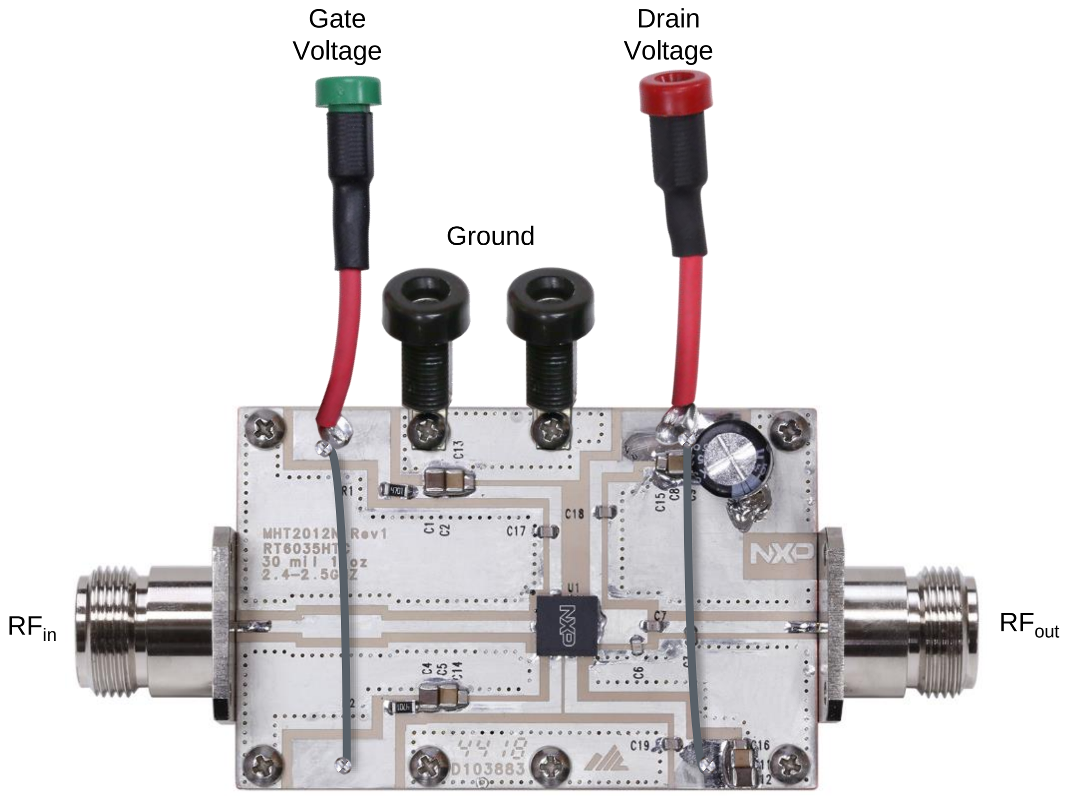




**Typical Performance:** $V_{DD}$ = 28 Vdc, $P_{in}$ = 11 dBm, $I_{DQ1}$ = 15 mA, $I_{DQ2}$ = 75 mA

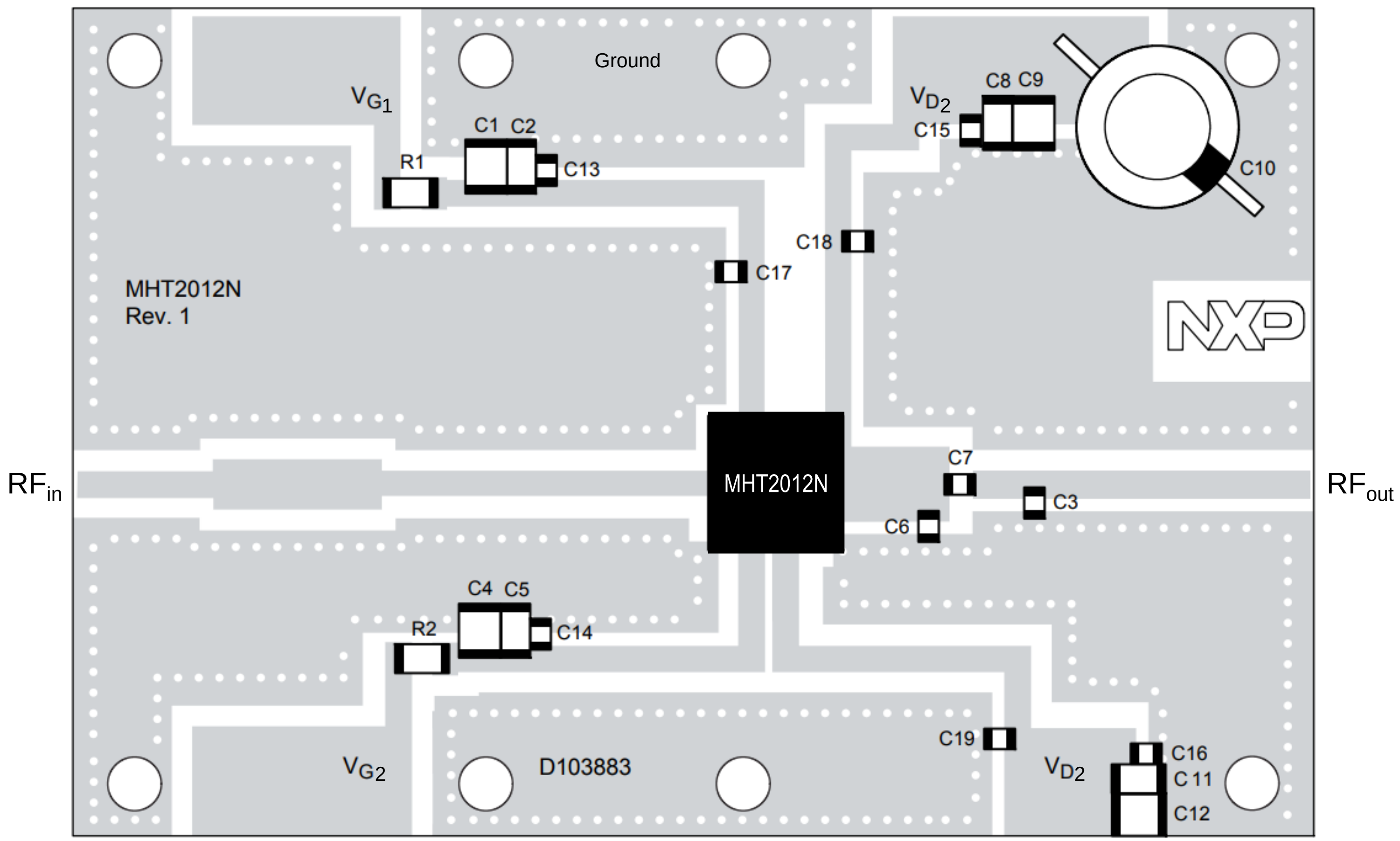
| Frequency (MHz) | Signal Type | $G_{ps}$ (dB) | PAE (%) | $P_{out}$ (W) |
|---|---|---|---|---|
| 2400 | CW | 30.1 | 51.3 | 13.0 |
| 2450 | | 30.0 | 51.4 | 12.7 |
| 2500 | | 29.7 | 50.5 | 11.7 |

# Quick Start

1. Mount the reference circuit onto a heatsink capable of dissipating more than 10 W in order to provide enough thermal dissipation
2. Connect the ground.
3. Terminate the RF output with a 50 ohm load capable of handling more than 11 W.
4. Connect the RF input to a 50 ohm source with the RF off.
5. Connect the gate voltage, set to 0 V.
6. Connect the drain voltage ($V_{DD}$) and raise it slowly to 28 V. Current should be 0 A.
7. Raise the gate voltage slowly until the drain current reaches the desired level (typical drain quiescent current for the first stage $I_{DQ1}$ = 15 mA, for the second stage $I_{DQ2}$ = 75 mA, with gate voltage typically around 4.8 V for both stages).
8. Raise the RF input slowly to 13 dBm.
9. Check the RF output power (typically 12 W), the drain current (around 1 A for this power level) and the temperature of the board.



# Component Placement Reference

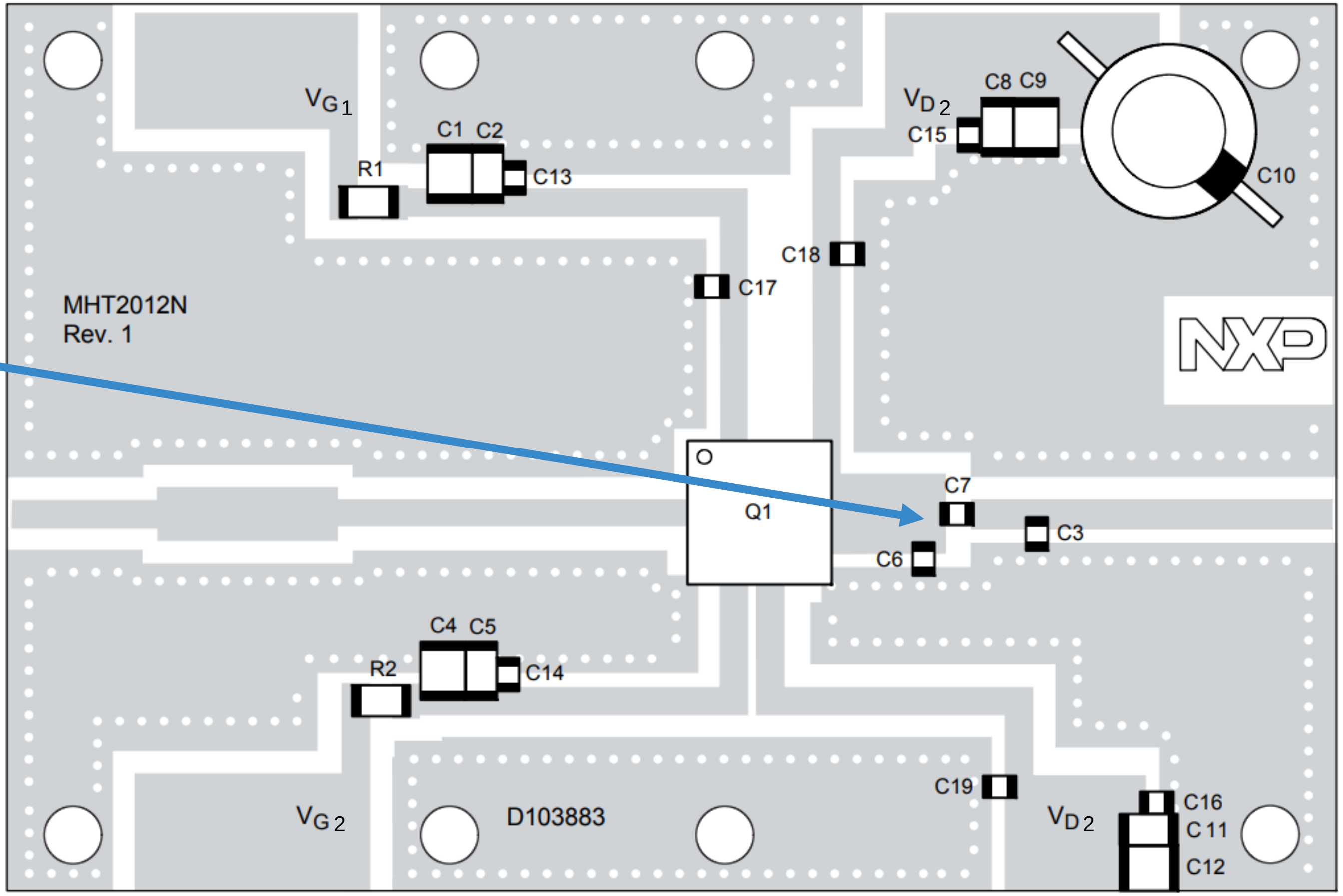


# Bill of Materials

| Part | Description | Part Number | Manufacturer |
|---|---|---|---|
| C1, C4, C9, C12 | 10 μF Chip Capacitor | GRM32ER61H106KA12L | Murata |
| C2, C5, C8, C11 | 0.1 μF Chip Capacitor | GRM32NR72A104KA01B | Murata |
| C3 | 0.5 pF Chip Capacitor | ATC600F0R5BT250XT | ATC |
| C6 | 1.6 pF Chip Capacitor | ATC600F1R6BT250XT | ATC |
| C7 | 4.7 pF Chip Capacitor | ATC600F4R7BT250XT | ATC |
| C10 | 220 μF, 50 V Electrolytic Capacitor | 227CKS050M | Illinois Capacitor |
| C13, C14, C15, C16, C17, C18, C19 | 5.6 pF Chip Capacitor | ATC600F5R6BT250XT | ATC |
| Q1 | RF Power LDMOS Transistor | MHT2012N | NXP |
| R1, R2 | 4.7 kΩ, 1/4 W Chip Resistor | CRCW12064K70FKEA | Vishay |
| PCB | Rogers RT6035HTC, 0.030″, $\varepsilon_r$ = 3.5 | D103883 | MTL |

# Tuning Tips

Moving C6 closer to C7 increases efficiency



# Load Pull Performance

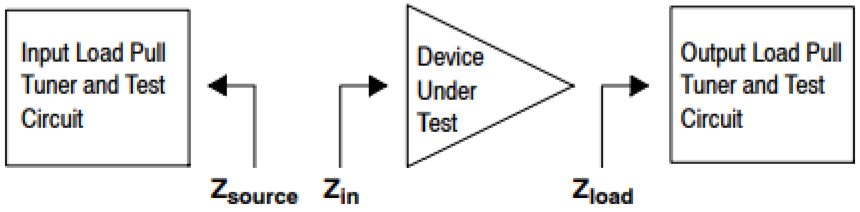
| f (MHz) | $Z_{source}$ (Ω) | $Z_{in}$ (Ω) | Max Efficiency | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | P1dB | | | | | |
| | | | $Z_{load}$ (1) (Ω) | Gain (dB) | (dBm) | (W) | $\eta_D$ (%) | PAE (%) |
| 2400 | 40.9 + j23.6 | 58.6 – j22.8 | 4.19 – j1.25 | 30.5 | 40.9 | 12 | 56.2 | 56.1 |
| 2450 | 38.1 + j30.8 | 56.8 – j34.4 | 4.01 – j1.06 | 30.2 | 41.0 | 13 | 56.8 | 56.7 |
| 2500 | 32.9 + j30.7 | 48.5 – j37.7 | 3.63 – j1.34 | 30.4 | 41.1 | 13 | 59.5 | 59.4 |

| f (MHz) | $Z_{source}$ (Ω) | $Z_{in}$ (Ω) | Max Efficiency | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | P3dB | | | | | |
| | | | $Z_{load}$ (2) (Ω) | Gain (dB) | (dBm) | (W) | $\eta_D$ (%) | PAE (%) |
| 2400 | 40.9 + j23.6 | 51.9 – j26.8 | 4.28 – j1.45 | 28.5 | 41.6 | 15 | 54.3 | 54.2 |
| 2450 | 38.1 + j30.8 | 48.5 – j35.0 | 4.19 – j1.50 | 28.2 | 41.9 | 15 | 55.2 | 55.1 |
| 2500 | 32.9 + j30.7 | 40.4 – j36.5 | 3.94 – j1.74 | 28.4 | 42.0 | 16 | 57.0 | 56.9 |

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.

$Z_{source}$ = Measured impedance presented to the input of the device at the package reference plane.
$Z_{in}$ = Impedance as measured from gate contact to ground.
$Z_{load}$ = Measured impedance presented to the output of the device at the package reference plane.

**Note: Measurement made on a per side basis.**



# Revision History

- The following table summarizes revisions to the content of the MHT2012N 2450 MHz Reference Circuit zip file.

| Revision | Date | Description |
|---|---|---|
| 0 | September 2019 | • Initial Release |

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