NB7V52MMNGEVB

NB752MMNGEVB Evaluation Board User's Manual

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EVAL BOARD USER'S MANUAL

Introduction

ON Semiconductor has developed the QFN16EVB evaluation board for its high-performance devices packaged in the 16-pin QFN. This evaluation board was designed to provide a flexible and convenient platform to quickly evaluate, characterize and verify the operation of various ON Semiconductor products. Many QFN16EVBs are dedicated with a device already installed, and can be ordered from www.onsemi.com at the specific device web page.

Evaluation Board Manual Contents:

- Information on16-Lead QFN Evaluation Board
- Assembly Instructions
- Appropriate Lab Setup
- Board Schematic
- Bill of Materials

This user's manual provides detailed information on board contents, layout and its use. This manual should be used in conjunction with NB7V52M data sheet which contains full technical details on the device specifications and operations.

Board Layout

The QFN16 Evaluation Board provides a high bandwidth, 50 Ω controlled impedance environment and is implemented in four layers. The first layer or primary trace layer is 0.008″ thick Rogers RO4003 material, and is designed to have equal electrical length on all signal traces from the device under test (DUT) pins to the SMA connectors. The second layer is the 1.0 oz copper ground plane and is primarily dedicated for the SMA connector ground plane. FR4 dielectric material is placed between the second and third layers and between third and fourth layers. The third layer is also 1.0 oz copper plane. A portion of this layer is designated for the device VCC and DUTGND power planes. The fourth layer is the secondary trace layer.

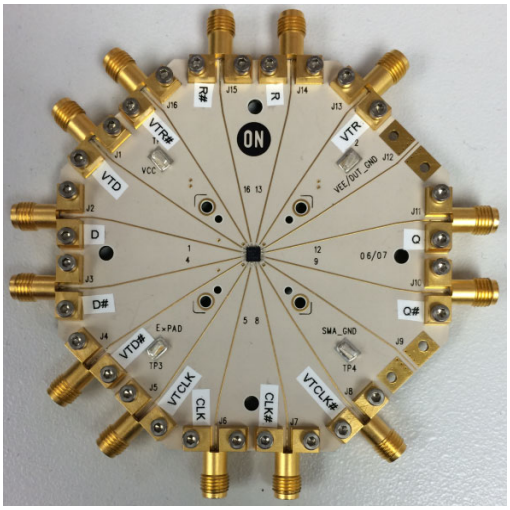


Figure 1. NB7V52MMNGEVB Evaluation Board (Top View)

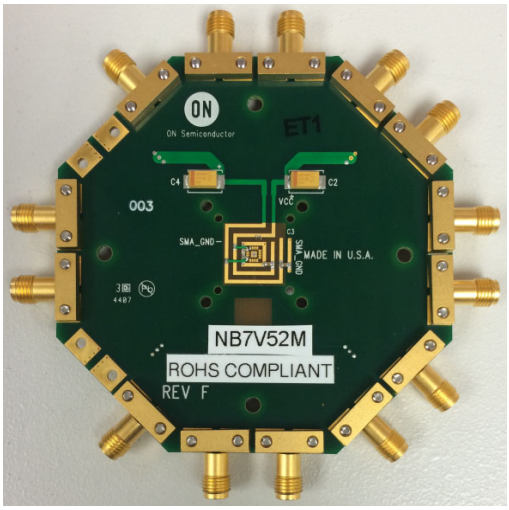


Figure 2. NB7V52MMNGEVB Evaluation Board (Bottom View)

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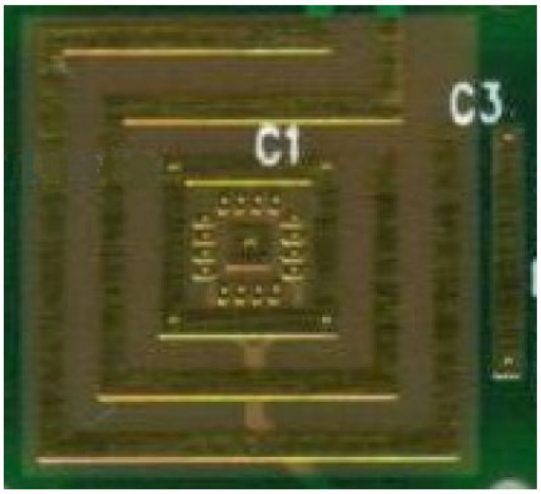


Figure 3. Enlarged Bottom View

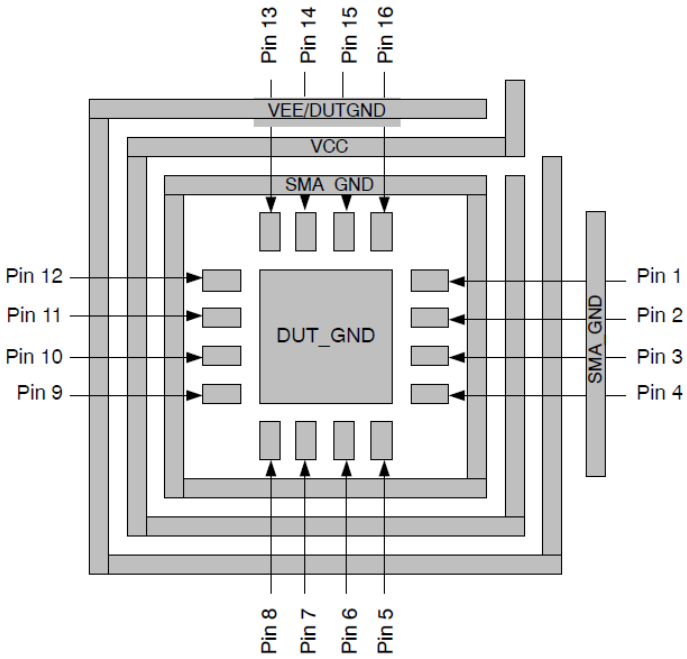


Figure 4. Enlarged Bottom View of Evaluation Board

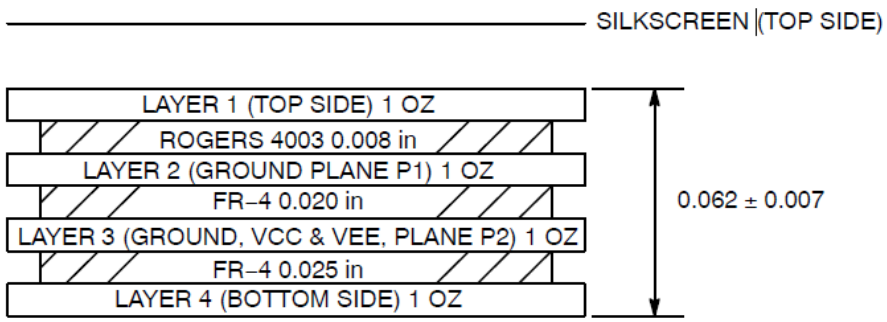
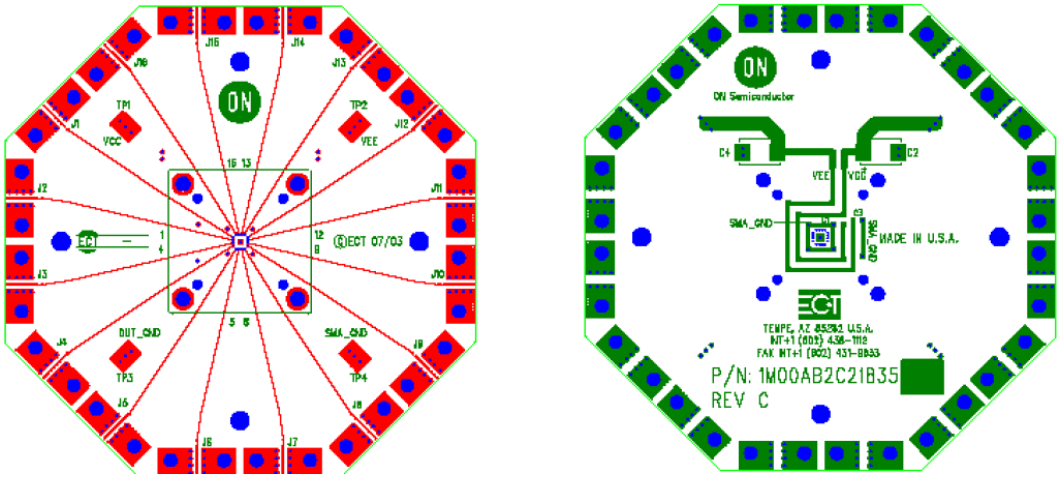


Figure 5. Evaluation Board Layout, 4-Layer



Top View Bottom View

Figure 6. Evaluation Board Layout

Evaluation Board Assembly Instructions

The QFN−16 evaluation board is designed for characterizing devices in a 50 Ω laboratory environment using high bandwidth equipment. Each signal trace on the board has a via at the DUT pin, which provides an option of placing a termination resistor on the board bottom, depending on the input/output configuration (See Table 1, Example Configuration List). Table 5 contains the Bill of Materials for this evaluation board.

The QFN16EVB was designed to accommodate a custom QFN−16 socket. Therefore, some external components are installed on the bottom side of the board.

Solder the Device on the Evaluation Board

The soldering of a device to the evaluation board can be accomplished by hand soldering or solder reflow techniques using solder paste. Make sure pin 1 of the device is located properly and all the pins are aligned to the footprint pads. Solder the QFN−16 device to the evaluation board. As mentioned earlier, many QFN16EVB's are dedicated with a device already installed, and can be ordered from www.onsemi.com at the specific device webpage.

Connecting Power and Ground

On the top side of the evaluation board, solder the four surface mount test pint clips (anvils) to the pads labeled V_{CC}, V_{EE}/DUTGND, SMAGND, and ExPad. ExPad is connected to the exposed flag and is typically recommended to be tied to V_{EE}/DUTGND, the negative supply of the device.

The positive power supply connector is labeled V_{CC}. Depending on the device, the negative power supply nomenclature is labeled either GND or V_{EE}. To help avoid confusion with the use of this board, the negative supply connector is labeled V_{EE}/DUTGND. SMAGND is the ground for the SMA connectors and is not to be confused with the device ground, V_{EE}/DUTGND. SMAGND and DUTGND can be connected in a single-supply application. The power pin layout and typical connection for the evaluation board is shown in Figure 7.

It is recommended to add bypass capacitors to reduce unwanted noise from the power supplies. Connect 0.1 μF capacitors from V_{CC} and V_{EE}/DUTGND to SMAGND.

Output Loading/Termination

CML Outputs

For the termination of CML outputs, operation with negative supply voltages is recommended to enable the use of the 50-Ω internal impedance of an oscilloscope or other measurement instrument. Since CML output termination requires 50-Ω to V_{CC}, off-setting the power supply such that V_{CC} = 0 V and DUTGND= −2.5 V or −1.8 V, will allow oscilloscope and VCC to be at the same potential. CML outputs can now be conveniently terminated using the 50-Ω internal impedance of oscilloscope or other measurement instrument.

Installing SMA Connectors

Each configuration indicates the number of SMA connectors needed to populate an evaluation board for a given device. Each input and output requires one SMA connector. Install all the required SMA connectors onto the board and solder the center signal conductor pin to the board on J1 through J16. Please note that the alignment of the signal connector pin of the SMA connector to the metal trace on the board can influence lab results. The launch and reflection of the signals are largely influenced by imperfect alignment and soldering of the SMA connector.

Validating the Assembled Board

After assembling the evaluation board, it is recommended to perform continuity checks on all soldered areas before commencing with the evaluation process. Time Domain Reflectometry (TDR) is another highly recommended validation test.

Table 1. NB7V52M EVALUATION BOARD CONFIGURATION

Device	J1	J2	J3	J4	J5	J6	J7	J8	J9	J10	J11	J12	J13	J14	J15	J16
Pin #	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Connector	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No	Yes	Yes	No	Yes	Yes	Yes	Yes
Wire	No	No	No	No	No	No	No	No	V_{EE}	No	No	V_{CC}	No	No	No	No

NOTE: Exposed Pad = DUTGND, Exopsed Pad should be tied to V_{EE}/DUTGND

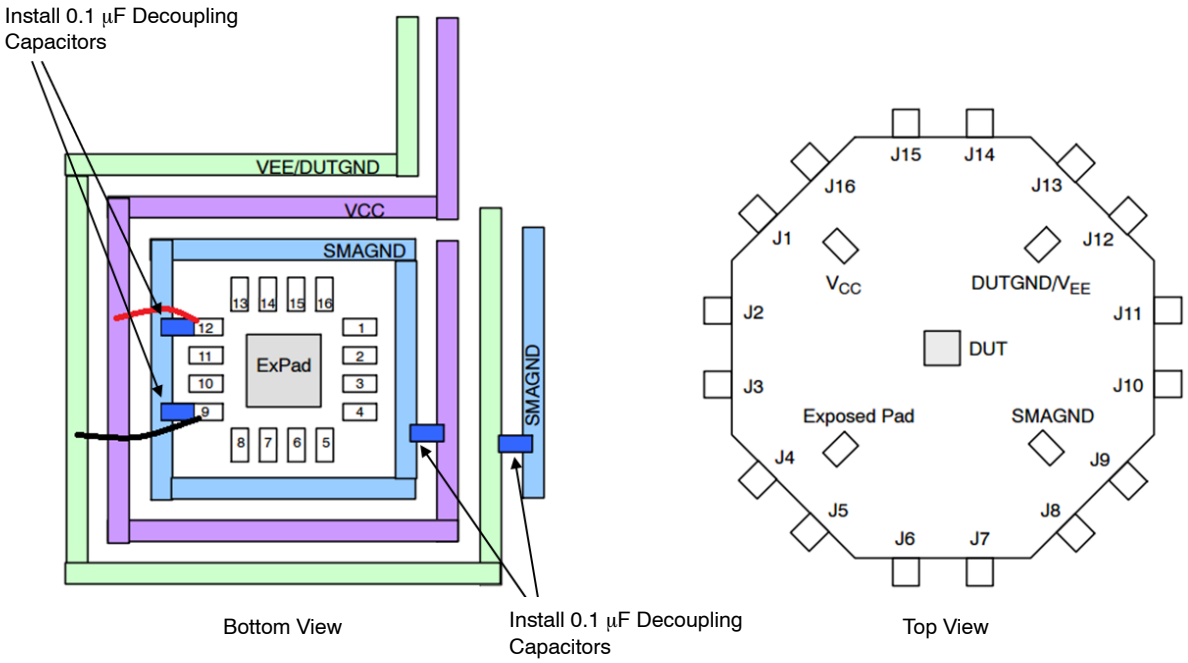


Figure 7. Power Supply Configuration for NB7V52MMNGEVB

QUICK START LAB SET-UP USER'S GUIDE

Equipment Required

1. DC Power Supply
2. Generator
3. Oscilloscope
4. DC Power Supply Connectors
5. 50-Ω SMA Connectors for I/O's

Block Diagram

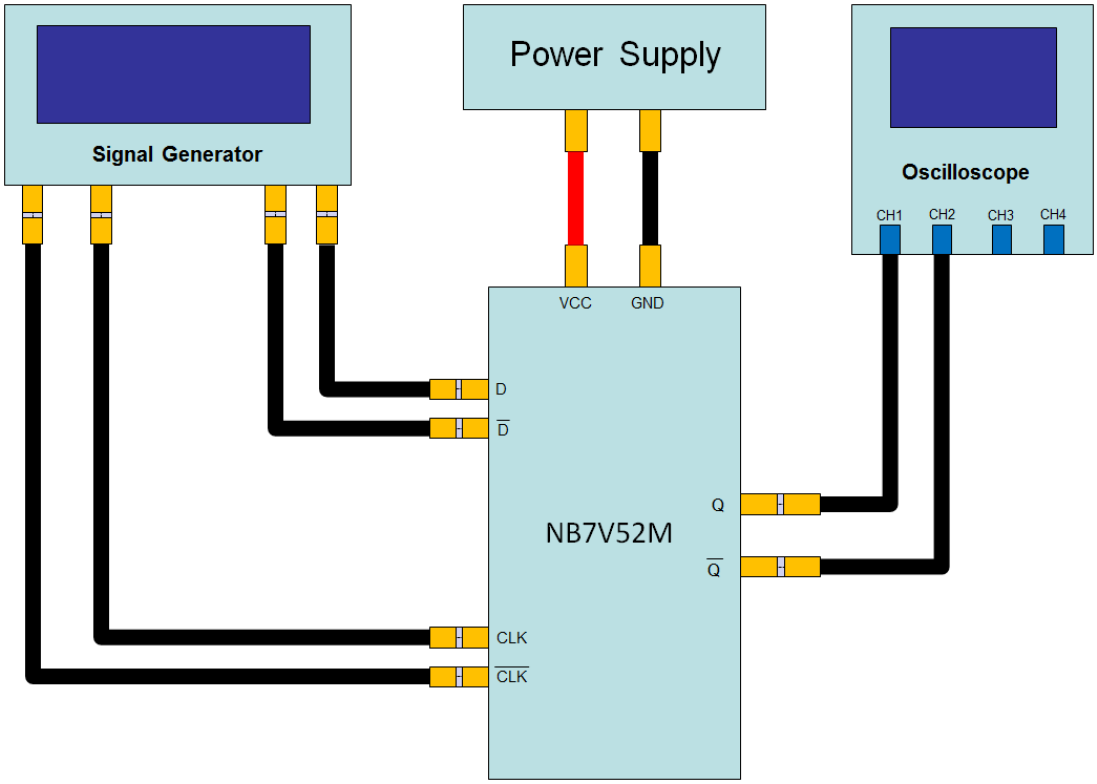


Figure 8. NB7V52MMNGEVB Test Block Diagram

Test and Measurement Setup Procedures

1. Connect VCC, SMAGND, and V_{EE}/DUTGND of the NB7V52M to a DC power supply. See Table 2 for appropriate levels.
2. Connect output of generator to CLK & $\overline{CLK}$ with 50-Ω connectors to DUT. See NB7V52M data sheet for appropriate input levels.
3. Connect output of generator to D & $\overline{D}$ with 50-Ω connectors to DUT. See NB7V52M data sheet for appropriate input levels.
4. Connect NB7V52M outputs Q & $\overline{Q}$ to appropriate oscilloscope channel. Board does not have 50-Ω output termination resistors, thus internal 50-Ω of oscilloscope can be used to properly terminate outputs.
5. Connect internal 50-Ω pins VTCLK, $\overline{VTCLK}$, VTD, $\overline{VTD}$, VTR and $\overline{VTR}$ to appropriate levels. See Figures 9–11 for appropriate Input level interface.
6. Connect R & $\overline{R}$ Input/Output select values to appropriate levels. See Table 3 for levels.

NOTE: See NB7V52M data sheet for D to CLK set up and hold times.

Power-Up Sequence

1. Turn On DUT Power Supply
2. Enable Generator Outputs
3. Monitor Q & $\overline{Q}$ Outputs with Oscilloscope

Table 2. POWER SUPPLY LEVELS

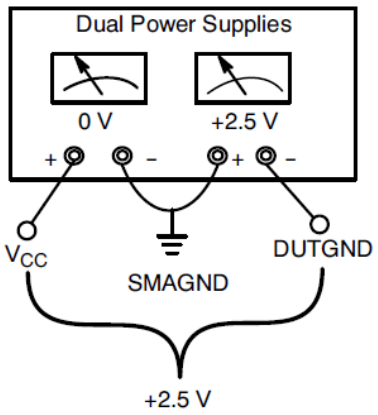
Outputs	Power Supply	V_{CC}	V_{EE}/DUTGND	SMAGND	ExPad (Typ)
CML	2.5 V	0 V	−2.5 V	0 V	V_{EE}/DUTGND
CML	1.8 V	0 V	−1.8 V	0 V	V_{EE}/DUTGND

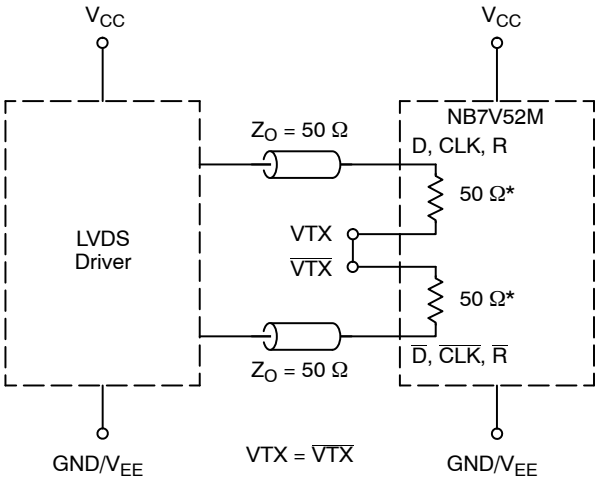
Table 3. RESET INPUT/OUTPUT SELECT TRUTH TABLE

R	$\overline{R}$	D	CLK	Q
H	L	X	X	L
L	H	L	Z	L
L	H	H	Z	H

Table 4. NB7V52M CML OUTPUTS “SPLIT” POWER SUPPLY CONFIGURATION

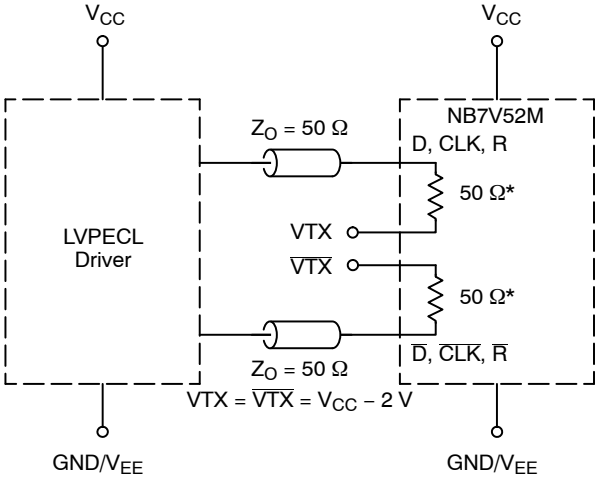
Device Pin Power Supply Convertor	“Split” Power Supply
V_{CC}	V_{CC} = 0 V
SMAGND	V_{TT} = 0 V
DUTGND	DUTGND = −2.5 V or −1.8 V





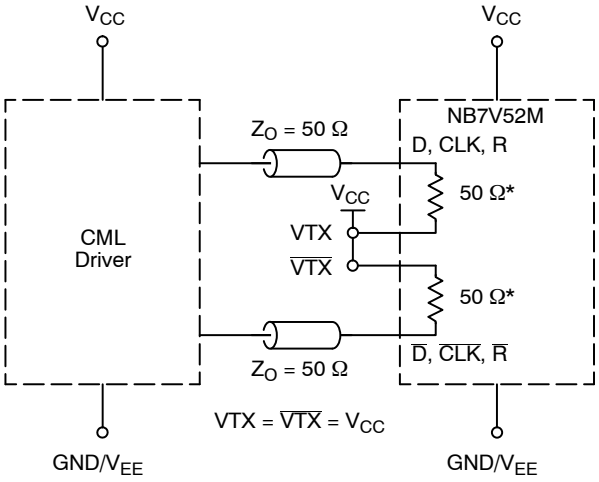
NOTE: X = D, CLK, R & $\overline{X}$ = $\overline{D}$, $\overline{CLK}$, $\overline{R}$

Figure 9. LVDS Interface



NOTE: X = D, CLK, R & $\overline{X}$ = $\overline{D}$, $\overline{CLK}$, $\overline{R}$

Figure 10. LVPECL Interface



NOTE: X = D, CLK, R & $\overline{X}$ = $\overline{D}$, $\overline{CLK}$, $\overline{R}$

Figure 11. Standard 50 Ω CML Interface

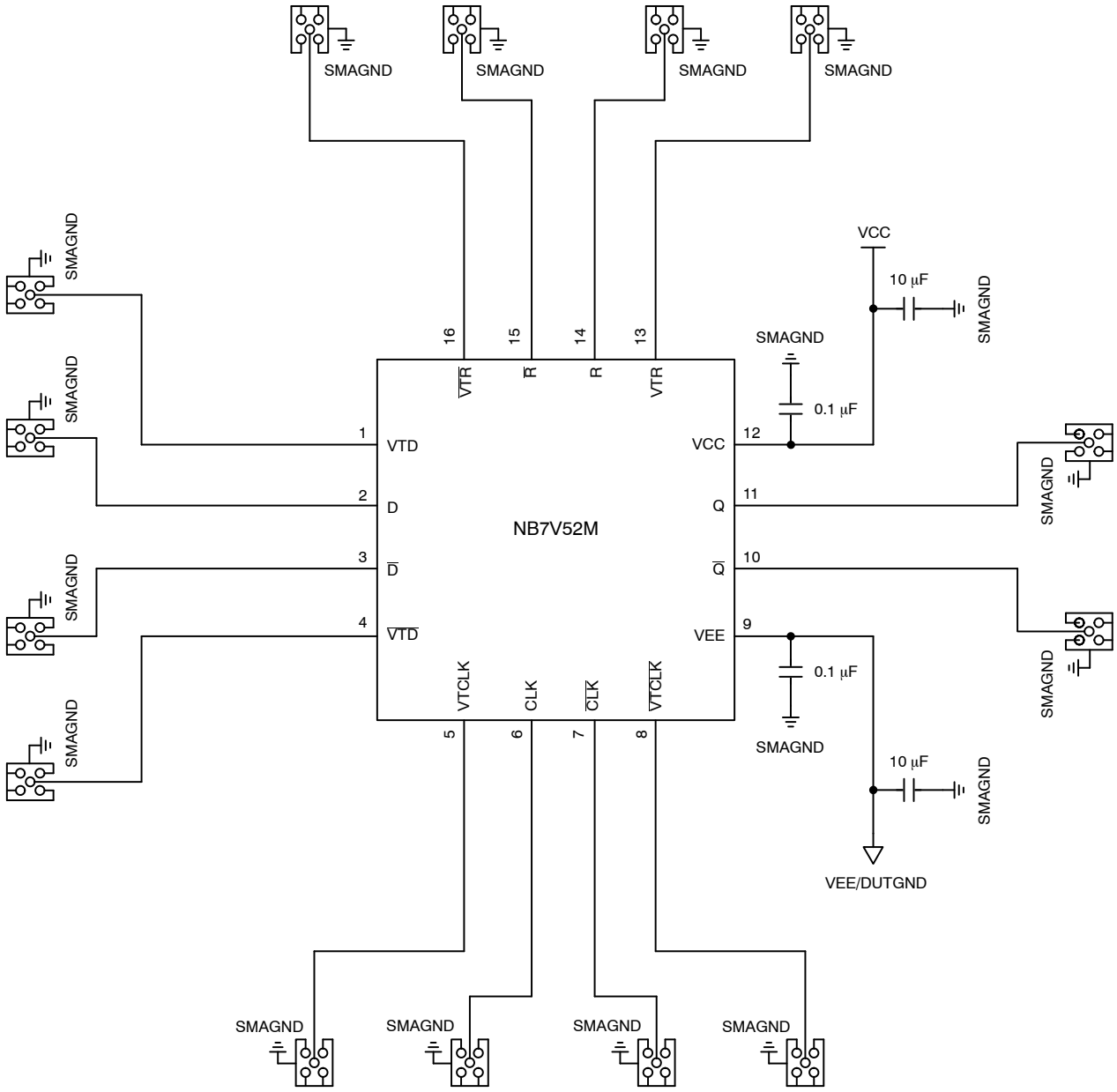


Figure 12. NB7V52MNGEVB Schematic

TYPICAL OUTPUT WAVEFORMS

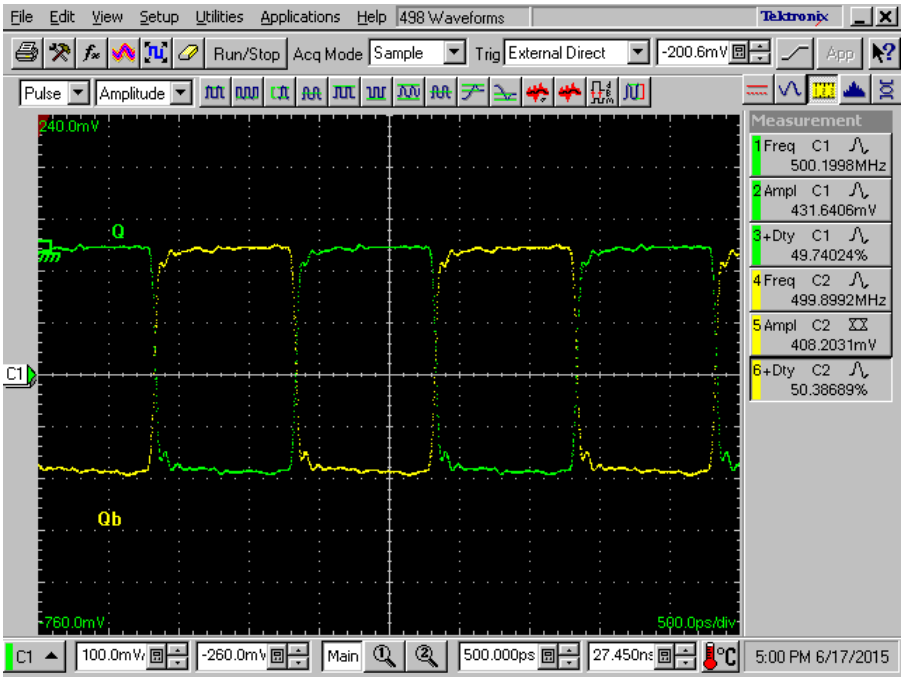


Figure 13. Typical Q & $\overline{Q}$ at F_{IN} = 1 GHz, V_{CC} = 1.8 V, 25°C

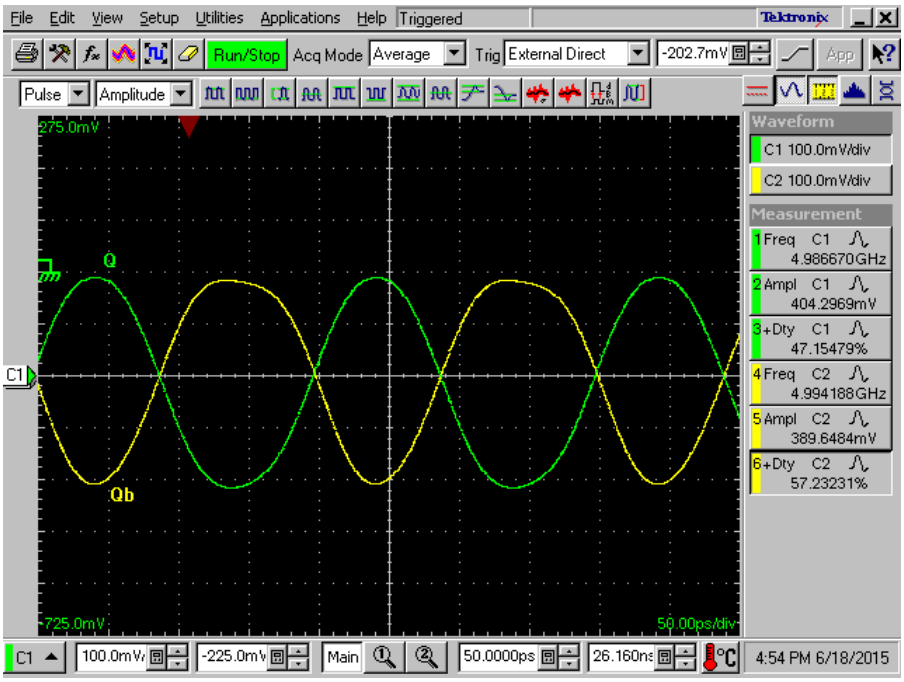


Figure 14. Typical Q & $\overline{Q}$ at F_{IN} = 10 GHz, V_{CC} = 1.8 V, 25°C

BILL OF MATERIALS

Table 5. NB7V52MMNGEVB BILL OF MATERIALS

Components	Qty.	Description	Manufacturer	Part Number	Web Site
SMA Connector	14	SMA Connector, Side Launch, Gold Plated	Rosenberger	32K243−40ME3	www.rosenberger.com
Surface Mount Test Points	4	SMT Miniature Test Point	Keystone	5015	www.keyelco.com
Chip Capacitor	2	0402 0.1 μF ±10%	Kemet	C0402C105K9PACTU	www.kemet.com
Chip Capacitor	2	0603 0.1 μF ±10%	Kemet	C0603C105K8PACTU	www.kemet.com
Chip Capacitor	2	22 μF ±10%	Kemet	T495C226K025ATE300	www.kemet.com
Evaluation Board	1	QFN 16 Evaluation Board	ON Semiconductor	QFN16EVB	www.onsemi.com
Device Samples	1	QFN 16 Package Device	ON Semiconductor	NB7V52MMNG	www.onsemi.com

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