LM4873 Boomer® Audio Power Amplifier Series Dual 2.1W Audio Amplifier Plus Stereo Headphone Function

Check for Samples: LM4873

FEATURES

- **Input Mux Control and Two Separate Inputs Per Channel**
- **Stereo Headphone Amplifier Mode**
- **"Click and Pop" Suppression Circuitry**
- **Thermal Shutdown Protection Circuitry**
- **PCB Area-Saving DSBGA and Thin DSBGA Packages**
- **TSSOP and HTSSOP and WQFN Packages**

APPLICATIONS

- **Multimedia Monitors**
- **Portable and Desktop Computers**
- **Portable Audio Systems**

KEY SPECIFICATIONS

- **P_O at 1% THD+N**
  - **LM4873LQ, 3Ω, 4Ω Loads 2.4W (typ), 2.1 W (typ)**
  - **LM4873MTE-1, 3Ω, 4Ω loads 2.4W (typ), 2.1 W (typ)**
  - **LM4873IBL, 8Ω Load 1.1 W (typ)**
  - **LM4873MTE, 4Ω 1.9 W (typ)**
  - **LM4873, 8Ω 1.1 W (typ)**
- **Single-Ended Mode THD+N at 75 mW Into 32Ω 0.5 % (max)**
- **Shutdown Current 0.7 µA (typ)**
- **Supply Voltage Range 2 to 5.5 V**

DESCRIPTION

The LM4873 is a dual bridge-connected audio power amplifier which, when connected to a 5V supply, will deliver 2.1W to a 4Ω load or 2.4W to a 3Ω load with less than 1.0% THD+N (see Notes below). In addition, the headphone input pin allows the amplifiers to operate in single-ended mode when driving stereo headphones. A MUX control pin allows selection between the two stereo sets of amplifier inputs. The MUX control can also be used to select two different closed-loop responses.

Boomer audio power amplifiers were designed specifically to provide high quality output power from a surface mount package while requiring few external components. To simplify audio system design, the LM4873 combines dual bridge speaker amplifiers and stereo headphone amplifiers on one chip.

The LM4873 features an externally controlled, low-power consumption shutdown mode, a stereo headphone amplifier mode, and thermal shutdown protection. It also utilizes circuitry to reduce "clicks and pops" during device turn-on.

Note: An LM4873MTE-1, LM4873MTE, or LM4873LQ that has been properly mounted to a circuit board will deliver 2.1W into 4Ω. The other package options for the LM4873 will deliver 1.1W into 8Ω. See the APPLICATION INFORMATION sections for further information concerning the LM4873MTE-1, LM4873MTE, and the LM4873LQ.

Note: An LM4873MTE-1, LM4873MTE, or LM4873LQ that has been properly mounted to a circuit board and forced-air cooled will deliver 2.4W into 3Ω.

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Connection Diagrams

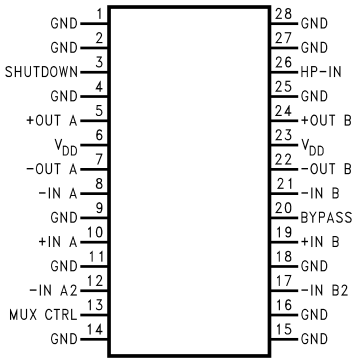

Figure 1. Top View
See Package Number PWP0028A
for Exposed-DAP HTSSOP

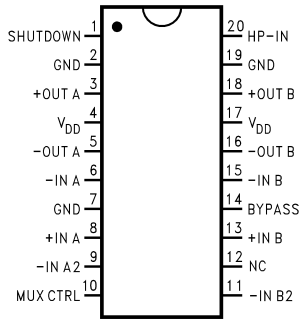

Figure 2. Top View
See Package Number PW0020A for TSSOP
See Package Number PWP0020A
for Exposed-DAP HTSSOP

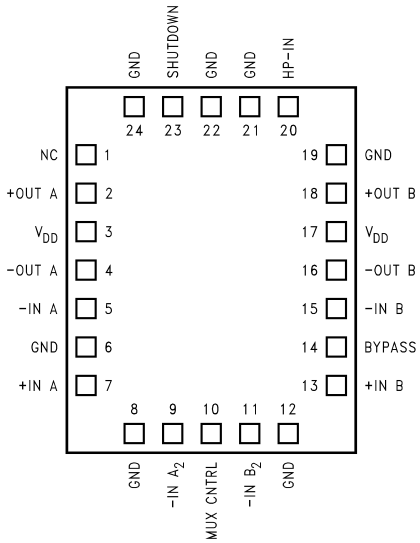

Figure 3. Top View
See Package Number NHW0024A
for Exposed-DAP WQFN

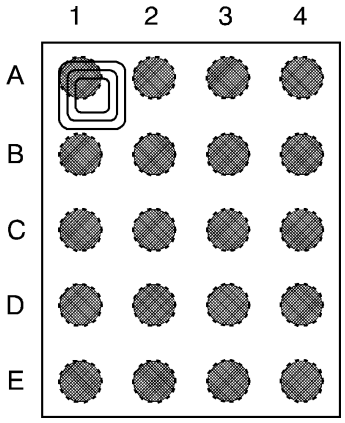

Figure 4. Top View
(Bump-side down)
See Package Number BLA20AAB for DSBGA
See Package Number YZR0020AAA

LM4873IBP PIN DESIGNATIONS

Pin (Bump) Number	Pin (Bump) Function	Pin (Bump) Number	Pin (Bump) Function
A1	-IN A_1	C3	V_{DD}
A2	-IN A_2	C4	+IN B
A3	-IN B_2	D1	+OUT A
A4	-IN B_1	D2	GND
B1	-OUT A	D3	GND
B2	GND	D4	+OUT B
B3	GND	E1	MUX CTRL
B4	-OUT B	E2	SHUTDOWN
C1	+IN A	E3	HP-IN
C2	V_{DD}	E4	BYPASS

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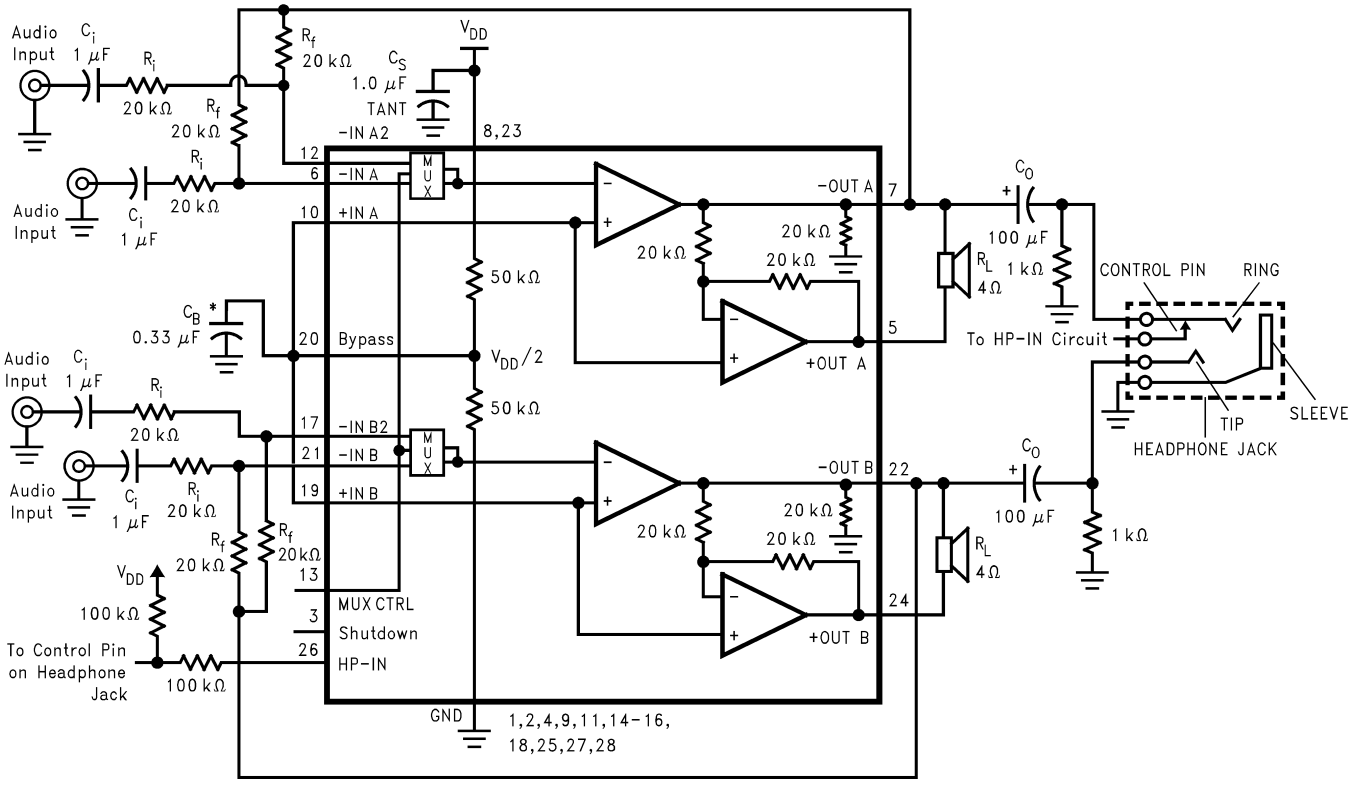
Typical Application



Note: Pin out shown for the 28-pin Exposed-DAP HTSSOP package. Refer to the Connection Diagrams for the pin out of the 20-pin Exposed-DAP HTSSOP, Exposed-DAP WQFN, and DSBGA packages.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS (1) (2)

Supply Voltage			6.0V
Storage Temperature			−65°C to +150°C
Input Voltage			−0.3V to V_{DD} +0.3V
Power Dissipation (3)			Internally limited
ESD Susceptibility (4)			2000V
ESD Susceptibility (5)			200V
Junction Temperature			150°C
Solder Information	SOIC Package	Vapor Phase (60 sec.)	215°C
		Infrared (15 sec.)	220°C
Thermal Resistance		θ_{JC} (typ)—PW0020A	20°C/W
		θ_{JA} (typ)—PW0020A	80°C/W
		θ_{JC} (typ)—PWP0020A	2°C/W
		θ_{JA} (typ)—PWP0020A	41°C/W (6)
		θ_{JA} (typ)—PWP0020A	51°C/W (7)
		θ_{JA} (typ)—PWP0020A	90°C/W (8)
		θ_{JC} (typ)—PWP0028A	2°C/W
		θ_{JA} (typ)—PWP0028A	41°C/W (9)
		θ_{JA} (typ)—PWP0028A	51°C/W (10)
		θ_{JA} (typ)—PWP0028A	90°C/W (11)
		θ_{JC} (typ)—NHW0024A	3.0°C/W
		θ_{JA} (typ)—NHW0024A	42°C/W (12)
		θ_{JA} (typ)—DSBGA	60°C/W (13)

(1) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device operates within the Operating Ratings. Specifications are not ensured for parameters where no limit is given. The typical value however, is a good indication of device performance.
(3) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A)/\theta_{JA}$. For the LM4873, T_{JMAX} = 150°C. For the θ_{JA}s for different packages, please see the APPLICATION INFORMATION section or the Absolute Maximum Ratings section.
(4) Human body model, 100 pF discharged through a 1.5 kΩ resistor.
(5) Machine model, 220 pF–240 pF discharged through all pins.
(6) The given θ_{JA} is for an LM4873 packaged in an PWP0020A with the Exposed-DAP soldered to an exposed 2in^2 area of 1oz printed circuit board copper.
(7) The given θ_{JA} is for an LM4873 packaged in an PWP0020A with the Exposed-DAP soldered to an exposed 1in^2 area of 1oz printed circuit board copper.
(8) The given θ_{JA} is for an LM4873 packaged in an PWP0020A with the Exposed-DAP not soldered to printed circuit board copper.
(9) The given θ_{JA} is for an LM4873 packaged in an PWP0028A with the Exposed-DAP soldered to an exposed 2in^2 area of 1oz printed circuit board copper.
(10) The given θ_{JA} is for an LM4873 packaged in an PWP0028A with the Exposed-DAP soldered to an exposed 1in^2 area of 1oz printed circuit board copper.
(11) The given θ_{JA} is for an LM4873 packaged in an PWP0028A with the Exposed-DAP not soldered to printed circuit board copper.
(12) The given θ_{JA} is for an LM4873 packaged in an NHW0024A with the Exposed-DAP soldered to an exposed 2in^2 area of 1oz printed circuit board copper.
(13) The θ_{JA} is specified for an LM4873 packaged in a BLA20AAB or YZR0020AAA with their four ground connections soldered to a 3in^2, 1oz copper plane.

OPERATING RATINGS

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$	−40°C ≤ T_A ≤ 85°C
Supply Voltage		2.0V ≤ V_{DD} ≤ 5.5V

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ELECTRICAL CHARACTERISTICS (1) (2)

The following specifications apply for V_{DD}= 5V unless otherwise noted. Limits apply for T_A= 25°C.

Symbol	Parameter	Conditions	LM4873		Units (Limits)
			Typical (3)	Limit (4)	
V_{DD}	Supply Voltage			2	V (min)
				5.5	V (max)
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, I_O = 0A (5) , HP-IN = 0V	7.5	15	mA (max)
		V_{IN} = 0V, I_O = 0A (5) , HP-IN = 4V	5.8	6	mA (min)
I_{SD}	Shutdown Current	V_{DD} applied to the SHUTDOWN pin	0.7	2	µA (max)
V_{IH}	Headphone High Input Voltage			4	V (min)
V_{IL}	Headphone Low Input Voltage			0.8	V (max)

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device operates within the Operating Ratings. Specifications are not ensured for parameters where no limit is given. The typical value however, is a good indication of device performance.
(2) All voltages are measured with respect to the ground (GND) pins, unless otherwise specified.
(3) Typicals are specified at 25°C and represent the parametric norm.
(4) Datasheet min/max specification limits are ensured by design, test, or statistical analysis.
(5) The quiescent power supply current depends on the offset voltage when a practical load is connected to the amplifier.

ELECTRICAL CHARACTERISTICS FOR BRIDGED-MODE OPERATION (1) (2)

The following specifications apply for V_{DD}= 5V unless otherwise specified. Limits apply for T_A= 25°C.

Symbol	Parameter	Conditions		LM4873		Units (Limits)
				Typical (3)	Limit (4)	
V_{OS}	Output Offset Voltage	V_{IN} = 0V		5	50	mV (max)
P_O	Output Power (5)	THD+N = 1%, f = 1kHz (6)	LM4873MTE-1, R_L = 3Ω	2.4		W
			LM4873MTE, R_L = 3Ω	2.2		W
			LM4873LQ, R_L = 3Ω	2.2		W
			LM4873MTE-1, R_L = 4Ω	2.1		W
			LM4873MTE, R_L = 4Ω	1.9		W
			LM4873LQ, R_L = 4Ω	1.9		W
			LM4873MT, R_L = 4Ω	1.9		W
			LM4873, R_L = 8Ω	1.1	1.0	W (min)
		THD+N = 10%, f = 1kHz (6)	LM4873MTE-1, R_L = 3Ω	3.0		W
			LM4873LQ, R_L = 3Ω	3.0		W
			LM4873MTE-1, R_L = 4Ω	2.6		W
			LM4873LQ, R_L = 4Ω	2.6		W
			LM4873, R_L = 8Ω	1.5		W
		THD+N = 1%, f = 1kHz, R_L = 32Ω		0.34		W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device operates within the Operating Ratings. Specifications are not ensured for parameters where no limit is given. The typical value however, is a good indication of device performance.
(2) All voltages are measured with respect to the ground (GND) pins, unless otherwise specified.
(3) Typicals are specified at 25°C and represent the parametric norm.
(4) Datasheet min/max specification limits are ensured by design, test, or statistical analysis.
(5) Output power is measured at the device terminals.
(6) When driving 3Ω or 4Ω loads and operating on a 5V supply, the LM4873LQ must be mounted to a circuit board that has a minimum of 2.5in^2 of exposed, uninterrupted copper area connected to the WQFN package's exposed DAP.

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ELECTRICAL CHARACTERISTICS FOR BRIDGED-MODE OPERATION (1) (2) (continued)

The following specifications apply for V_{DD}= 5V unless otherwise specified. Limits apply for T_A= 25°C.

Symbol	Parameter	Conditions		LM4873		Units (Limits)
				Typical (3)	Limit (4)	
THD+N	Total Harmonic Distortion+Noise	20Hz ≤ f ≤ 20kHz, A_{VD} = 2	LM4873MTE-1, R_L = 4Ω, P_O = 2W	0.3		%
			LM4873LQ, R_L = 4Ω, P_O = 2W			
			LM4873, R_L = 8Ω, P_O = 1W			
PSRR	Power Supply Rejection Ratio	V_{DD} = 5V, V_{RIPPLE} = 200mV_{RMS}, R_L = 8Ω, C_B = 1.0µF		67		dB
X_{TALK}	Channel Separation	f = 1kHz, C_B = 1.0µF		80		dB
SNR	Signal To Noise Ratio	V_{DD} = 5V, P_O = 1.1W, R_L = 8Ω		97		dB

ELECTRICAL CHARACTERISTICS FOR SINGLE-ENDED OPERATION (1) (2) (3)

The following specifications apply for V_{DD}= 5V unless otherwise specified. Limits apply for T_A= 25°C.

Symbol	Parameter	Conditions	LM4873		Units (Limits)
			Typical (4)	Limit (5)	
V_{OS}	Output Offset Voltage	V_{IN} = 0V	5	50	mV (max)
P_O	Output Power	THD+N = 0.5%, f = 1 kHz, R_L = 32Ω	85	75	mW (min)
		THD+N = 1%, f = 1 kHz, R_L = 8Ω	340		mW
		THD+N = 10%, f = 1 kHz, R_L = 8Ω	440		mW
THD+N	Total Harmonic Distortion+Noise	A_V = −1, P_O = 75mW, 20Hz ≤ f ≤ 20kHz, R_L = 32Ω	0.2		%
PSRR	Power Supply Rejection Ratio	C_B = 1.0µF, V_{RIPPLE} = 200mV_{RMS}, f = 1kHz	52		dB
X_{TALK}	Channel Separation	f = 1kHz, C_B = 1.0µF	60		dB
SNR	Signal To Noise Ratio	V_{DD} = 5V, P_O = 340mW, R_L = 8Ω	94		dB

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device operates within the Operating Ratings. Specifications are not ensured for parameters where no limit is given. The typical value however, is a good indication of device performance.
(2) All voltages are measured with respect to the ground (GND) pins, unless otherwise specified.
(3) Refer to Figure 1
(4) Typicals are specified at 25°C and represent the parametric norm.
(5) Datasheet min/max specification limits are ensured by design, test, or statistical analysis.

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TYPICAL PERFORMANCE CHARACTERISTICS MTE (20-PIN) AND LQ (24-PIN) SPECIFIC CHARACTERISTICS

LM4873MTE, LM4873LQ THD+N vs Output Power

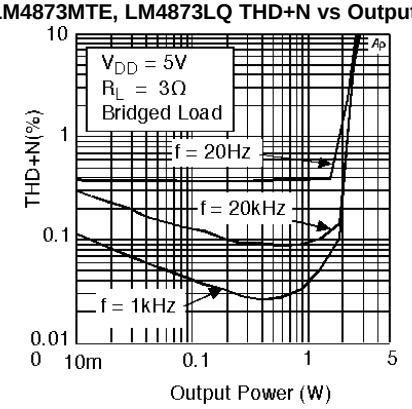

Figure 5.

LM4873MTE, LM4873LQ THD+N vs Frequency

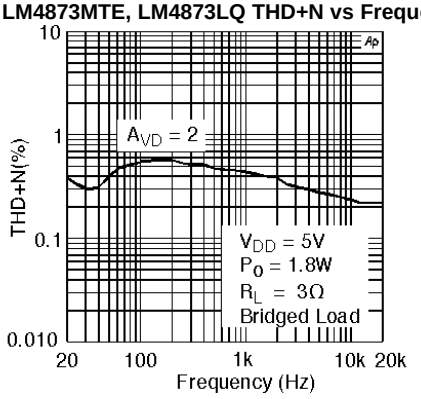

Figure 6.

LM4873MTE, LM4873LQ THD+N vs Output Power

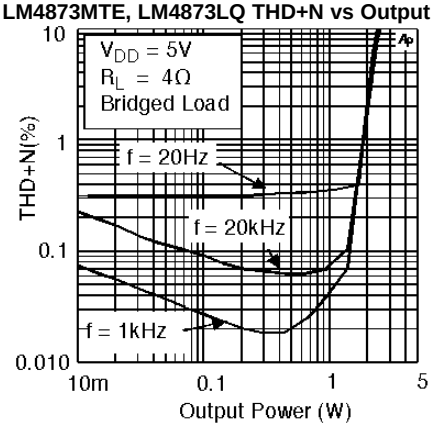

Figure 7.

LM4873MTE, LM4873LQ Power Dissipation vs Power Output

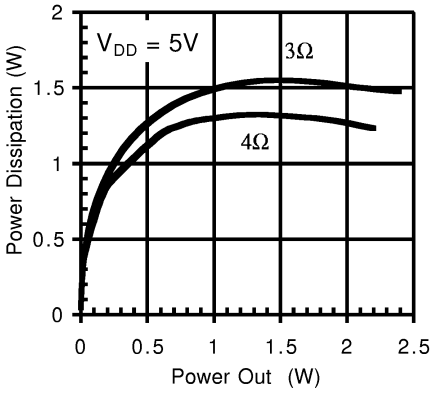

Figure 8.

LM4873MTE Power Derating Curve

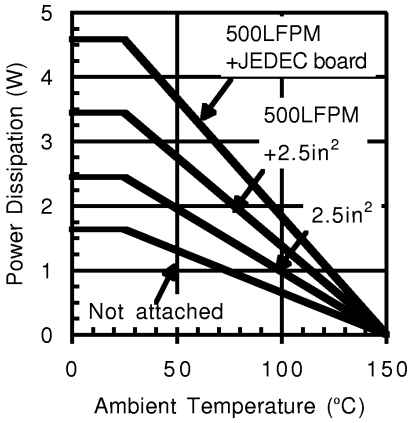

Figure 9.

LM4873LQ Power Derating Curve

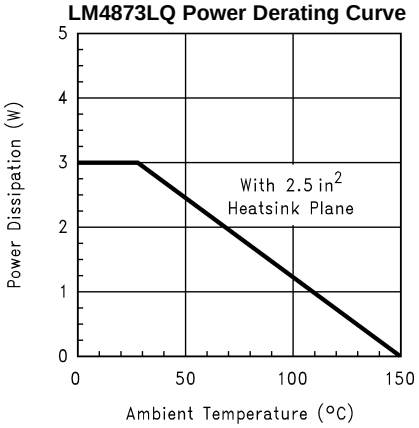

Figure 10.

Figure 9 shows the LM4873MTE's and the LM4873LQ's thermal dissipation ability at different ambient temperatures given these conditions: **500LFPM + JEDEC board:** The part is soldered to a 1S2P 20-lead exposed-DAP HTSSOP test board with 500 linear feet per minute of forced-air flow across it.**Board information** - copper dimensions: 74x74mm, copper coverage: 100% (buried layer) and 12% (top/bottom layers), 16 vias under the exposed-DAP. **500LFPM + 2.5in^2:** The part is soldered to a 2.5in^2, 1 oz. copper plane with 500 linear feet per minute of forced-air flow across it. **2.5in^2:** The part is soldered to a 2.5in^2, 1oz. copper plane. **Not Attached:** The part is not soldered down and is not forced-air cooled.

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TYPICAL PERFORMANCE CHARACTERISTICS MTE-1 (28 PIN) SPECIFIC CHARACTERISTICS

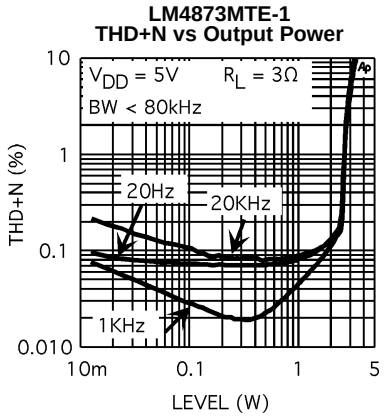

Figure 11.

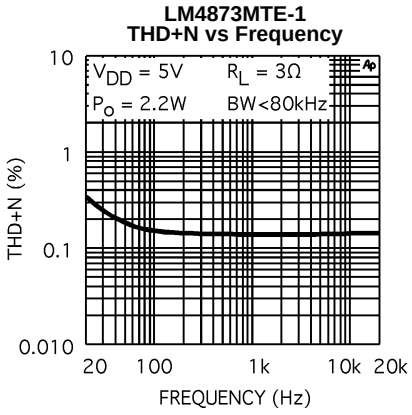

Figure 12.

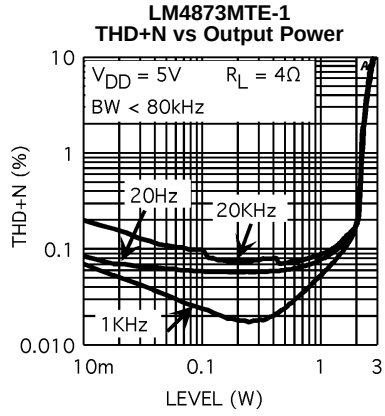

Figure 13.

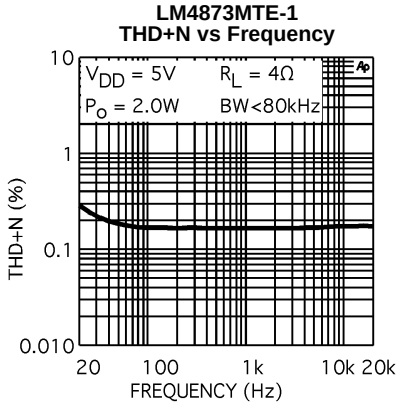

Figure 14.

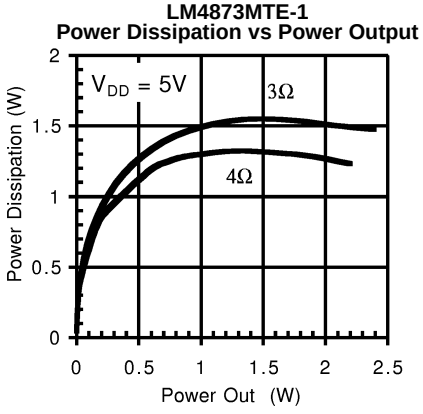

Figure 15.

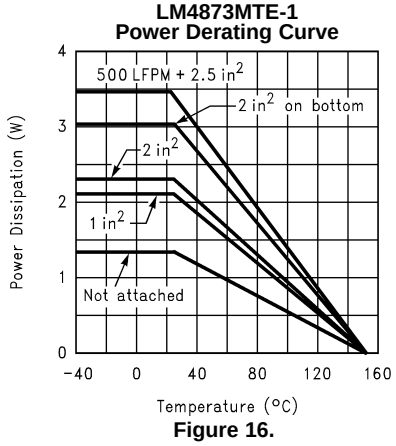

Figure 16.

Figure 15 shows the LM4835MTE-1's thermal dissipation ability at different ambient temperatures given these conditions: **500LFPM + 2in^2:** The part is soldered to a 2in^2, 1 oz. copper plane with 500 linear feet per minute of forced-air flow across it. **2in^{2}on bottom:** The part is soldered to a 2in^2, 1oz. copper plane that is on the bottom side of the PC board through 21 8 mil vias.**2in^2:** The part is soldered to a 2in^2, 1oz. copper plane. **1in^2:** The part is soldered to a 1in^2, 1oz. copper plane. **Not Attached:** The part is not soldered down and is not forced-air cooled.

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TYPICAL PERFORMANCE CHARACTERISTICS

THD+N vs Frequency

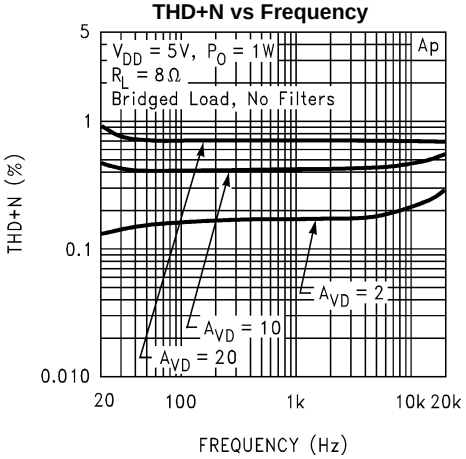

Figure 17.

THD+N vs Frequency

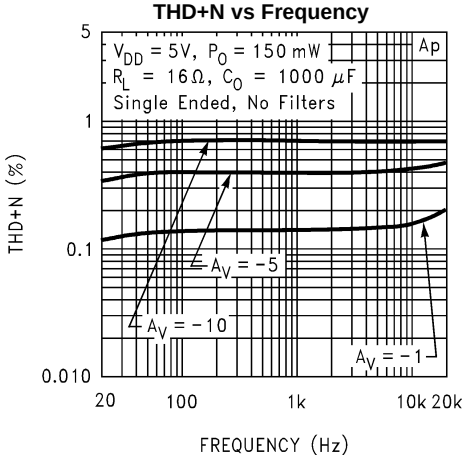

Figure 18.

THD+N vs Frequency

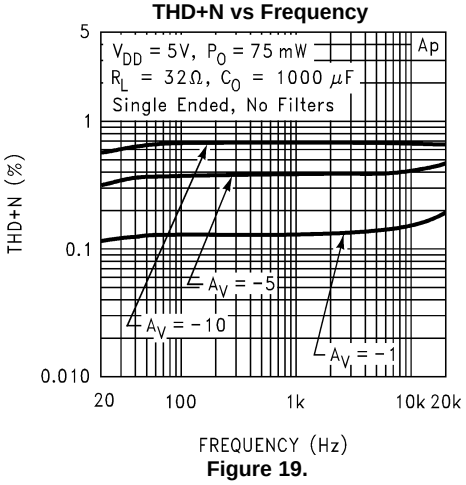

Figure 19.

THD+N vs Output Power

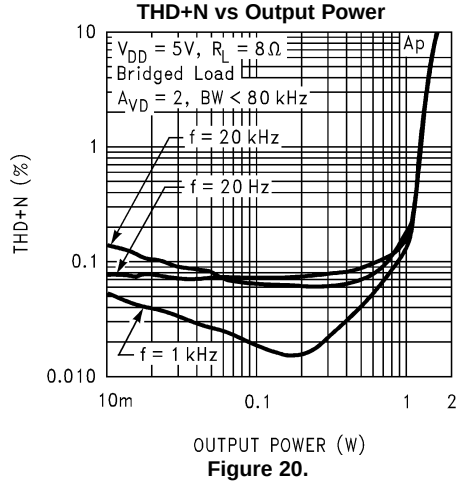

Figure 20.

THD+N vs Output Power

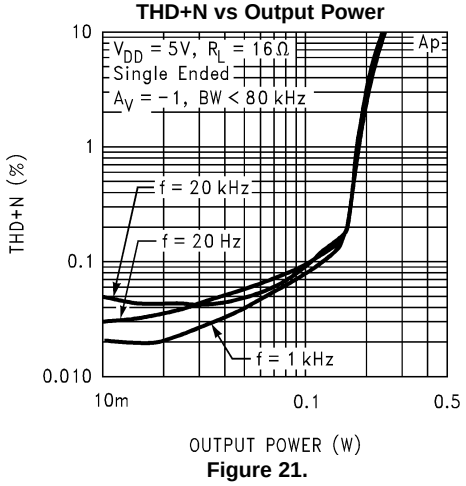

Figure 21.

THD+N vs Output Power

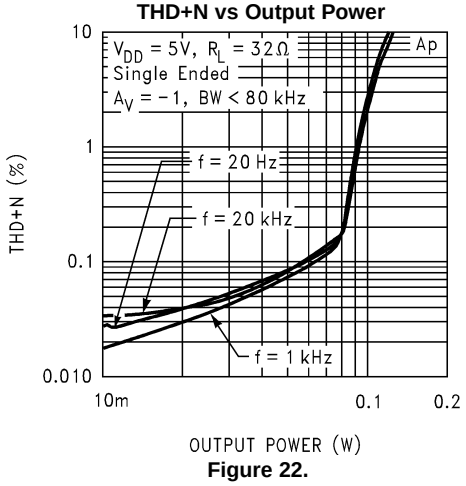

Figure 22.

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

THD+N vs Output Power

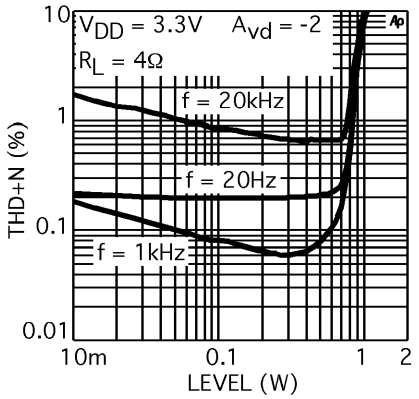

Figure 23.

THD+N vs Frequency

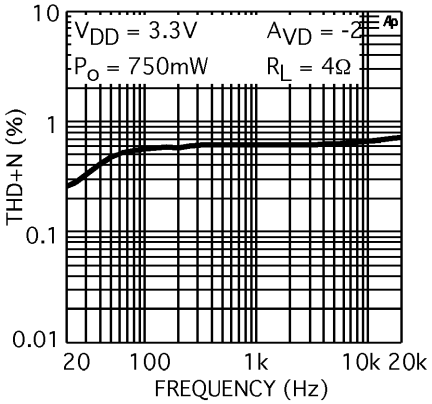

Figure 24.

THD+N vs Output Power

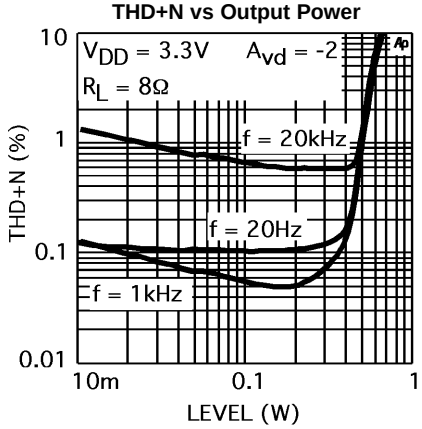

Figure 25.

THD+N vs Frequency

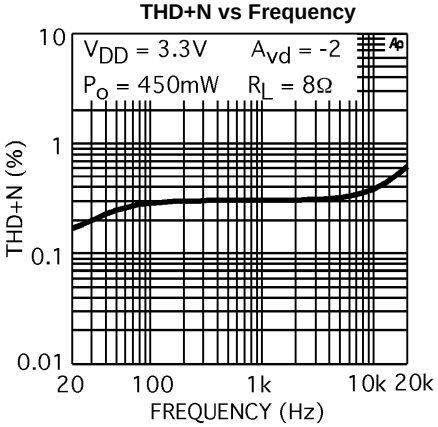

Figure 26.

Output Power vs Load Resistance

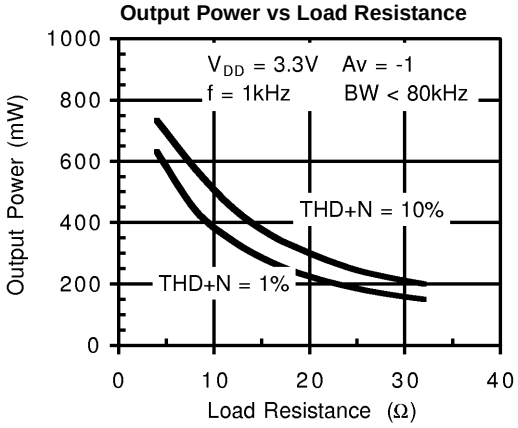

Figure 27.

Power Dissipation vs Supply Voltage

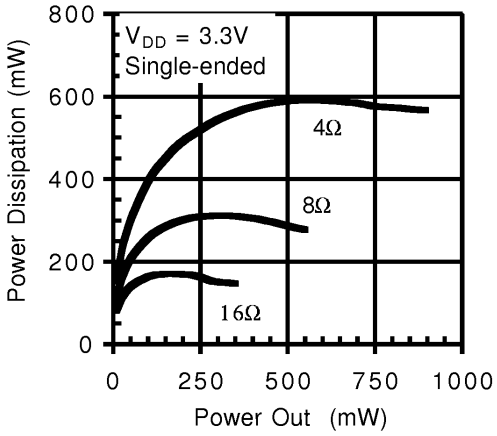

Figure 28.

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Output Power vs Supply Voltage

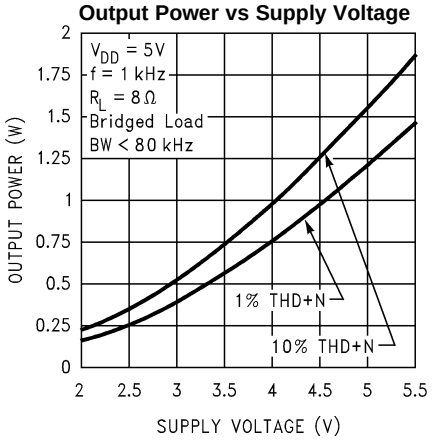

Figure 29.

Output Power vs Supply Voltage

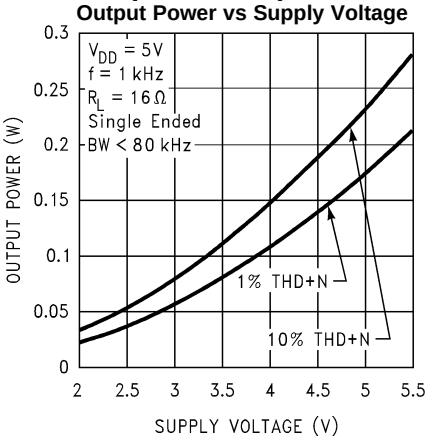

Figure 30.

Output Power vs Supply Voltage

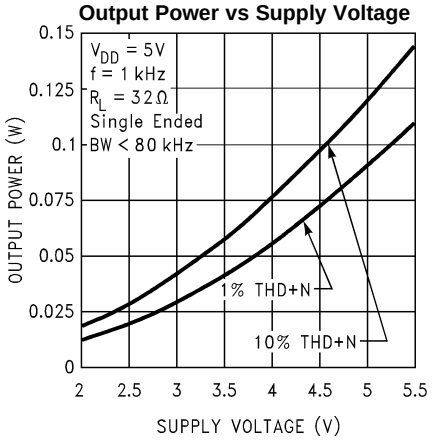

Figure 31.

Output Power vs Load Resistance

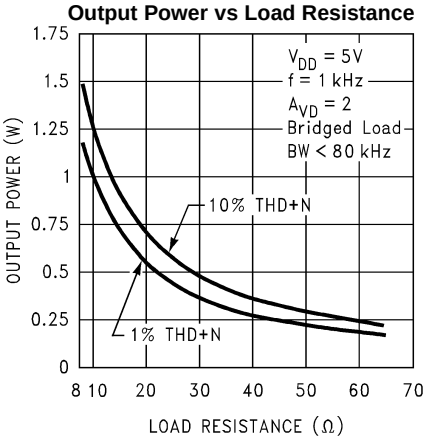

Figure 32.

Output Power vs Load Resistance

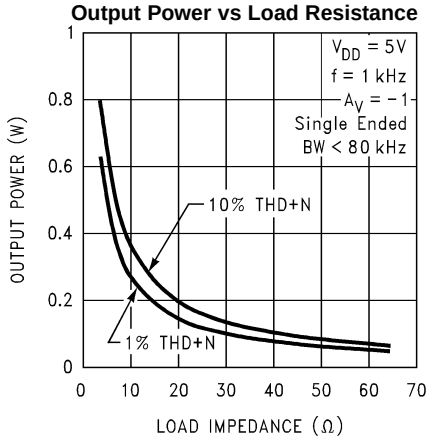

Figure 33.

LM4873IBL
Stereo Output Power vs Power Dissipation

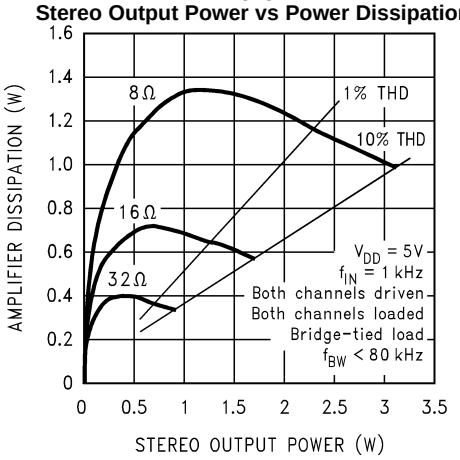

Figure 34.

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Power Dissipation vs Output Power

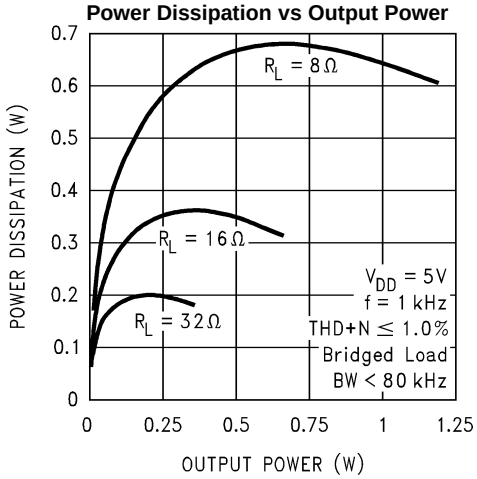

Figure 35.

Dropout Voltage vs Supply Voltage

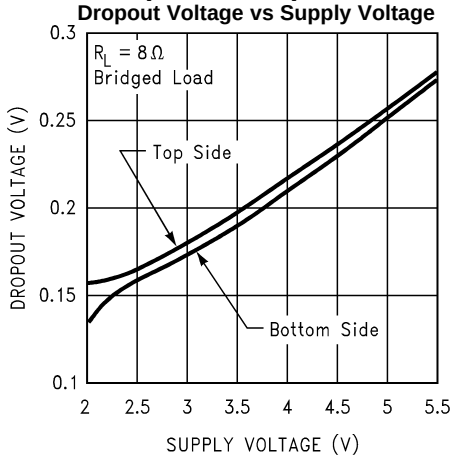

Figure 36.

Power Derating Curve

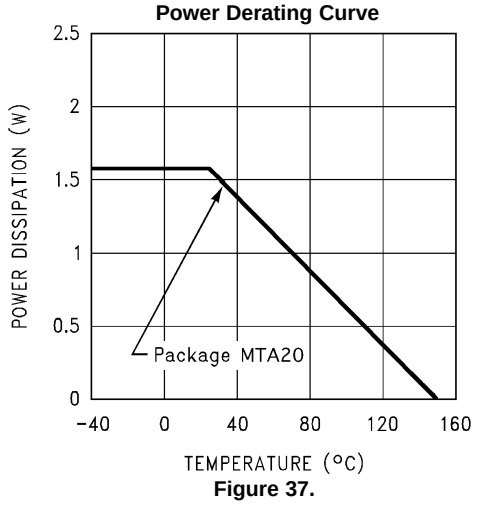

Figure 37.

Power Dissipation vs Output Power

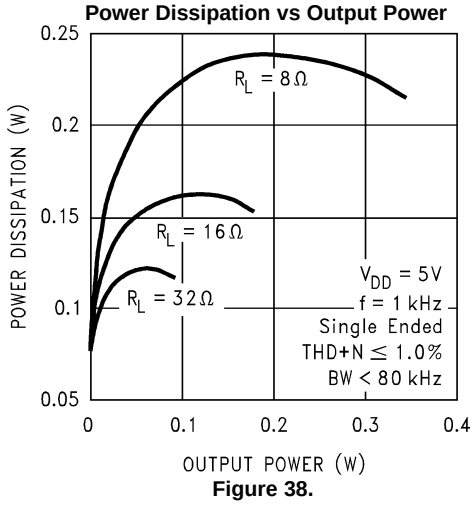

Figure 38.

Noise Floor

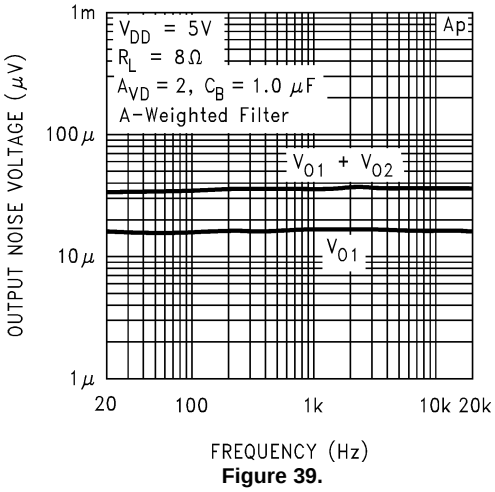

Figure 39.

Channel Separation

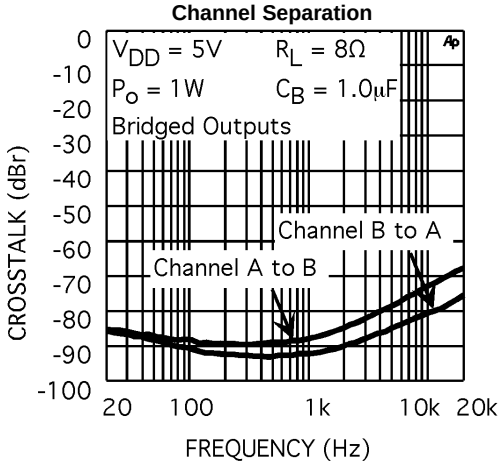

Figure 40.

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Channel Separation

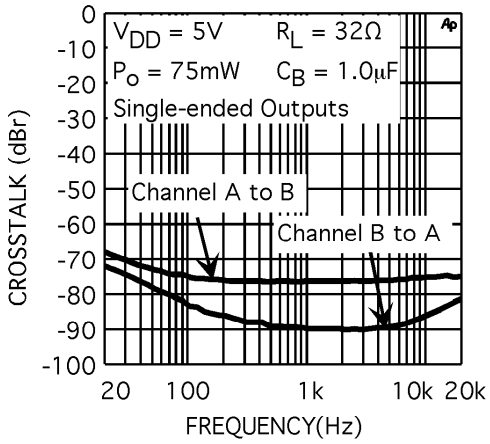

Figure 41.

Power Supply Rejection Ratio

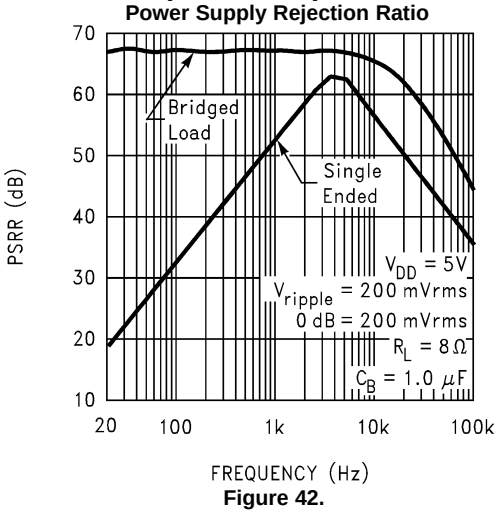

Figure 42.

Open Loop Frequency Response

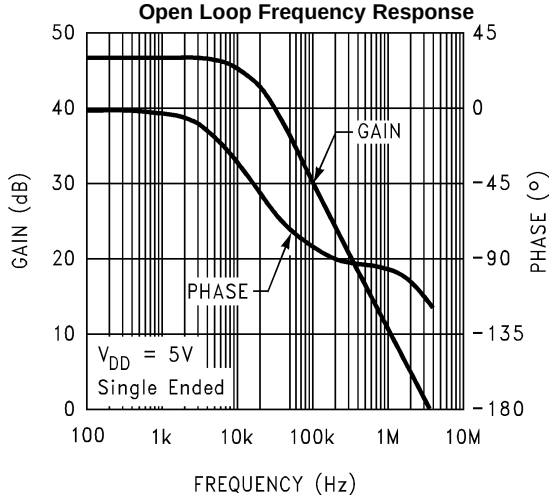

Figure 43.

Supply Current vs Supply Voltage

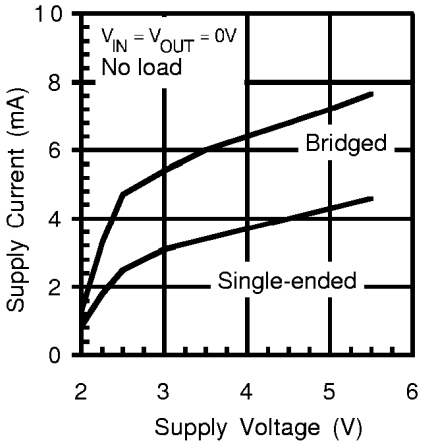

Figure 44.

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Table 1. External Components Description

Components		Functional Description
1.	R_i	The inverting input resistance, along with R_f, set the closed-loop gain. R_i, along with C_i, form a high pass filter with $f_c = 1/(2\pi R_i C_i)$.
2.	C_i	The input coupling capacitor blocks DC voltage at the amplifier's input terminals. C_i, along with R_i, create a highpass filter with $f_c = 1/(2\pi R_i C_i)$. Refer to the section, SELECTING PROPER EXTERNAL COMPONENTS, for an explanation of determining the value of C_i.
3.	R_f	The feedback resistance, along with R_i, set the closed-loop gain.
4.	C_S	The supply bypass capacitor. Refer to the POWER SUPPLY BYPASSING section for information about properly placing, and selecting the value of, this capacitor.
5.	C_B	The capacitor, C_B, filters the half-supply voltage present on the BYPASS pin. Refer to the SELECTING PROPER EXTERNAL COMPONENTS section for information concerning proper placement and selecting C_B's value.

APPLICATION INFORMATION

LM4863 PIN CONFIGURATION COMPATIBILITY

The LM4873's pin configuration simplifies the process of upgrading systems that use the LM4863. Except for its four MUX function pins, the LM4873's pin configuration matches the LM4863's pin configuration. If the LM4873's MUX functionality is not needed when replacing an LM4863, connect the MUX CTRL pin to either V_{DD} or ground. As shown in Table 2, grounding the MUX CTRL pin selects stereo input 1 (–IN A1 and –IN B1), whereas applying V_{DD} to the MUX CTRL pin selects stereo input 2 (–IN A2 and –IN B2).

STEREO-INPUT MULTIPLEXER (STEREO MUX)

Typical LM4873 applications use the MUX to switch between two stereo input signals. Each stereo channel's gain can be tailored to produce the required output signal level. Choosing the input and feedback resistor ratio sets a MUX channel's gain. Another configuration uses the MUX to select two different gains or frequency compensated gains to amplify a single pair of stereo input signals. Figure 45 shows two different feedback networks, Network 1 and Network 2. Network 1 produces increasing gain as the input signal's frequency decreases. This can be used to compensate a small, full-range speaker's low frequency response roll-off. Network 2 sets the gain for an alternate load such as headphones. Connecting the MUX CTRL and HP-IN pins together applies the same control voltage to the MUX pins when connecting and disconnecting headphones using the headphone jack shown in Figure 46 or Figure 47. Simultaneously applying the control voltage automatically selects the amplifier (headphone or bridge loads) and switches the gain (MUX channel selection). Alternatively, leave the control pins independently accessible. This allows a user to select bass boost as needed. This alternative user-selectable bass-boost scheme requires connecting equal ratio resistor feedback networks to each MUX input channel. The value of the resistor in the RC network is chosen to give a gain that is necessary to achieve the desired bass-boost.

Switching between the MUX channels may change the input signal source or the feedback resistor network. During the channel switching transition, the average voltage level present on the internal amplifier's input may change. This change can slew at a rate that may produce audible voltage transients or clicks in the amplifier's output signal. Using the MUX to select between two vastly dissimilar gains is a typical transient-producing situation. As the MUX is switched, an audible click may occur as the gain suddenly changes.

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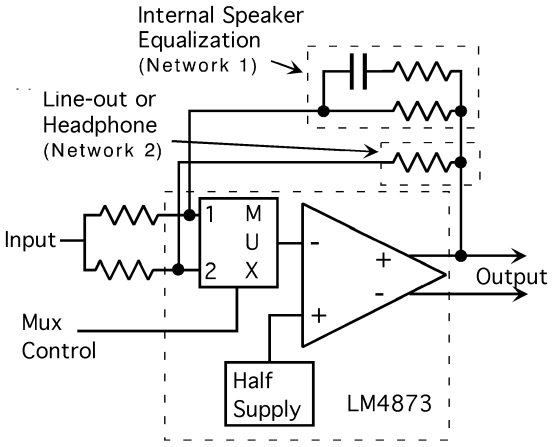

Figure 45. Input MUX Example

DSBGA PACKAGE PCB MOUNTING CONSIDERATIONS

PCB layout specifications unique to the LM4873's DSBGA package are found in Texas Instruments' AN-1112 (literature number SNVA009).

EXPOSED-DAP PACKAGE PCB MOUNTING CONSIDERATIONS

The LM4873's exposed-DAP (die attach paddle) packages (MTE, MTE-1, LQ) provide a low thermal resistance between the die and the PCB to which the part is mounted and soldered. This allows rapid heat transfer from the die to the surrounding PCB copper traces, ground plane and, finally, surrounding air. The result is a low voltage audio power amplifier that produces 2.1W at ≤ 1% THD with a 4Ω load. This high power is achieved through careful consideration of necessary thermal design. Failing to optimize thermal design may compromise the LM4873's high power performance and activate unwanted, though necessary, thermal shutdown protection.

The MTE, MTE-1, and LQ packages must have their DAPs soldered to a copper pad on the PCB. The DAP's PCB copper pad is connected to a large plane of continuous unbroken copper. This plane forms a thermal mass and heat sink and radiation area. Place the heat sink area on either outside plane in the case of a two-sided PCB, or on an inner layer of a board with more than two layers. Connect the DAP copper pad to the inner layer or backside copper heat sink area with 32(4x8) ((MTE), 40(4x10) (MTE-1), or 6(3x2) (LQ) vias. The via diameter should be 0.012in–0.013in with a 1.27mm pitch. Ensure efficient thermal conductivity by plating-through and solder-filling the vias.

Best thermal performance is achieved with the largest practical copper heat sink area. If the heatsink and amplifier share the same PCB layer, a nominal 2.5in^2 (min) area is necessary for 5V operation with a 4Ω load. Heatsink areas not placed on the same PCB layer as the LM4873 should be 5in^2 (min) for the same supply voltage and load resistance. The last two area recommendations apply for 25°C ambient temperature. Increase the area to compensate for ambient temperatures above 25°C. In systems using cooling fans, the LM4873MTE can take advantage of forced air cooling. With an air flow rate of 450 linear-feet per minute and a 2.5in^2 exposed copper or 5.0in^2 inner layer copper plane heatsink, the LM4873MTE can continuously drive a 3Ω load to full power. The LM4873LQ achieves the same output power level without forced air cooling. In all circumstances and conditions, the junction temperature must be held below 150°C to prevent activating the LM4873's thermal shutdown protection. The LM4873's power de-rating curve in the TYPICAL PERFORMANCE CHARACTERISTICS shows the maximum power dissipation versus temperature. Example PCB layouts for the exposed-DAP TSSOP and LQ packages are shown in the RECOMMENDED PRINTED CIRCUIT BOARD LAYOUT section. Further detailed and specific information concerning PCB layout, fabrication, and mounting an LQ (WQFN) package is available from Texas Instruments' AN-1187 (literature number SNOA401).

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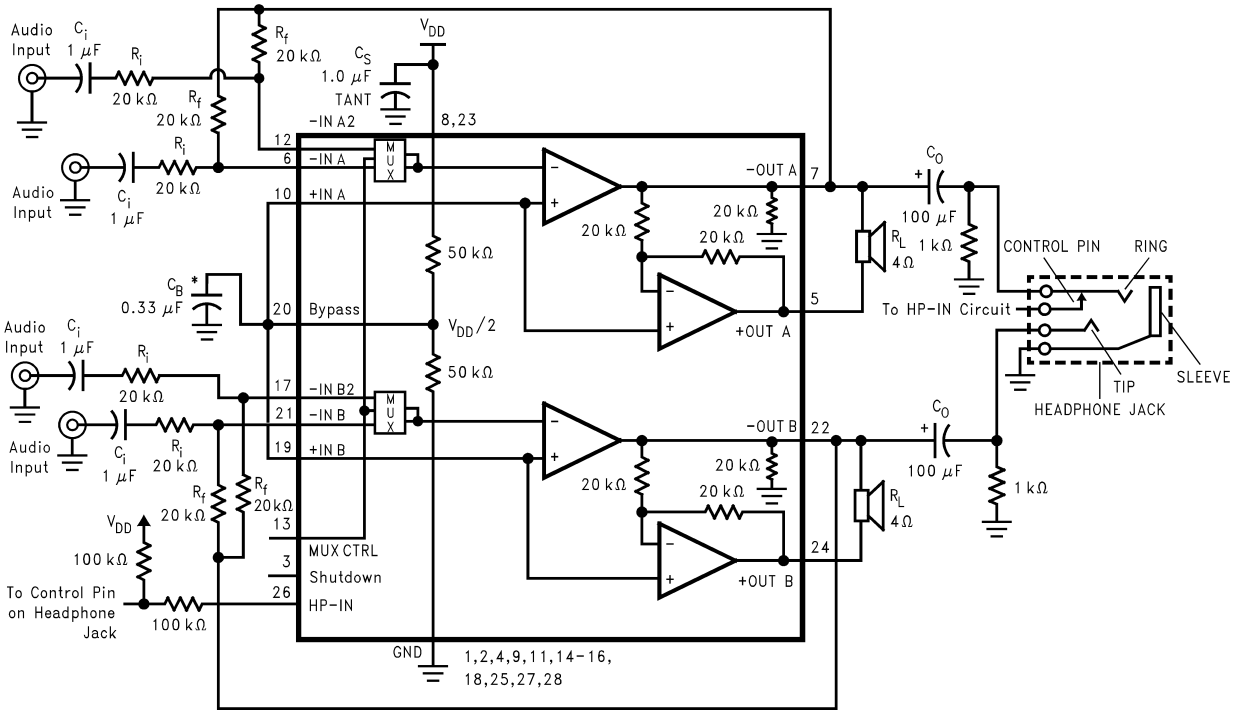
PCB LAYOUT AND SUPPLY REGULATION CONSIDERATIONS FOR DRIVING 3Ω AND 4Ω LOADS

Power dissipated by a load is a function of the voltage swing across the load and the load's impedance. As load impedance decreases, load dissipation becomes increasingly dependent on the interconnect (PCB trace and wire) resistance between the amplifier output pins and the load's connections. Residual trace resistance causes a voltage drop, which results in power dissipated in the trace and not in the load as desired. For example, 0.1Ω trace resistance reduces the output power dissipated by a 4Ω load from 2.1W to 2.0W. This problem of decreased load dissipation is exacerbated as load impedance decreases. Therefore, to maintain the highest load dissipation and widest output voltage swing, PCB traces that connect the output pins to a load must be as wide as possible.

Poor power supply regulation adversely affects maximum output power. A poorly regulated supply's output voltage decreases with increasing load current. Reduced supply voltage causes decreased headroom, output signal clipping, and reduced output power. Even with tightly regulated supplies, trace resistance creates the same effects as poor supply regulation. Therefore, making the power supply traces as wide as possible helps maintain full output voltage swing.



* Refer to the section SELECTING PROPER EXTERNAL COMPONENTS, for a detailed discussion of C_B size.
Pin out shown for the 28-pin Exposed-DAP TSSOP package. Refer to the Connection Diagrams for the pin out of the 20-pin Exposed-DAP TSSOP, Exposed-DAP WQFN, and DSBGA package.

Figure 46. Typical Audio Amplifier Application Circuit

BRIDGE CONFIGURATION EXPLANATION

As shown in Figure 46, the LM4873 consists of two pairs of operational amplifiers, forming a two-channel (channel A and channel B) stereo amplifier. (Though the following discusses channel A, it applies equally to channel B.) External resistors R_f and R_i set the closed-loop gain of Amp1A, whereas two internal 20kΩ resistors set Amp2A's gain at −1. The LM4873 drives a load, such as a speaker, connected between the two amplifier outputs, −OUTA and +OUTA.

Figure 46 shows that Amp1A's output serves as Amp2A's input. This results in both amplifiers producing signals identical in magnitude, but 180° out of phase. Taking advantage of this phase difference, a load is placed between −OUTA and +OUTA and driven differentially (commonly referred to as “bridge mode”). This results in a differential gain of

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$$A_{VD} = 2 * (R_f/R_i) \quad (1)$$

Bridge mode amplifiers are different from single-ended amplifiers that drive loads connected between a single amplifier's output and ground. For a given supply voltage, bridge mode has a distinct advantage over the single-ended configuration: its differential output doubles the voltage swing across the load. This produces four times the output power when compared to a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited or that the output signal is not clipped. To ensure minimum output signal clipping when choosing an amplifier's closed-loop gain, refer to the AUDIO POWER AMPLIFIER DESIGN section.

Another advantage of the differential bridge output is no net DC voltage across the load. This is accomplished by biasing channel A's and channel B's outputs at half-supply. This eliminates the coupling capacitor that single supply, single-ended amplifiers require. Eliminating an output coupling capacitor in a single-ended configuration forces a single-supply amplifier's half-supply bias voltage across the load. This increases internal IC power dissipation and may permanently damage loads such as speakers.

POWER DISSIPATION

Power dissipation is a major concern when designing a successful single-ended or bridged amplifier. Equation 2 states the maximum power dissipation point for a single-ended amplifier operating at a given supply voltage and driving a specified output load.

$$P_{DMAX} = (V_{DD})^2/(2\pi^2 R_L) \quad \text{Single-Ended} \quad (2)$$

However, a direct consequence of the increased power delivered to the load by a bridge amplifier is higher internal power dissipation for the same conditions.

The LM4873 has two operational amplifiers per channel. The maximum internal power dissipation per channel operating in the bridge mode is four times that of a single-ended amplifier. From Equation 3, assuming a 5V power supply and a 4Ω load, the maximum single channel power dissipation is 1.27W or 2.54W for stereo operation.

$$P_{DMAX} = 4 * (V_{DD})^2/(2\pi^2 R_L) \quad \text{Bridge Mode} \quad (3)$$

The LM4873's power dissipation is twice that given by Equation 2 or Equation 3 when operating in the single-ended mode or bridge mode, respectively. Twice the maximum power dissipation point given by Equation 3 must not exceed the power dissipation given by Equation 4:

$$P_{DMAX}' = (T_{JMAX} - T_A)/\theta_{JA} \quad (4)$$

The LM4873's T_{JMAX} = 150°C. In the LQ package soldered to a DAP pad that expands to a copper area of 5in^2 on a PCB, the LM4873's θ_{JA} is 20°C/W. In the MTE and MTE-1 packages soldered to a DAP pad that expands to a copper area of 2in^2 on a PCB, the LM4873's θ_{JA} is 41°C/W. At any given ambient temperature T_A, use Equation 4 to find the maximum internal power dissipation supported by the IC packaging. Rearranging Equation 4 and substituting P_{DMAX} for P_{DMAX}' results in Equation 5. This equation gives the maximum ambient temperature that still allows maximum stereo power dissipation without violating the LM4873's maximum junction temperature.

$$T_A = T_{JMAX} - 2*P_{DMAX}\,\theta_{JA} \quad (5)$$

For a typical application with a 5V power supply and an 4Ω load, the maximum ambient temperature that allows maximum stereo power dissipation without exceeding the maximum junction temperature is approximately 99°C for the LQ package and 45°C for the MTE and MTE-1 packages.

$$T_{JMAX} = P_{DMAX}\,\theta_{JA} + T_A \quad (6)$$

Equation 6 gives the maximum junction temperature T_{JMAX}. If the result violates the LM4873's 150°C, reduce the maximum junction temperature by reducing the power supply voltage or increasing the load resistance. Further allowance should be made for increased ambient temperatures.

The above examples assume that a device is a surface mount part operating around the maximum power dissipation point. Since internal power dissipation is a function of output power, higher ambient temperatures are allowed as output power or duty cycle decreases.

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If the result of Equation 2 is greater than that of Equation 3, then decrease the supply voltage, increase the load impedance, or reduce the ambient temperature. If these measures are insufficient, a heat sink can be added to reduce θ_{JA}. The heat sink can be created using additional copper area around the package, with connections to the ground pin(s), supply pin and amplifier output pins. External, solder attached SMT heatsinks such as the Thermalloy 7106D can also improve power dissipation. When adding a heat sink, the θ_{JA} is the sum of θ_{JC}, θ_{CS}, and θ_{SA}. (θ_{JC} is the junction-to-case thermal impedance, θ_{CS} is the case-to-sink thermal impedance, and θ_{SA} is the sink-to-ambient thermal impedance.) Refer to the TYPICAL PERFORMANCE CHARACTERISTICS curves for power dissipation information at lower output power levels.

POWER SUPPLY BYPASSING

As with any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. Applications that employ a 5V regulator typically use a 10 µF in parallel with a 0.1 µF filter capacitors to stabilize the regulator's output, reduce noise on the supply line, and improve the supply's transient response. However, their presence does not eliminate the need for a local 1.0 µF tantalum bypass capacitance connected between the LM4873's supply pins and ground. Do not substitute a ceramic capacitor for the tantalum. Doing so may cause oscillation. Keep the length of leads and traces that connect capacitors between the LM4873's power supply pin and ground as short as possible. Connecting a 1µF capacitor, C_B, between the BYPASS pin and ground improves the internal bias voltage's stability and improves the amplifier's PSRR. The PSRR improvements increase as the bypass pin capacitor value increases. Too large, however, increases turn-on time and can compromise amplifier's click and pop performance. The selection of bypass capacitor values, especially C_B, depends on desired PSRR requirements, click and pop performance (as explained in the section, SELECTING PROPER EXTERNAL COMPONENTS), system cost, and size constraints.

MICRO-POWER SHUTDOWN

The voltage applied to the SHUTDOWN pin controls the LM4873's shutdown function. Activate micro-power shutdown by applying V_{DD} to the SHUTDOWN pin. When active, the LM4873's micro-power shutdown feature turns off the amplifier's bias circuitry, reducing the supply current. The logic threshold is typically $V_{DD}/2$. The low 0.7 µA typical shutdown current is achieved by applying a voltage that is as near as V_{DD} as possible to the SHUTDOWN pin. A voltage that is less than V_{DD} may increase the shutdown current. Table 2 shows the logic signal levels that activate and deactivate micro-power shutdown and headphone amplifier operation.

There are a few ways to control the micro-power shutdown. These include using a single-pole, single-throw switch, a microprocessor, or a microcontroller. When using a switch, connect an external 10kΩ pull-up resistor between the SHUTDOWN pin and V_{DD}. Connect the switch between the SHUTDOWN pin and ground. Select normal amplifier operation by closing the switch. Opening the switch connects the SHUTDOWN pin to V_{DD} through the pull-up resistor, activating micro-power shutdown. The switch and resistor ensure that the SHUTDOWN pin will not float. This prevents unwanted state changes. In a system with a microprocessor or a microcontroller, use a digital output to apply the control voltage to the SHUTDOWN pin. Driving the SHUTDOWN pin with active circuitry eliminates the pull up resistor.

Table 2. Logic Level Truth Table for SHUTDOWN, HP-IN, and MUX Operation

SHUTDOWN PIN	HP-INPIN	MUX CHANNEL SELECT PIN	OPERATIONAL MODE (MUX INPUT CHANNEL #)
Logic Low	Logic Low	Logic Low	Bridged Amplifiers (1)
Logic Low	Logic Low	Logic High	Bridged Amplifiers (2)
Logic Low	Logic High	Logic Low	Single-Ended Amplifiers (1)
Logic Low	Logic High	Logic High	Single-Ended Amplifiers (2)
Logic High	X	X	Micro-Power Shutdown

HP-IN FUNCTION

Applying a voltage between 4V and V_{DD} to the LM4873's HP-IN headphone control pin turns off Amp2A and Amp2B, muting a bridged-connected load. Quiescent current consumption is reduced when the IC is in this single-ended mode.

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Figure 47 shows the implementation of the LM4873's headphone control function. With no headphones connected to the headphone jack, the R1-R2 voltage divider sets the voltage applied to the HP-IN pin (pin 16) at approximately 50mV. This 50mV enables Amp1B and Amp2B, placing the LM4873 in bridged mode operation. The output coupling capacitor blocks the amplifier's half supply DC voltage, protecting the headphones.

The HP-IN threshold is set at 4V. While the LM4873 operates in bridged mode, the DC potential across the load is essentially 0V. Therefore, even in an ideal situation, the output swing cannot cause a false single-ended trigger. Connecting headphones to the headphone jack disconnects the headphone jack contact pin from −OUTA and allows R1 to pull the HP Sense pin up to V_{DD}. This enables the headphone function, turns off Amp2A and Amp2B, and mutes the bridged speaker. The amplifier then drives the headphones, whose impedance is in parallel with resistor R2 and R3. These resistors have negligible effect on the LM4873's output drive capability since the typical impedance of headphones is 32Ω.

Figure 47 also shows the suggested headphone jack electrical connections. The jack is designed to mate with a three-wire plug. The plug's tip and ring should each carry one of the two stereo output signals, whereas the sleeve should carry the ground return. A headphone jack with one control pin contact is sufficient to drive the HP-IN pin when connecting headphones.

A microprocessor or a switch can replace the headphone jack contact pin. When a microprocessor or switch applies a voltage greater than 4V to the HP-IN pin, a bridge-connected speaker is muted and Amp1A and Amp2A drive a pair of headphones.

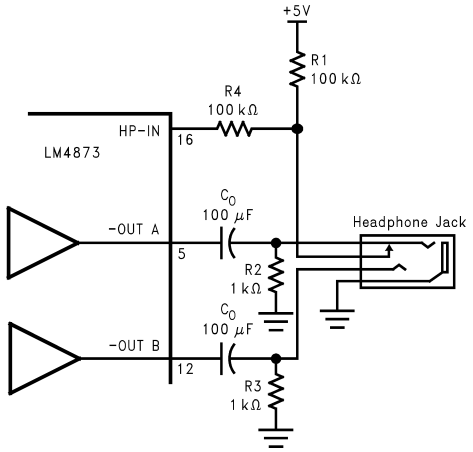

Figure 47. Headphone Circuit

SELECTING PROPER EXTERNAL COMPONENTS

Optimizing the LM4873's performance requires properly selecting external components. Though the LM4873 operates well when using external components with wide tolerances, best performance is achieved by optimizing component values.

The LM4873 is unity-gain stable, giving a designer maximum design flexibility. The gain should be set to no more than a given application requires. This allows the amplifier to achieve minimum THD+N and maximum signal-to-noise ratio. These parameters are compromised as the closed-loop gain increases. However, low gain demands input signals with greater voltage swings to achieve maximum output power. Fortunately, many signal sources such as audio CODECs have outputs of $1V_{RMS}$ ($2.83V_{P-P}$). Please refer to the AUDIO POWER AMPLIFIER DESIGN section for more information on selecting the proper gain.

Input Capacitor Value Selection

Amplifying the lowest audio frequencies requires high value input coupling capacitor (C_i in Figure 46). A high value capacitor can be expensive and may compromise space efficiency in portable designs. In many cases, however, the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 150 Hz. Applications using speakers with this limited frequency response reap little improvement by using large input capacitor.

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Besides effecting system cost and size, C_i has an affect on the LM4873's click and pop performance. When the supply voltage is first applied, a transient (pop) is created as the charge on the input capacitor changes from zero to a quiescent state. The magnitude of the pop is directly proportional to the input capacitor's size. Higher value capacitors need more time to reach a quiescent DC voltage (usually $V_{DD}/2$) when charged with a fixed current. The amplifier's output charges the input capacitor through the feedback resistor, R_f. Thus, pops can be minimized by selecting an input capacitor value that is no higher than necessary to meet the desired −3dB frequency.

As shown in Figure 46, the input resistor (R_I) and the input capacitor, C_I produce a −3dB high pass filter cutoff frequency that is found using Equation 7.

$$f_{-3\,dB} = \frac{1}{2\pi R_{IN} C_I} \tag{7}$$

As an example when using a speaker with a low frequency limit of 150Hz, C_i, using Equation 4 is 0.063µF. The 1.0µF C_i shown in Figure 46 allows the LM4873 to drive high efficiency, full range speaker whose response extends below 30Hz.

Bypass Capacitor Value Selection

Besides minimizing the input capacitor size, careful consideration should be paid to value of C_B, the capacitor connected to the BYPASS pin. Since C_B determines how fast the LM4873 settles to quiescent operation, its value is critical when minimizing turn-on pops. The slower the LM4873's outputs ramp to their quiescent DC voltage (nominally 1/2 V_{DD}), the smaller the turn-on pop. Choosing C_B equal to 1.0 µF along with a small value of C_i (in the range of 0.1 µF to 0.39 µF), produces a click-less and pop-less shutdown function. As discussed above, choosing C_i no larger than necessary for the desired bandwith helps minimize clicks and pops.

OPTIMIZING CLICK AND POP REDUCTION PERFORMANCE

The LM4873 contains circuitry that minimizes turn-on and shutdown transients or “clicks and pop”. For this discussion, turn-on refers to either applying the power supply voltage or when the shutdown mode is deactivated. While the power supply is ramping to its final value, the LM4873's internal amplifiers are configured as unity gain buffers. An internal current source changes the voltage of the BYPASS pin in a controlled, linear manner. Ideally, the input and outputs track the voltage applied to the BYPASS pin. The gain of the internal amplifiers remains unity until the voltage on the bypass pin reaches 1/2 V_{DD} . As soon as the voltage on the bypass pin is stable, the device becomes fully operational. Although the BYPASS pin current cannot be modified, changing the size of C_B alters the device's turn-on time and the magnitude of “clicks and pops”. Increasing the value of C_B reduces the magnitude of turn-on pops. However, this presents a tradeoff: as the size of C_B increases, the turn-on time increases. There is a linear relationship between the size of C_B and the turn-on time. Here are some typical turn-on times for various values of C_B:

C_B	T_{ON}
0.01µF	20ms
0.1µF	200ms
0.22µF	440ms
0.47µF	940ms
1.0µF	2sec

In order eliminate “clicks and pops”, all capacitors must be discharged before turn-on. Rapidly switching V_{DD} may not allow the capacitors to fully discharge, which may cause “clicks and pops”. In a single-ended configuration, the output is coupled to the load by C_{OUT}. This capacitor usually has a high value. C_{OUT} discharges through internal 20kΩ resistors. Depending on the size of C_{OUT}, the discharge time constant can be relatively large. To reduce transients in single-ended mode, an external 1kΩ–5kΩ resistor can be placed in parallel with the internal 20kΩ resistor. The tradeoff for using this resistor is increased quiescent current.

NO LOAD STABILITY

The LM4873 may exhibit low level oscillation when the load resistance is greater than 10kΩ. This oscillation only occurs as the output signal swings near the supply voltages. Prevent this oscillation by connecting a 5kΩ between the output pins and ground.

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AUDIO POWER AMPLIFIER DESIGN

Audio Amplifier Design: Driving 1W into an 8Ω Load

The following are the desired operational parameters:

Power Output:	$1W_{RMS}$
Load Impedance:	8Ω
Input Level:	$1V_{rms}$
Input Impedance:	20kΩ
Bandwidth:	100Hz−20kHz ± 0.25dB

The design begins by specifying the minimum supply voltage necessary to obtain the specified output power. One way to find the minimum supply voltage is to use the Output Power vs Supply Voltage curve in the TYPICAL PERFORMANCE CHARACTERISTICS section. Another way, using Equation 8, is to calculate the peak output voltage necessary to achieve the desired output power for a given load impedance. To account for the amplifier's dropout voltage, two additional voltages, based on the Dropout Voltage vs Supply Voltage in the TYPICAL PERFORMANCE CHARACTERISTICS curves, must be added to the result obtained by Equation 8. The result in Equation 9.

$$V_{OUTPEAK} = \sqrt{(2R_L P_O)} \quad (8)$$

$$V_{DD} \geq (V_{OUTPEAK} + (V_{ODTOP} + V_{ODBOT})) \quad (9)$$

The Output Power vs Supply Voltage graph for an 8Ω load indicates a minimum supply voltage of 4.6V. This is easily met by the commonly used 5V supply voltage. The additional voltage creates the benefit of headroom, allowing the LM4873 to produce peak output power in excess of 1W without clipping or other audible distortion. The choice of supply voltage must also not create a situation that violates maximum power dissipation as explained above in the POWER DISSIPATION section.

After satisfying the LM4873's power dissipation requirements, the minimum differential gain needed to achieve 1W dissipation in an 8Ω load is found using Equation 10.

$$A_{VD} \geq \sqrt{(P_O R_L)}/(V_{IN}) = V_{orms}/V_{inrms} \quad (10)$$

Thus, a minimum gain of 2.83 allows the LM4873's to reach full output swing and maintain low noise and THD+N performance. For this example, let $A_{VD} = 3$.

The amplifier's overall gain is set using the input (R_i) and feedback (R_f) resistors. With the desired input impedance set at 20kΩ, the feedback resistor is found using Equation 11.

$$R_f/R_i = A_{VD}/2 \quad (11)$$

The value of R_f is 30kΩ.

The last step in this design example is setting the amplifier's −3dB frequency bandwidth. To achieve the desired ±0.25dB pass band magnitude variation limit, the low frequency response must extend to at least one-fifth the lower bandwidth limit and the high frequency response must extend to at least five times the upper bandwidth limit. The gain variation for both response limits is 0.17dB, well within the ±0.25dB desired limit. The results are an

$$f_L = 100Hz/5 = 20Hz$$

and an

$$f_H = 20kHz*5 = 100kHz.$$

As mentioned in the External Components Description, R_i and C_i create a highpass filter that sets the amplifier's lower bandpass frequency limit. Find the coupling capacitor's value using Equation 12.

$$C_i \geq 1/(2\pi R_i f_L) \quad (12)$$

The result is

$$1/(2\pi*20k\Omega*20Hz) = 0.398\mu F. \quad (13)$$

Use a 0.39µF capacitor, the closest standard value.

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The product of the desired high frequency cutoff (100kHz in this example) and the differential gain, AVD, determines the upper passband response limit. With A_{VD} = 3 and f_H = 100kHz, the closed-loop gain bandwidth product (GBWP) is 300kHz. This is less than the LM4873's 3.5MHz GBWP. With this margin, the amplifier can be used in designs that require more differential gain while avoiding performance-restricting bandwidth limitations.

RECOMMENDED PRINTED CIRCUIT BOARD LAYOUT

Figure 48 through Figure 50 show the recommended two-layer PC board layout that is optimized for the 20-pin MTE-packaged LM4873 and associated external components. Figure 51 through Figure 55 show the recommended four-layer PC board layout that is optimized for the 24-pin LQ-packaged LM4873 and associated external components. Figure 56 through Figure 60 show the recommended four-layer PC board layout that is optimized for the 20-pin DSBGA-packaged LM4873 and associated external components. These circuits are designed for use with an external 5V supply and 4Ω speakers.

These circuit boards are easy to use. Apply 5V and ground to the board's V_{DD} and GND pads, respectively. Connect 4Ω speakers between the board's −OUTA and +OUTA and OUTB and +OUTB pads.

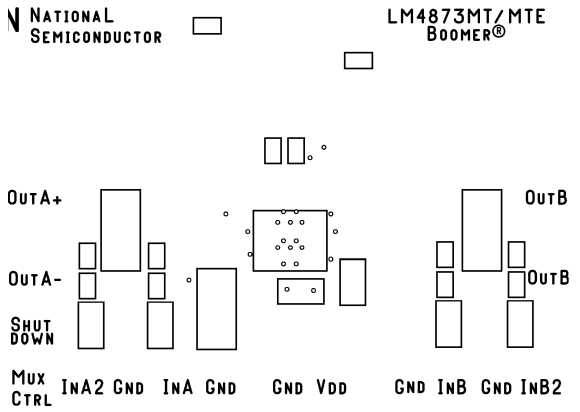

Figure 48. Recommended MTE PC Board Layout: Component-Side Silkscreen

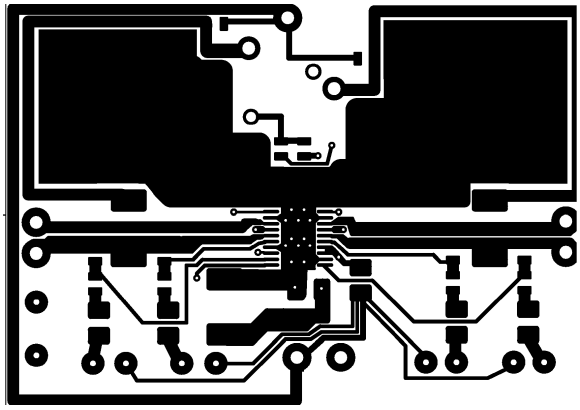

Figure 49. Recommended MTE PC Board Layout: Component-Side Layout

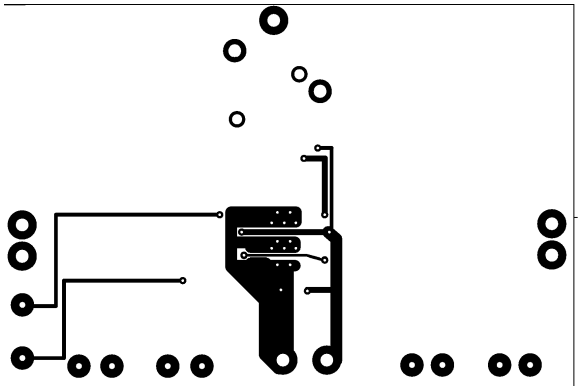

Figure 50. Recommended MTE PC Board Layout: Bottom-Side Layout

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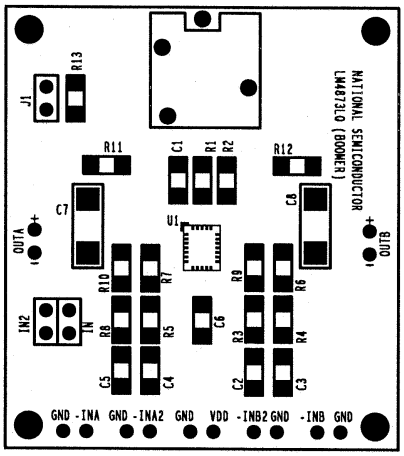

Figure 51. Recommended LQ PC Board Layout: Component-Side Silkscreen

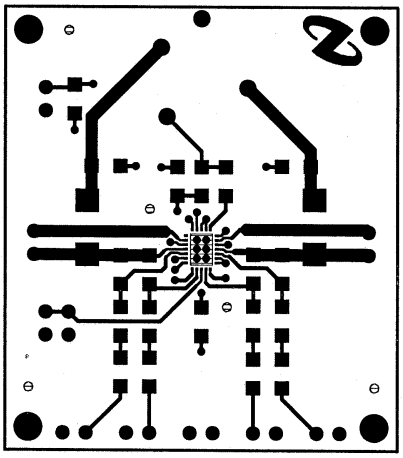

Figure 52. Recommended LQ PC Board Layout: Component-Side Layout

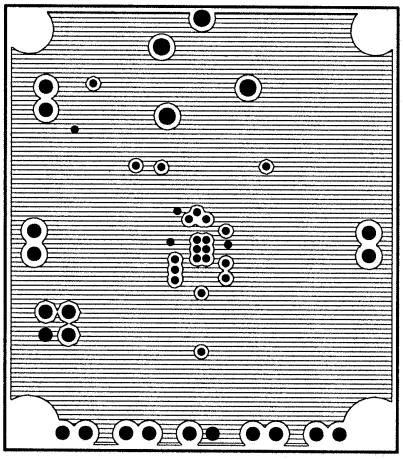

Figure 53. Recommended LQ PC Board Layout: Upper Inner-Layer Layout

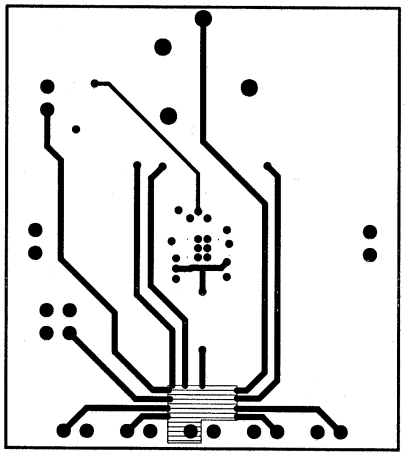

Figure 54. Recommended LQ PC Board Layout: Lower Inner-Layer Layout

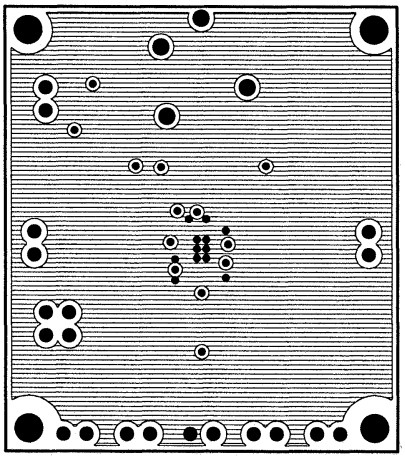

Figure 55. Recommended LQ PC Board Layout: Bottom-Side Layout

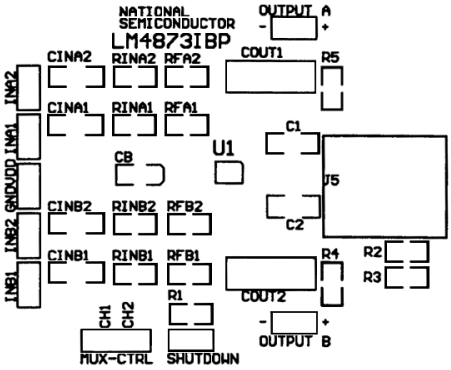

Figure 56. Recommended 20-pin DSBGA PC Board Layout: Component-Side Silkscreen

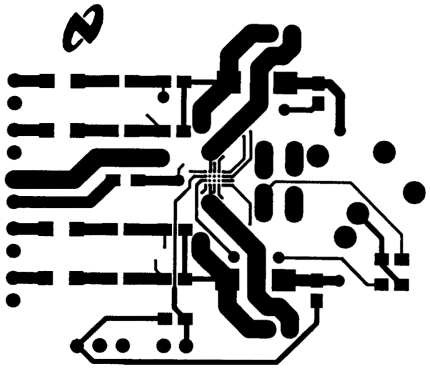

Figure 57. Recommended 20-pin DSBGA PC Board Layout: Component-Side Layout

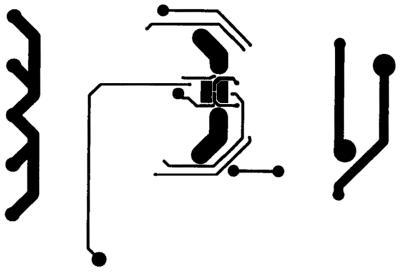

Figure 58. Recommended 20-pin DSBGA PC Board Layout: Upper Inner-Layer Layout

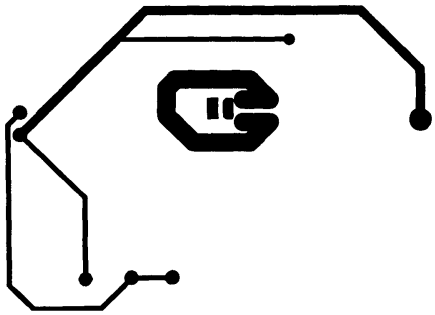

Figure 59. Recommended 20-pin DSBGA PC Board Layout: Lower Inner-Layer Layout

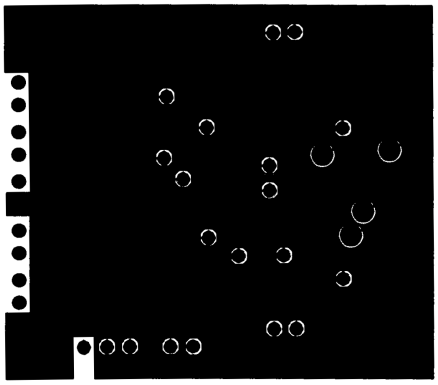

Figure 60. Recommended 20-pin DSBGA PC Board Layout: Bottom-Side Layout

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REVISION HISTORY

Changes from Revision D (May 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format	24

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM4873MTE/NOPB	ACTIVE	HTSSOP	PWP	20	250	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM		LM4873 MTE	Samples
LM4873MTEX/NOPB	ACTIVE	HTSSOP	PWP	20	2500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 85	LM4873 MTE	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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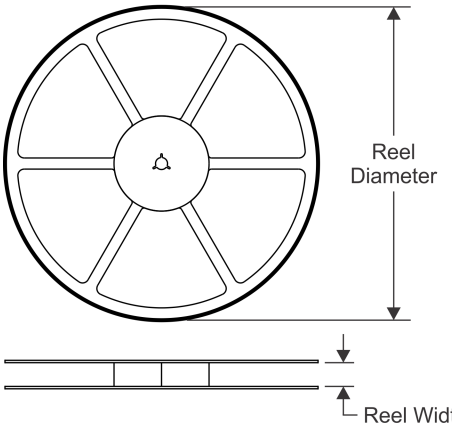
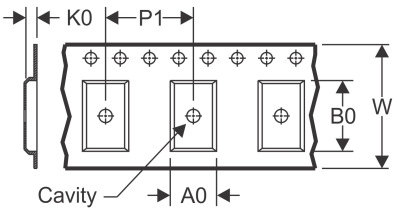
TAPE AND REEL INFORMATION

REEL DIMENSIONS

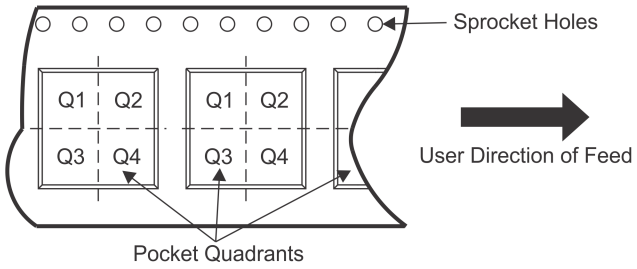


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

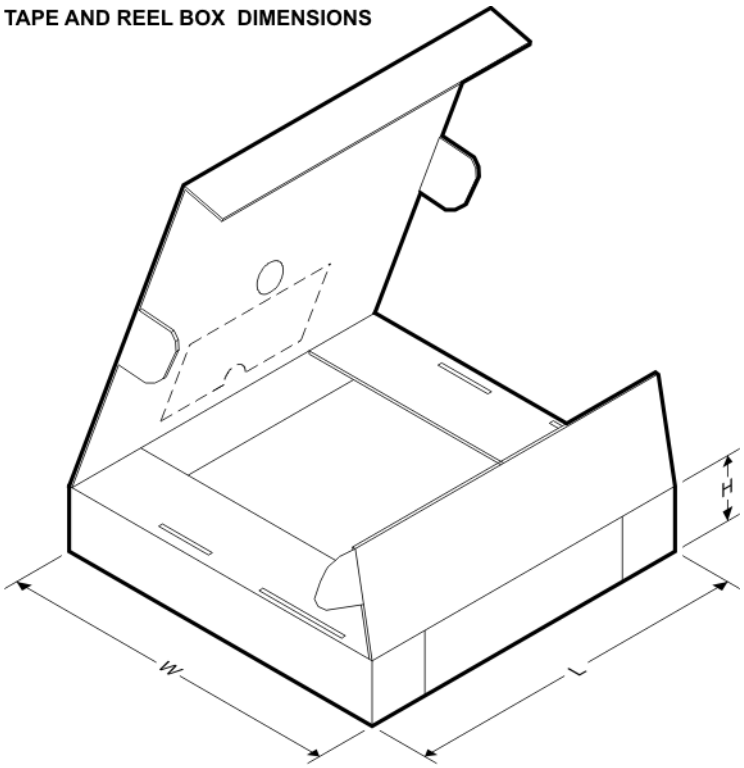
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM4873MTE/NOPB	HTSSOP	PWP	20	250	178.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
LM4873MTEX/NOPB	HTSSOP	PWP	20	2500	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

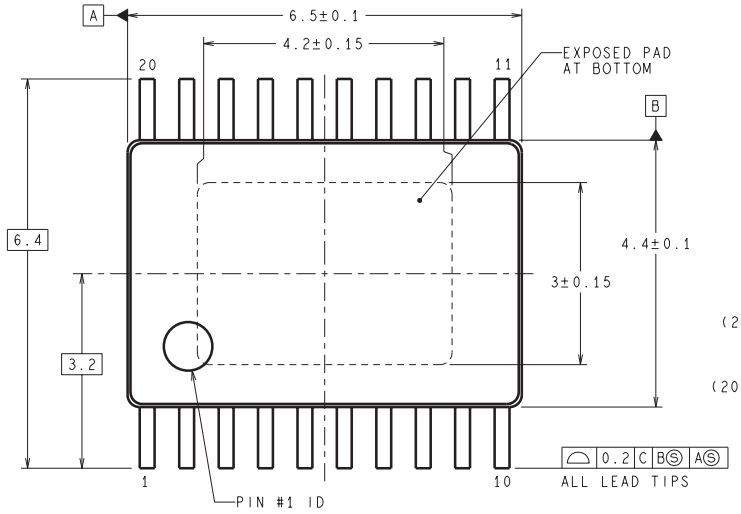
TAPE AND REEL BOX DIMENSIONS

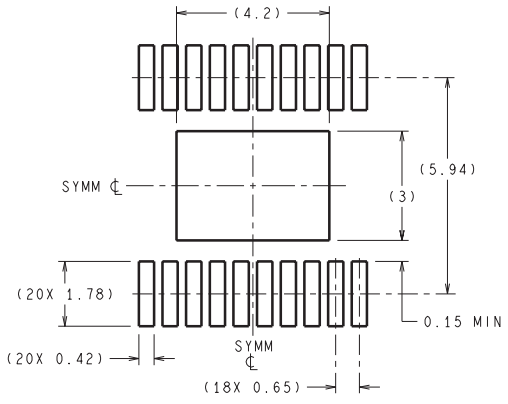


*All dimensions are nominal

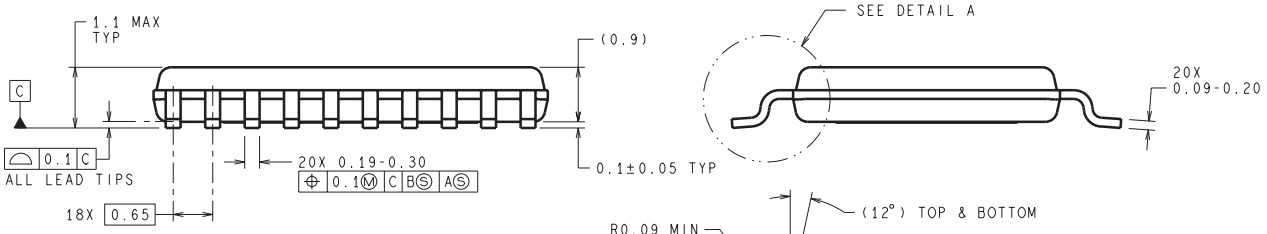
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM4873MTE/NOPB	HTSSOP	PWP	20	250	210.0	185.0	35.0
LM4873MTEX/NOPB	HTSSOP	PWP	20	2500	367.0	367.0	35.0

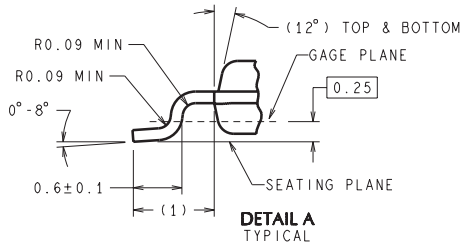
PWP0020A





RECOMMENDED LAND PATTERN





DETAIL A
TYPICAL

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY

MXA20A (Rev C)

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