LTM4630EY-1
High Efficiency, PolyPhase 105A Step-Down Power µModule™ Regulator

DESCRIPTION

Demonstration Circuit 2164A-B features a PolyPhase® design using the LTM®4630EY-1 (A-grade), the high efficiency, high density, dual 18A, switch mode step-down power module regulator. The input voltage is from 4.5V to 15V. The output voltage is jumper selectable from 0.9V to 1.8V. DC2164A-B can deliver nominal 105A output current. As explained in the data sheet, output current derating is necessary for certain V_{IN}, V_{OUT}, and thermal conditions. The LTM4630-1A on DC2164A-B always operate in continuous conduction mode. The switching frequency can be programmed through a resistor or can be synchronized to an external clock signal. The board allows the user to program how its output voltage ramps up and down through the TRACK pin. The output voltage is tightly regulated between V_O^+ and V_O^- through remote output voltage sensing which improves output voltage regulation at heavy loads. The LTM4630-1A has ±0.8% total DC errors. These features and the availability of the LTM4630EY-1 in a compact 16mm × 16mm × 5.01mm BGA package make it ideal for use in many high-density point-of-load regulation applications. The LTM4630-1 data sheet must be read in conjunction with this demo manual for working on or modifying the demo circuit DC2164A-B.

Design files for this circuit board are available at http://www.linear.com/demo/DC2164A-B

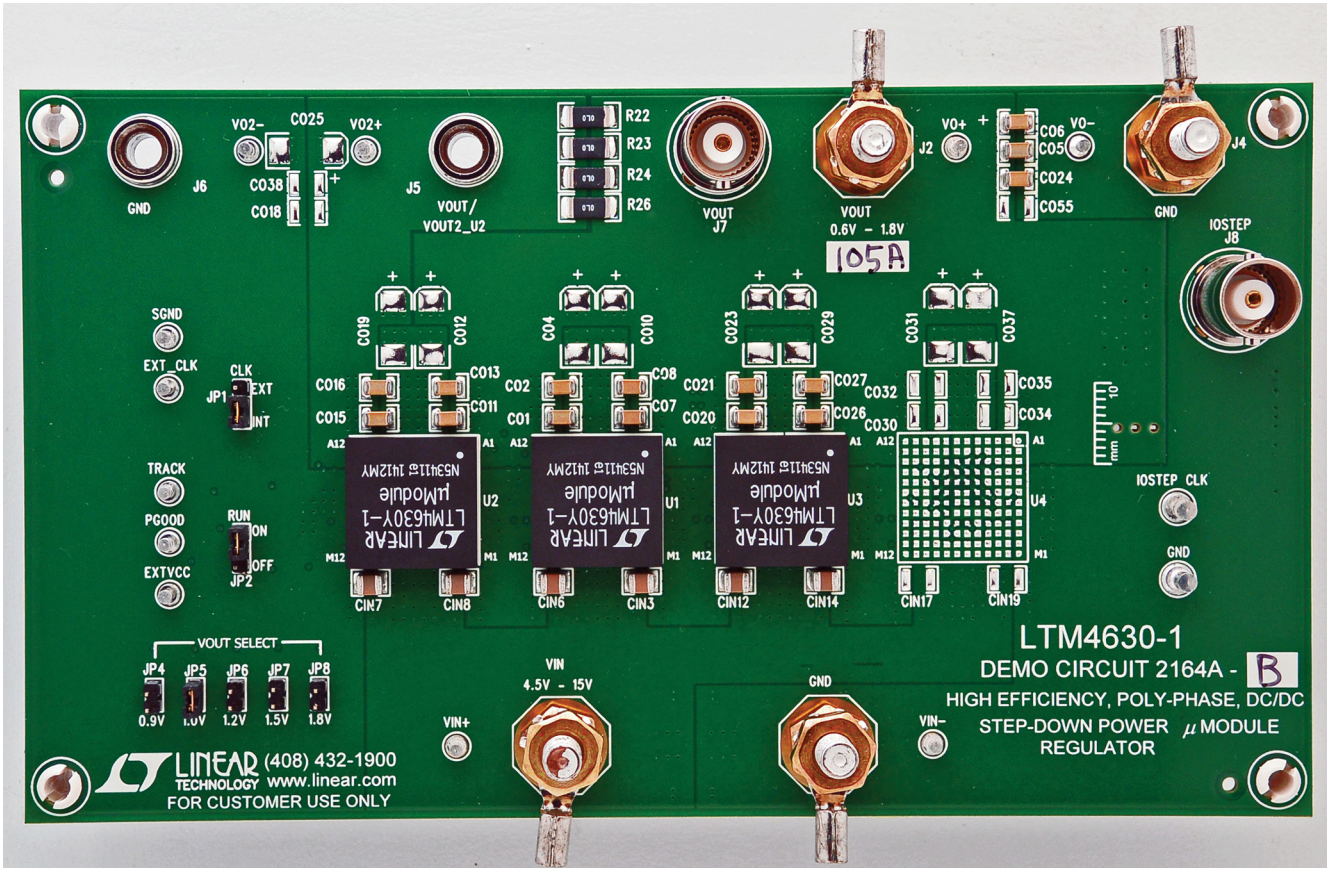


Figure 1. 105A PolyPhase LTM4630-1/DC2164A-B Demo Board

PERFORMANCE SUMMARY

Specifications are at T_A = 25°C

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range		4.5		15	V
Output Voltage V_{OUT}	V_{IN} = 4.5 ~ 15V, I_{OUT} = 0A ~ 105A, JP5: 1V		1 ±0.8% (0.992 ~ 1.008)		V
Maximum Continuous Output Current	Derating Is Necessary for Certain V_{IN}, V_{OUT} and Thermal Conditions, See Data Sheet for Detail		105		A
Default Operating Frequency			400		kHz
Resistor Programmable Frequency Range		400		780	kHz
External Clock Sync. Frequency Range		400		780	kHz
Efficiency	V_{IN} = 12V, V_{OUT} = 1V, I_{OUT} = 105A, f_{SW} = 400kHz		83.8 (See Figure 3)		%
Load Transient	V_{IN} = 12V, V_{OUT} = 1V, I_{STEP} = 0A ~ 26.25A		<53.1 (See Figure 4)		mV

QUICK START PROCEDURE

Demonstration circuit 2164A-B is easy to set up to evaluate the performance of PolyPhase operation of the LTM4630EY-1. Due to the high input/output current, user should select the proper input supply/load/cable which can sustain the full load operation. It's recommended to pull load current from J2 and J4. The load current pulled from J5 and J6 shouldn't exceed 18A. Please refer to Figure 2 for proper measurement setup and follow the procedure below:

1. Place jumpers in the following positions for a typical 1V_{OUT} application:

JP1	*JP2*	*JP4 ~ JP8*
CLK	**RUN**	**VOUT SELECT**
INT	OFF	ON JP5/1.0V

2. With power off, connect the input power supply, load and meters as shown in Figure 2. Preset the load to 0A and V_{IN} supply to 12V.
3. Turn on the power supply at the input. Place JP2 to ON position. The output voltage between V_O^+ and V_O^- should be 1V ±0.8% (0.992V ~ 1.008V).
4. Once the proper output voltage is established, adjust the load within the operating range and observe the output voltage regulation, output voltage ripple, efficiency and other parameters. Output voltage ripple should be measured at J7 with BNC cables. 50Ω termination should be set on the oscilloscope or BNC cables.
5. (Optional) For optional load transient test, apply an adjustable pulse signal between IOSTEP CLK and GND test point. Pulse amplitude (3V ~ 3.5V) sets the load step current amplitude. The output transient current can be monitored at the BNC connector J8 (5mV/A). The pulse signal should be very small duty cycle (<10%) to limit the thermal stress on the transient load circuit.
6. (Optional) LTM4630-1 can be synchronized to an external clock signal. Place the JP1 jumper on EXT and apply a clock signal (0V ~ 5V, square wave) on the EXT_CLK test point.
7. (Optional) The outputs of LTM4630-1 can track another supply. The output voltage tracks the voltage on TRACK when a valid signal is applied on the test point.
8. (Optional) DC2164A-B can be configured to a dual outputs configuration with V_0 at 87A load current and V_{02} at 18A load current. Stuff 0Ω resistor on R61 and 0.1µF on C14. Remove R22, R23, R24, R26, R27, R28, R32, R33, R35. Output voltage V_{02} is set by R37 based on the equation V_{02} = 0.6V(1 + 60.4k/R37).

QUICK START PROCEDURE

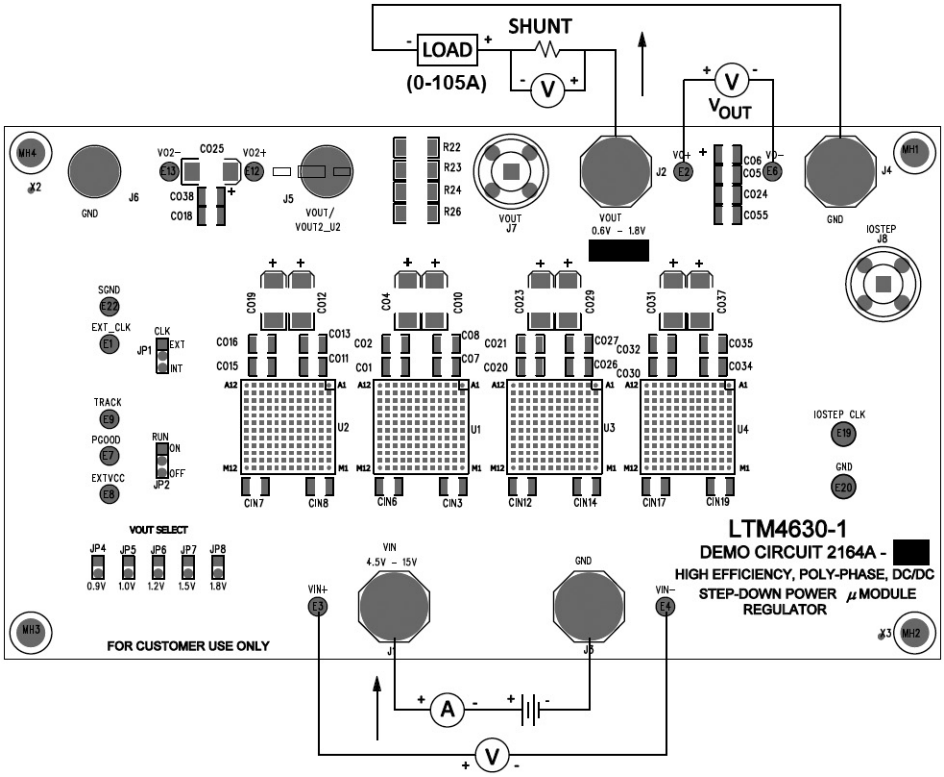


Figure 2. Test Setup of DC2164A-B

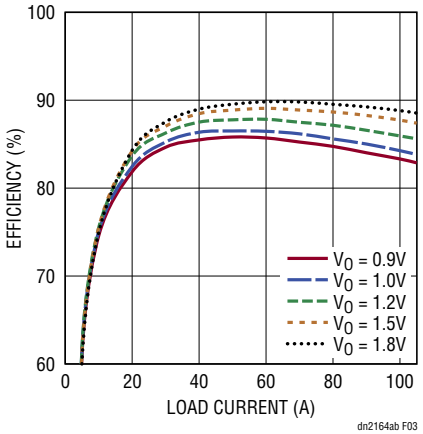


Figure 3. Measured Efficiency V_{IN} = 12V, f_{SW} = 400kHz

QUICK START PROCEDURE

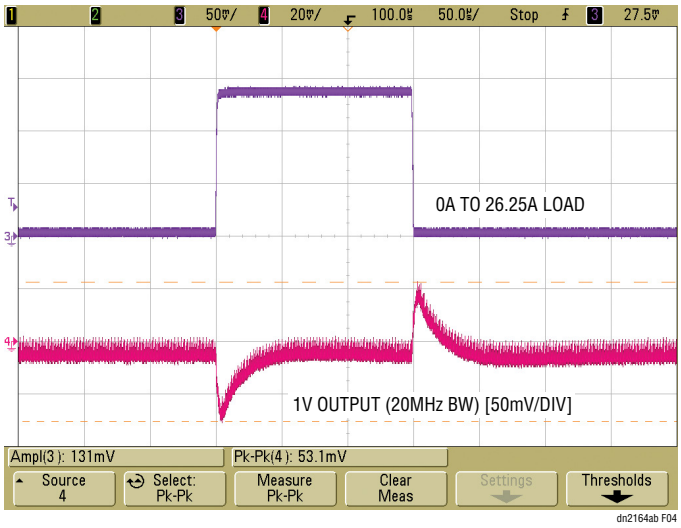


Figure 4. Load Transient 0A to 26.25A (V_{IN} = 12V, V_{OUT} = 1V)

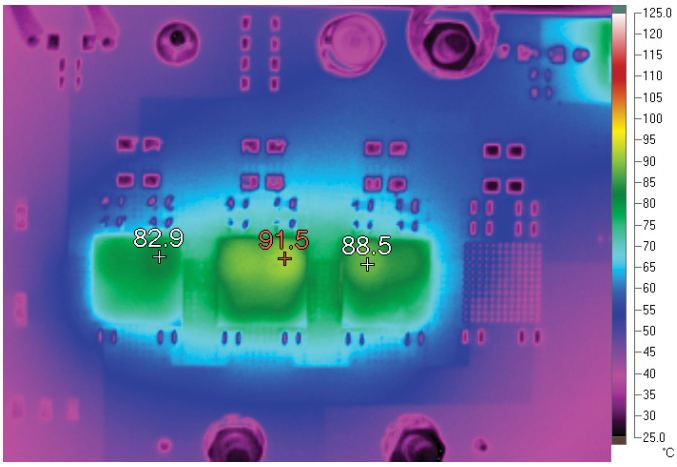


Figure 5. Thermal Capture at $12V_{IN}$, $1V_{OUT}$, 105A (T_A = 25°C, 400 LFM Airflow and No Heat Sink)

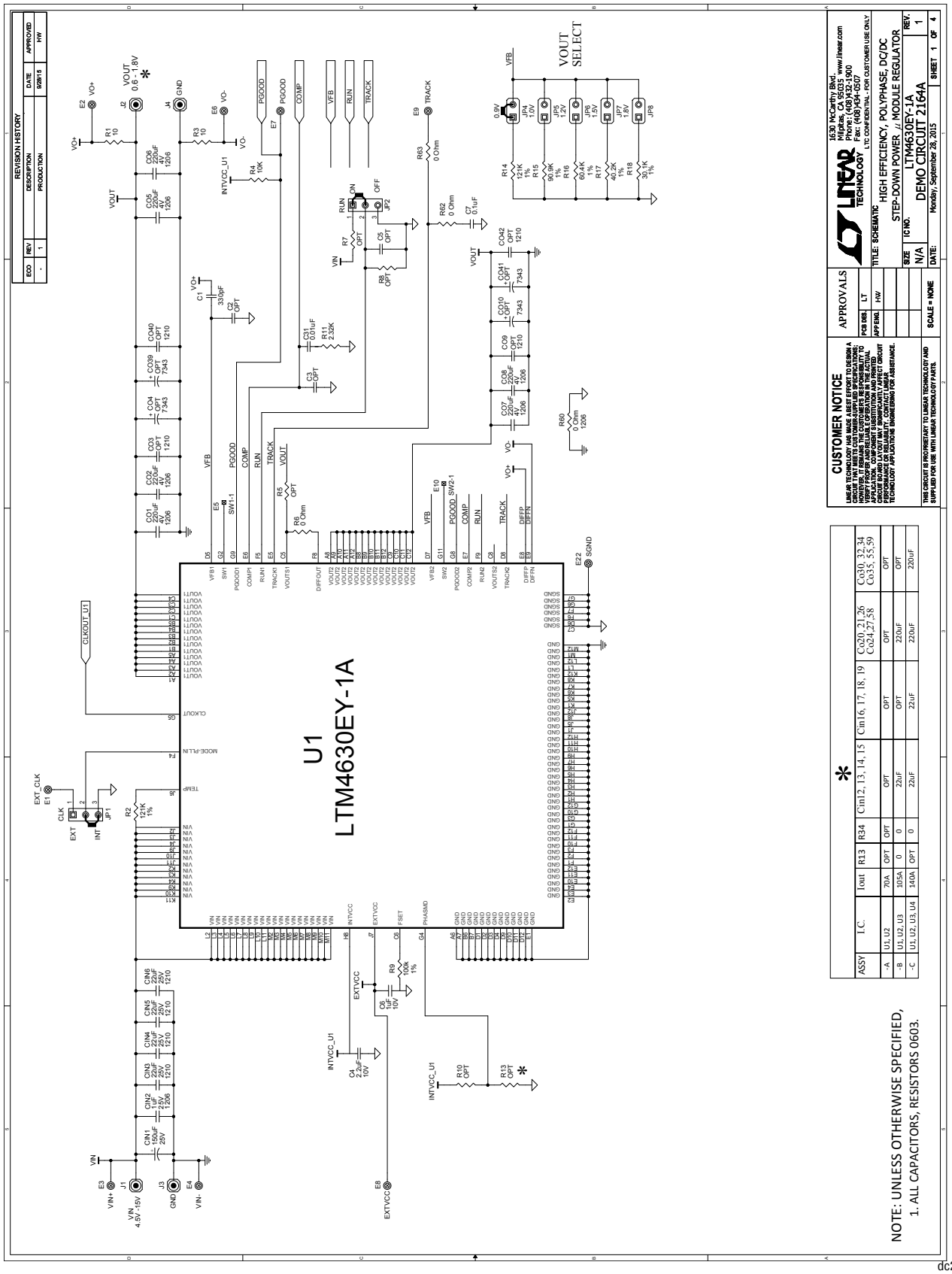
PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Required Circuit Components				
1	1	CIN1	CAP, 150µF 25% 25V ALUM	SUN ELECT., 25CE150AX
2	2	CIN2, CIN11	CAP, 1206 1µF 10% 25V X5R	TAIYO YUDEN, TMK316BJ105KL-T
3	12	CIN3-CIN10, CIN12-CIN15	CAP, 1210 22µF 10% 25V X5R	AVX, 12103D226KAT2A
4	18	CO1, CO2, CO5, CO6, CO7, CO8, CO11, CO13, CO15, CO16, CO56, CO57, CO20, CO21, CO26, CO27, CO24, CO58	CAP, 1206 220µF 20% 4V X5R	MURATA, GRM31CR60G227ME11L
5	1	C1	CAP, 0603 330pF 10% 50V NPO	AVX, 06035A331KAT2A
6	4	C4, C10, C18, C22	CAP, 0603 2.2µF 20% 10V X5R	TAIYO YUDEN, LMK107BJ225MA-T
7	6	C6, C11, C19, C23, C27, C28	CAP, 0603 1µF 10% 10V X7R	TAIYO YUDEN, LMK107BJ105KA-T
8	2	C7, C25	CAP, 0603 0.1µF 10% 25V X7R	AVX, 06033C104KAT2A
9	2	C24, C31	CAP, 0603 0.01µF 10% 100V X7R	AVX, 06031C103KAT2A
10	2	Q1, Q2	MOSFET, N-CH D-S 30V TO252	VISHAY, SUD50N04-8M8P-4GE3
11	4	R1, R3, R25, R29	RES, 0603 10Ω 5% 1/10W	VISHAY, CRCW060310R0JNEA
12	5	R2, R14, R21, R39, R47	RES, 0603 121k 1% 1/10W	VISHAY, CRCW0603121KFKEA
13	4	R4, R36, R41, R54	RES, 0603 10k 5% 1/10W	VISHAY, CRCW060310K0JNEA
14	4	R9, R31, R43, R51	RES, 0603 100k 1% 1/10W	VISHAY, CRCW0603100KFKEA
15	1	R11	RES, 0603 2.32k 1% 1/10W	VISHAY, CRCW06032K32FKEA
16	1	R15	RES, 0603 90.9k 1% 1/10W	VISHAY, CRCW060390K9FKEA
17	1	R16	RES, 0603 60.4k 1% 1/10W	VISHAY, CRCW060360K4FKEA
18	1	R17	RES, 0603 40.2k 1% 1/10W	VISHAY, CRCW060340K2FKEA
19	1	R18	RES, 0603 30.1k 1% 1/10W	VISHAY, CRCW060330K1FKEA
20	2	R56, R57	RES, 2512 0.010Ω 1% 1W	VISHAY, WSL2512R01000FEA
21	3	U1, U2, U3	IC, VOLTAGE REGULATOR, BGA	LINEAR TECH., LTM4630IY-1A#PBF

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Additional Demo Board Circuit Components				
1	0	CIN16-CIN19	DO NOT STUFF	
2	0	CO3, CO9, CO14, CO17, CO18, CO22, CO28, CO30, CO32-CO36, CO38, CO40, CO42, CO45, CO46, CO48, CO50, CO52, CO54, CO55, CO59	CAP, 1210 OPTION	OPTION
3	0	CO4, CO10, CO12, CO19, CO23, CO25, CO29, CO31, CO37, CO39, CO41, CO43, CO44, CO47, CO49, CO51, CO53	CAP, 7343 OPTION	OPTION
4	0	C2, C3, C5, C8, C9, C12-, C17, C20, C21, C26, C29, C30, C32	CAP, 0603 OPTION	OPTION
5	0	R5, R7, R8, R10, R30, R37, R38, R42, R44, R48-R50, R52, R53, R55, R61, R64	RES, 0603 OPTION	OPTION
6	14	R6, R13, R19, R20, R27, R28, R32-R35, R40, R45, R62, R63	RES, 0603 0Ω JUMPER	VISHAY, CRCW06030000Z0EA
7	4	R22, R23, R24, R26	RES, 2010 0Ω JUMPER	VISHAY, CRCW20100000ZEA9
8	0	R58, R59	RES, 2512 OPTION	OPTION
9	1	R60	RES, 1206 0Ω JUMPER	VISHAY, CRCW12060000Z0EA
10	0	U4	DO NOT STUFF	
Hardware: For Demo Board Only				
1	11	E1-E4, E6-E9, E12, E13, E22	TESTPOINT, TURRET, 0.063"	MILL MAX, 2308-2-00-80-00-00-07-0
2	2	E19, E20	TESTPOINT, TURRET, 0.094"	MILL MAX, 2501-2-00-80-00-00-07-0
3	2	JP1, JP2	HEADER, 3 PIN 0.079 SINGLE ROW	SULLINS, NRPN031PAEN-RC
4	5	JP4, JP5, JP6, JP7, JP8	HEADER, 2 PIN 0.079 SINGLE ROW	SAMTEC, TMM-102-02-L-S
5	4	J1, J2, J3, J4	STUD, TEST PIN	PEM, KFH-032-10
6	8	J1, J2, J3, J4 (x2)	NUT, BRASS PL #10-32	ANY, 10-32M/S BR PL
7	4	J1, J2, J3, J4	LUG RING, #10	KEYSTONE, 8205
8	4	J1, J2, J3, J4	WASHER, TIN PLATED BRASS	ANY, #10EXT BZ TN
9	2	J5, J6	JACK, BANANA	KEYSTONE, 575-4
10	2	J7, J8	CON, BNC, 5 PINS	CONNEX, 112404
11	3	XJP1, XJP2, XJP4	SHUNT	SAMTEC, 2SN-BK-G

SCHEMATIC DIAGRAM



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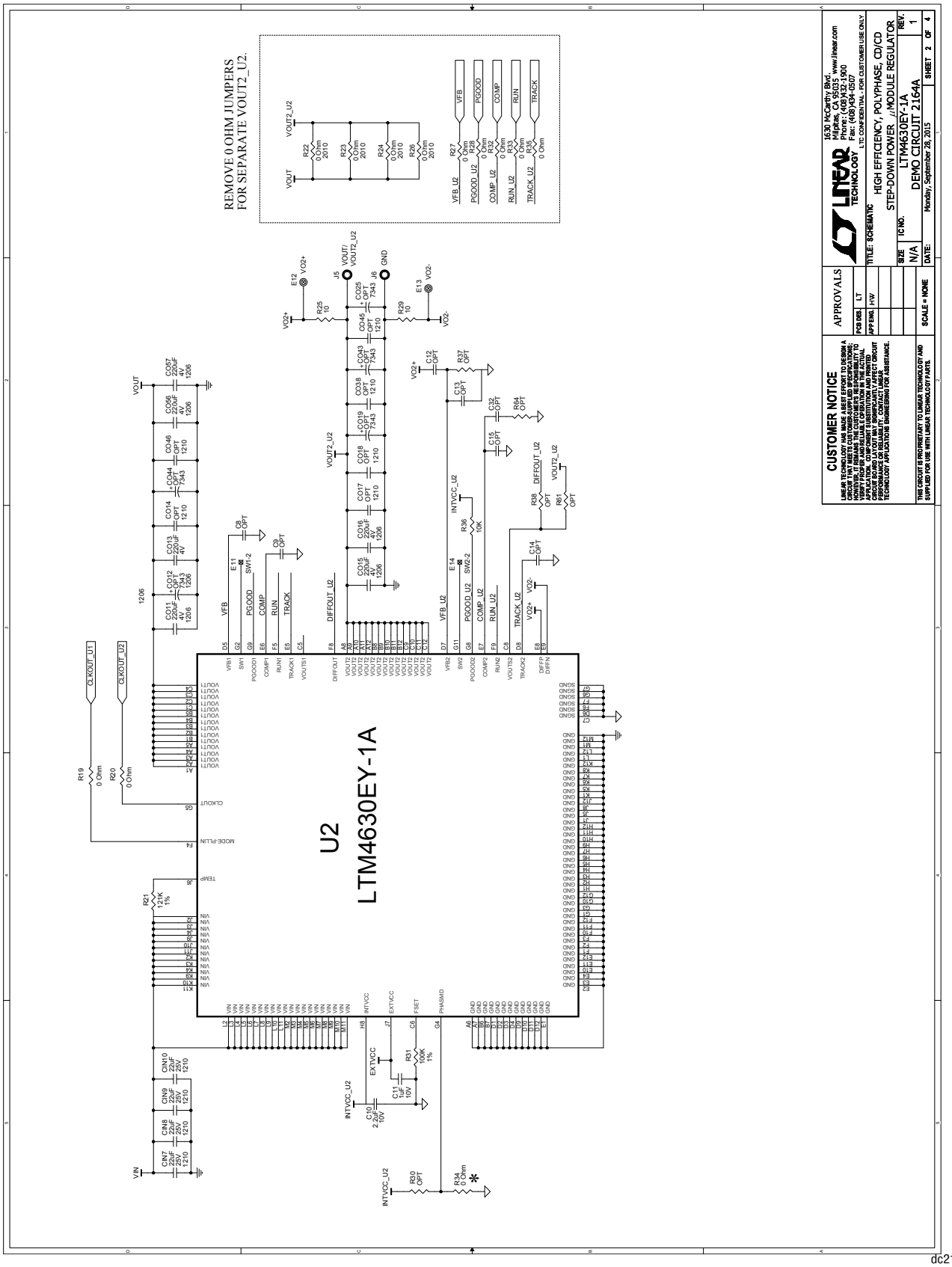

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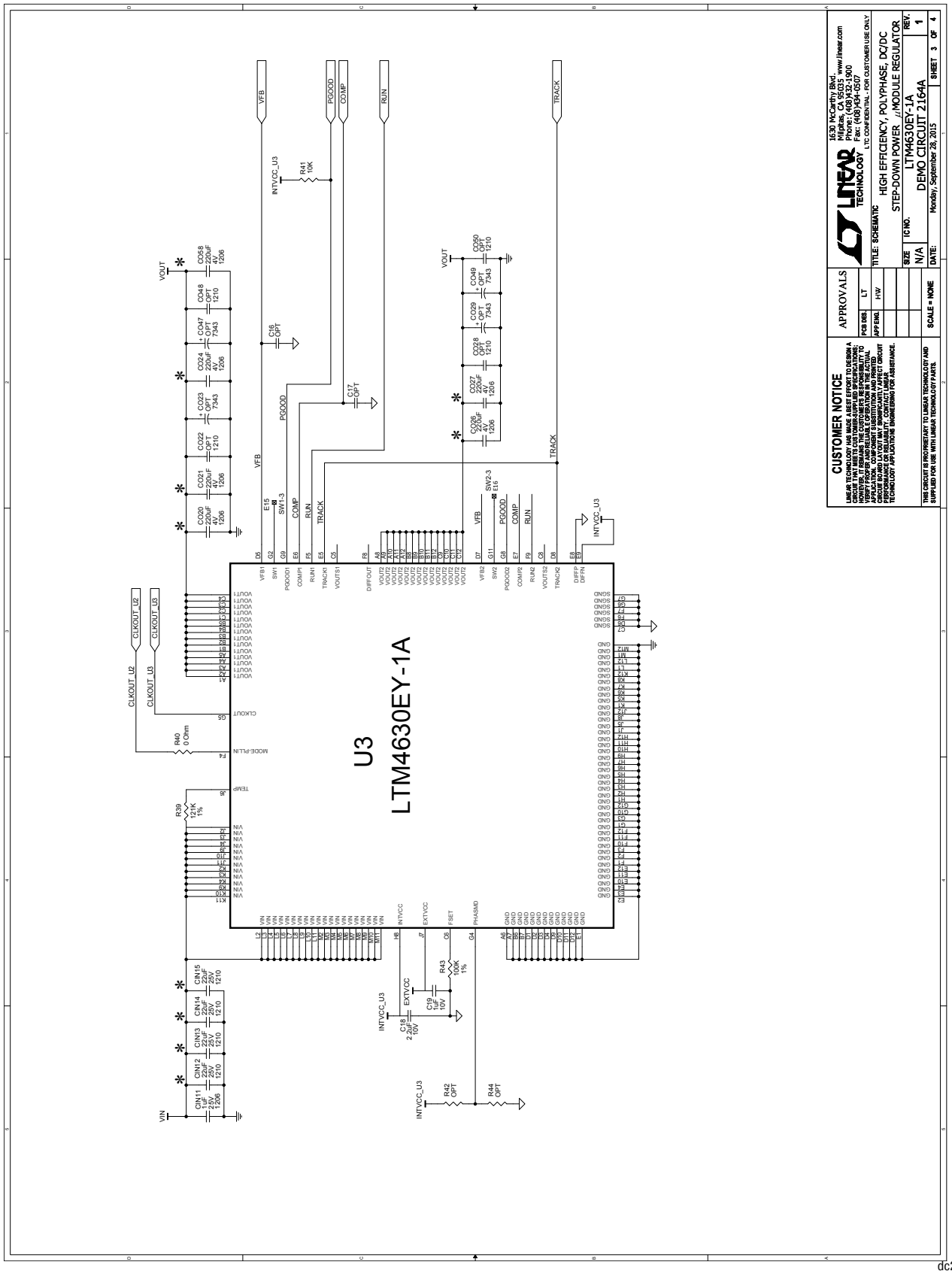

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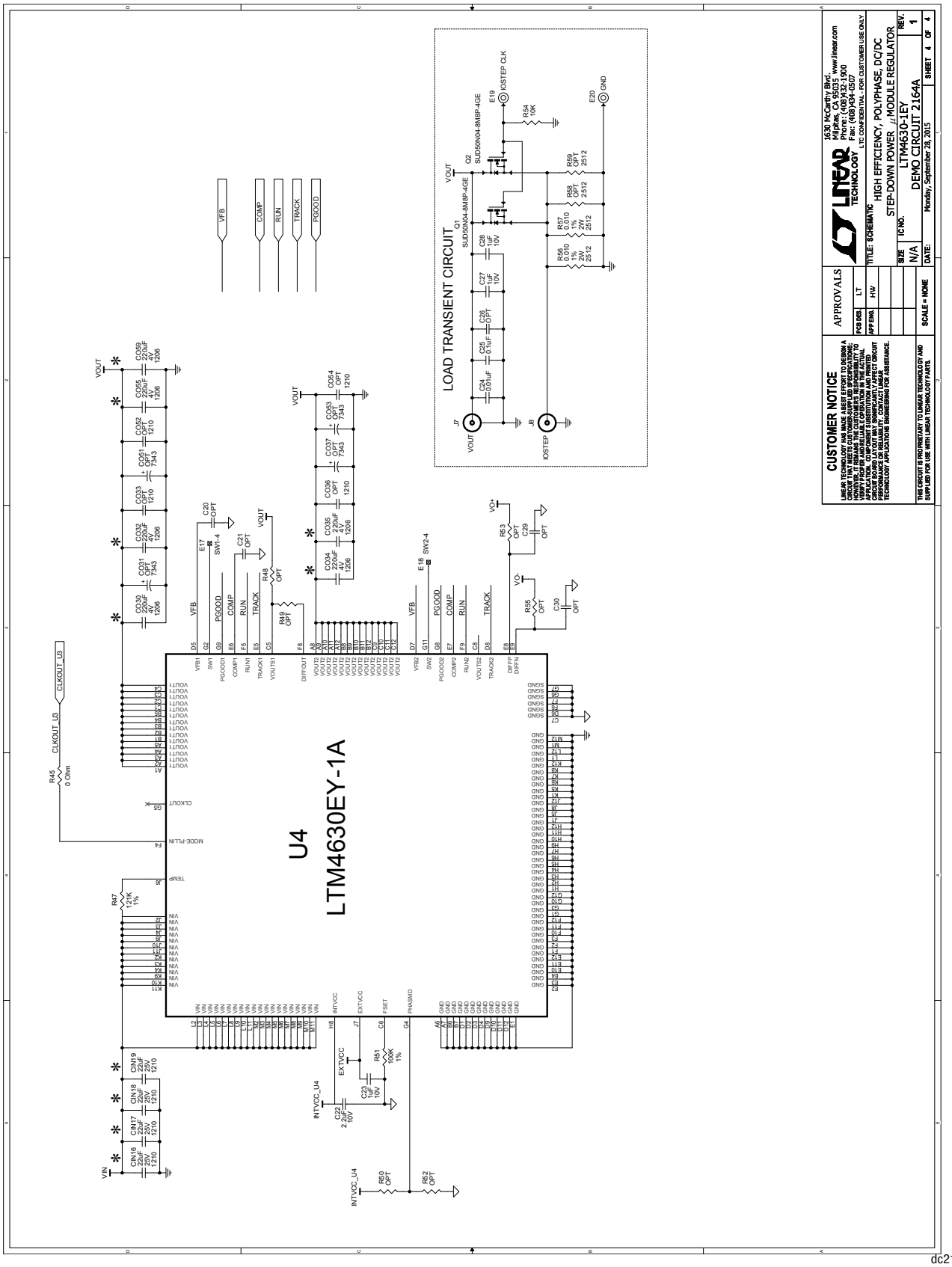

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