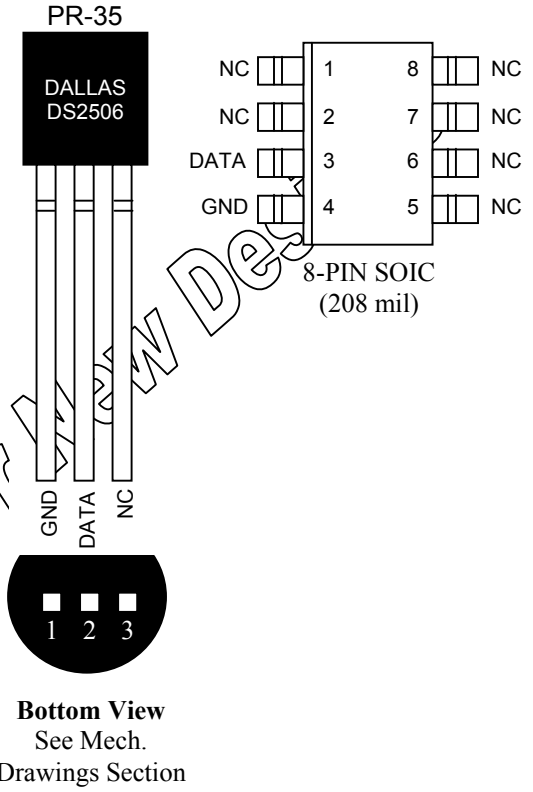
DS2506
64Kb Add-Only Memory

www.maxim-ic.com

FEATURES

- 65536 bits Electrically Programmable Read Only Memory (EPROM) communicates with the economy of one signal plus ground
- Unique, factory-lasered and tested 64-bit registration number (8-bit family code + 48-bit serial number + 8-bit CRC tester) assures absolute traceability because no two parts are alike
- Built-in multidrop controller ensures compatibility with other MicroLAN products
- EPROM partitioned into 256-bit pages for randomly accessing packetized data records
- Each memory page can be permanently write-protected to prevent tampering
- Device is an "add only" memory where additional data can be programmed into EPROM without disturbing existing data
- Architecture allows software to patch data by superseding an old page in favor of a newly programmed page
- Reduces control, address, data, power, and programming signals to a single data pin
- Directly connects to a single port pin of a microprocessor and communicates at up to 16.3 kbits per second
- Overdrive mode boosts communication speed to 142 kbits per second
- 8-bit family code specifies DS2506 communications requirements to reader
- Presence detector acknowledges when the reader first applies voltage
- Low cost PR35 or 8-pin SOIC surface mount package
- Reads over a wide voltage range of 2.8V to 6.0V from -40°C to +85°C; programs at 11.5V to 12.0V from -40°C to +50°C

PIN ASSIGNMENT



Bottom View
See Mech.
Drawings Section

ORDERING INFORMATION

DS2506	PR35 Package
DS2506S	8-Pin SOIC Package

Not Recommended for New Design

SILICON LABEL DESCRIPTION

The DS2506 64Kb Add-Only Memory identifies and stores relevant information about the product to which it is associated. This lot or product specific information can be accessed with minimal interface, for example a single port pin of a microcontroller. The DS2506 consists of a factory-lasered registration number that includes a unique 48-bit serial number, an 8-bit CRC, and an 8-bit Family Code (0FH) plus 64Kb of user-programmable EPROM. The power to program and read the DS2506 is derived entirely from the 1-Wire communication line. Data is transferred serially via the 1-Wire protocol which requires only a single data lead and a ground return. The entire device can be programmed and then write-protected if desired. Alternatively, the part may be programmed multiple times with new data being appended to, but not overwriting, existing data with each subsequent programming of the device. Note: Individual bits can be changed only from a logical 1 to a logical 0, never from a logical 0 to a logical 1. A provision is also included for indicating that a certain page or pages of data are no longer valid and have been replaced with new or updated data that is now residing at an alternate page address. This page address redirection allows software to patch data and enhance the flexibility of the device as a stand-alone database. The 48-bit serial number that is factory-lasered into each DS2506 provides a guaranteed unique identity which allows for absolute traceability. The PR35 and SOIC packages provide a compact enclosure that allows standard assembly equipment to handle the device easily for attachment to printed circuit boards or wiring. Typical applications include storage of calibration constants, maintenance records, asset tracking, product revision status and access codes.

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OVERVIEW

The block diagram in Figure 1 shows the relationships between the major control and memory sections of the DS2506. The DS2506 has three main data components: 1) 64-bit lasered ROM, 2) 65536-bits EPROM Data Memory, and 3) 2816-bits EPROM Status Memory. The device derives its power for read operations entirely from the 1-Wire communication line by storing energy on an internal capacitor during periods of time when the signal line is high and continues to operate off of this “parasite” power source during the low times of the 1-Wire line until it returns high to replenish the parasite (capacitor) supply. During programming, 1-Wire communication occurs at normal voltage levels and then is pulsed momentarily to the programming voltage to cause the selected EPROM bits to be programmed. The 1-Wire line must be able to provide 12 volts and 10 milliamperes to adequately program the EPROM portions of the part. Whenever programming voltages are present on the 1-Wire line a special high voltage detect circuit within the DS2506 generates an internal logic signal to indicate this condition. The hierarchical structure of the 1-Wire protocol is shown in Figure 2. The bus master must first provide one of the six ROM Function Commands, 1) Read ROM, 2) Match ROM, 3) Search ROM, 4) Skip ROM, 5) Overdrive-Skip ROM or 6) Overdrive-Match ROM. Upon completion of an Overdrive ROM command byte executed at regular speed, the device will enter the Overdrive mode where all subsequent communication occurs at a higher speed. These commands operate on the 64-bit lasered ROM portion of each device and can singulate a specific device if many are present on the 1-Wire line as well as indicate to the bus master how many and what types of devices are present. The protocol required for these ROM Function Commands is described in Figure 8. After a ROM Function Command is successfully executed, the memory functions that operate on the EPROM portions of the DS2506 become accessible and the bus master may issue any one of the five Memory Function Commands specific to the DS2506 to read or program the various data fields. The protocol for these Memory Function Commands is described in Figure 5. All data is read and written least significant bit first.

64-BIT LASERED ROM

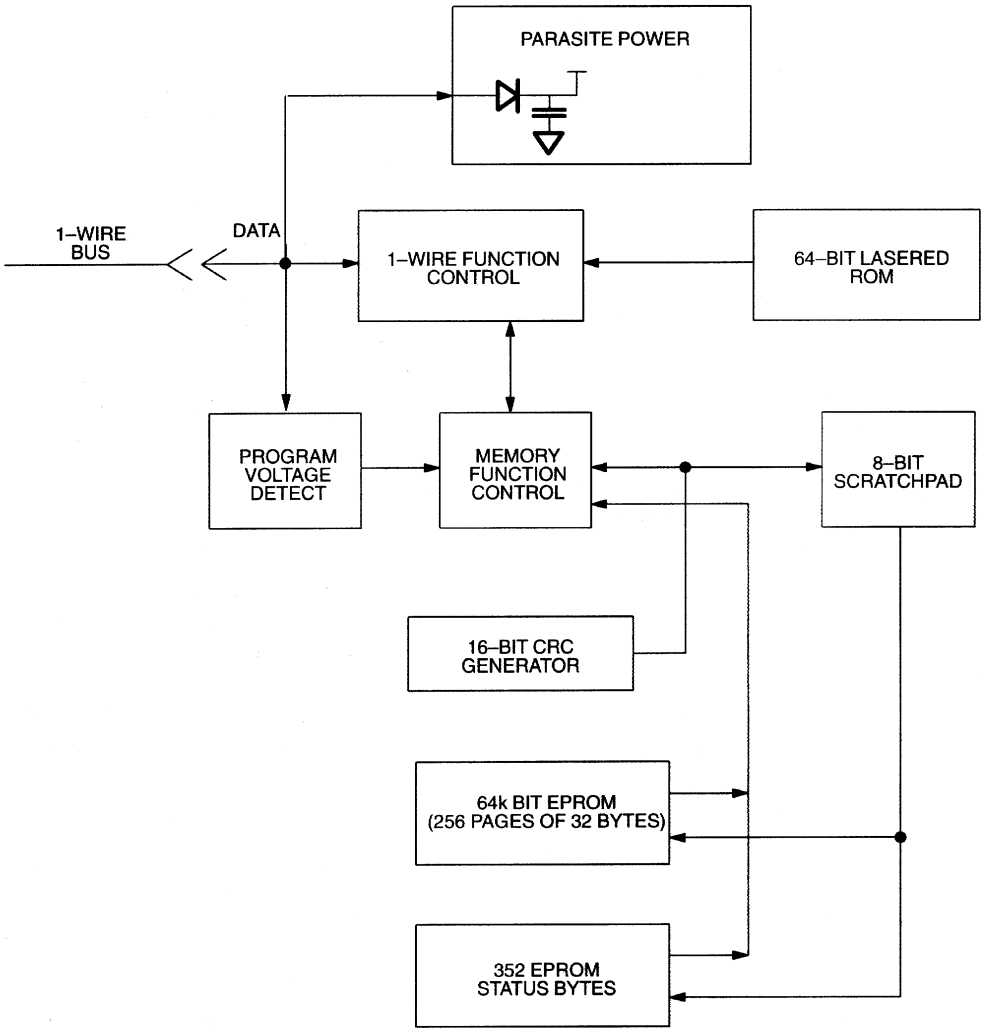
Each DS2506 contains a unique ROM code that is 64 bits long. The first 8 bits are a 1-Wire family code. The next 48 bits are a unique serial number. The last 8 bits are a CRC of the first 56 bits. (See Figure 3). The 64-bit ROM and ROM Function Control section allow the DS2506 to operate as a 1-Wire device and

follow the 1-Wire protocol detailed in the section "1-Wire Bus System." The memory functions required to read and program the EPROM sections of the DS2506 are not accessible until the ROM function protocol has been satisfied. This protocol is described in the ROM functions flow chart (Figure 8). The 1-Wire bus master must first provide one of six ROM function commands: 1) Read ROM, 2) Match ROM, 3) Search ROM, 4) Skip ROM, 5) Overdrive-Skip ROM or 6) Overdrive-Match ROM. After a ROM function sequence has been successfully executed, the bus master may then provide any one of the memory function commands specific to the DS2506 (Figure 5).

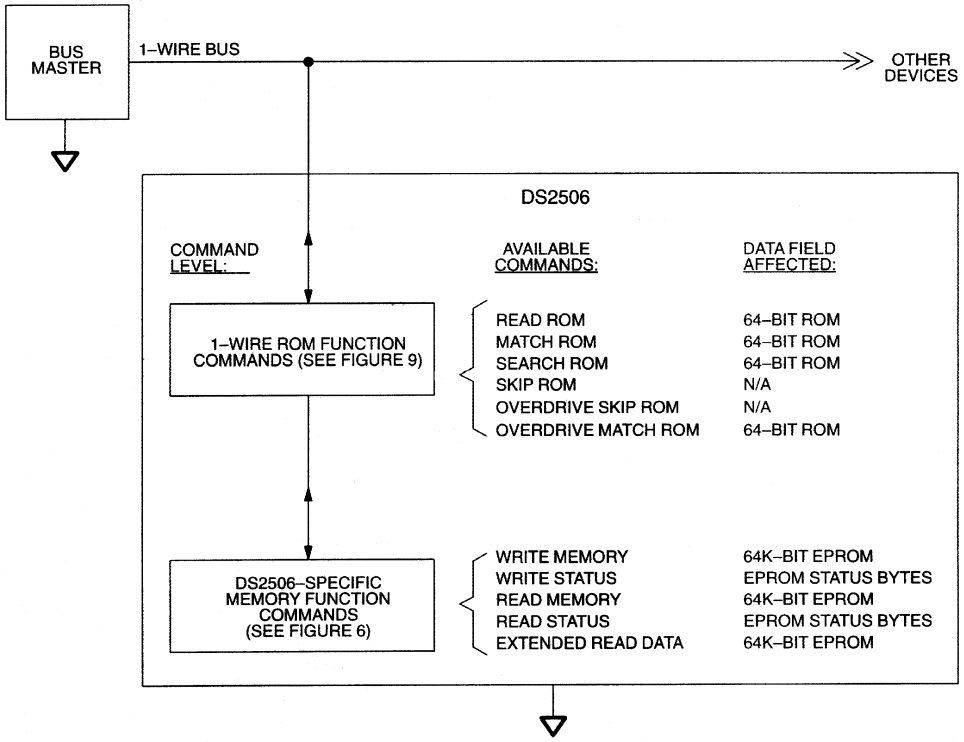
The 1-Wire CRC of the lasered ROM is generated using the polynomial $X^8 + X^5 + X^4 + 1$. Additional information about the Dallas Semiconductor 1-Wire Cyclic Redundancy Check is available in the Book of DS19xx iButton Standards. The shift register acting as the CRC accumulator is initialized to zero. Then starting with the least significant bit of the family code, 1 bit at a time is shifted in. After the 8th bit of the family code has been entered, then the serial number is entered. After the 48th bit of the serial number has been entered, the shift register contains the CRC value. Shifting in the 8 bits of CRC should return the shift register to all zeroes.

Designs

DS2506 BLOCK DIAGRAM Figure 1



HIERARCHICAL STRUCTURE FOR 1-WIRE PROTOCOL Figure 2



64-BIT LASERED ROM Figure 3

8-Bit CRC Code		48-Bit Serial Number		8-Bit Family Code (0FH)	
MSB	LSB	MSB	LSB	MSB	LSB

65536-BITS EPROM

The memory map in Figure 4 shows the 65536-bit EPROM section of the DS2506 which is configured as 256 pages of 32 bytes each. The 8-bit scratchpad is an additional register that acts as a buffer when programming the memory. Data is first written to the scratchpad and then verified by reading an 16-bit CRC from the DS2506 that confirms proper receipt of the data and address. If the buffer contents are correct, a programming voltage should be applied and the byte of data will be written into the selected address in memory. This process insures data integrity when programming the memory. The details for reading and programming the 65536-bit EPROM portion of the DS2506 are given in the Memory Function Commands section.

EPROM STATUS BYTES

In addition to the 65536 bits of data memory the DS2506 provides 2816 bits of Status Memory accessible with separate commands.

The EPROM Status Bytes can be read or programmed to indicate various conditions to the software interrogating the DS2506. The first 32 bytes of the EPROM Status Memory (addresses 000 to 01FH) contain the Write Protect Page bits which inhibit programming of the corresponding page in the 65536-bit main memory area if the appropriate write protection bit is programmed. Once a bit has been programmed in the Write Protect Page section of the Status Memory, the entire 32 byte page that corresponds to that bit can no longer be altered but may still be read.

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The next 32 bytes of the EPROM Status Memory (addresses 020 to 03FH) contain the Write Protect bits which inhibit altering the Page Address Redirection Byte corresponding to each page in the 65536-bit main memory area.

The following 32 bytes within the EPROM Status Memory (addresses 040 to 05FH) are reserved for use by the iButton operating software TMEX. Their purpose is to indicate which memory pages are already in use. Originally, all of these bits are unprogrammed, indicating that the device does not store any data. As soon as data is written to any page of the device under control of TMEX, the bit inside this bitmap corresponding to that page will be programmed to 0, marking this page as used. These bits are application flags only and have no impact on the internal logic of the DS2506.

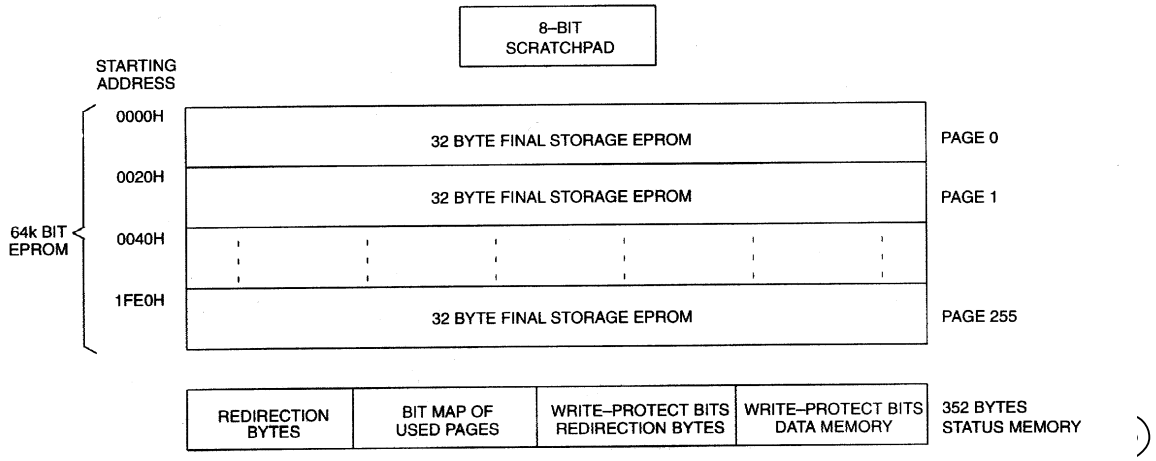
The next 256 bytes of the EPROM Status Memory (addresses 100H to 1FFH) contain the Page Address Redirection Bytes which indicate if one or more of the pages of data in the 65536-bit EPROM section have been invalidated by software and redirected to the page address contained in the appropriate redirection byte. The hardware of the DS2506 makes no decisions based on the contents of the Page Address Redirection Bytes. Since with EPROM technology bits can only be changed from a logical 1 to a logical 0 by programming, it is not possible to simply rewrite a page if the data requires changing or updating. But with space permitting, an entire page of data can be redirected to another page within the DS2506. Under TMEX a page is redirected by writing the one's complement of the new page address into the Page Address Redirection Byte that corresponds to the original (replaced) page. This architecture allows the user's software to make a "data patch" to the EPROM by indicating that a particular page or pages should be replaced with those indicated in the Page Address Redirection Bytes. To leave an authentic audit trail of data patches, it is recommended to also program the write protect bit of the Page Address Redirection Byte, after the page redirection is programmed. Without this protection, it is still possible to modify the Page Address Redirection Byte, making it point to a different memory page than the true one.

If a Page Address Redirection Byte has a FFH value, the data in the main memory that corresponds to that page is valid. If a Page Address Redirection Byte has some other hex value than FFH, the data in the page corresponding to that redirection byte is invalid. According to the TMEX definitions the valid data can now be found at the one's complement of the page address indicated by the hex value stored in the associated Page Address Redirection Byte. A value of FDH in the redirection byte for page 1, for example, would indicate that the updated data is now in page 2. The status memory is programmed similarly to the data memory. Details for reading and programming the EPROM status memory portion of the DS2506 are given in the Memory Function Commands section.

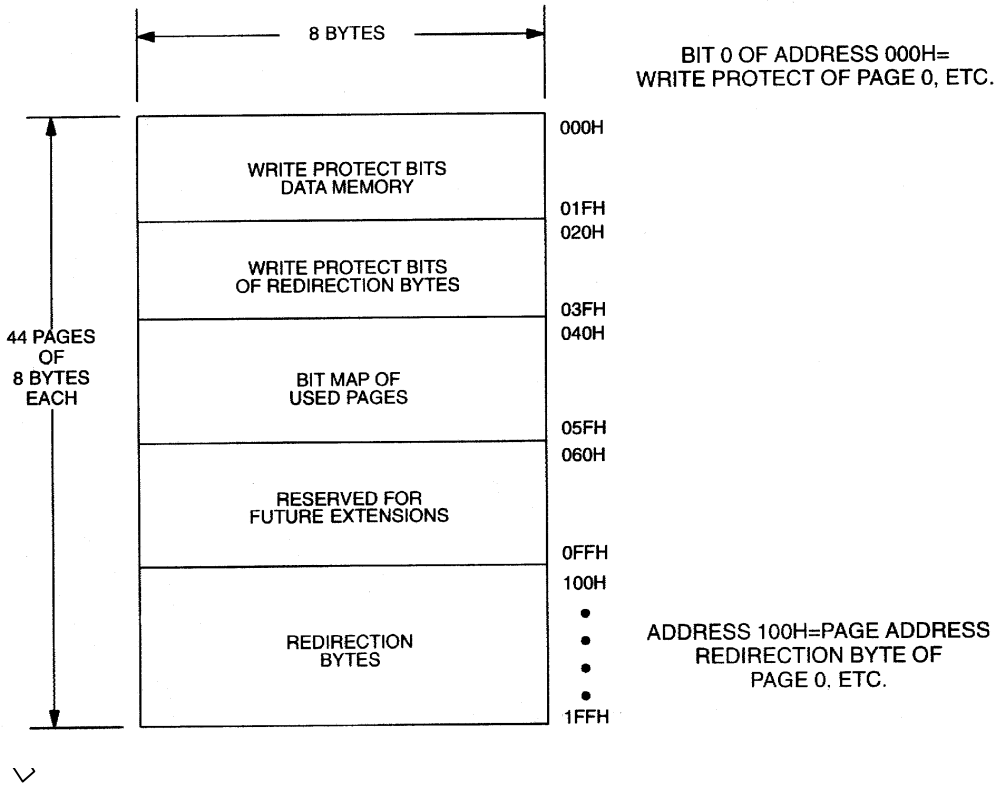
The Status Memory address range of the DS2506 extends from 000 to 1FFH. The memory locations 60H to 0FFH and 200H and higher are physically not implemented. Reading these locations will usually result in FFH bytes. Attempts to write to these locations will be ignored.

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DS2506 MEMORY MAP Figure 4



STATUS MEMORY MAP



MEMORY FUNCTION COMMANDS

The "Memory Function Flow Chart" (Figure 5) describes the protocols necessary for accessing the various data fields within the DS2506. The Memory Function Control section, 8-bit scratchpad, and the Program Voltage Detect circuit combine to interpret the commands issued by the bus master and create the correct control signals within the device. A three byte protocol is issued by the bus master. It is comprised of a command byte to determine the type of operation and two address bytes to determine the specific starting byte location within a data field. The command byte indicates if the device is to be read or written. Writing data involves not only issuing the correct command sequence but also providing a 12-volt programming voltage at the appropriate times. To execute a write sequence, a byte of data is first loaded into the scratchpad and then programmed into the selected address. Write sequences always occur a byte at a time. To execute a read sequence, the starting address is issued by the bus master and data is read from the part beginning at that initial location and continuing to the end of the selected data field or until a reset sequence is issued. All bits transferred to the DS2506 and received back by the bus master are sent least significant bit first.

READ MEMORY [F0H]

The Read Memory command is used to read data from the 65536 bits EPROM data field. The bus master follows the command byte with a two byte address (TA1=(T7:T0), TA2=(T15:T8)) that indicates a starting byte location within the data field. With every subsequent read data time slot the bus master receives data from the DS2506 starting at the initial address and continuing until the end of the 65536 bits data field is reached or until a Reset Pulse is issued. If reading occurs through the end of memory space, the bus master may issue sixteen additional read time slots and the DS2506 will respond with a 16-bit CRC of the command, address bytes and all data bytes read from the initial starting byte through the last byte of memory. This CRC is the result of clearing the CRC generator and then shifting in the command byte followed by the two address bytes and the data bytes beginning at the first addressed memory location and continuing through to the last byte of the EPROM data memory. After the CRC is received by the bus master, any subsequent read time slots will appear as logical 1s until a Reset Pulse is issued. Any reads ended by a Reset Pulse prior to reaching the end of memory will not have the 16-bit CRC available.

Typically a 16-bit CRC would be stored with each page of data to insure rapid, error-free data transfers that eliminate having to read a page multiple times to determine if the received data is correct or not. (See Book of DS19xx iButton Standards, Chapter 7 for the recommended file structure to be used with the 1-Wire environment). If CRC values are imbedded within the data, a Reset Pulse may be issued at the end of memory space during a Read Memory command.

READ STATUS [AAH]

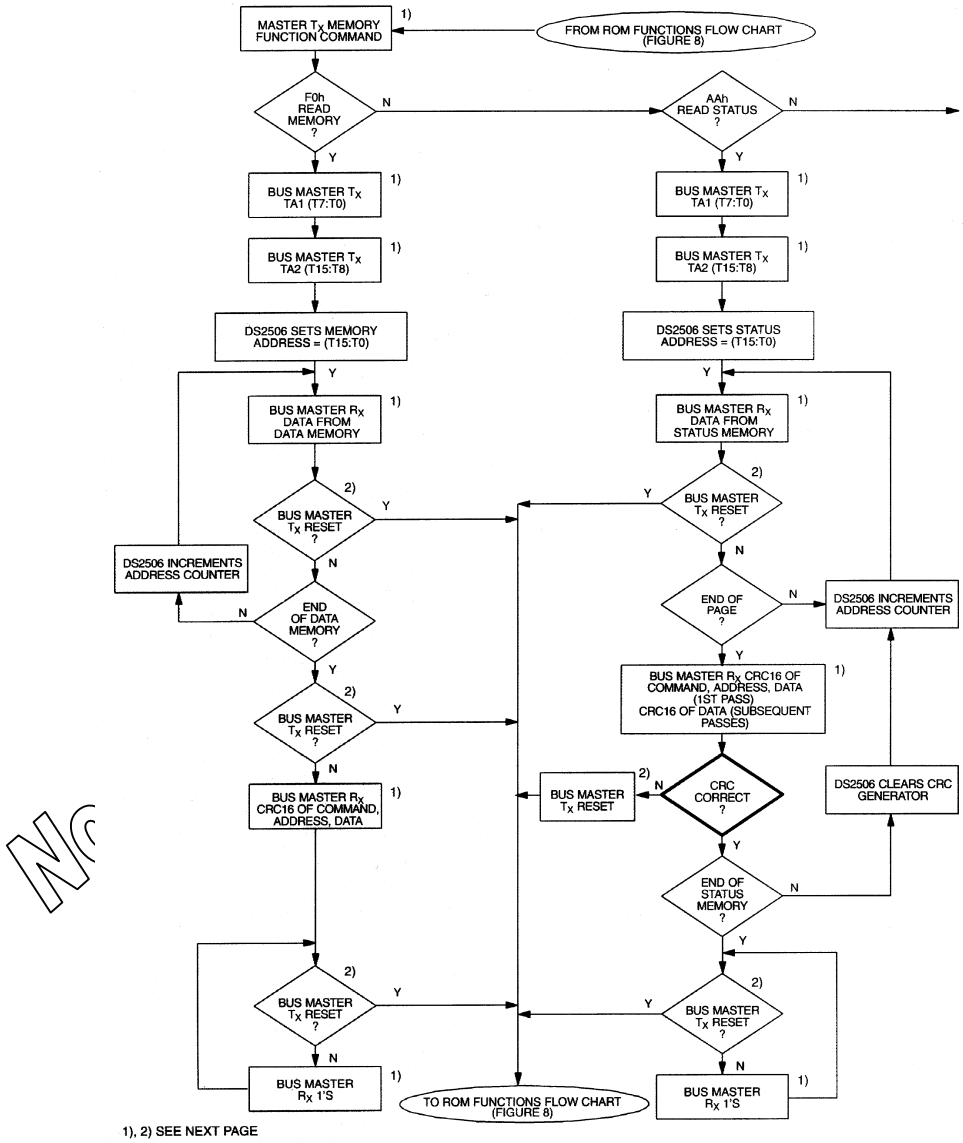
The Read Status command is used to read data from the EPROM Status data field. The bus master follows the command byte with a two byte address (TA1=(T7:T0), TA2=(T15:T8)) that indicates a starting byte location within the data field. With every subsequent read data time slot the bus master receives data from the DS2506 starting at the supplied address and continuing until the end of an eight byte page of the EPROM Status data field is reached. At that point the bus master will receive a 16-bit CRC of the command byte, address bytes and status data bytes. This CRC is computed by the DS2506 and read back by the bus master to check if the command word, starting address and data were received correctly. If the CRC read by the bus master is incorrect, a Reset Pulse must be issued and the entire sequence must be repeated.

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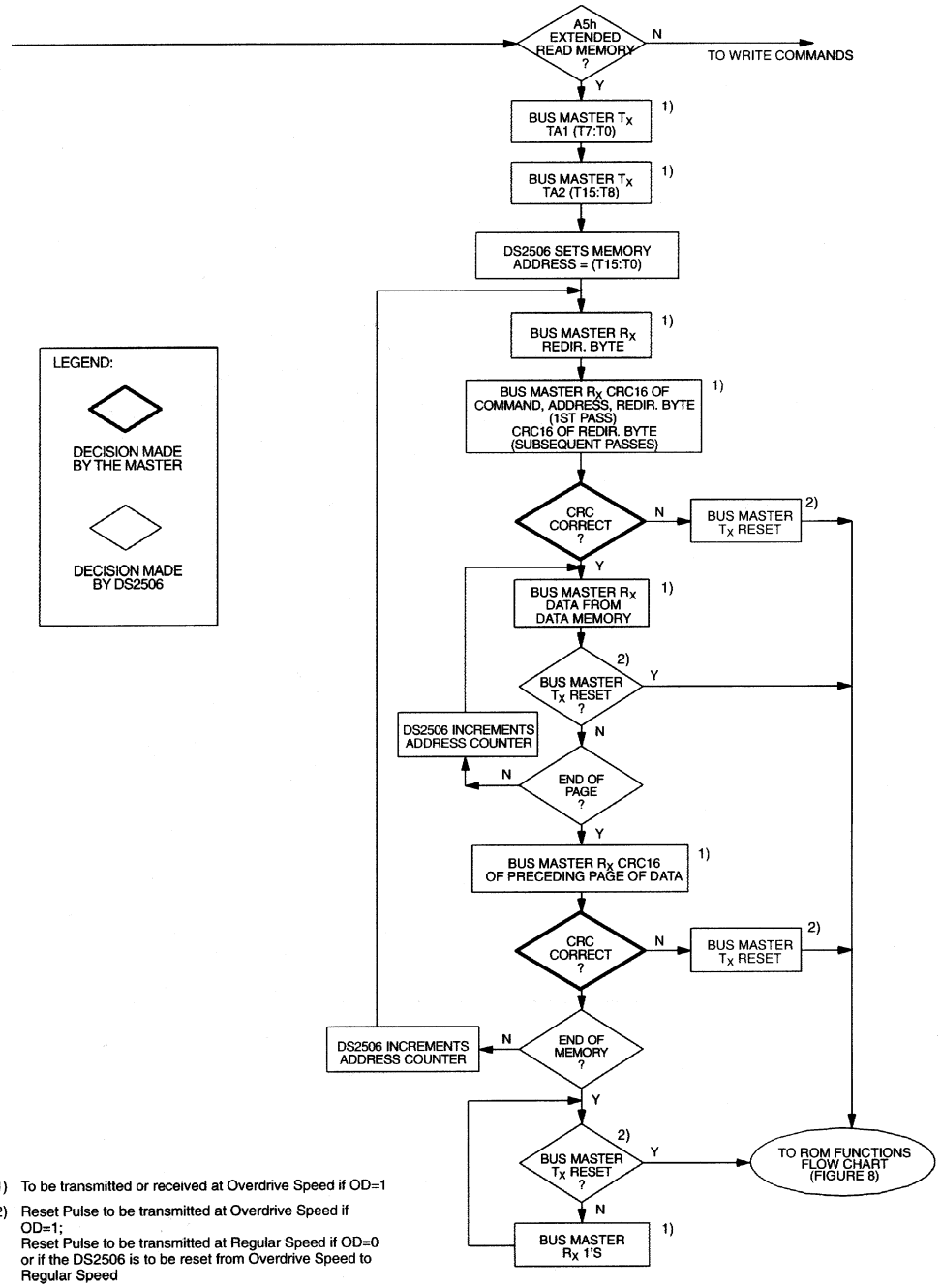
Note that the initial pass through the Read Status flow chart will generate a 16-bit CRC value that is the result of clearing the CRC generator and then shifting in the command byte followed by the two address bytes, and finally the data bytes beginning at the first addressed memory location and continuing through to the last byte of the addressed EPROM Status data page. The last byte of a Status data page always has an ending address of xx7 or xxFH. Subsequent passes through the Read Status flow chart will generate a 16-bit CRC that is the result of clearing the CRC generator and then shifting in the new data bytes starting at the first byte of the next page of the EPROM Status data field.

This feature is provided since the EPROM Status information may change over time making it impossible to program the data once and include an accompanying CRC that will always be valid. Therefore, the Read Status command supplies a 16-bit CRC that is based on and always is consistent with the current data stored in the EPROM Status data field.

MEMORY FUNCTION FLOW CHART Figure 5



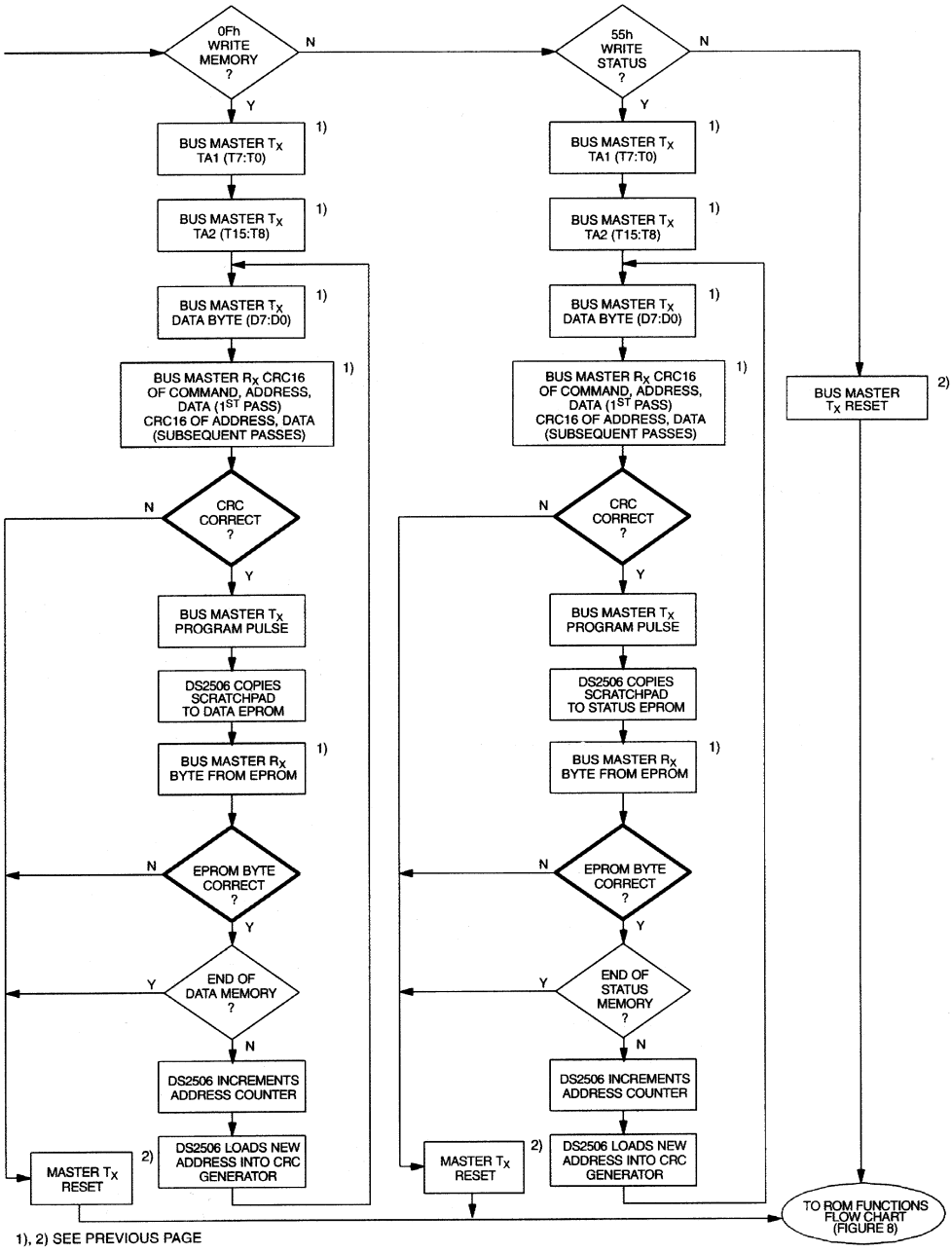
MEMORY FUNCTION FLOW CHART Figure 5 (cont'd)



1) To be transmitted or received at Overdrive Speed if OD=1

2) Reset Pulse to be transmitted at Overdrive Speed if OD=1;
Reset Pulse to be transmitted at Regular Speed if OD=0 or if the DS2506 is to be reset from Overdrive Speed to Regular Speed

MEMORY FUNCTION FLOW CHART Figure 5 (cont'd)



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After the 16-bit CRC of the last EPROM Status data page is read, the bus master will receive logical 1s from the DS2506 until a Reset Pulse is issued. The Read Status command sequence can be ended at any point by issuing a Reset Pulse.

EXTENDED READ MEMORY [A5H]

The Extended Read Memory command supports page redirection when reading data from the 65536-bit EPROM data field. One major difference between the Extended Read Memory and the basic Read Memory command is that the bus master receives the Redirection Byte first before investing time in reading data from the addressed memory location. This allows the bus master to quickly decide whether to continue and access the data at the selected starting page or to terminate and restart the reading process at the redirected page address. A non-redirected page is identified by a Redirection Byte with a value of FFH (see description of EPROM Status Bytes). If the Redirection Byte is different than this, the master has to complement it to obtain the new page number. Multiplying the page number by 32 (20H) results in the new address the master has to send to the DS2506 to read the updated data replacing the old data. There is no logical limitation in the number of redirections of any page. The only limit is the number of available memory pages within the DS2506.

In addition to page redirection, the Extended Read Memory command also supports "bit-oriented" applications where the user cannot store a 16-bit CRC with the data itself. With bit-oriented applications the EPROM information may change over time within a page boundary making it impossible to include an accompanying CRC that will always be valid. Therefore, the Extended Read Memory command concludes each page with the DS2506 generating and supplying a 16-bit CRC that is based on and therefore always consistent with the current data stored in each page of the 65536-bit EPROM data field.

After having sent the command code of the Extended Read Memory command, the bus master follows the command byte with a two byte address (TA1=(T7:T0), TA2=(T15:T8)) that indicates a starting byte location within the data field. By sending eight read data time slots, the master receives the Redirection Byte associated with the page given by the starting address. With the next sixteen read data time slots, the bus master receives a 16-bit CRC of the command byte, address bytes and the Redirection Byte. This CRC is computed by the DS2506 and read back by the bus master to check if the command word, starting address and Redirection Byte were received correctly.

If the CRC read by the bus master is incorrect, a Reset Pulse must be issued and the entire sequence must be repeated. If the CRC received by the bus master is correct, the bus master issues read time slots and receives data from the DS2506 starting at the initial address and continuing until the end of a 32 byte page is reached. At that point the bus master will send sixteen additional read time slots and receive a 16-bit CRC that is the result of shifting into the CRC generator all of the data bytes from the initial starting byte to the last byte of the current page.

With the next 24 read data time slots the master will receive the Redirection Byte of the next page followed by a 16-bit CRC of the Redirection Byte. After this, data is again read from the 65536-bit EPROM data field starting at the beginning of the new page. This sequence will continue until the final page and its accompanying CRC are read by the bus master. The Extended Read Memory command provides a 16-bit CRC at two locations within the transaction flow chart: 1) after the Redirection Byte and 2) at the end of each memory page. The CRC at the end of the memory page is always the result of clearing the CRC generator and shifting in the data bytes beginning at the first addressed memory location of the EPROM data page until the last byte of this page. With the initial pass through the Extended Read Memory flow chart the 16-bit CRC value is the result of shifting the command byte into the cleared CRC generator, followed by the two address bytes and the Redirection Byte. Subsequent

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passes through the Extended Read Memory flow chart will generate a 16-bit CRC that is the result of clearing the CRC generator and then shifting in the Redirection Byte only.

After the 16-bit CRC of the last page is read, the bus master will receive logical 1s from the DS2506 until a Reset Pulse is issued. The Extended Read Memory command sequence can be exited at any point by issuing a Reset Pulse.

WRITING EPROM MEMORY

The DS2506 has two independent EPROM memory fields, Data Memory and Status Memory. The function flow for writing either field is almost identical. After the appropriate write command has been issued, the bus master will send a two byte starting address (TA1=(T7:T0), TA2=(T15:T8)) and a byte of data (D7:D0). A 16-bit CRC of the command byte, address bytes, and data byte is computed by the DS2506 and read back by the bus master to confirm that the correct command word, starting address, and data byte were received.

If the CRC read by the bus master is incorrect, a Reset Pulse must be issued and the entire sequence must be repeated. If the CRC received by the bus master is correct, a programming pulse (12 volts on the 1-Wire bus for 480 µs) is issued by the bus master. Prior to programming, the entire EPROM memory field will appear as logical 1s. For each bit in the data byte provided by the bus master that is set to a logical 0, the corresponding bit in the selected byte of the EPROM memory is programmed to a logical 0 after the programming pulse has been applied.

After the 480 µs programming pulse is applied and the data line returns to the idle level (5 volts), the bus master issues eight read time slots to verify that the appropriate bits have been programmed. The DS2506 responds with the data from the selected EPROM address sent least significant bit first. This byte contains the bit-wise logical AND of all data ever written to this address. If the EPROM byte contains 1s in bit positions where the byte issued by the master contained 0s, a Reset Pulse should be issued and the current byte address should be programmed again. If the DS2506 EPROM byte contains 0s in the same bit positions as the data byte, the programming was successful and the DS2506 will automatically increment its address counter to select the next byte in the EPROM memory field. The new two byte address will also be loaded into the 16-bit CRC generator as a starting value. The bus master will issue the next byte of data using eight write time slots.

As the DS2506 receives this byte of data into the scratchpad, it also shifts the data into the CRC generator that has been preloaded with the current address and the result is a 16-bit CRC of the new data byte and the new address. After supplying the data byte, the bus master will read this 16-bit CRC from the DS2506 with sixteen read time slots to confirm that the address incremented properly and the data byte was received correctly. If the CRC is incorrect, a Reset Pulse must be issued and the write sequence must be restarted. If the CRC is correct, the bus master will issue a programming pulse and the selected byte in memory will be programmed.

Note that the initial pass through the write flow chart will generate an 16-bit CRC value that is the result of shifting the command byte into the CRC generator, followed by the two address bytes, and finally the data byte. Subsequent passes through the write flow chart due to the DS2506 automatically incrementing its address counter will generate a 16-bit CRC that is the result of loading (not shifting) the new (incremented) address into the CRC generator and then shifting in the new data byte.

For both of these cases, the decision to continue (to apply a program pulse to the DS2506) is made entirely by the bus master, since the DS2506 will not be able to determine if the 16-bit CRC calculated by the bus master agrees with the 16-bit CRC calculated by the DS2506. If an incorrect CRC is ignored and

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a program pulse is applied by the bus master, incorrect programming could occur within the DS2506. Also note that the DS2506 will always increment its internal address counter after the receipt of the eight read time slots used to confirm the programming of the selected EPROM byte. The decision to continue is again made entirely by the bus master. Therefore if the EPROM data byte does not match the supplied data byte but the master continues with the write command, incorrect programming could occur within the DS2506. The write command sequence can be ended at any point by issuing a Reset Pulse.

WRITE MEMORY [0FH]/SPEED WRITE MEMORY [F3H]

The Write Memory command is used to program the 65536-bit EPROM data field. The details of the functional flow chart are described in the section "WRITING EPROM MEMORY."

The data memory address range is 0000H to 1FFFH. If the bus master sends a starting address higher than this, the three most significant address bits are set to zeros by the internal circuitry of the chip. This will result in a mismatch between the CRC calculated by the DS2506 and the CRC calculated by the bus master, indicating an error condition.

To save time when writing more than one consecutive byte of the DS2506's data memory it is possible to omit reading the 16-bit CRC which allows verification of data and address before the data is copied to the EPROM memory. At regular speed this saves 16 time slots or 976 µs for every byte to be programmed. This speed-programming mode is accessed with the command code F3H instead of 0FH. It follows basically the same flow chart as the Write Memory command, but skips sending the CRC immediately preceding the program pulse. This command should only be used if the electrical contact between bus master and the DS2506 is firm since a poor contact may result in corrupted data inside the EPROM memory.

WRITE STATUS [55H]/SPEED WRITE STATUS [F5H]

The Write Status command is used to program the 2816-bit EPROM Status Memory field. The details of the functional flow chart are described in the section "WRITING EPROM MEMORY."

The Status Memory address range is 0000H to 01FFH. Attempts to write to the not implemented status memory locations will be ignored. If the bus master sends a starting address higher than 1FFFH, the three most significant address bits are set to zeros by the internal circuitry of the chip. This will result in a mismatch between the CRC calculated by the DS2506 and the CRC calculated by the bus master, indicating an error condition. To save time when writing more than one consecutive byte of the DS2506's status memory it is possible to omit reading the 16-bit CRC which allows verification of data and address before the data is copied to the EPROM memory. At regular speed this saves 16 time slots or 976 µs for every byte to be programmed. This speed-programming mode is accessed with the command code F5H instead of 55H. It follows basically the same flow chart as the Write Status command, but skips sending the CRC immediately preceding the program pulse. This command should only be used if the electrical contact between bus master and the DS2506 is firm since a poor contact may result in corrupted data inside the EPROM status memory.

Not Recommended for New Designs

1-WIRE BUS SYSTEM

The 1-Wire bus is a system which has a single bus master and one or more slaves. In all instances, the DS2506 is a slave device. The bus master is typically a microcontroller. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1-Wire signalling (signal type and timing). A 1-Wire protocol defines bus transactions in terms of the bus state during specified time slots that are initiated on the falling edge of sync pulses from the bus master. For a more detailed protocol description, refer to Chapter 4 of the Book of DS19xx iButton Standards.

Hardware Configuration

The 1-Wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1-Wire bus must have an open drain connection or 3-state outputs. The DS2506 is an open drain part with an internal circuit equivalent to that shown in Figure 6. The bus master can be the same equivalent circuit. If a bi-directional pin is not available, separate output and input pins can be tied together.

The bus master requires a pullup resistor at the master end of the bus, with the bus master circuit equivalent to the one shown in Figures 7a and 7b. The value of the pullup resistor should be approximately 5 kΩ for short line lengths.

A multidrop bus consists of a 1-Wire bus with multiple slaves attached. At regular speed the 1-Wire bus has a maximum data rate of 16.3 kbits per second. The speed can be boosted to 142 kbits per second by activating the Overdrive mode. If the bus master is also required to perform programming of the EPROM portions of the DS2506, a programming supply capable of delivering up to 10 milliamps at 12 volts for 480 µs is required. The idle state for the 1-Wire bus is high. If, for any reason, a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 16 µs (overdrive speed) or more than 120 µs (regular speed), one or more of the devices on the bus may be reset.

Not Recommended for New Designs

Transaction Sequence

The sequence for accessing the DS2506 via the 1-Wire port is as follows:

- Initialization
- ROM Function Command
- Memory Function Command
- Read/Write Memory/Status

INITIALIZATION

All transactions on the 1-Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by a presence pulse(s) transmitted by the slave(s).

The presence pulse lets the bus master know that the DS2506 is on the bus and is ready to operate. For more details, see the "1-Wire Signalling" section.

ROM FUNCTION COMMANDS

Once the bus master has detected a presence, it can issue one of the six ROM function commands. All ROM function commands are 8 bits long. A list of these commands follows (refer to flowchart in Figure 8):

Read ROM [33H]

This command allows the bus master to read the DS2506's 8-bit family code, unique 48-bit serial number, and 8-bit CRC. This command can be used only if there is a single DS2506 on the bus. If more than one slave is present on the bus, a data collision will occur when all slaves try to transmit at the same time (open drain will produce a wired-AND result). The resultant family code and 48-bit serial number will usually result in a mismatch of the CRC.

Match ROM [55H]

The match ROM command, followed by a 64-bit ROM sequence, allows the bus master to address a specific DS2506 on a multidrop bus. Only the DS2506 that exactly matches the 64-bit ROM sequence will respond to the subsequent memory function command. All slaves that do not match the 64-bit ROM sequence will wait for a reset pulse. This command can be used with a single or multiple devices on the bus.

Skip ROM [CCH]

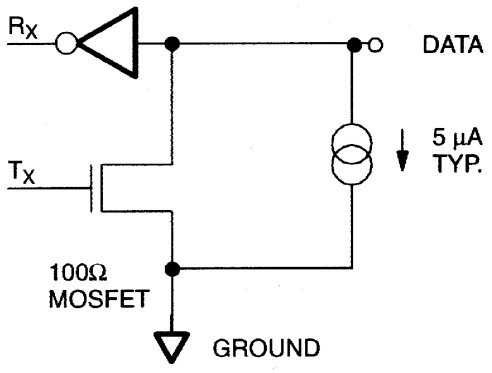
This command can save time in a single drop bus system by allowing the bus master to access the memory functions without providing the 64-bit ROM code. If more than one slave is present on the bus and a read command is issued following the Skip ROM command, data collision will occur on the bus as multiple slaves transmit simultaneously (open drain pulldowns will produce a wired-AND result).

Search ROM [F0H]

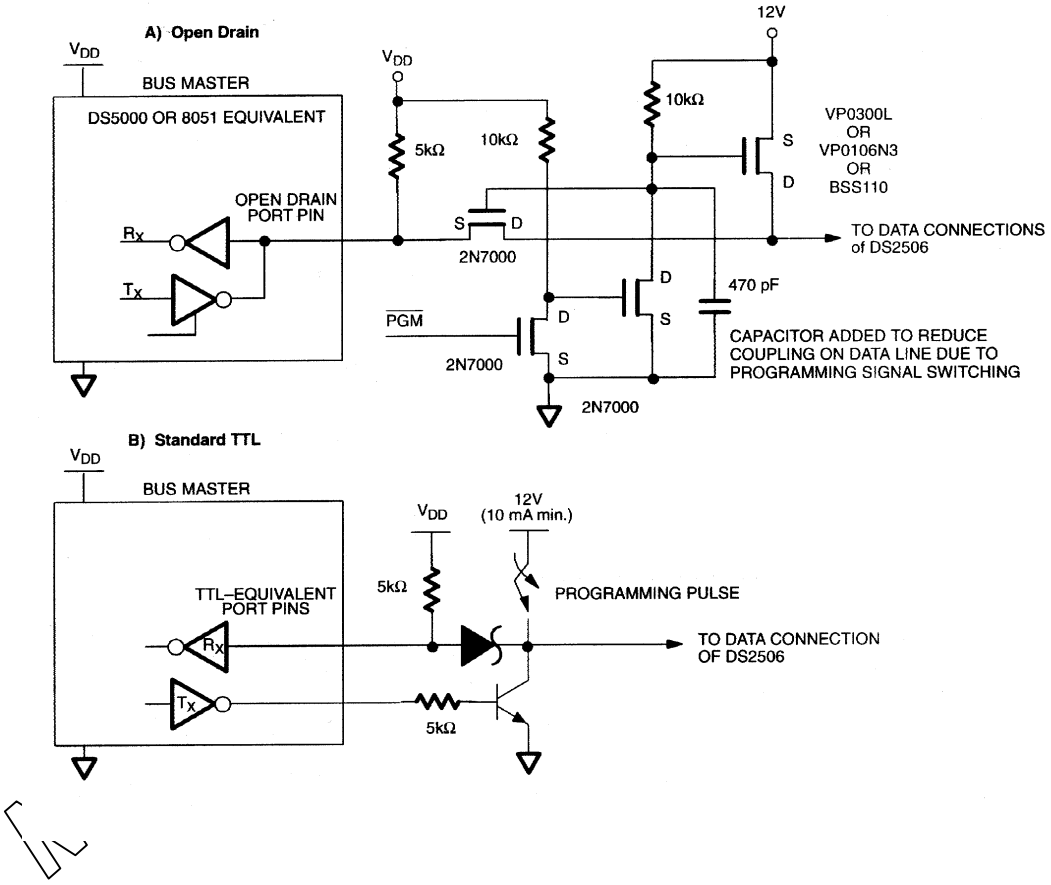
When a system is initially brought up, the bus master might not know the number of devices on the 1-Wire bus or their 64-bit ROM codes. The search ROM command allows the bus master to use a process of elimination to identify the 64-bit ROM codes of all slave devices on the bus. The ROM search process is the repetition of a simple 3-step routine: read a bit, read the complement of the bit, then write the desired value of that bit. The bus master performs this simple, 3-step routine on each bit of the ROM. After one complete pass, the bus master knows the contents of the ROM in one device. The remaining number of devices and their ROM codes may be identified by additional passes. See Chapter 5 of the Book of DS19xx iButton Standards for a comprehensive discussion of a ROM search, including an actual example.

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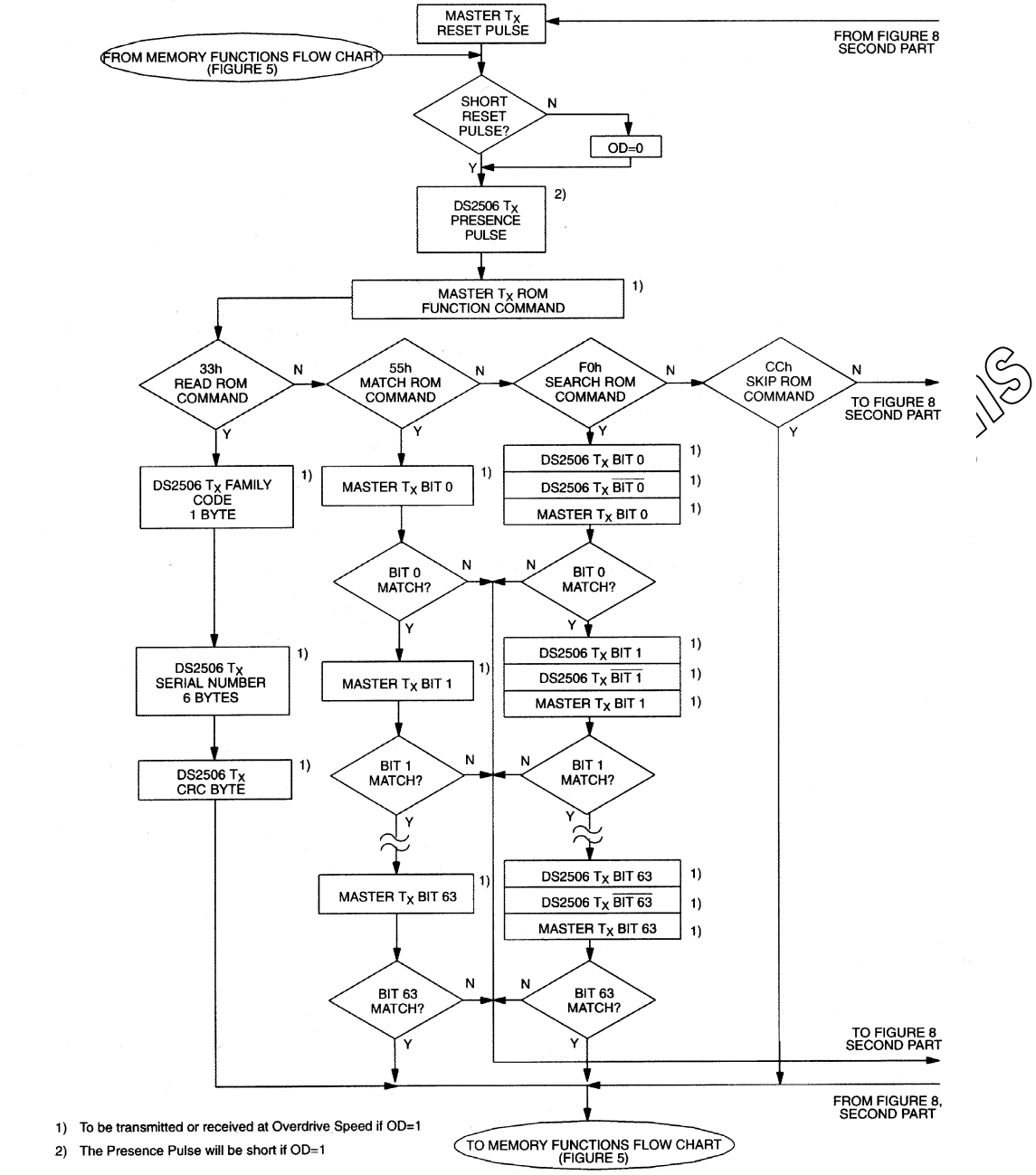
DS2506 EQUIVALENT CIRCUIT Figure 6



BUS MASTER CIRCUIT Figure 7

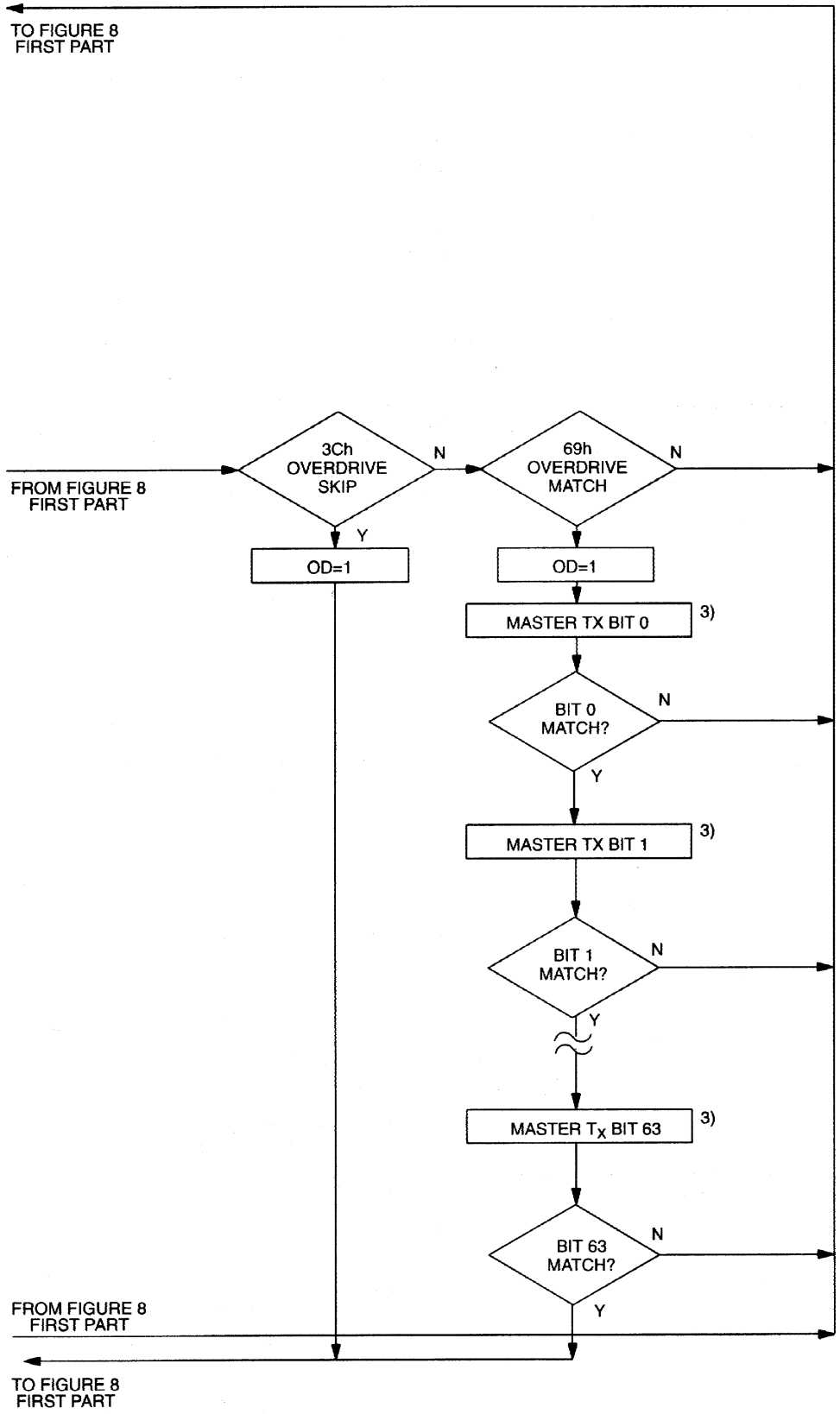


ROM FUNCTIONS FLOW CHART Figure 8



1) To be transmitted or received at Overdrive Speed if OD=1
2) The Presence Pulse will be short if OD=1

ROM FUNCTIONS FLOW CHART Figure 8 (cont'd)



Overdrive Skip ROM [3CH]

On a single-drop bus this command can save time by allowing the bus master to access the memory functions without providing the 64-bit ROM code. Unlike the normal Skip ROM command the Overdrive Skip ROM sets the DS2506 in the Overdrive Mode (OD=1). All communication following this command has to occur at Overdrive Speed until a reset pulse of minimum 480 µs duration resets all devices on the bus to regular speed (OD=0).

When issued on a multidrop bus this command will set all Overdrive-capable devices into Overdrive mode. To subsequently address a specific Overdrive-capable device, a reset pulse at Overdrive speed has to be issued followed by a Match ROM or Search ROM command sequence. This will shorten the time for the search process. If more than one slave supporting Overdrive is present on the bus and the Overdrive Skip ROM command is followed by a read command, data collision will occur on the bus as multiple slaves transmit simultaneously (open drain pulldowns will produce a wire-AND result).

Overdrive Match ROM [69H}

The Overdrive Match ROM command, followed by a 64-bit ROM sequence transmitted at Overdrive Speed, allows the bus master to address a specific DS2506 on a multidrop bus and to simultaneously set it in Overdrive Mode. Only the DS2506 that exactly matches the 64-bit ROM sequence will respond to the subsequent memory function command. Slaves already in Overdrive mode from a previous Overdrive Skip or Match command will remain in Overdrive mode. All other slaves that do not match the 64-bit ROM sequence or do not support Overdrive will return to or remain at regular speed and wait for a reset pulse of minimum 480 µs duration. The Overdrive Match ROM command can be used with a single or multiple devices on the bus.

1-Wire Signalling

The DS2506 requires strict protocols to insure data integrity. The protocol consists of five types of signaling on one line: Reset Sequence with Reset Pulse and Presence Pulse, Write 0, Write 1, Read Data and Program Pulse. All these signals except presence pulse are initiated by the bus master. The DS2506 can communicate at two different speeds, regular speed and Overdrive Speed. If not explicitly set into the Overdrive Mode, the DS2506 will communicate at regular speed. While in Overdrive Mode the fast timing applies to all communication-related wave forms.

The initialization sequence required to begin any communication with the DS2506 is shown in Figure 9. A Reset Pulse followed by a Presence Pulse indicates the DS2506 is ready to accept a ROM command. The bus master transmits (TX) a reset pulse (t_{RSTL}, minimum 480 µs at regular speed, 48 µs at Overdrive Speed). The bus master then releases the line and goes into receive mode (RX). The 1-Wire bus is pulled to a high state via the pullup resistor. After detecting the rising edge on the data pin, the DS2506 waits (t_{PDH}, 15-60 µs at regular speed, 2-6 µs at overdrive speed) and then transmits the presence pulse (t_{PDL}, 60-240 µs at regular speed, 8-24 µs at Overdrive Speed).

A Reset Pulse of 480 µs or longer will exit the Overdrive Mode returning the device to regular speed. If the DS2506 is in Overdrive Mode and the Reset Pulse is no longer than 80 µs the device will remain in Overdrive Mode.

Read/Write Time Slots

The definitions of write and read time slots are illustrated in Figure 10. All time slots are initiated by the master driving the data line low. The falling edge of the data line synchronizes the DS2506 to the master by triggering a delay circuit in the DS2506. During write time slots, the delay circuit determines when the DS2506 will sample the data line. For a read data time slot, if a "0" is to be transmitted, the delay circuit

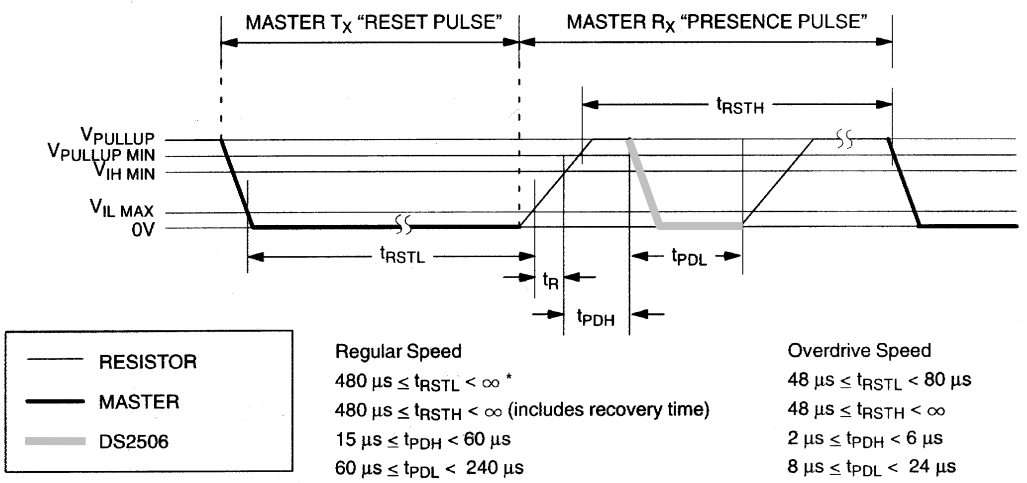
Not Recommended for New Designs

determines how long the DS2506 will hold the data line low overriding the 1 generated by the master. If the data bit is a "1", the device will leave the read data time slot unchanged.

PROGRAM PULSE

To copy data from the 8-bit scratchpad to the EPROM Data or Status Memory, a program pulse of 12 volts is applied to the data line after the bus master has confirmed that the CRC for the current byte is correct. During programming, the bus master controls the transition from a state where the data line is idling high via the pullup resistor to a state where the data line is actively driven to a programming voltage of 12 volts providing a minimum of 10 mA of current to the DS2506. This programming voltage (Figure 11) should be applied for 480 µs, after which the bus master returns the data line to an idle high state controlled by the pullup resistor. Note that due to the high voltage programming requirements for any 1-Wire EPROM device, it is not possible to multi-drop non-EPROM based 1-Wire devices with the DS2506 during programming. An internal diode within the non-EPROM based 1-Wire devices will attempt to clamp the data line at approximately 8 volts and could potentially damage these devices.

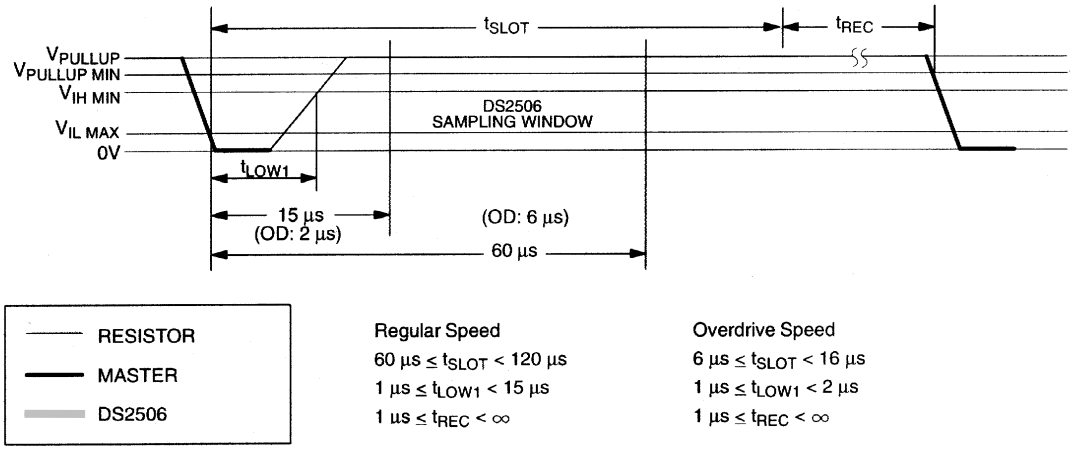
INITIALIZATION PROCEDURE "RESET AND PRESENCE PULSES" Figure 9



* In order not to mask interrupt signaling by other devices on the 1-Wire bus, $t_{RSTL} + t_R$ should always be less than 960 µs.

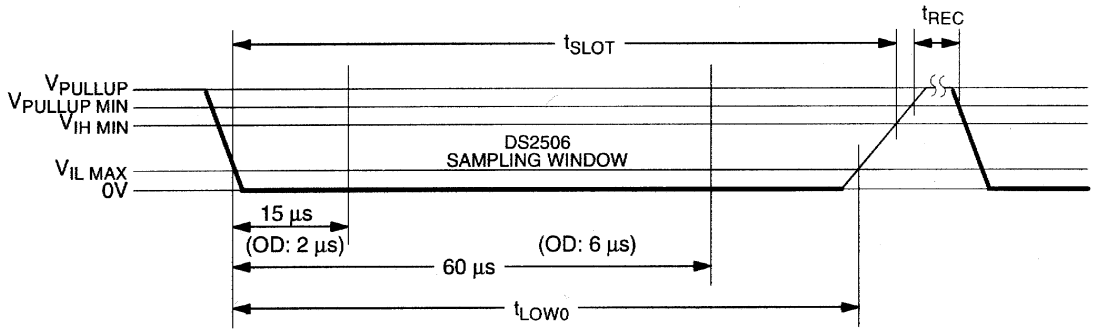
READ/WRITE TIMING DIAGRAM Figure 10

Write-one Time Slot



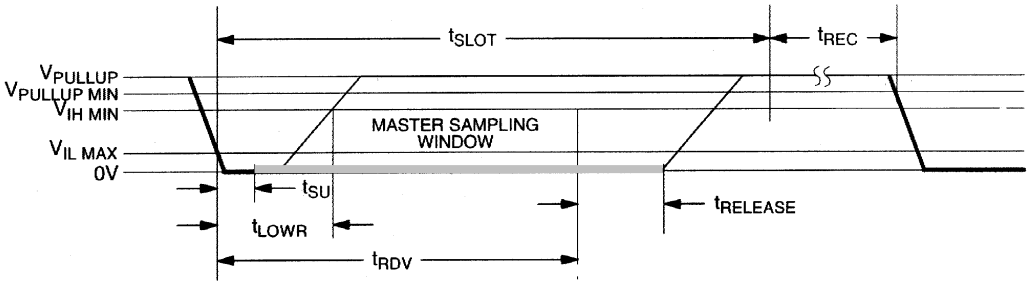
READ/WRITE TIMING DIAGRAM Figure 10 (cont'd)

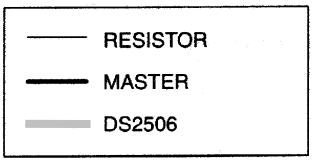
Write-zero Time Slot



Regular Speed	Overdrive Speed
60 µs ≤ t_{LOW0} < t_{SLOT} < 120 µs	6 µs ≤ t_{LOW0} < t_{SLOT} < 16 µs
1 µs ≤ t_{REC} < ∞	1 µs ≤ t_{REC} < ∞

Read-data Time Slot





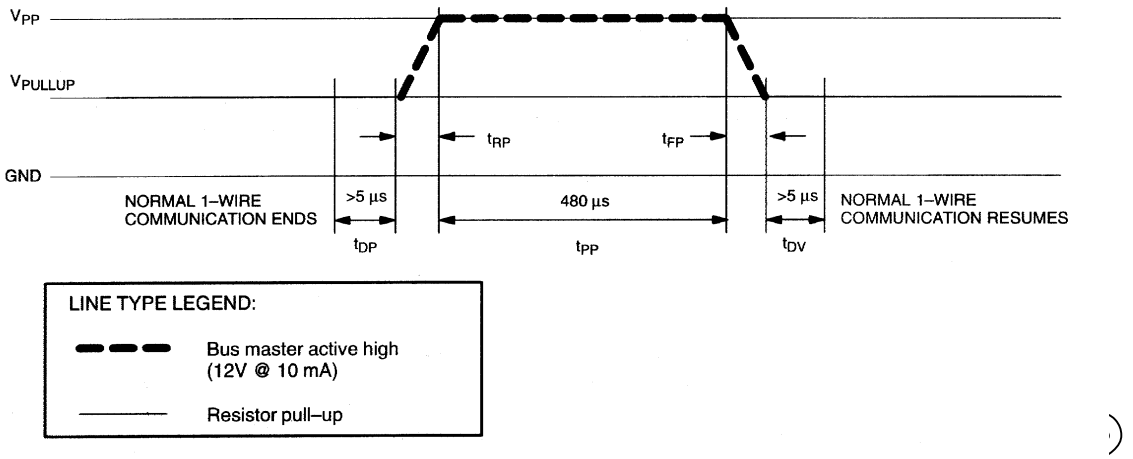
Regular Speed	Overdrive Speed
60 µs ≤ t_{SLOT} < 120 µs	6 µs ≤ t_{SLOT} < 16 µs
1 µs ≤ t_{LOWR} < 15 µs	1 µs ≤ t_{LOWR} < 2 µs
0 ≤ $t_{RELEASE}$ < 45 µs	0 ≤ $t_{RELEASE}$ < 4 µs
1 µs ≤ t_{REC} < ∞	1 µs ≤ t_{REC} < ∞
t_{RDV} = 15 µs	t_{RDV} = 2 µs
t_{SU} < 1 µs	t_{SU} < 1 µs

NOTE:

For read-data time slots the optimal sampling point for the master is as close as possible to the end time of the t_{RDV} period without exceeding 15 µs for regular speed or 2 µs for overdrive speed. For the case of a read-one time slot, this maximizes the amount of time for the pull-up resistor to recover the line to a high level. For a read-zero time slot it ensures that a read will occur before the fastest 1-Wire device releases the line ($t_{RELEASE}$ = 0).

Not Recommended

PROGRAM PULSE TIMING DIAGRAM Figure 11



CRC GENERATION

With the DS2506 there are two different types of CRCs (Cyclic Redundancy Checks). One CRC is a 8-bit type and is stored in the most significant byte of the 64-bit ROM. The bus master can compute a CRC value from the first 56 bits of the 64-bit ROM and compare it to the value stored within the DS2506 to determine if the ROM data has been received error-free by the bus master. The equivalent polynomial function of this CRC is: $X^8 + X^5 + X^4 + 1$. This 8-bit CRC is received in the true (non-inverted) form when reading the ROM of the DS2506. It is computed once at the factory and lasered into the ROM.

The other CRC is a 16-bit type, generated according to the standardized CRC16-polynomial function $X^{16} + X^{15} + X^2 + 1$. This CRC is used to safeguard user-defined EPROM data when reading data memory or status memory. It is the same type of CRC as is used with NV RAM based iButtons to safeguard data packets of the iButton File Structure. In contrast to the 8-bit CRC, the 16-bit CRC is always returned in the complemented (inverted) form. A CRC-generator inside the DS2506 chip (Figure 12) will calculate a new 16-bit CRC at every situation shown in the command flow chart of Figure 5.

The DS2506 provides this CRC-value to the bus master to validate the transfer of command, address, and data to and from the bus master. When reading the data memory of the DS2506 with the Read Memory command, the 16-bit CRC is only transmitted as the end of the memory is reached. This CRC is generated by clearing the CRC generator, shifting in the command, low address, high address and every data byte starting at the first addressed memory location and continuing until the end of the implemented data memory is reached.

When reading the status memory with the Read Status command, the 16-bit CRC is transmitted when the end of each 8 byte page of the status memory is reached. At the initial pass through the Read Status flow chart the 16-bit CRC will be generated by clearing the CRC generator, shifting in the command byte, low address, high address and the data bytes beginning at the first addressed memory location and continuing until the last byte of the addressed EPROM Status data page is reached. Subsequent passes through the Read Status flow chart will generate a 16-bit CRC that is the result of clearing the CRC generator and then shifting in the new data bytes starting at the first byte of the next page of the EPROM Status data field and continuing until the last byte of the page is reached.

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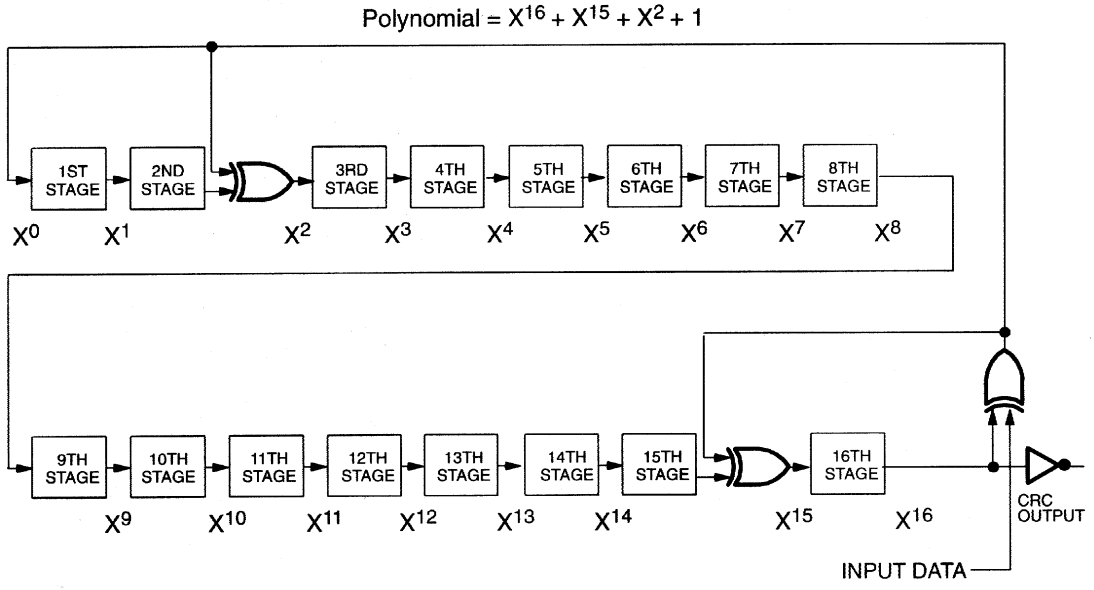
When reading the data memory of the DS2506 with the Extended Read Memory command, there are two situations where a 16-bit CRC is transmitted. One 16-bit CRC follows each Redirection Byte, another 16-bit CRC is received after the last byte of a memory data page is read. The CRC at the end of the memory page is always the result of clearing the CRC generator and shifting in the data bytes beginning at the first addressed memory location of the EPROM data page until the last byte of this page. With the initial pass through the Extended Read Memory flow chart the 16-bit CRC value is the result of shifting the command byte into the cleared CRC generator, followed by the two address bytes and the Redirection Byte. Subsequent passes through the Extended Read Memory flow chart will generate a 16-bit CRC that is the result of clearing the CRC generator and then shifting in the Redirection Byte only.

When writing to the DS2506 (either data memory or status memory), the bus master receives a 16-bit CRC to verify the correctness of the data transfer before applying the programming pulse. With the initial pass through the Write Memory/Status flow chart the 16-bit CRC will be generated by clearing the CRC generator, shifting in the command, address low, address high and the data byte. Subsequent passes through the Write Memory/Status flow chart due to the DS2506 automatically incrementing its address counter will generate an 16-bit CRC that is the result of loading (not shifting) the new (incremented) address into the CRC generator and then shifting in the new data byte.

The comparison of CRC values and decision to continue with an operation are determined entirely by the bus master. There is no circuitry on the DS2506 that prevents a command sequence from proceeding if the CRC stored in or calculated by the DS2506 does not match the value generated by the bus master. For more details on generating CRC values including example implementations in both hardware and software, see the Book of DS19xx iButton Standards.

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CRC-16 HARDWARE DESCRIPTION AND POLYNOMIAL Figure 12



ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.5V to +12.0V
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	See J-STD-020A specification

* This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS (V_{PUP}=2.8V to 6.0V; -40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.2			V	1, 6
Logic 0	V_{IL}	-0.3		+0.8	V	1, 10
Output Logic Low @ 4 mA	V_{OL}			0.4	V	1
Output Logic High	V_{OH}		V_{PUP}	6.0	V	1, 2
Input Load Current	I_L		5		µA	3
Operating Charge	Q_{OP}			30	nC	7, 8
Programming Voltage @ 10 mA	V_{PP}	11.5		12.0	V	11

CAPACITANCE (T_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data (1-Wire)	$C_{IN/OUT}$			800	pF	9

AC ELECTRICAL CHARACTERISTICS (V_{PUP}=2.8V to 6.0V; -40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Time Slot	t_{SLOT}	60		120	µs	
Write 1 Low Time	t_{LOW1}	1		15	µs	
Write 0 Low Time	t_{LOW0}	60		120	µs	
Read Data Valid	t_{RDV}		15		µs	12
Release Time	$t_{RELEASE}$	0	15	45	µs	
Read Data Setup	t_{SU}			1	µs	5
Recovery Time	t_{REC}	1			µs	
Reset Time High	t_{RSTH}	480			µs	4
Reset Time Low	t_{RSTL}	480			µs	
Presence Detect High	t_{PDHIGH}	15		60	µs	
Presence Detect Low	t_{PDLOW}	60		240	µs	
Delay to Program	t_{DP}	5			µs	
Delay to Verify	t_{DV}	5			µs	
Program Pulse Width	t_{PP}	480			µs	11
Program Voltage Rise Time	t_{RP}	0.5		5.0	µs	11
Program Voltage Fall Time	t_{FP}	0.5		5.0	µs	11

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AC ELECTRICAL CHARACTERISTICS OVERDRIVE SPEED

(V_{PUP}=2.8V to 6.0V; -40°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Time Slot	t_{SLOT}	6		16	µs	
Write 1 Low Time	t_{LOW1}	1		2	µs	
Write 0 Low Time	t_{LOW0}	6		16	µs	
Read Data Valid	t_{RDV}		2		µs	12
Release Time	$t_{RELEASE}$	0	1.5	4	µs	
Read Data Setup	t_{SU}			1	µs	5
Recovery Time	t_{REC}	1			µs	
Reset Time High	t_{RSTH}	48			µs	4
Reset Time Low	t_{RSTL}	48		80	µs	
Presence Detect High	t_{PDHIGH}	2		6	µs	
Presence Detect Low	t_{PDLOW}	8		24	µs	

NOTES:

1. All voltages are referenced to ground.

2. V_{PUP}= external pullup voltage.

3. Input load is to ground.

4. An additional reset or communication sequence cannot begin until the reset high time has expired.

5. Read data setup time refers to the time the host must pull the 1-Wire bus low to read a bit. Data is guaranteed to be valid within 1 µs of this falling edge.

6. V_{IH} is a function of the external pullup resistor and V_{PUP}.

7. 30 nanocoulombs per 72 time slots @ 5.0V.

8. At V_{CC}=5.0V with a 5 kΩ pullup to V_{CC} and a maximum time slot of 120 µs.

9. Capacitance on the data pin could be 800 pF when power is first applied. If a 5 kΩ resistor is used to pullup the data line to V_{CC}, 5 µs after power has been applied the parasite capacitance will not affect normal communications.

10. Under certain low voltage conditions V_{ILMAX} may have to be reduced to as much as 0.5V to always guarantee a presence pulse.

11. Operational temperature range for memory programming is -40°C to +50°C.

12. For read-data time slots the optimal sampling point for the master is as close as possible to the end time of the t_{RDV} period without exceeding 15 µs for regular speed or 2 µs for overdrive speed. For the case of a read-one time slot, this maximizes the amount of time for the pull-up resistor to recover the line to a high level. For a read-zero time slot it ensures that a read will occur before the fastest 1-Wire device releases the line ($t_{RELEASE}$ = 0).

Not Recommended for New Designs